L62xx motor drivers: contribution of internal resistance and propagation delay in current control circuitry

Introduction

Some devices of the L62xx family integrate peak current control functions: the load current is measured through an external shunt resistor (R_{SENSEX}) and compared to a reference value (V_{REFX}). When the comparator triggers, a decay sequence is started with the duration set by an RC network.

This document investigates how the following parameters affect the set point of the current regulator:

- Parasitic resistances between the power stage and shunt resistor
- Propagation delay of the current control loop

The parasitic resistances do not affect the overcurrent protection.

Table 1 lists the devices concerned by this application note.

Table 1. Devices list

Devices	Description
L6207, L6207Q, L6227, L6227Q	Dual full bridge drivers with PWM current controller
L6208, L6208Q, L6228, L6228Q	Drivers for bipolar stepper motor
L6235, L6235Q, L6229, L6229Q	Drivers for three-phase brushless DC motor

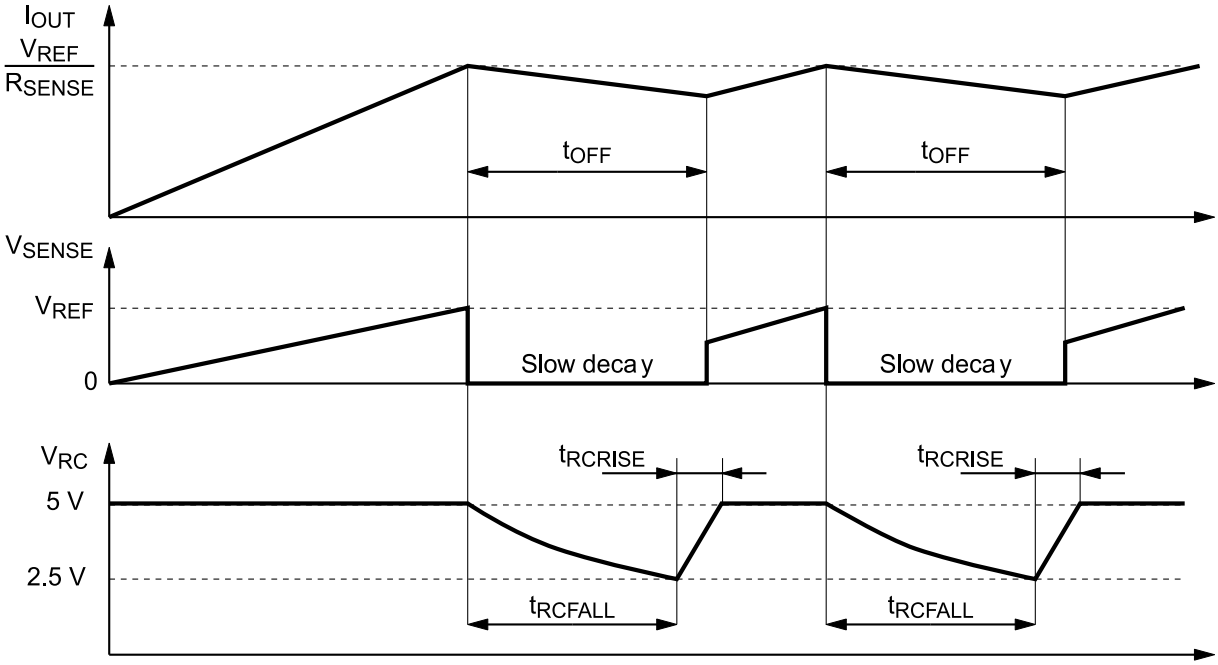
1 Current sensing circuit

The PWM current control of the L62xx family is based on a peak detection with constant decay time.

The current flowing into the load is converted to voltage by the external shunt resistance to be compared with the target reference.

When the target reference is reached, the control circuitry commutates the power stage to the decay mode and triggers a monostable. This condition is maintained until the monostable returns to its steady-state according to the timing imposed by the external RC network.

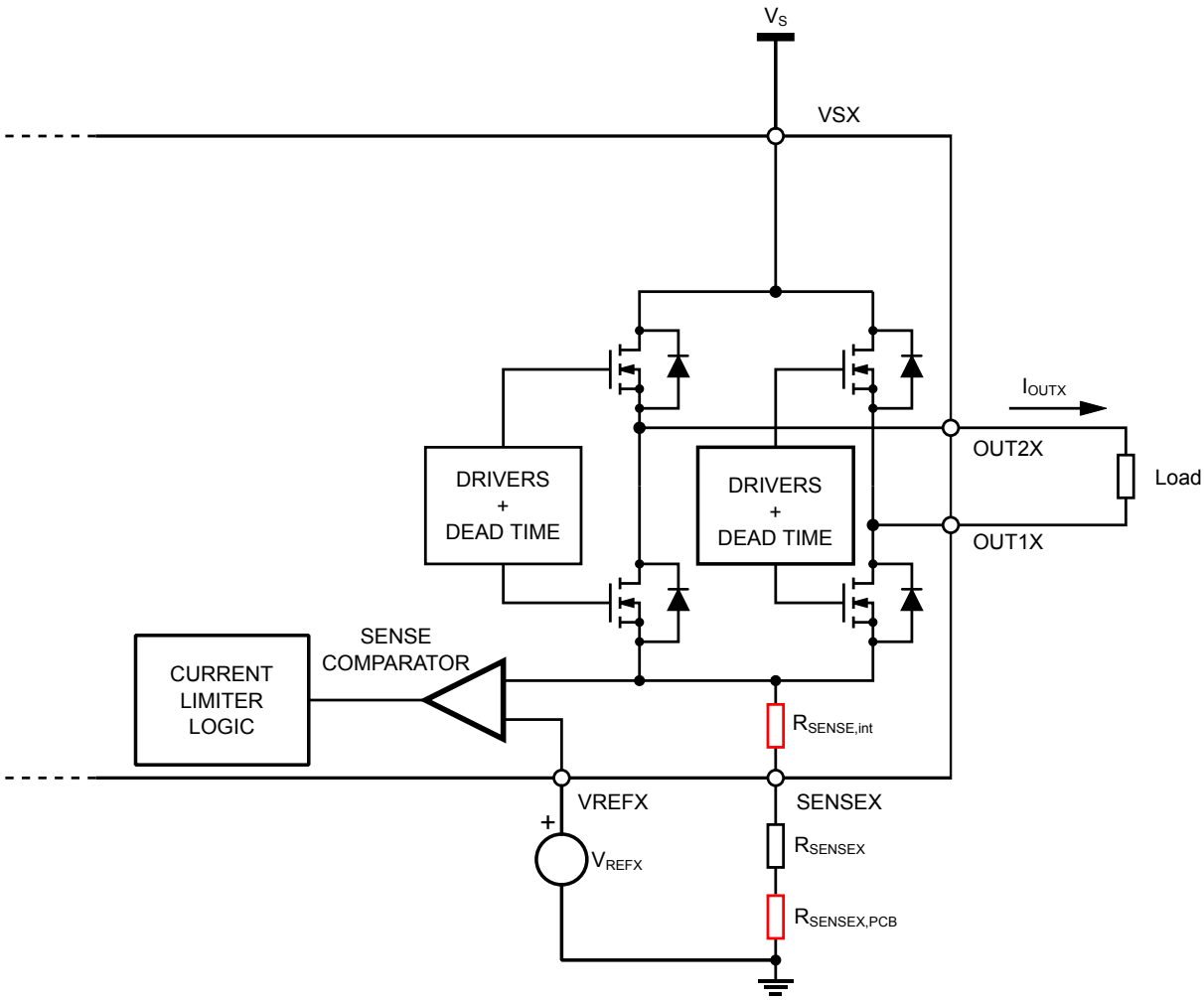
Figure 1. PWM current limiter example (L6207/27)



1.1 Effect of parasitic resistances on PWM current control

The input of the control circuitry's comparator is not directly connected to the shunt and its voltage also depends on two parasitic resistances: internal connection between power stage and SENSEx pin and PCB traces (see Figure 2).

Figure 2. Current sensing circuit and parasitic resistances



The internal connection resistance depends on package and its typical value is listed in Table 2.

Table 2. Internal resistance contribution of different packages

Package	Typical internal resistance ($R_{SENSE,int}$)
SO-24	10 mΩ
PowerSO 36	< 5 mΩ
QFN48 7x7 mm	30 mΩ
QFN32 5x5 mm	40 mΩ

The contribution of PCB traces depends on layout and is hardly predictable. The best solution is to minimize it, mounting the shunt resistors as near as possible to the SENSEX pins and keeping the ground connection as short as possible.

Parasitic resistances cause an extra drop at comparator input:

Equation 1

$$V_{COMP} = I_{OUTX} \times \left(R_{SENSEX} + R_{SENSEX,PCB} + R_{SENSE,int}\right) \quad (1)$$

Lowering the peak current level compared to the ideal set point:

Equation 2

$$I_{peak,ID} = \frac{V_{REFX}}{R_{SENSEX}} \quad (2)$$

Equation 3

$$I_{peak,actual} = \frac{V_{REFX}}{R_{SENSEX} + R_{SENSEX,PCB} + R_{SENSE,int}} \quad (3)$$

Equation 4

$$I_{peak,actual} = I_{peak,ID} \times \left(\frac{R_{SENSEX}}{R_{SENSEX} + R_{SENSEX,PCB} + R_{SENSE,int}}\right) \quad (4)$$

To minimize the error, a higher value for the shunt resistor must be selected.

Figure 3. Peak current error vs. shunt resistor

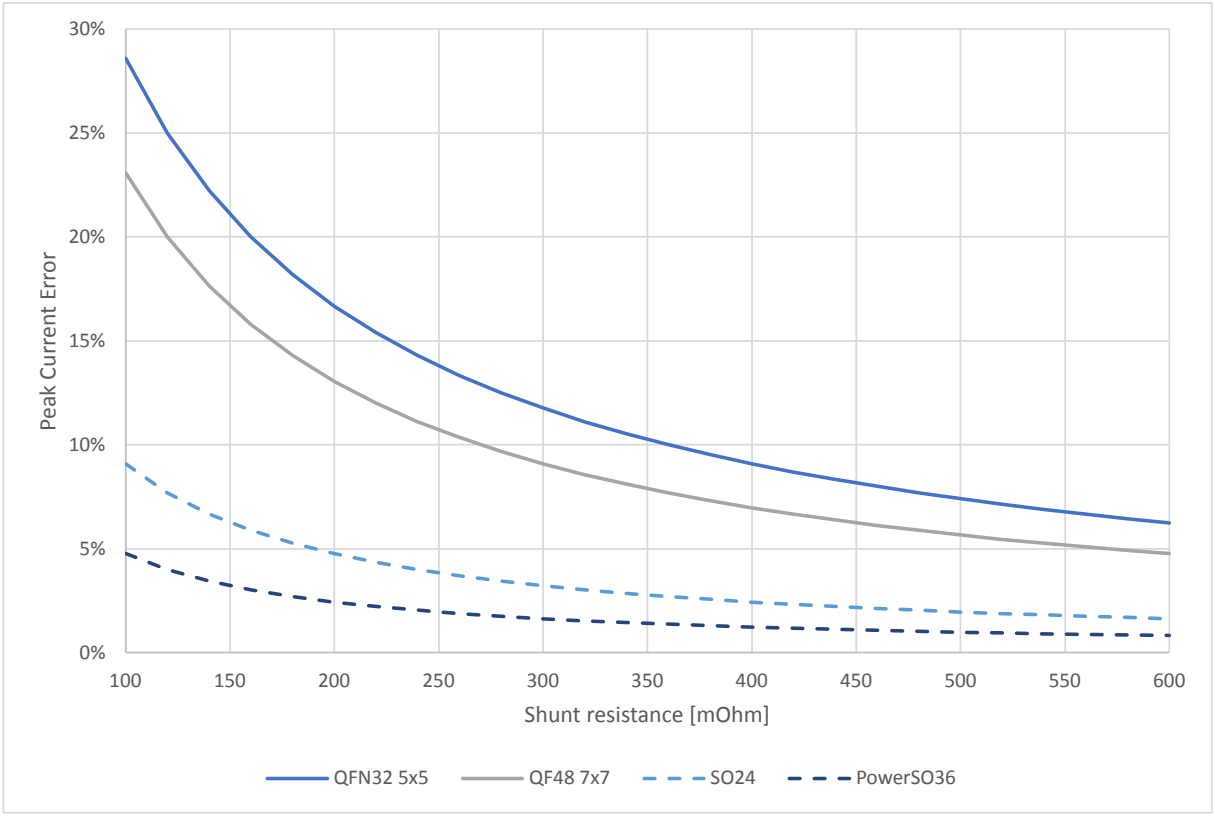
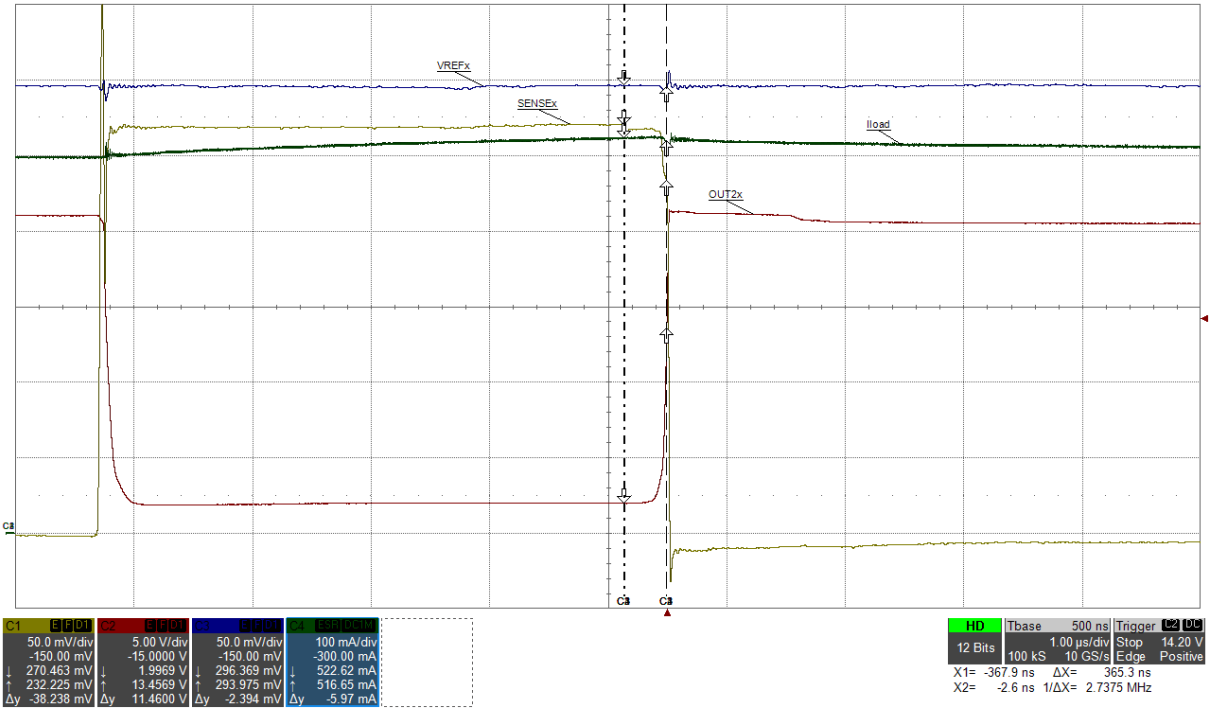


Figure 4 shows the effect of internal parasitic resistance on the L6227Q.

Figure 4. Parasitic resistance effect example (L6227Q)



1.2 Effect of propagation delay on PWM current control

The turning-off of the power stage is delayed by t_{PROP} (500 ns typical) with respect to comparator triggering. This is related to both the intervention time of the control circuitry and power MOSFETs commutation timings.

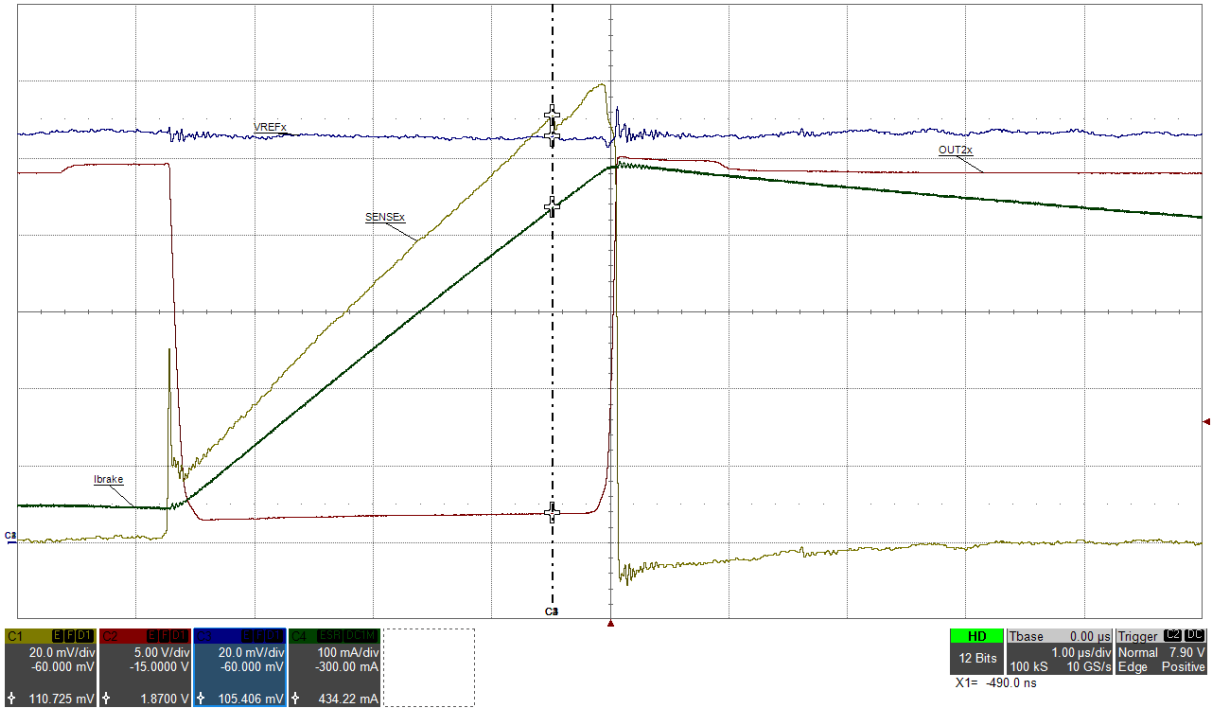
Consequently, the actual peak current is always higher than the threshold value: the higher the charging slope, the bigger the error:

Equation 5

$$\Delta I_{PEAK} = \frac{dI_{load}}{dt} \times t_{PROP} \quad (5)$$

Current slope is directly related to the characteristics of the load (inductance) and supply voltage.

Figure 5. Propagation delay effect example



2 Conclusions and overall behavior

As described in previous sections, the parasitic resistance always introduces a negative error (that is, actual current lower than target) and the propagation delay a positive one.

For this reason, in many cases the two effects compensate each other.

However, in particular cases one of the two could cause a not negligible difference between expected and actual peak current:

- Low shunt resistance value;
- Fast current slope (that is, low inductance and/or high supply voltage).

Revision history

Table 3. **Document revision history**

Date	Version	Changes
21-Mar-2023	1	Initial release.

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