PCB design optimization for maximizing thermal dissipation in MasterGaN family

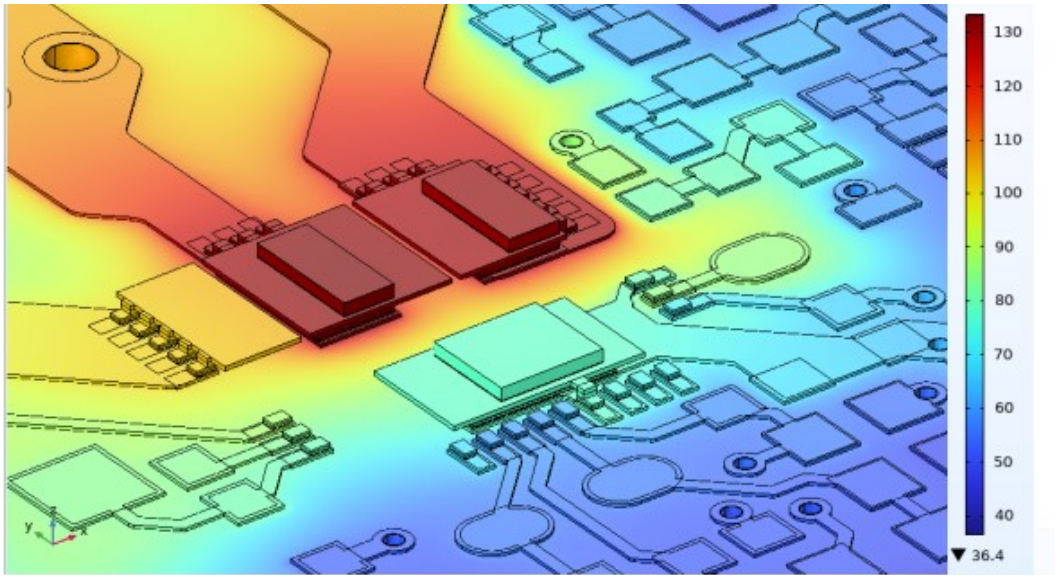
Introduction

The MasterGaN family has been designed to facilitate the creation of very compact power converter solutions. The MasterGaN series is an advanced power system-in-package, integrating a gate driver and two enhanced mode GaN transistors in half-bridge configuration. It is available in a compact 9 x 9 mm QFN package, and it operates in industrial temperature range of -40 ˚C to +125 ˚C.

Every GaN is connected to its exposed pad which in turn is connected to the PCB, heat dissipation, therefore, takes place via the exposed pads connected to the PCB [1] , [2] .

The PCB becomes of particular importance for effective thermal management to avoid critical temperature above 125 ˚C.

Figure 1. MASTERGAN1 exposed pads power dissipation



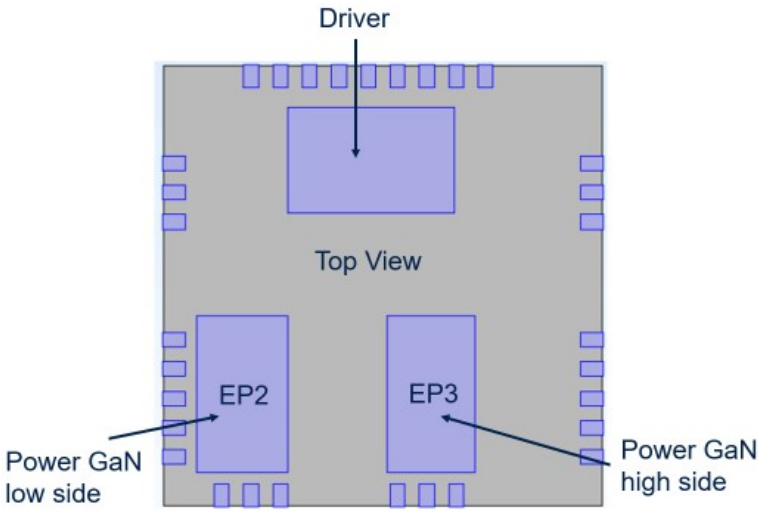
High output power with high power density can be realized only by giving the right weight and attention to the thermal aspect in the design phase so the heat management concept also needs to be developed.

This paper is intended to describe the experimental method used to obtain thermal resistance and its dependence on different PCB parameters. A guide to designing a PCB having a desired thermal resistance is also provided. Practical suggestions are provided to use an additional heatsink, if needed. The main outcome of this application note is that a standard two-layer PCB stack-up can be considered to obtain effective thermal dissipation for the MasterGaN 9x9 QFN package.

1 Experimental thermal jig design criteria and set-up

The exposed pads EP2 (sense) and EP3 (out) of the MasterGaN series have been designed to dissipate the heat produced respectively by low-side and high-side GaN (see Figure 2).

Figure 2. MASTERGAN1 exposed pads top view



The portion of PCB connected to said exposed pads is used to transfer the heat generated by the GaN's power losses from junction to external environment and maintain the junction temperature increase within the defined maximum level. An optimized design helps to increase the maximum target power of the final application.

The aim of this study is to provide a practical tool to anticipate the maximum power that could be managed by MasteGaN without exceeding the maximum rating and using standard and low-cost PCB design solutions.

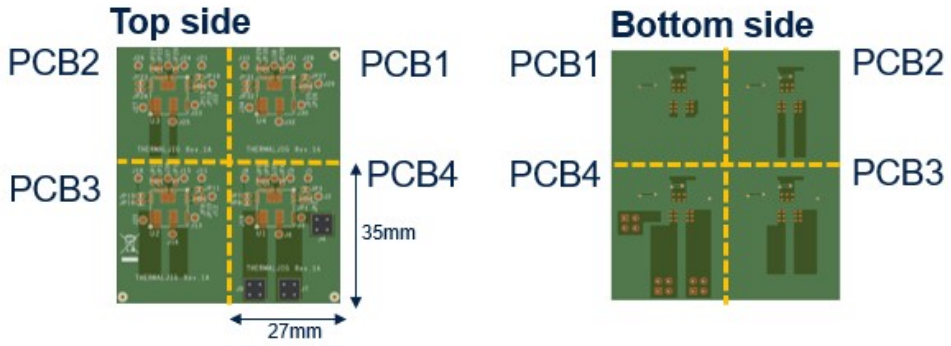
1.1 Thermal jig design specifications

Different design combinations have been realized in order to study in detail the effect of copper area, PCB thickness and thermal vias number on the power dissipation by measuring the external package temperature.

Specific thermal jigs have been designed with the following specs:

- **Rev. 1.0**: 2-layer PCB thickness=1 mm
- **Rev. 1.6**: 2-layer PCB thickness=1.6 mm
- **Rev. A**: 6 TH VIAS (thermal vias)
- **Rev. B**: 9 TH VIAS (thermal vias)
- **Rev. V6**: MASTERGAN1
- **Rev. V7**: MASTERGAN4

Figure 3. **Thermal jig top and bottom view**



As shown in Figure 3, every jig is composed of four independent boards containing MasterGaN.

In each board, every EP is soldered to a copper area that is increased properly step-by-step as described in Table 1.

Table 1. **PCB copper area definition**

PCB number	Top area–low side (mm^2)	Top area–high side (mm^2)	Bottom area-low side (mm^2)	Bottom area-high side (mm^2)	Total copper area (mm^2)
PCB1	12.1	8.13	12.1	8.13	40.27
PCB2	42.04	27.42	42.04	27.42	138.92
PCB3	89.86	63.34	89.86	63.34	306.38
PCB4	135.92	126.72	135.92	126.72	525.28

The total PCB area is reported in the right column; PCB 4 is about thirteen times the PCB1 area.

1.2 Test set-up

The two integrated GaN of the half-bridge are the main contributors to the power dissipation through the exposed pads of the bottom side but at thermal regime, the MasterGaN top side package appears as the single source of power.

In fact, a set of experiments has been performed to evaluate the impact of the mutual thermal resistance between OUT EP and SENSE EP. Each GaN of the half-bridge has been singularly forced to dissipate and the temperature of the opposite EP has been measured with no practical contribution of opposite EPs being found.

Even if, for the sake of simplicity, the results of this experiment have not been reported entirely in this document, from a practical point of view, each EP dissipates only the power of the GaN assembled on it.

Figure 4. Jig test set up for thermal measurements

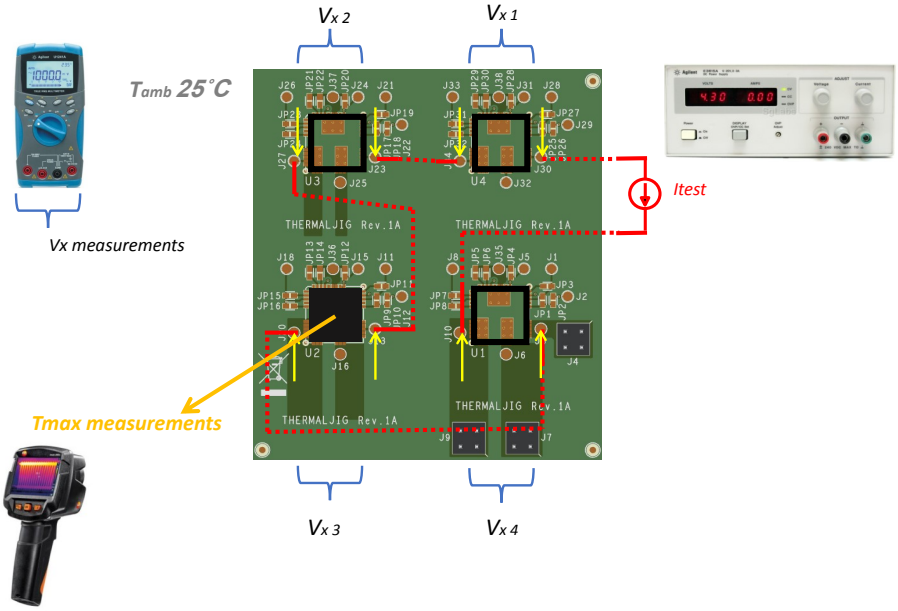


Figure 4 represents the jig test set-up. A thermal image sensor can estimate the maximum temperature on the top side package.

The ΨTC (junction to top case thermal resistance) of the package has been estimated equal to 0.3 °C/W, so the top case temperature can be assumed to be almost equal to the junction temperature. This consideration ensures an accurate temperature measurement without entering into contact with IC's body (that is, without modifying the environmental conditions).

A flat black silk screen has been used in order to maximize the homogeneity of jig emissivity and reduce the measurement error. The thermal resistance of the jig is not affected by the board's color.

A fixed test current I_{test} has been forced from the high-side GaN's drain to the low-side GaN's source of each MasterGaN in order to activate a reverse conduction of the two series GaN.

The measured voltage depends on the single GaN voltage threshold and its R_{Dson} as expressed in Eq. (1) :

$$V_{rev\ GaN} = V_{th} + R_{DSon} \cdot I_{Test} \quad (1)$$

So, for each MasterGaN the forced power dissipation could be expressed as Eq. (2):

$$P_{Diss\ MG} = (V_{rev\ GaN\ LS} + V_{rev\ GaN\ HS}) \cdot I_{Test} \quad (2)$$

Finally, every board of the jig has been put in series in order to stimulate the four devices with the same current. The value of the power is selected to be similar to the one present in a real power application board independently from the topology.

A thermal map of the four devices for each PCB have been acquired at the same time and at the same room temperature of about 25 °C.

$$\Delta T = T_{max} - T_{amb} \quad (3)$$

Systematic errors are eliminated in data comparison and a higher temperature could be related to higher thermal resistance of the PCB.

However, a slight difference of a couple of degrees between temperatures may be due to different voltage values across the GaN of the half-bridge: this difference is related with the variation of the Vth in Eq. (1)

For those reasons the thermal resistance defined as Eq. (4):

$$R_{th} = \frac{T_{max} - T_{amb}}{P_{Diss\ MG}} \quad (4)$$

has been here considered as a normalized parameter independent of the fluctuations of the applied power and suitable for final considerations.

2 Data analysis

After one hour warm-up with the same setup previously described (Figure 4), thermal maps have been acquired for every type of PCB.

To increase the statistical population, the analysis has been made for both MASTERGAN4 and MASTERGAN1 where the GaN R_{Dson} is passing from 225 mΩ to 150 mΩ @ 25 ˚C as for spec [1] , [2] .

2.1 Thermal maps acquisition

A fixed test current I_{test} of 200 mA has been applied from LS source to HS drain of the half-bridge, forcing a reverse conduction of the two series GaNs of each MasterGaN. Thermal maps have been acquired and reported in Figure 5 and Figure 6.

Figure 5. MASTERGAN4 jig thermal map

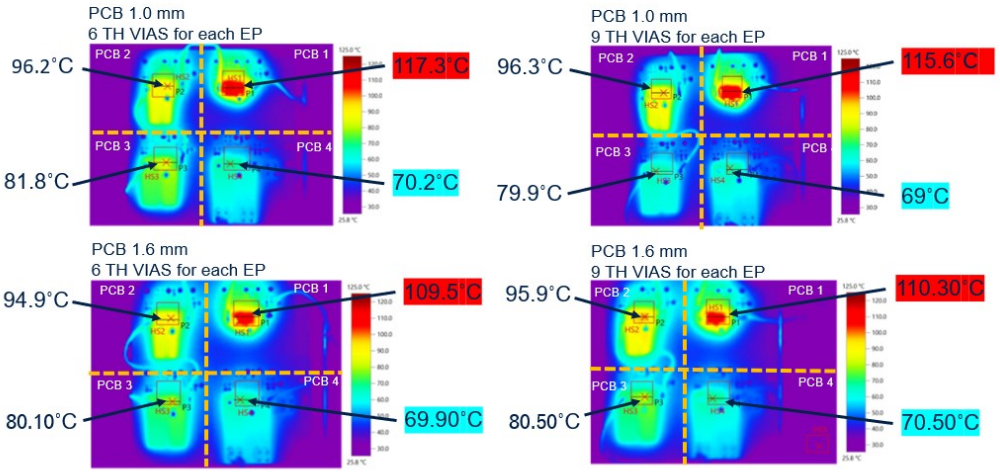
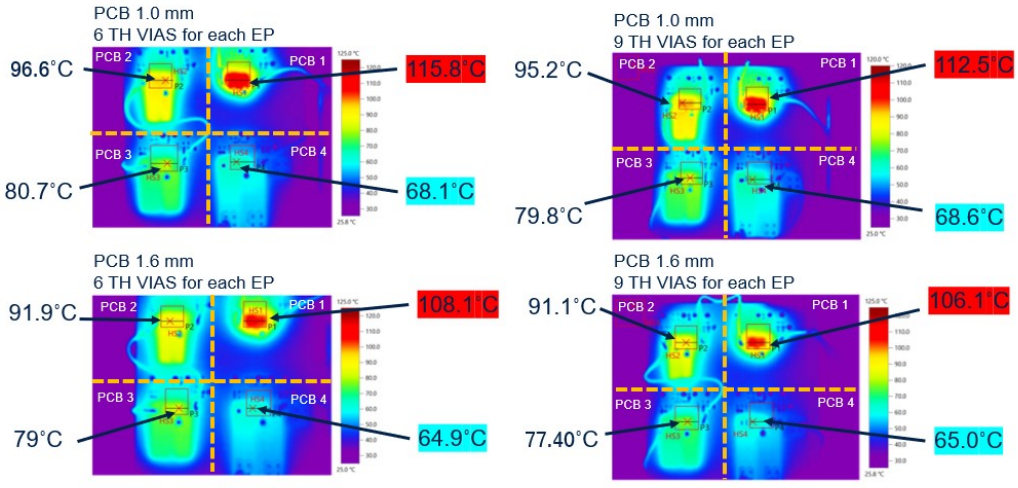


Figure 6. MASTERGAN1 jig thermal map



Thermal maps have been acquired at the same test set-up condition. The jig is perpendicular to the image sensor lens. The ambient temperature has been registered at 25 ˚C.

According to Eq. (1) a slightly different voltage drop Vx has been measured depending on both RDs_{on} of MASTERGAN4 or MASTERGAN1 and V_{th} fluctuation.

2.2 Temperature variation with PCB area

The data of the thermal maps of Figure 5 and Figure 6 have been analyzed and graphed:

Figure 7. MASTERGAN1–temperature vs. copper area

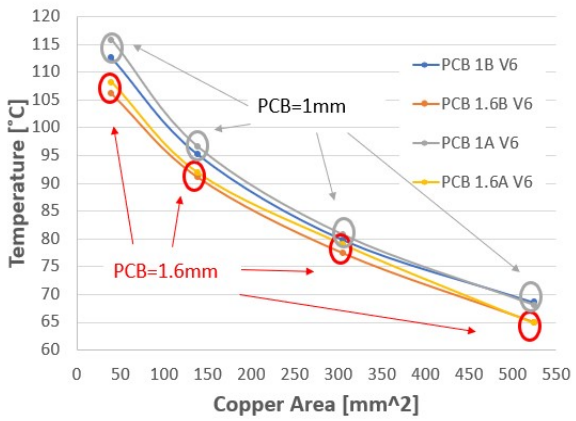
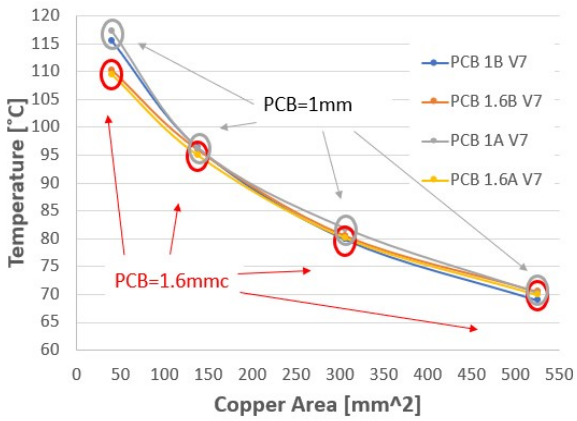


Figure 8. MASTERGAN4–temperature vs. copper area



At thermal regime, an amount temperature of 5 ˚C to 8 ˚C is saved in the 1.6 mm PCB thickness solution with respect to the thickness one of 1 mm. This observation can be related to a more dissipative PCB resin composition: for this reason, it is worth double checking the thermal performance of the final application in case PCB material is different.

The temperature is halved by increasing the PCB area more than ten times passing from 40 mm^2 to 525 mm^2.

In the MASTERGAN1 jig using 9 TH VIAS instead of 6 helps to dissipate heat from PADs but this effect is not be observed and confirmed in MASTERGAN4 jig.

2.3 PCB thickness impact on the thermal resistance

The same data have been expressed in terms of normalized thermal resistance: trends of Figure 9 and Figure 10 are similar to Figure 7 and Figure 8.

Figure 9. MASTERGAN1–PCB thickness comparison

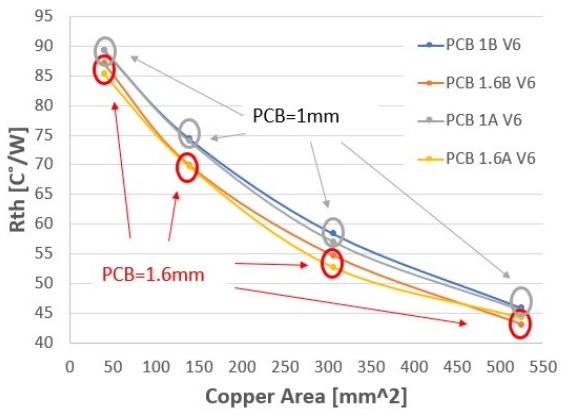
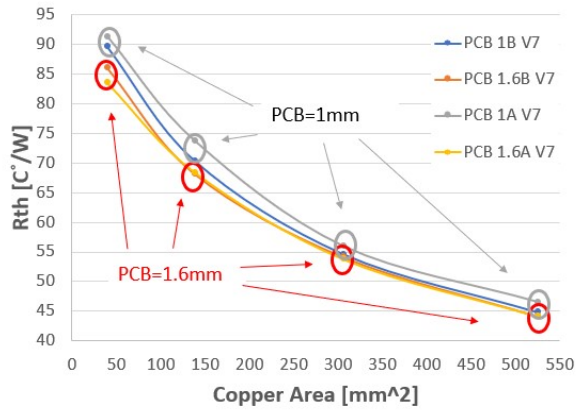


Figure 10. MASTERGAN4–PCB thickness comparison



A lower temperature allowed in the 1.6 mm PCB solution corresponds to a lower jig thermal resistance.

R_{th} could be reduced from 90 ˚C/W to about 45 ˚C/W by increasing the dissipating copper area by about twelve times.

A further R_{th} reduction to about 35 ˚C/W could be reached only by adding a proper designed heatsink (see next section).

2.4 Pads TH VIAS impact on thermal resistance

The same data have been reworked to highlight the difference in emission due to TH VIAS under the exposed pads area.

Figure 11. MASTERGAN1 - 6 TH VIAS vs. 9 TH VIAS in PCB 1 mm

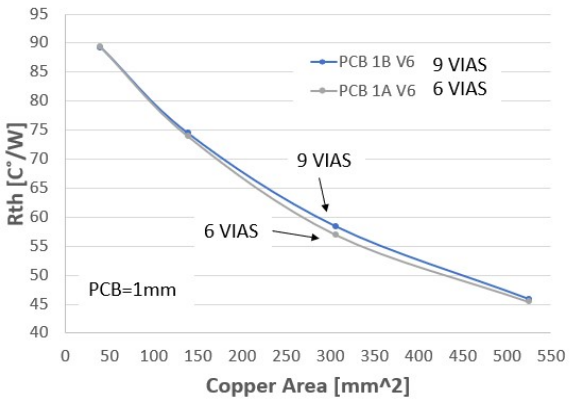


Figure 12. MASTERGAN4 - 6 TH VIAS vs. 9 TH VIAS in PCB 1 mm

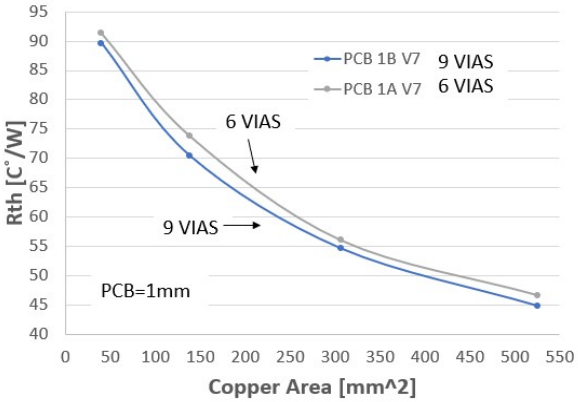


Figure 13. MASTERGAN1 - 6 TH VIAS vs. 9 TH VIAS in PCB 1.6 mm

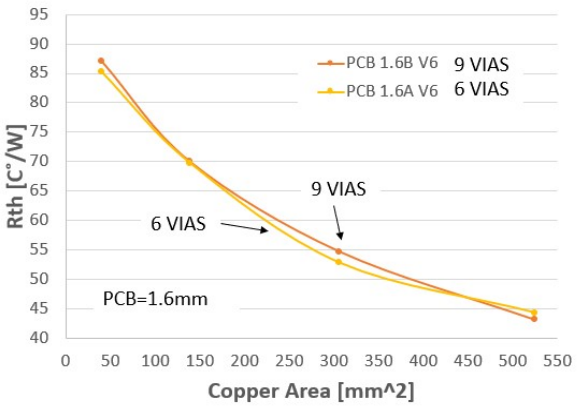
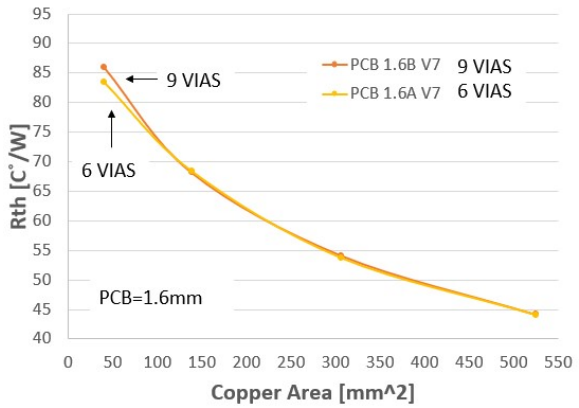


Figure 14. MASTERGAN4 - 6 TH VIAS vs. 9 TH VIAS in PCB 1.6 mm



In this design it seems that adding only three TH VIAS passing from Rev.A to B is not enough to make an observable difference.

2.5 Adding a heatsink to PCB 4 of jig 1.6B V6

PCB number 4 of jig 1.6 B V 6 (with MASTERGAN1) has been selected as the top solution without a heatsink with a final R_{th}~45 ˚C/W.

As shown in Figure 15, a small heatsink (20 mm x 23 mm x 12 mm, Rth ~27 °C/W) on the bottom side has been added and a thermal map has been acquired.

Figure 15. Bottom side added heatsink with Rth~27°C/W

The MASTERGAN1 temperature decreases from 65 ˚C to 57.6 ˚C and the estimated thermal resistance is passing from 43.8 ˚C/W to 34.5 ˚C/W.

3 Power design thermal consideration

Depending on PCB design, the following table represents the maximum power that MasterGaN could dissipate in a power supply application typically sized for operating in the range T_{max} ambient of 50 ˚C up to T_{max} admitted of 125 ˚C.

3.1 Calculation of the maximum power allowed on MasterGaN package

Each total PCB area is corresponding to an associated thermal resistance junction to ambient.

Simply inverting formula Eq. (4) and using the R_{th} values associated to different PCB areas, it is possible to extract maximum power admitted on the package as:

$$P_{Diss\ MG} = \frac{T_{max} - T_{amb}}{R_{th}} \quad (5)$$

Using experimental data, an estimation of the maximum power admitted on MasterGaN package coupled with a standard 2-layer PCB has been extracted and reported in the following table:

Table 2. Power dissipation admitted on the package

PCB number	Total dissipation area [mm^2]	$R_{thj\text{-}a}$ (˚C/W)	$T_{amb\ max}$ [˚C]	T_{max} [˚C]	$P_{Diss\_max\ admitted\ on\ MG}$ [W]
PCB1	40.27	87.01	50	125	0.86
PCB2	138.924	69.97	50	125	1.07
PCB3	306.384	54.67	50	125	1.37
PCB4	525.288	43.08	50	125	1.74
PCB4 +HSINK	525.3+Hsink	34.50	50	125	2.17

Important considerations for the design of a power supply could be summarized as:

- $P_{MG\ tot}$=1.74 W maximum power with 525 mm^2 of copper area without heatsink
- $P_{MG\ tot}$ =2.17 W with additional 27 °C/W heatsink

Taking care of these limit values and depending on the topology, a designer can fix definitively the maximum power associated to the whole converter operating at a well-defined switching frequency.

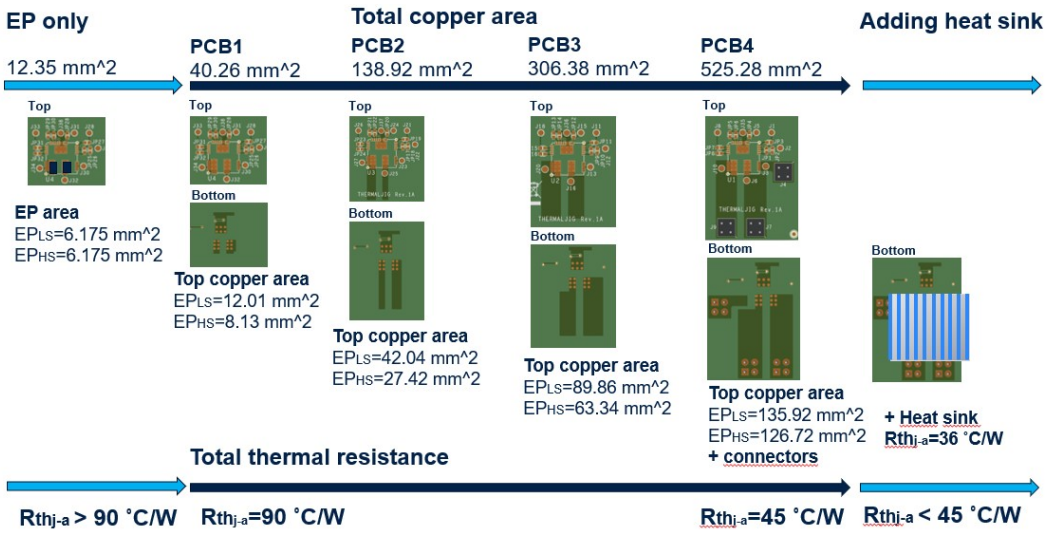
These numbers serve to define the maximum power available using only the dissipation area of the PCB.

Finally, it allows us to understand how the final application is compact and if the heatsink is needed.

4 PCB design summary and conclusions

Figure 16 shows the evolution of the thermal resistance starting from a very small PCB copper area corresponding to an exposed pad area of over 500 mm^2. The trend evolution has then been studied applying a small dissipator to the bottom face of the bigger PCB board.

Figure 16. Thermal resistance variation vs. PCB copper area



It has been observed that MasterGaN combined with a standard FR4 1.6 mm-2 layers-2 oz (70 um) PCB needs almost a total dissipating copper area of 525 mm^2 in order to reach a total R_{th} of about 45 °C/W and dissipates 1.74 W from the two EPs (ΔT=75 °C).

Further thermal resistance reduction to about 35 °C/W could be reached only adding a small sized heatsink on the back PCB side. In this way, the power dissipated could increase up to 2.17 W (ΔT=75 °C) (Table 2).

5 PCB thermal design example in PFC preregulators

In this section, a practical GaN PCB design has been realized and tested on a synchronous power factor corrector preregulator [5] . In this topology, the high variation of the input mains voltage forces a high peak current into the main switch between the boost inductor and ground. The selected topology of the synchronous PFC boost lends itself to putting the MASTERGAN1 in critical thermal condition.

5.1 EVLMG1 PFC release 0 vs. release 1

The EVLMG1 PFC is a MASTERGAN1 based solution that allows a synchronous PFC boost operating both CCM and TM mode depending on the controller [3] ,[4] .

CAD simulations of Figure 17 have been provided to study the heat path in the PCB, splitting the applied power side by side and then evaluating the final effect on the package.

At thermal regime, it has been confirmed that the two dissipating GaN can be seen as a single heat source above the two exposed pads area of the package.

However, it has been observed that the best solution is to increase the area of one side proportionally to its amount of power dissipated. In this design 70% of losses is dissipated on the low-side exposed pad and only 30% on the high-side and, as consequence, the copper area has been designed asymmetrically.

Figure 17. PCB R1 thermal CAD simulations

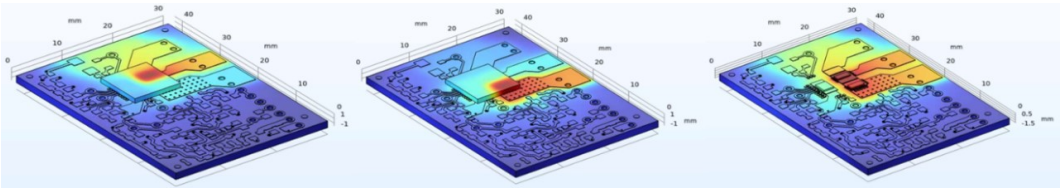
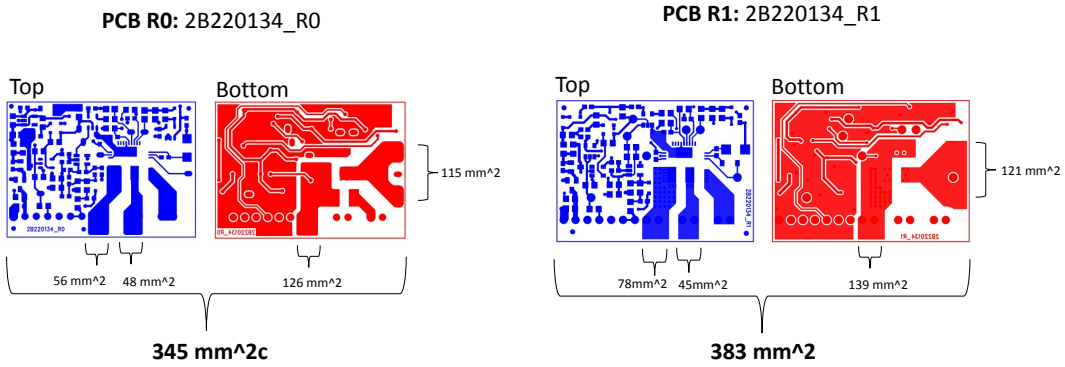


Figure 18 shows the first release PCB R0 compared with the second release PCB R1.

Figure 18. EVLMG1 PFC R0 vs. R1 PCB area comparison



About 70% of the power dissipation is in the low-side switch and for that reason the copper area around the exposed pad EP2 has been increased and it is not symmetrical in respect to the high-side copper area of EP3.

Previous studies have been applied here to improve the thermal aspects passing from rev.0 to rev.1. The copper area improvements are highlighted in red in the following Table 3.

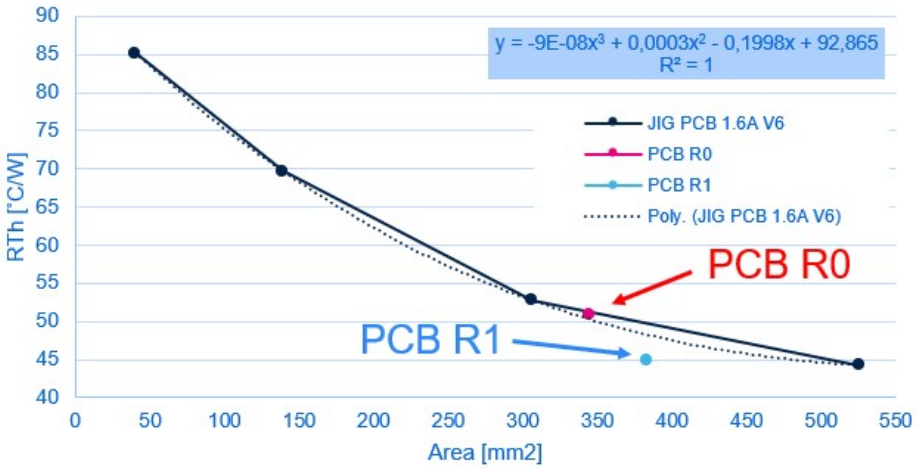
Table 3. EVLMG1 PFC R0 vs. R1 PCB area comparison

PCB release	Top–low-side area (mm^2)	Top–high-side area (mm^2)	Bottom–low-side area (mm^2)	Bottom–high-side area (mm^2)	Total copper area (mm^2)	TH Vias under EP	Ext.TH Vias
PCB_R0	56	48	126	115	345	5	0
PCB_R1	78 (+40%)	45 (-0.6%)	139 (+5%)	121 (+5%)	383 (+11%)	5	+30

The low-side area is deliberately larger because the topology provides for greater dissipation on the LS switch. The number of TH VIAS under exposed pads has not been changed but thirty TH VIAS have been added close to the EP2 area of the low-side to help thermal dissipation.

PCB 1,6 A V 6 (1.6 mm, 6 TH VIAS under EPs of MASTERGAN1) plot has been here considered and the polynomial trend has been extracted and reported in Figure 19.

Figure 19. R_{th} vs. PCB area

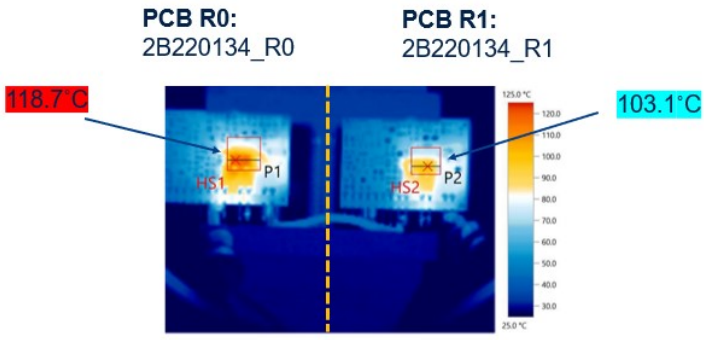


The polynomial trend can be expressed with the following Eq. (6):

$$Rth = 92.8 - 0.2 \cdot A_{PCB} + 3 \times 10^{-4} \cdot {A_{PCB}}^2 - 9 \times 10^{-8} \cdot {A_{PCB}}^3 \quad (6)$$

The first PCB of EVLMG1 _PFC R0 is made by a standard two-layer 1,6 mm thickness and only five TH VIAS have been placed on the two GaN EPs.

Figure 20. Thermal map comparison in static conditions



As shown in Figure 20, comparing two solutions, the PCB R1 stays 15 ˚C cooler in respect to the previous version with an estimated thermal resistance reduction of about 7 ˚C/W.

PCB R0 with about 52 ˚C/W and a total copper area of 345 mm^2 is on the trend and shows that the model can predict R_{th} of a generic MasterGaN board.

Second release PCB R1 with a total copper area of 383 mm^2 shows a thermal resistance lower than predicted (about 45 ˚C/W) because thirty TH VIAS have been added around the exposed pads to increase low-side dissipation.

6 References

[1]
“High power density 600 V half-bridge driver with two enhancement mode GaN HEMT” MASTERGAN1 datasheet on www.st,com

[2]
“High power density 600 V half-bridge driver with two enhancement mode GaN HEMT” MASTERGAN4 datasheet on www.st.com

[3]
“CCM PFC controller with high voltage startup” L4985 datasheet on www.st.com

[4]
“10-pin transition mode PFC controller” L6564 Datasheet on www.st.com

[5]
Levati, F. (2020, September). Testing GaN HEMT Performance in High Power Factor Solutions. In *2020 AEIT International Annual Conference (AEIT)* (pp. 1-6). IEEE.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
21-Feb-2023	1	Initial release.

Contents

List of tables

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