Application note

High power inverse buck for dimmable LED application with MASTERGAN4, HVLED002 and VIPER06XS

Introduction

This document describes the EVLMG4-500WIBCK evaluation board, designed to drive a dimmable LED load with a GaN-based, synchronously rectified inverse buck topology. The switching element and diode are replaced by the MASTERGAN4, mounted on a daughterboard to obtain a compact and scalable application.

The inverse buck stage works in CCM (continuous current mode), in which the turn-on commutation of the low-side switch occurs in hard switch. The improvement is given by the MASTERGAN4, which increases the efficiency by substituting the traditional diode with an actively driven GaN transistor, in fact, this technology does not have the reverse recovery losses and minimizes the conduction losses of the rectifier switch.

The HVLED002 controller manages the inverse buck mainly composed by T1 and MASTERGAN4.

The supply of the HVLED002 is generated by the VIPER06XS, that converts the input voltage of the buck into the voltage needed at the V_i pin, eliminating the need of an external power supply.

The circuit is shipped configured to generate 1A, but different output currents are selectable by changing the shunt resistor combination on the daughterboard with the MASTERGAN4.

The board operates with 400 V input voltage and output voltage range between 150 V and 350 V.

The constant current over the entire output voltage range is guaranteed using the fixed-off-time algorithm.

A dimming circuit is present on the board. It consists of two circuits: the analog and PWM circuit. It enables the regulation of the output current between 100% and 0%. Based on its input voltage, one of the two circuits is automatically activated. If LED dimming is not required, the dimming voltage may not be applied. In this case the output current is fixed and is the maximum allowed.

1 Schematics

Figure 1. EVLGM4-500WIBCK daughterboard

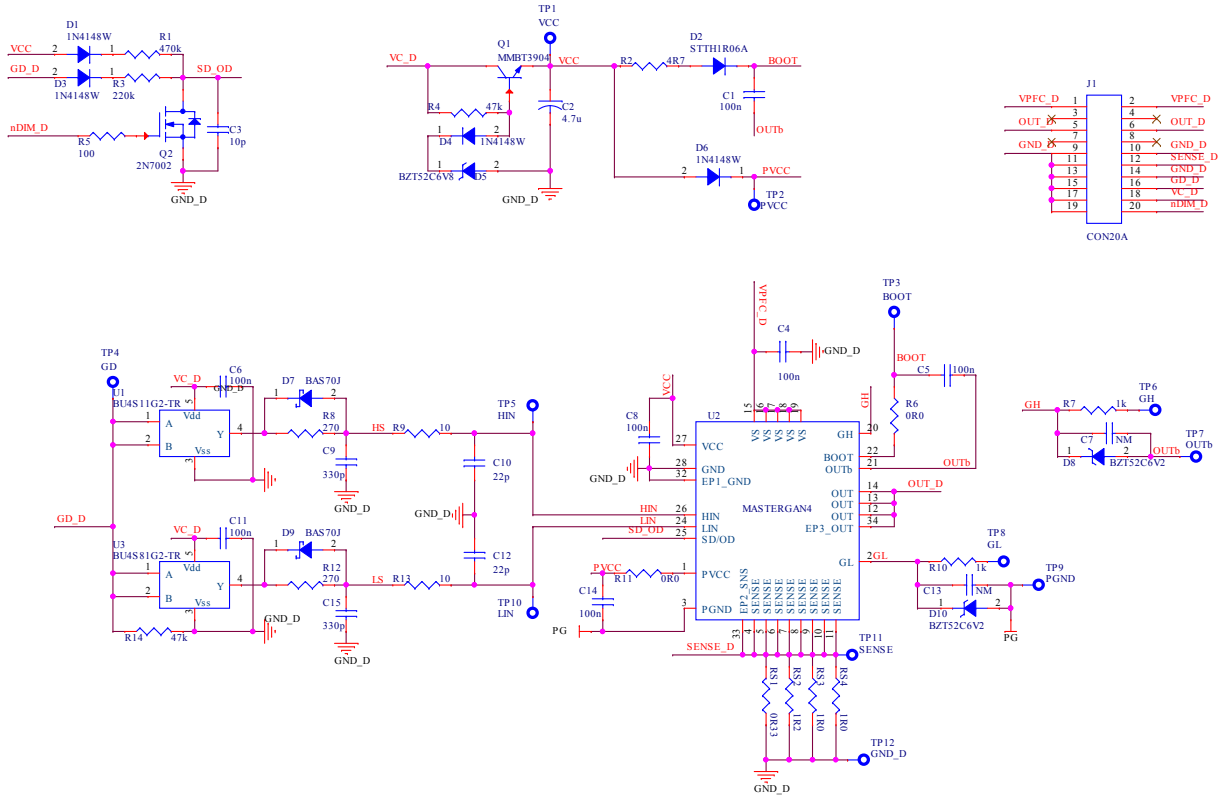
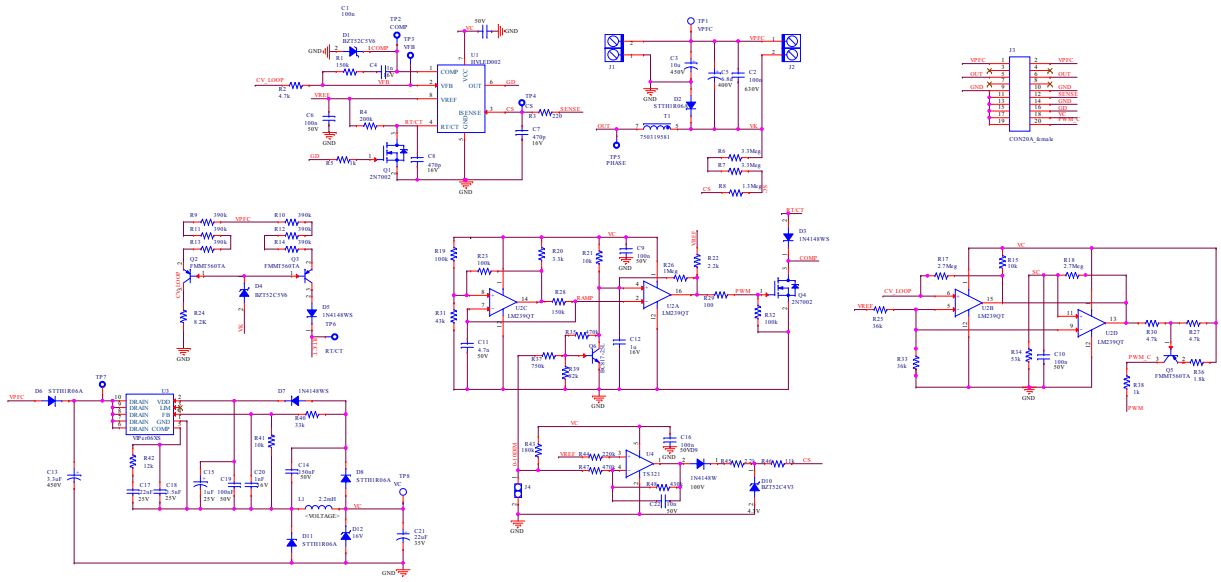


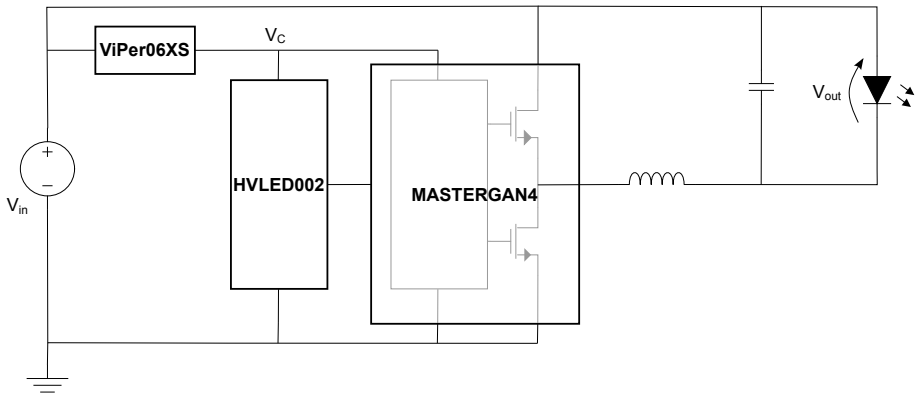
Figure 2. EVLGM4-500WIBCK motherboard



2 Basic equation for the inverse buck converter

This section describes the basic equations of the inverse buck working in CCM. As shown below, the working principle is the same as standard buck.

Figure 3. Inverse buck with MASTERGAN4, HVLED002, and VIPER06XS



During the on-time, the inductor current variation is:

$$\Delta I_{L,on} = \int_{t}^{t+t_{on}} \frac{1}{L} v(t)dt = \frac{1}{L}(V_{in} - V_{out})t_{on} \quad (1)$$

During the off-time:

$$\Delta I_{L,off} = \int_{t_{on}}^{t_{on}+t_{off}} \frac{1}{L} v(t)dt = \frac{1}{L} V_{out} t_{off} \quad (2)$$

The current variation must be the same during both intervals:

$$\Delta I_{L,on} = \Delta I_{L,off} \quad (3)$$

The duty cycle is defined as:

$$D = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on}+t_{off}} = \frac{V_{out}}{V_{in}} \quad (4)$$

3 Component dimensioning and frequency behavior

For the component dimensioning and the choice of the right inductor, a study of the frequency variation is requested.

The period is:

$$T = \frac{1}{f_{sw}} = t_{on} + t_{off} = \frac{\Delta I\, L}{V_{in} - V_{out}} + \frac{\Delta I\, L}{V_{out}}$$

Defined $V_{out} = kV_{in}$ with $k = 0, \ldots, 1$, the switching period can be rewritten:

$$T = \Delta IL \frac{V_{in}}{(V_{in} - kV_{in})kV_{in}}$$

and the frequency is:

$$f_{sw} = k(1-k)\frac{V_{in}}{\Delta IL}$$

Figure 4. Normalized switching frequency as a function of output voltage.

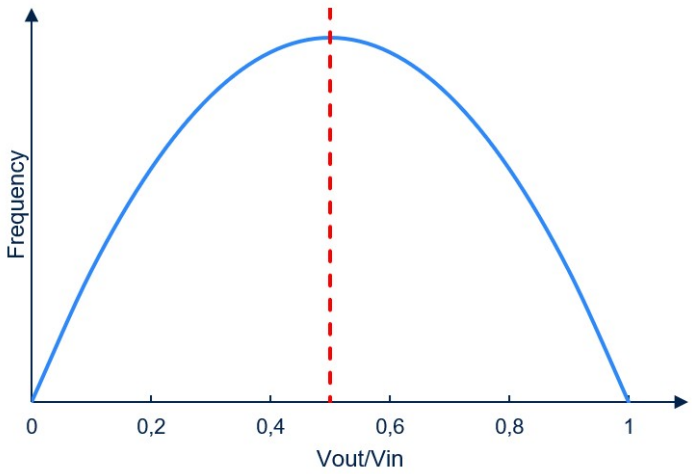


Figure 4 shows that the frequency has a parabolic behavior, with the maximum at output voltage equal to half the input voltage.

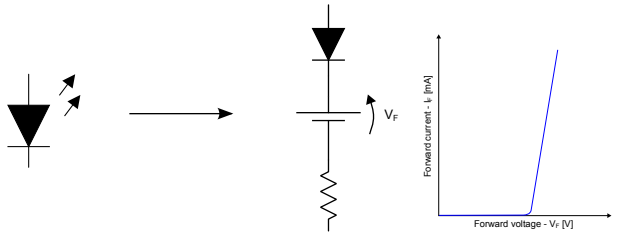
Once the maximum frequency is fixed, the inductor value is:

$$L = \frac{V_{out}(V_{in} - V_{out})}{\Delta I\, Vin\, f_{sw}}$$

4 Buck as current generator and fixed-off-time (FOT) algorithm

4.1 FOT algorithm description

Figure 5. LED structure



The inverse buck converter can be used as current generator to drive an LED string.

The constant current control is typically used when the LEDs are connected in series, in a string configuration. In this way, the same current flows in the LEDs, translating this, in a uniform brightness.

The LED structure can be modeled as in Figure 5, with an ideal diode, one equivalent on-resistance and a voltage generator.

Once the number of LEDs and consequently the output voltage is fixed, an embedded circuit is necessary to keep constant the average current that flows in the LEDs.

The average current is equal to:

$$I_{avg} = I_{peak} - \frac{\Delta I}{2}$$

To ensure that it remains constant, it is possible to act either on I_{peak} or on ΔI.

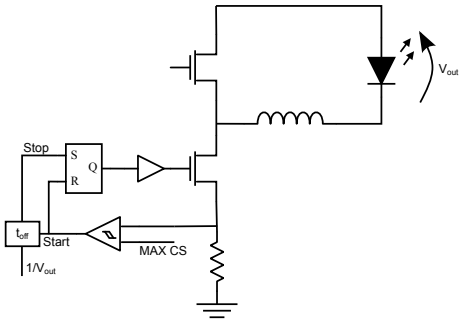
Acting on ΔI allows to use a simple peak current mode controller.

Recalling Eq 3, the easy way to control the ΔI is to properly modify the off-time. In fact:

$$t_{off} = \frac{1}{L} \Delta I V_{out}$$

Making the off-time inversely proportional to the output voltage, the ripple can be made ideally constant in any operating condition. This is the most important advantage of the fixed-off-time algorithm applied in LED lighting: it dramatically simplifies the control algorithm that does not require close control loop (and relevant compensation network) and allows to use easy controller.

Figure 6. FOT block diagram

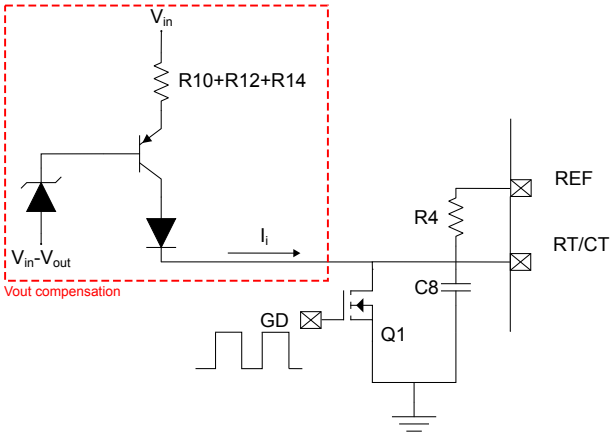


4.2 Constant output current with HVLED002

The MASTERGAN4 is driven by the HVLED002. This controller is a peak current mode PWM controller designed for lighting application.

By design, the HVLED002 sets the on- and off-time through the capacitor C8 and resistor R4, depending on the charge and discharge time of C8.

Figure 7. **FOT with HVLEDD002**



The FOT algorithm is implemented with a dedicated external circuit, as illustrated in Figure 7.
The on-time ends when the SENSE pin reaches the maximum current sense threshold (MAX CS).
During this time, the RT/CT pin is set low by the MOSFET Q1, controlled by the OUTPUT pin of the HVLED002.
At this point, the internal comparator switches the PWM latch, setting the OUTPUT pin low and starts the off-time.
With this configuration, based on C8, R4, and Q1, the off-time is fixed by the charge and the discharge of C8.
To obtain the inverse proportion between Vout and toff, different circuits are possible.
In accordance with the application, the user can choose the most appropriate solution.
The direct Vout reading compensation is shown on the board.
It is made by adding a current path between the buck's output and the RT/CT pin. In this way, a current proportional to Vout is injected and this changes the charge of C8. With:

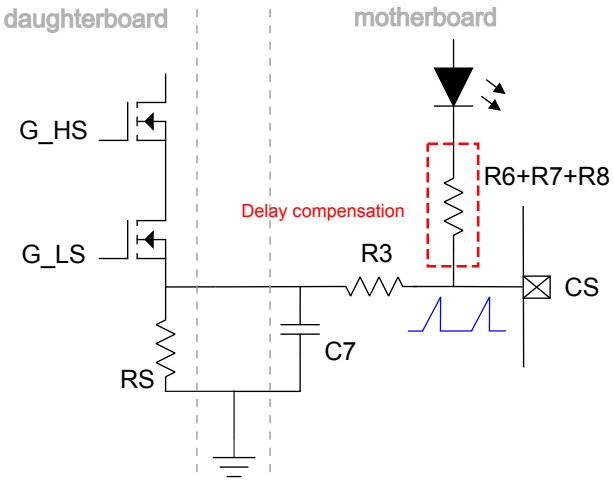
$$I = \frac{V_{pfc} - V_{BE} - V_z - V_k}{R10 + R12 + R14} \cong \frac{V_{out}}{R10 + R12 + R14}$$

The off-time ends when the RT/CT pin researches the maximum applicable voltage (Vcs).
Hence:

$$t_{off} = C_8 \frac{V_{cs}}{I} = C_8 V_{cs} \frac{R10 + R12 + R14}{V_{out}}$$

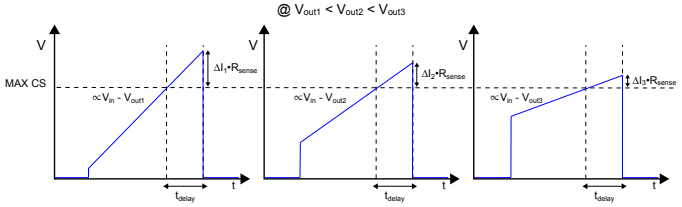
4.3 Output current variation given Vout

Figure 8. **Delay compensation basic schematic**



Nominally, thanks to the above described compensation technique, the output current should remain constant over the whole range of output voltages. This is true if the HVLED002 and MASTERGAN4 do not have any delays. Actually, both have some delay.

Figure 9. Voltage at sense pin of HVLED002



Even if the sense pin of HVLED002 detects the maximum input signal at time t_0, the sum of the propagation delays of MASTERGAN4's driver and the HVLED002 comparator causes an error on the inductor peak current that varies according to the output voltage.

To overcome this problem, an offset proportional to $V_{in} - V_{out}$ is inserted, through the resistance between V_k and CS.

Indeed, the real current seen at the output is:

$$I_{L,pk} = \frac{1}{L}(V_{in} - V_{out})\left(t_{on} + t_{delay}\right)$$

with the extra current due to delay:

$$I_{L,delay} = \frac{1}{L}(V_{in} - V_{out})t_{delay}$$

The necessary offset is equal to:

$$V_{cs,on} = I_{L,delay}\, R_{sense}$$

Inserting this offset, the reference voltage at the sense pin is no longer 0 V, but $V_{cs,on}$, and current variation is consequently reduced.

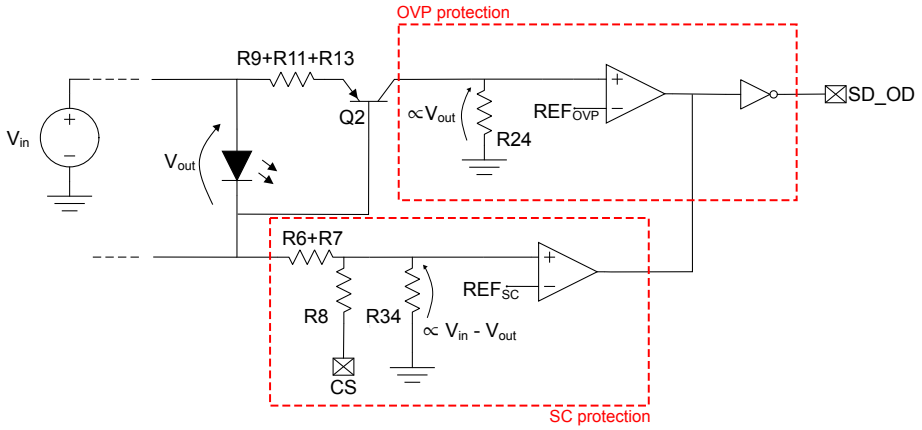
Increasing V_{out}, the extra current decreases and therefore the offset voltage decreases too and its contribution becomes negligible.

Choosing the right value of $R6, R7, R8$, the variation of output current caused by propagation delay is minimized.

5 Overvoltage and short-circuit protection

To prevent malfunctioning and possible damage to the board, two protections have been inserted: one for the overvoltage and the second one for the short-circuit. The two circuits are based on the LM239 comparator and drive the base of Q5, which is connected, through the connector, to the SD_OD pin of MASTERGAN4 to interrupt the GaN driving signal generation.

Figure 10. OV and SC protection



5.1 Overvoltage protection

The overvoltage protection is guaranteed by the R9, R11, and R13 path and by the one of four comparators embedded in the LM239.

The protection detects the V_{out} voltage and when the latter exceeds the maximum output voltage value, the current increases in the path and consequently the drop voltage across R24 increases (CV_LOOP).

When the reference voltage at the inverting pin of the comparator is exceeded, the output's trigger goes down and therefore, PWM_C goes high. PWM_C is connected through J3 and Q2 on the daughterboard at the SD_OD pin of MASTERGAN4, disabling any switching activity.

Contemporarily, the COMP pin goes down and the HVLED002 stops working.

5.2 Short-circuit protection

The circuit that detects the short-circuit works in the same way as the overvoltage protection: the output of the second trigger goes down when the signal of the non-inverting pin reaches the threshold voltage.

In this case, on the contrary, the current path is no longer proportional to V_{out}, but to $V_k = V_{in} - V_{out}$, thus making it possible to detect when the load is lower than the minimum operating level.

Also in this case, the short-circuit protection disables the MASTERGAN4.

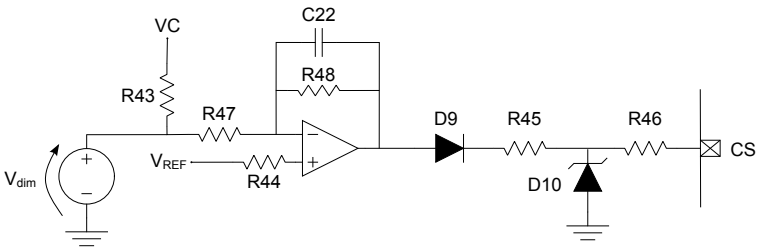
6 Dimming

It is possible to modify the light intensity by just changing the output current for the given V_{out}. To do this, two dimming circuits are embedded: the first one, named analog dimming, and the second one, named PWM (or digital) dimming. The current variation obtained with this circuit combination has linear characteristics: a remote control can implement different characteristics.

Both circuits are controlled by the J6 connector and automatically become active when the J6 voltage enters their respective operating ranges.

6.1 Analog dimming

Figure 11. Analog dimming



The purpose of the analog dimming circuit is to modify the average LED current. Adjusting the input voltage on connector J6, it is possible inject an offset voltage on pin CS and modify the peak current threshold of the HVLED002.

Indeed, the output voltage of the op amp's analog dimming is:

$$V_{OA,dim} = V_{ref}\left(1 + \frac{R48}{R47}\right) - V_{dim}\left(\frac{R48}{R47}\right)$$

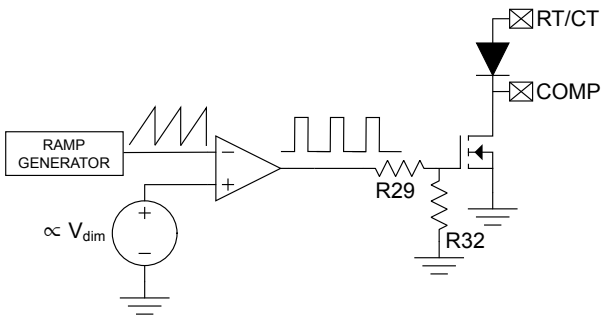
This voltage is translated to an offset.

Initially, the input voltage of the J6 connector is set at its maximum. Decreasing its voltage, the analog dimming circuit injects an offset signal as large as the J6's voltage decrease; in this way, the mean output current decreases since the peak current is set by the sense pin of the HVLED002.

Decreasing the output current means decreasing both the peak and the minimum values of inductor current. In order to avoid the adoption of a complex circuit to prevent the high-side GaN to work in reverse mode, the analog dimming circuit is designed to operate as long as the minimum current is equal or greater than 0.

6.2 PWM dimming

Figure 12. PWM dimming



When analog dimming reaches minimum dimming level, the PWM dimming circuit becomes active.

The output voltage of this circuit is a pulse modulated square wave with 5 V – 0 V amplitude, connected to the COMP pin. When PWM state is 0 V, the COMP pin is set high, providing the current according to analog dimming minimum level, while, when the PWM state is 5 V, the COMP pin is set low and the switching activity of the HVLED002 is stopped, providing zero output current. Contemporarily, the PWM node is connected through the resistance R38 and the connector at the SD_OD pin. In this way, the MASTERGAN4 is disabled during inactive phase of the PWM dimming algorithm.

Decreasing the J6 voltage, the PWM high level percentage increases, further decreasing the output current too.

7 Power losses

One of the most important parameters of a power circuit is the losses. The latter are related to the efficiency, the higher the losses, the lower the efficiency.

In fact:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

The losses are responsible for heat that must be dissipated.

In this circuit the major contributions are given by the two GaN inside the MASTERGAN4, the inductance, the input and the output capacitance.

7.1 Power GaN losses

The losses associated to the GaN are mainly due to two mechanisms: the switching losses that occur every time the low and the high-side open and close and the conduction losses, due to the non-zero resistance when the switching is closed.

7.1.1 GaN switching losses

In the inverse buck, the circuit works in hard switching. This means that the low-side switch is closed/opened when the voltage of drain capacitance is non-zero and the high-side switch is carrying some current: this results in losses during switching.

The switching losses are given by two fundamental contributions: the output capacitance losses of GaN and the crossover losses.

The output capacitance losses are equal to:

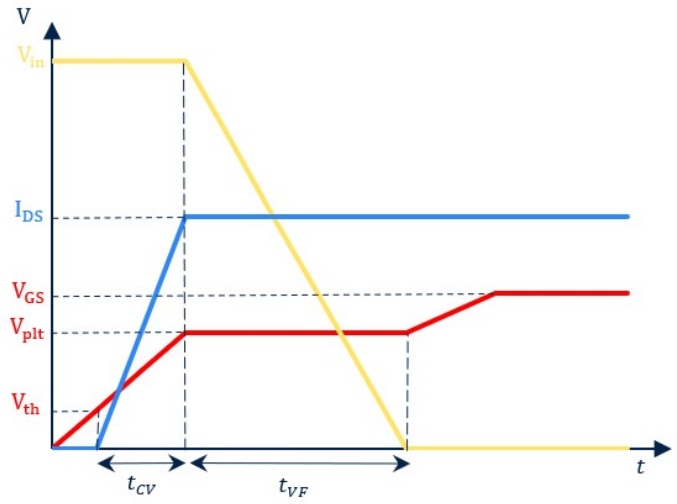
$$P_{Coss} = \frac{1}{2}(C_{oss,LS} + C_{oss,HS} + C_{par,l})V_{in}^2$$

with $C_{par,l}$ the parasitic capacitance of the inductor.

The crossover losses are present due to the “Miller Plateau”, that is, due to the fact that V_{gs} does not increase linearly.

For crossover losses, a distinction must be made between switching on and switching off.

Figure 13. Zoom during the turn-on crossover, highlighting the three fundamental waveforms



During the switching on:

$$P_{cross,ON} = \frac{1}{2} V_{in} I_{out,min}(t_{CR} + t_{VF}) f_{sw}$$

with:

- t_{CR} : the time required to bring the current equal to I_D.

$$t_{CR} = \frac{Q_{gs}}{I_g}$$

with Q_{gs} from graph and

$$I_g = \frac{V_g}{R_{g,on}}$$

In this case, the voltage applied at the gate is equal to:

$$V_g = V_{drive,on} - \left(\frac{V_{plateau} + V_{th}}{2}\right)$$

- t_{VF} : the time required to bring the voltage between drain and source to 0.

$$t_{VF} = \frac{Q_{gs}}{I_g}$$

with Q_{gs} from graph and

$$I_g = \frac{V_g}{R_{g,on}}$$

In this case, the voltage applied at the gate is equal to:

$$V_g = V_{drive,on} - V_{plateau}$$

During the switching off:

$$P_{cross,OFF} = \frac{1}{2} V_{in} I_{out,max} (t_{VR} + t_{CF}) f_{sw}$$

with:

- t_{VR} : the time required to bring the voltage between drain and source to V_{in}.

$$t_{VR} = \frac{Q_{gs}}{I_g}$$

with Q_{gs} from graph and

$$I_g = \frac{V_g}{R_{g,off}}$$

In this case, the voltage applied at the gate is equal to:

$$V_g = V_{plateau} - V_{drive,off}$$

- t_{CF} : the time required to bring the current to 0.

$$t_{CF} = \frac{Q_{gs}}{I_g}$$

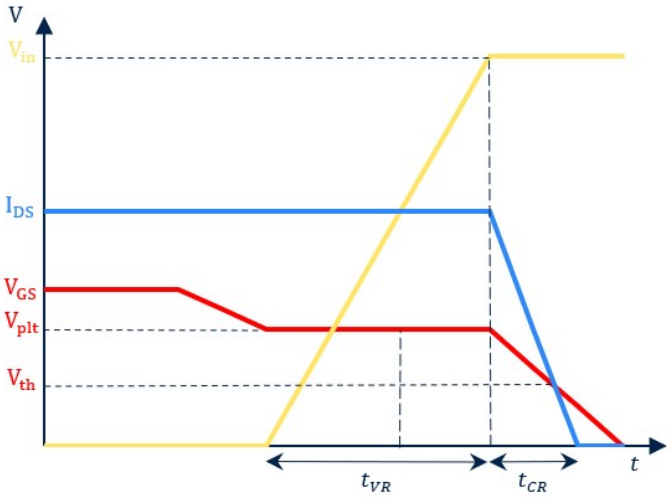
with Q_{gs} from graph and

$$I_g = \frac{V_g}{R_{g,off}}$$

In this case, the voltage applied at the gate is equal to:

$$V_g = \left(\frac{V_{plateau} + V_{th}}{2}\right) - V_{drive,off}$$

Figure 14. **Zoom during the turn-off crossover, highlighting the three fundamental waveforms**



These two losses appear to be the dominant ones regarding switching losses. However, they are not the only ones present; although negligible, there are losses due to gate charge and deadtime between low and high-side.

The losses due to the gate charge are:

$$P_g = (C_{g,HS} + C_{g,\ LS})\, V_{gs}^2\, f_{sw}$$

where $C_{g,HS}$ is the total capacitance at high-side and $C_{g,LS}$ is the total capacitance at low-side.

Another loss present is due to the reverse conduction of the high-side GaN during deadtime between the switch-off and the switch-on of the two sides. To minimize these losses, an optimum deadtime is necessary.

The deadtime losses are equal to:

$$E_{dt} = \left(I_{l,\ min}\, V_{gs1,\ rev}\, t_{sd1}\right) + \left(I_{l,\ max}\, V_{gs2,\ rev}\, t_{sd2}\right)$$

During the deadtime the GaN works in reverse conduction and develops a reverse voltage, depending on how much current flows and is shown from the datasheet: this effect represents a noticeable difference compared with Silicon Fets operation where reverse current, flowing into the body diode, generates a reverse voltage drop of around 1 V almost independently from reverse current.

7.1.2 GaN conduction losses

The conduction losses are related to non-zero resistance of GaN when the switching is closed and is equal to:

$$P_{cond} = I_{rms}^2\, R_{on}\left(T_j\right)$$

Regarding rms current, it is necessary to distinguish between current flowing during t_{on} and during t_{off}.

During t_{on}, the current flows in the low-side, consequently the conduction losses are associated to GaN at the low-side.

The rms current is equal to:

$$I_{rms,\,on}^2 = \frac{1}{T}\int_{t_0}^{t_0 + DT}\left(I_{MIN} + \frac{\Delta I}{DT}t\right)dt$$

$$= D\left(I_{OUT}^2 + \frac{\Delta I^2}{12}\right)$$

The high-side conduction losses are indeed associated during the t_{off} and is:

$$I_{rms,\,off}^2 = \frac{1}{T}\int_{t_0 + DT}^{T}\frac{1}{1-D}\left(-\frac{\Delta I}{T}t + I_{MAX} - DI_{MIN}\right)dt$$

$$= \left(1 - D\right)\left(I_{OUT}^2 + \frac{\Delta I^2}{12}\right)$$

The resistance is derived from the graph and depends on temperature junction temperature operation and driving voltage.

7.2 Inductance losses

The inductance losses are the sum of three contributions:

$$P_{ind} = P_{core} + P_{DC,ind} + P_{AC,ind}$$

The core losses are related to the non-linearity and hysteresis of the magnetic field and are typically provided by the manufacturer.

Regarding $P_{DC,ind}$ and $P_{AC,ind}$, these losses are due to the parasitic resistance of the inductance.

The DC losses are defined:

$$P_{DC,\ ind} = I_{rms}^2 R_{DC}$$

The AC losses are defined:

$$P_{AC,\ ind} = I_{rms,AC}^2 R_{AC}$$

with

$$I_{rms,AC} = \frac{\Delta I}{2\sqrt{3}}$$

and the AC resistance is more difficult to find and depends on the operating frequency.

7.3 Input and output capacitance losses

To calculate the losses due to the input and output capacitance, it is necessary use the equivalent series resistance (ESR), this parameter takes into account the non-ideality of the capacitances.

For the input capacitance losses, it is necessary to calculate the rms current and it is approximately equal to:

$$I_{rms,Cin} = \frac{I_{out}}{V_{in}}\sqrt{(V_{in} - V_{out})V_{out}}$$

So:

$$P_{Cin} = ERS_{Cin} I_{rms,Cin}^2$$

The output capacitance losses are equal to:

$$P_{Cout} = I_{rms,ac}^2 ESR_{Cout}$$

8 EVLMG4-500WIBCK measurements

Figure 15 shows the efficiency of the board for a target current Iout = 1 A, with the maximum efficiency for a Vout = 350 V and equal to 99,46%.

Figure 15. Efficiency vs. load

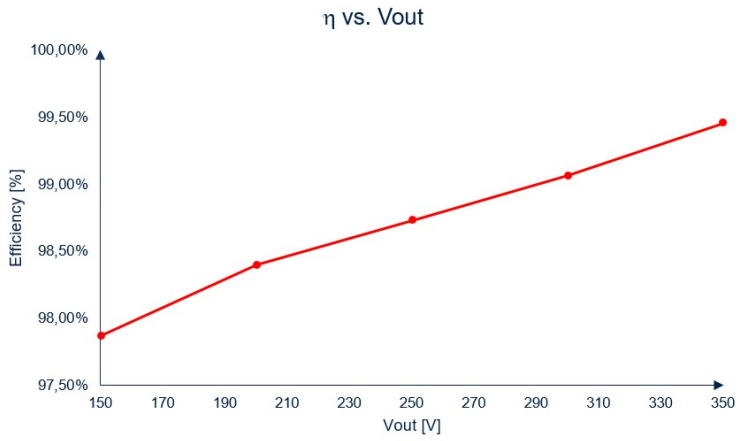


Figure 16 shows, indeed, the output variation in function of the output voltage, with ΔI = 5.12%.

Figure 16. Iout vs. load

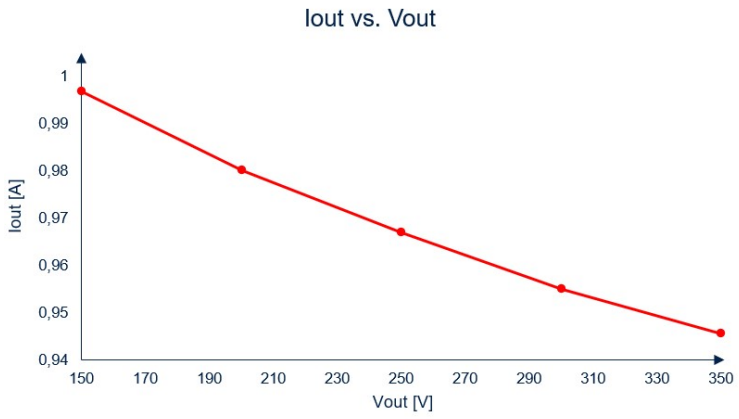
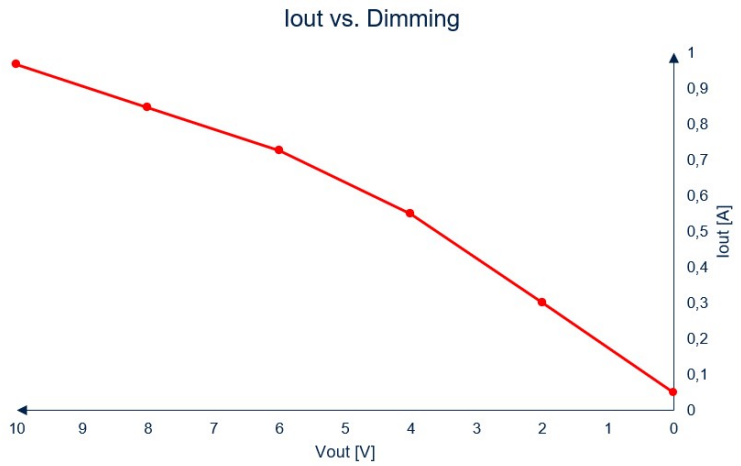


Figure 17 shows the decreasing of the current in function of the dimming input. The measurement is made with Vout = 250 V.

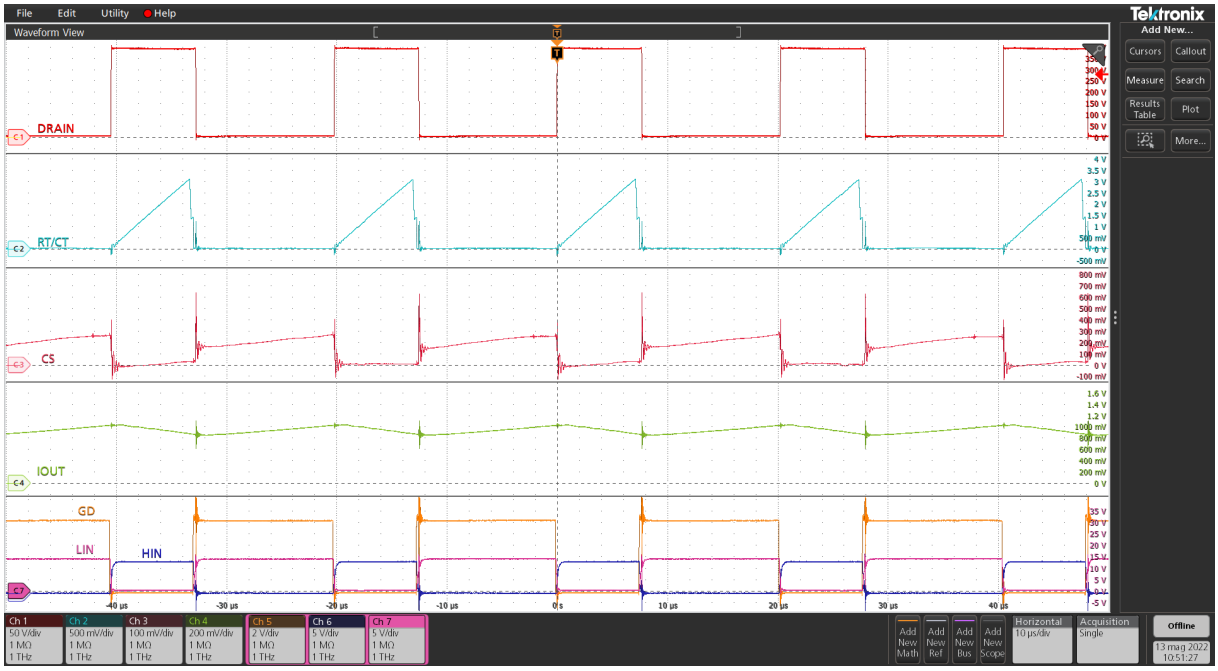
Figure 17. **Iout vs. dimming**



9 EVLMG4-500WIBCK waveforms

Figure 18 shows the signal behavior at steady-state conditions with Iout = 1 A and Vout = 250 V.

Figure 18. EVLMG4-500WIBCK steady-state at Vout = 250 V



Ch1: Drain – Ch2: RT/CT (TP6 on M) – Ch3: CS (TP4 on M)

Ch4: IOUT – Ch5: GD – Ch6: HIN (TP5 on D) – Ch7: LIN (TP10 on D)

Here below in Figure 19 and in Figure 20, the signal behavior when an overvoltage and overcurrent, respectively, are present at the output.

Figure 19. EVLMG4-500WIBCK overvoltage protection

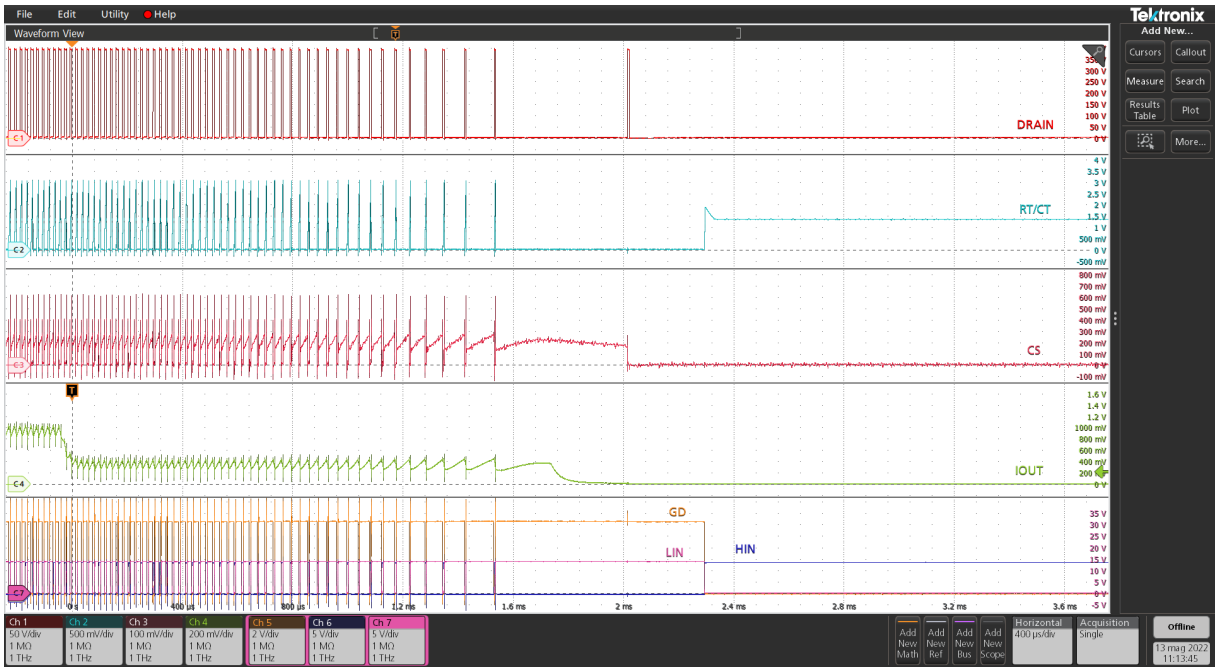
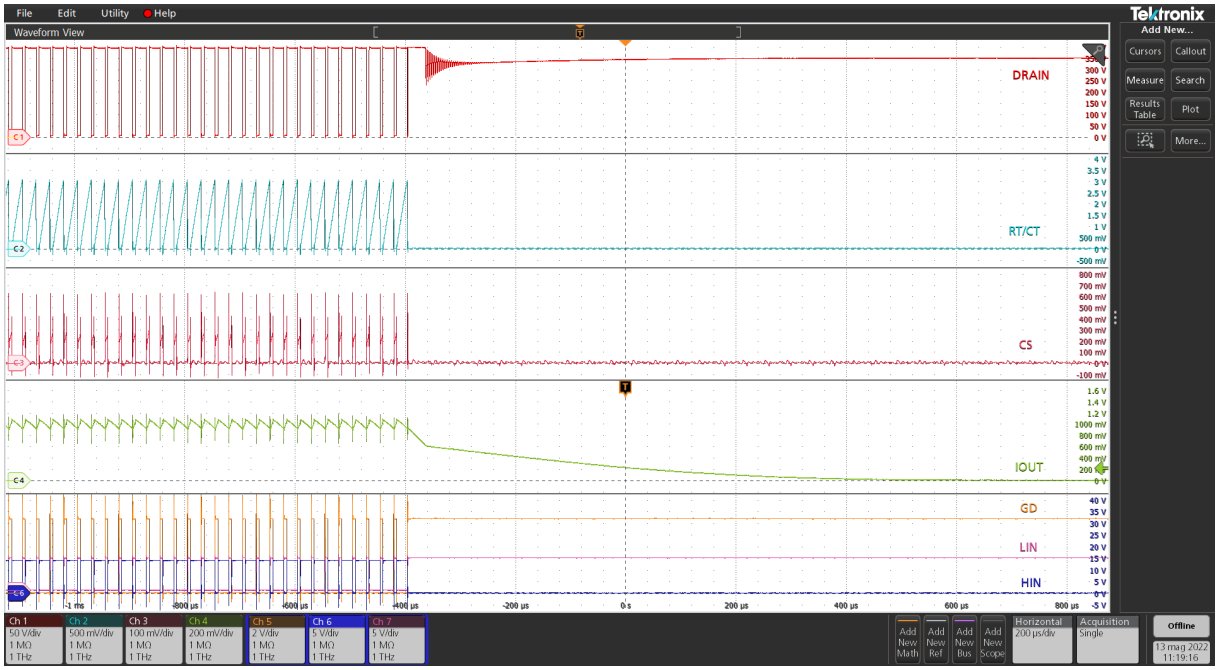


Figure 20. **ELVMG4-500WIBCK overcurrent protection**



In Figure 21 and Figure 22, the signal behavior when the lighting intensity of LED change is shown. In particular, in Figure 21 the analog dimming and in Figure 22 the PWM dimming is active.

Figure 21. **EVLMG4-500WIBCK analog dimming**

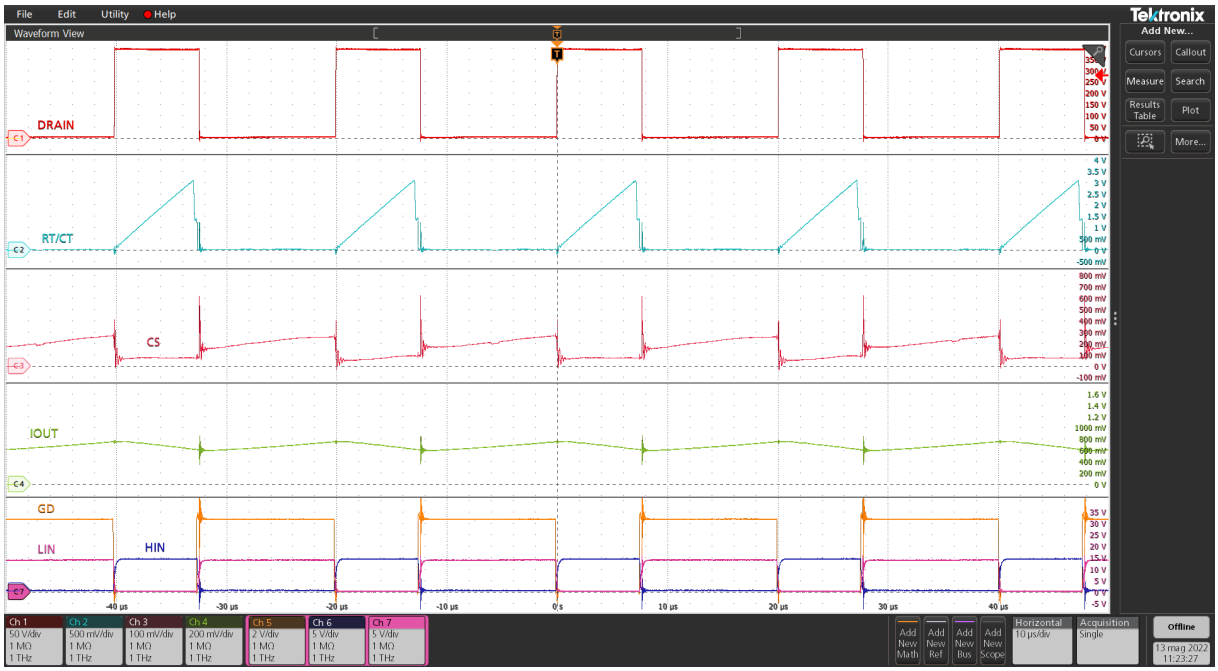
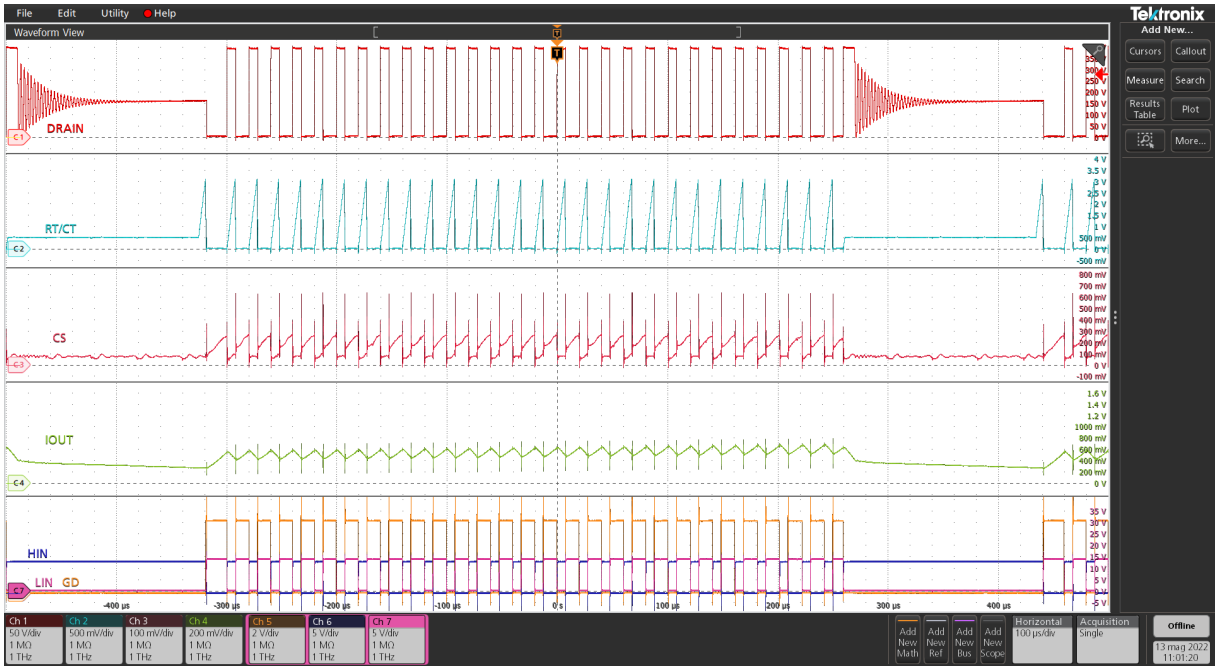


Figure 22. **EVLMG4-500WIBCK PWM dimming**

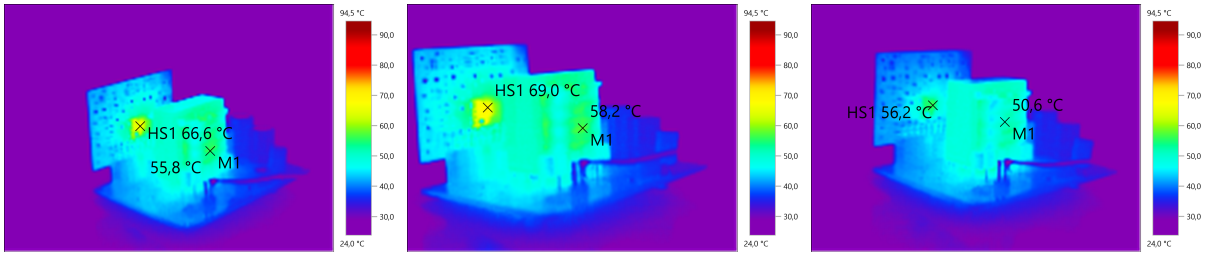


10 EVLMG4-500WIBCK thermal picture

Figure 23 shows the thermal map on the board when the output current is 0.7 A. The three figures show the different temperature for three different numbers of LEDs. More precisely, in (a) the output LED has a Vout = 150 V, in (b) the output LED has a Vout = 200 V, in which the frequency is maximum, and in (c) the output LED has a Vout = 350 V.

The HS1 point corresponds to the hottest point of the board, the MASTERGAN4 and M1 point the inductor temperature.

Figure 23. Thermal map for Iout = 0.7 A

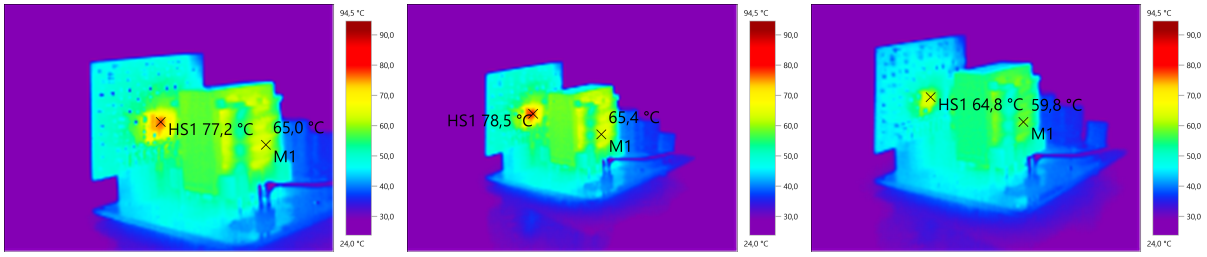


(a) (b) (c)

Figure 24 shows the thermal map on the board when the output current is 1 A. As in the previous figure, the three figures show the thermal temperature for (a) Vout = 150 V, (b) Vout = 200 V (maximum frequency) and (c) Vout = 350 V.

HS1 is the hottest point (MASTERGAN4) and M1 the inductor temperature.

Figure 24. Thermal map for Iout = 1 A

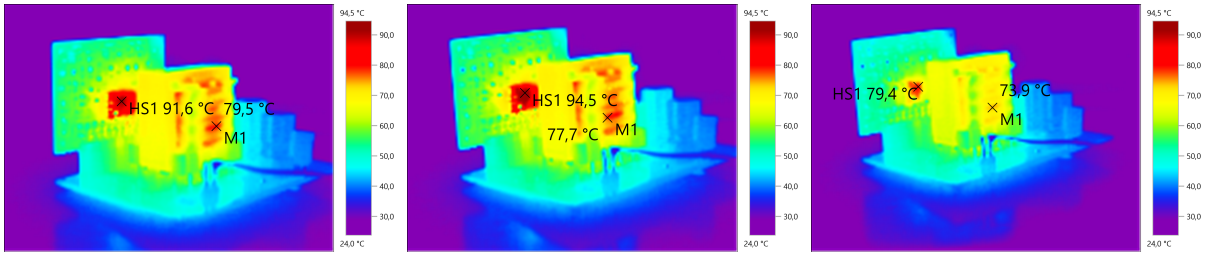


(a) (b) (c)

Figure 25 shows the thermal map on the board when the output current is 1.3 A. In (a) Vout = 150 V, (b) Vout = 200 V (maximum frequency) and (c) Vout = 350 V.

HS1 is the hottest point (MASTERGAN4) and M1 the inductor temperature.

Figure 25. Thermal map for Iout = 1.3 A



(a) (b) (c)

11 Benchmark with current technology

The use of GaN looks very promising as switching losses are reduced, due to the reduction of the parasitic gate capacitances and the absence of reverse recovery losses.

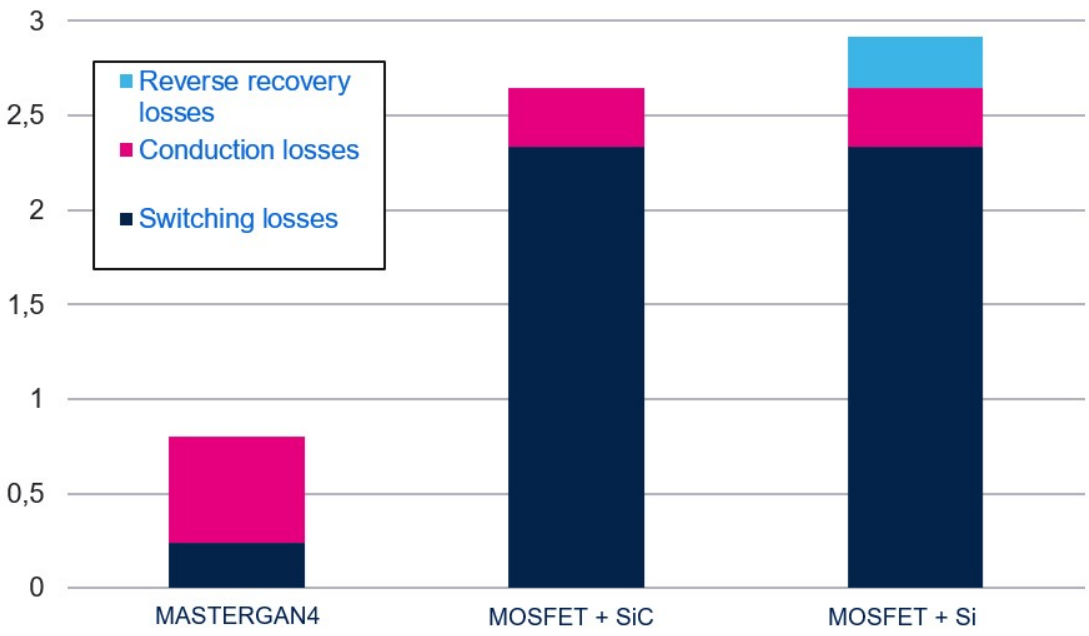
In this section, a benchmark with actual technology is made.

To do this, the actual daughterboard is first replaced with a daughterboard in which there is a MOSFET and a SiC diode, and then, the SiC diode is replaced with an Si.

The MOSFET (STF24N60M2) has an on-resistance very similar to the GaN on-resistance.

The first difference in this comparison is the high temperature of the MOSFET, which makes it impossible, without the use of a heatsink, to measure the maximum output average current (@Iout = 1.3 A).

Figure 26. Highlight the switching losses reduction



Revision history

Table 1. **Document revision history**

Date	Version	Changes
07-Nov-2022	1	Initial release.

Contents

List of tables

List of figures