Application note

AIS25BA: ultralow noise, wide bandwidth, 3-axis digital output accelerometer with TDM interface for automotive applications

Introduction

This document provides usage information and application hints related to ST's AIS25BA motion sensor.

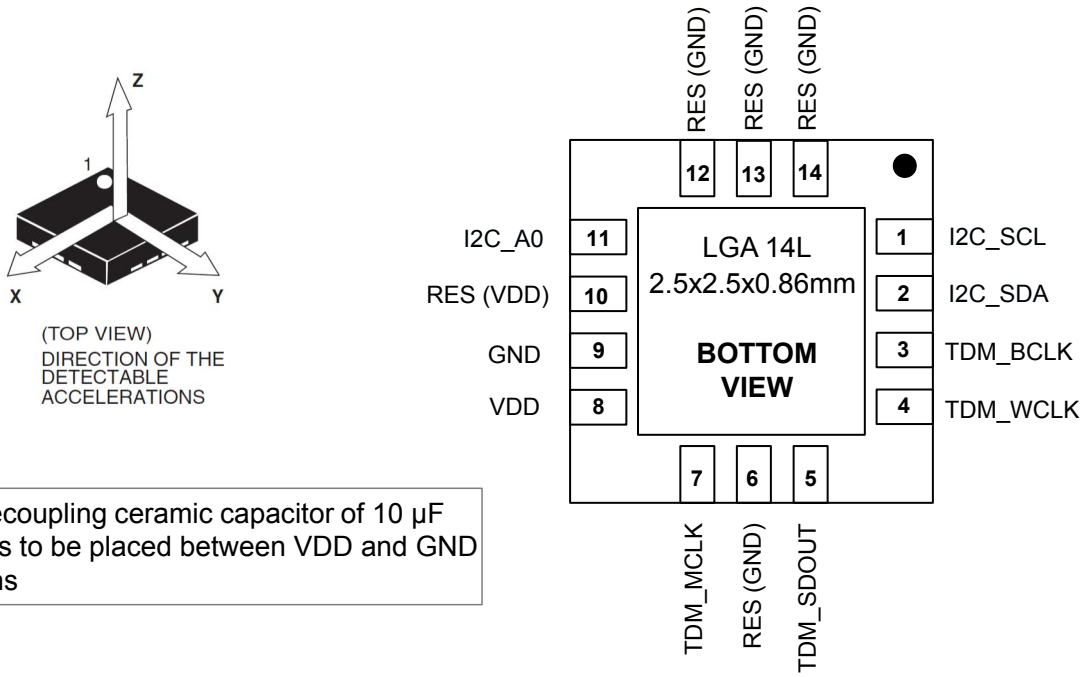
The AIS25BA is a high-performance 3-axis MEMS accelerometer with ultralow noise, low latency, wide and flat bandwidth, and a time-division multiplexing (TDM) interface designed to address automotive non-safety applications, in particular, road-noise cancellation (RNC) through active noise-control (ANC) techniques and vibration monitoring.

The device has a user-selectable full-scale acceleration range of ±3.85/±7.7 *g*, a 16-bit data output, and is capable of measuring accelerations with a signal bandwidth of 2400 Hz and just 266 µs latency.

The AIS25BA is available in a small thin plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +125 °C.

1 Pin description

Figure 1. Pin connections



Decoupling ceramic capacitor of 10 µF has to be placed between VDD and GND pins

Pin #	Name	Function	Pin status
1	I2C_SCL	I²C serial clock - SCL	Default: input open-drain
2	I2C_SDA	I²C serial data - SDA	Default: input open-drain
3	TDM_BCLK	TDM bit clock	Default: input open-drain
4	TDM_WCLK	TDM word clock	Default: input open drain
5	TDM_SDOUT	TDM serial data output	Default: input open-drain
6	RES (GND)	Connect to GND	Connect to GND
7	TDM_MCLK	TDM master clock	Default: input open-drain
8	VDD	Power supply	Power supply
9	GND	0 V power supply	0 V power supply
10	RES (VDD)	Connect to VDD	Connect to VDD
11	I2C_A0	I²C slave address selection	Default: input with pull-down
12	RES (GND)	Connect to GND	Connect to GND
13	RES (GND)	Connect to GND	Connect to GND
14	RES (GND)	Connect to GND	Connect to GND

2 Registers

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TEST_REG	0Bh	0	0	0	0	ST	0	0	0
WHO_AM_I	0Fh	0	0	1	0	0	0	0	0
TDM_cmax[11:8]	24h	0	0	0	0	TDM_ cmax11	TDM_ cmax10	TDM_ cmax9	TDM_ cmax8
TDM_cmax[7:0]	25h	TDM_ cmax7	TDM_ cmax6	TDM_ cmax5	TDM_ cmax4	TDM_ cmax3	TDM_ cmax2	TDM_ cmax1	TDM_ cmax0
CTRL_REG_1	26h	0	0	PD	0	0	0	0	0
TDM_CTRL_REG	2Eh	TDM_pd	Delayed	data_valid	mapping	0	WCLK_fq1	WCLK_fq0	0
CTRL_REG_2	2Fh	1	1	1	0	0	0	0	ODR_AUTO_EN
CTRL_REG_FS	30h	0	0	0	0	0	0	0	FS

3 Operating modes

The AIS25BA provides two operating modes:

- Disabled mode
- Normal mode

After the power supply is applied, the AIS25BA performs a 5.5 ms boot procedure to load the trimming parameters. After the boot is completed, the accelerometer is automatically configured in disabled mode.

The AIS25BA provides two interfaces:

- I²C digital interface, which is used to configure the device
- TDM interface, which is used to retrieve acceleration data

When the sensor is in disabled mode, almost all the internal blocks of the device are switched off. The I²C digital interface remains active to allow the communication with the device.

The AIS25BA can be configured in normal mode by setting the PD bit of the CTRL_REG_1 register to 0. In normal mode, the sensing chain is active.

In order to gather acceleration output data, the TDM interface must be enabled. It is recommended to set all TDM interface clocks (MCLK, BCLK, and WCLK) before enabling the interface itself. The TDM interface can be enabled by setting the TDM_pd bit of the TDM_CTRL_REG register to 0.

3.1 TDM interface configuration

The TDM interface can be configured through the TDM_CTRL_REG register.

Table 1. TDM_CTRL_REG (2Eh)

b7	b6	b5	b4	b3	b2	b1	b0
TDM_pd	Delayed	data_valid	mapping	0	WCLK_fq1	WCLK_fq0	0

- TDM_pd: enables TDM. If the TDM_pd bit is set to 0, the TDM interface is enabled, otherwise it is disabled.
- Delayed: TDM delayed configuration. If the Delayed bit is set to 0, TDM works with 'no-delayed' configuration, otherwise it works with 'delayed' configuration. Selecting 'no delayed' configuration, SLOT0 data is sampled on the first rising/falling edge (based on the value of the data_valid bit, as described below) after the rising edge of WCLK. Otherwise, selecting 'delayed' configuration, SLOT0 data is sampled on the second rising/falling edge after the rising edge of WCLK.
- data_valid: TDM data valid configuration. If the data_valid bit is set to 0, the data is sampled on the rising edge of the bit clock (BCLK), otherwise it is sampled on the falling edge.
- mapping: TDM mapping configuration. If the mapping bit is set to 0, accelerometer X-Y-Z data are mapped respectively in SLOT0, SLOT1, SLOT2, otherwise they are mapped in SLOT4, SLOT5, SLOT6. During the transfer of nonactive slots, the TDM_SDOUT pin is configured in high-impedance.
- WCLK_fq: TDM clock frequencies, described in the following section.

The AIS25BA offers four possible configurations for the TDM interface: the following table summarizes the Delayed and data_valid configuration associated to each supported TDM configuration.

Table 2. TDM configuration

Delayed	data_valid	TDM configuration
0	0	SLOT0 on first rising edge of BCLK after rising edge of WCLK
0	1	SLOT0 on first falling edge of BCLK after rising edge of WCLK
1	0	SLOT0 on second rising edge of BCLK after rising edge of WCLK
1	1	SLOT0 on second falling edge of BCLK after rising edge of WCLK

3.2 TDM clock frequency

The function of the WCLK signal is simply to identify the beginning of a frame; in particular the frame starts at the rising edge of the WCLK signal. The supported WCLK widths are:

- 16-slot width (1024 BCLK periods, 50% duty cycle)
- One-slot width (16 BCLK periods)
- One BCLK period

In TDM mode, the AIS25BA can output accelerometer data on the TDM_SDOUT pin at the following sampling rates:

- WCLK = 8 kHz
- WCLK = 16 kHz
- WCLK = 24 kHz

TDM clock frequency can be selected in two different ways:

- Using the WCLK_fq[1:0] bits of the TDM_CTRL_REG register. In this case, the ODR_AUTO_EN bit of the CTRL_REG_2 register must be set to 0. Available configurations for WCLK_fq bits are:
  - 00b: sampling rate equal to 8 kHz
  - 01b: sampling rate equal to 16 kHz
  - 10b: sampling rate equal to 24 kHz
- Using the output of the ODR_auto block (described in the AIS25BA datasheet) which receives as inputs both MCLK and the WCLK and computes the current sampling frequency as a ratio between MCLK and WCLK. The ODR_auto block can be enabled by setting to 1 the ODR_AUTO_EN bit of the CTRL_REG_2 register. Depending on the ratio between the MCLK and WCLK signals, the possible outputs of the ODR_auto block are:
  - sampling rate equal to 8 kHz (MCLK/WCLK = 1536)
  - sampling rate equal to 16 kHz (MCLK/WCLK = 768)
  - sampling rate equal to 24 kHz (MCLK/WCLK = 512)

Note: If the ratio between MCLK and WCLK differs from 1536, 768, and 512, the sampling is automatically forced to 8 kHz.

The sole purpose of the serial clock BCLK is to shift the data out of the serial TDM_SDOUT port. For this purpose, the TDM interface uses an internal counter that is set to one when the rising edge of the WCLK is detected, and it is reset to zero when the maximum number of BCLK in a WCLK period is reached.

The maximum number of BCLK contained in a WCLK period, called cmax, can be expressed as a function of both the BCLK and WCLK frequencies, and can be computed using the following equation:

$$cmax = \frac{BCLK}{WCLK} - 1$$

In order to support a serial clock BCLK variable in the range [1024 MHz, 12.288 MHz], and consequently to compute the correct maximum value of the internal TDM counter, two possible solutions can be selected:

- The cmax value at the input of the TDM interface can be computed automatically by the device. This functionality by default is enabled, and can be disabled by setting the ODR_AUTO_EN bit of the CTRL_REG_2 to 0.
- TDM cmax can be programmed through the register TDM_cmax.

3.3 Configuration switches

The TDM interface must be activated explicitly from the I²C interface. The first three samples after enabling the TDM interface must be discarded. This is due to the interface synchronization on the external WCLK. Moreover, the TDM protocol can be reconfigured on the fly, but also in this case the first three samples after the TDM configuration change will be invalid.

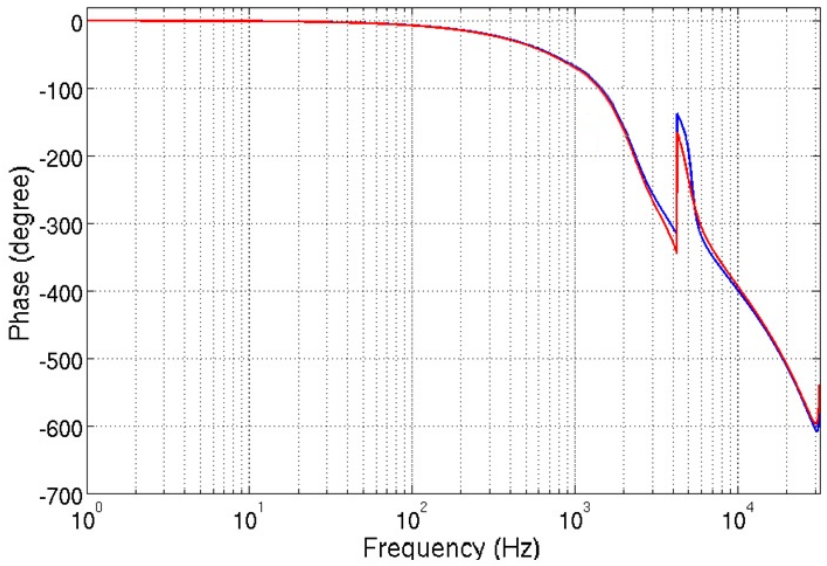
3.4 Latency

Latency is the time between an acceleration event applied to the AIS25BA and the measurement available on the TDM output channel.

There are three components that define the total latency of the signal chain:

- Sampling delay (T1): it is the delay corresponding to the time between the actual acceleration value and the internal value sampled at 64 kHz. The typical value of T1 is equal to 1 / 64 kHz = 15.625 µs.
- Phase delay (T2): it is the theoretical phase delay at the given input frequency, as shown in the AC response of the system in Figure 2 (the red line refers to the Z-axis, whereas the blue line refers to the X and Y axes). The typical value of T2 is equal to 215 µs in the range from 20 Hz to 2 kHz.
- Frame delay (T3): it corresponds to the delay between the time when the value is ready and when it is sent out through the TDM interface. The typical value of T3 is equal to 1 / WCLK (for example, for WCLK = 16 kHz, it corresponds to 1 / 16 kHz = 62.5 µs).

Figure 2. Frequency response - phase delay



The total latency is determined by the sum (T1 + T2 + T3) of these three components. Table 3 indicates the minimum and the maximum latency value for each WCLK value.

Table 3. AIS25BA latency values

WCLK	Min latency	Max latency
8 kHz	215 µs	355 µs
16 kHz	215 µs	300 µs
24 kHz	215 µs	270 µs

4 Reading output data

4.1 Startup sequence

Once the device is powered up, it automatically downloads the calibration coefficients from the embedded flash to the internal registers. When the boot procedure is completed, the accelerometer automatically enters disabled mode.

To turn on the accelerometer and gather acceleration data through the TDM interface, it is necessary to select the operating normal mode through the PD bit of the CTRL_REG_1 register and enable the TDM interface through the TDM_pd bit of the TDM_CTRL_REG register.

The following general-purpose sequence can be used to configure the accelerometer:

```
1. Write CTRL_REG_1 = 00h // Normal mode
2. Provide MCLK, BCLK and WCLK to TDM interface
3. Write TDM_CTRL_REG = 0xxx0000b // Enables TDM and selects configuration
4. Wait 4.5 ms // Wait the duration of the turn-on time
5. Start gathering acceleration data from the TDM interface
```

4.2 Understanding output data

The measured acceleration data are sent to the TDM interface slots configured through the mapping bit of the TDM_CTRL_REG register.

Acceleration output data are represented as 16-bit numbers in two's complement format.

Once retrieved from the active slots of the TDM interface, acceleration data must be converted to m*g* by multiplying the So sensitivity value. This sensitivity value depends on the selected full-scale range (refer to the datasheet). In detail:

- 0.122 m*g* / LSB (typ.) if the full scale is set to ±3.85 *g*
- 0.244 m*g* / LSB (typ.) if the full scale is set to ±7.7 *g*

4.2.1 Examples of output data

The following table provides a few basic examples of the accelerometer data that are read from the TDM output slots when the device is subjected to a given acceleration. The values listed are given under the hypothesis of perfect device calibration (that is, no offset, no gain error, and so forth).

Table 4. TDM output value vs. acceleration (full-scale = ±3.85 *g*)

Acceleration value [m*g*]	LSB (hexadecimal)	LSB (signed decimal)
0	0000h	0
350 m*g*	0B34h	2868
1000 m*g*	2004h	8196
-350 m*g*	F44Ch	-2868
-1000 m*g*	DFFCh	-8196

5 Self-test

The embedded self-test function allows checking the device functionality without moving it.

When the self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels, which are related to the full scale through the sensitivity value.

The accelerometer self-test function can be configured through the ST bit of the TEST_REG register. It is off when the ST bit is set to 0; it is enabled when the ST bit is set to 1.

When the accelerometer self-test is activated, the sensor output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

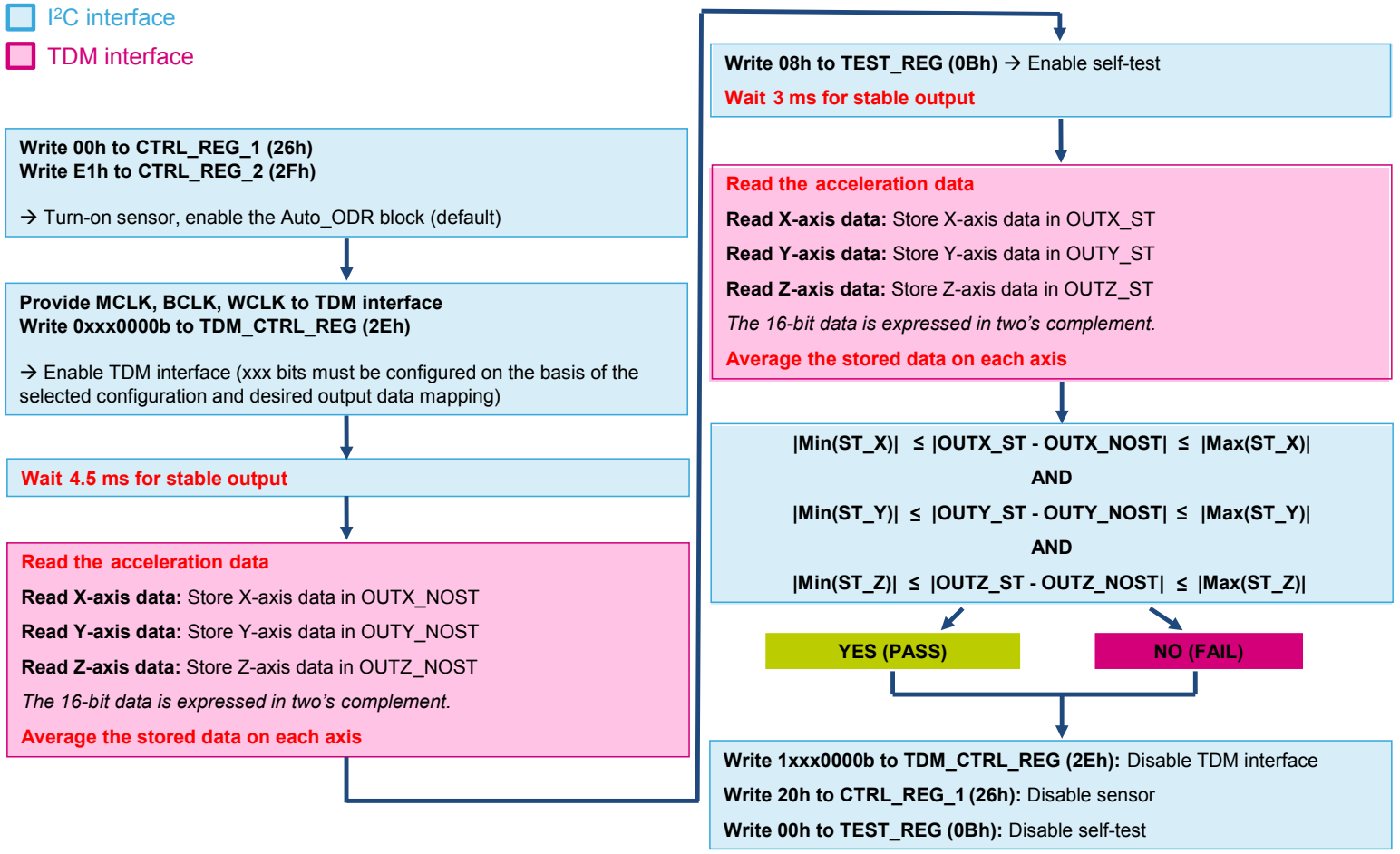
The procedure consists of:

1. enabling the accelerometer and TDM interface
2. averaging 5 samples before enabling the self-test
3. averaging 5 samples after enabling the self-test
4. computing the difference in absolute value for each axis and verifying that it falls within a given range. The minimum and maximum values are provided in the datasheet.

The complete self-test procedure is indicated in Figure 3. Accelerometer self-test procedure.

Figure 3. **Accelerometer self-test procedure**

Note: keep the device still during the self-test procedure



Revision history

Table 5. **Document revision history**

Date	Version	Changes
26-Sep-2022	1	Initial release

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