PM8805 PoE powered device interface, evaluation board

Introduction

This document describes the characteristics and functionality of the evaluation board, which is intended as a learning and development tool.

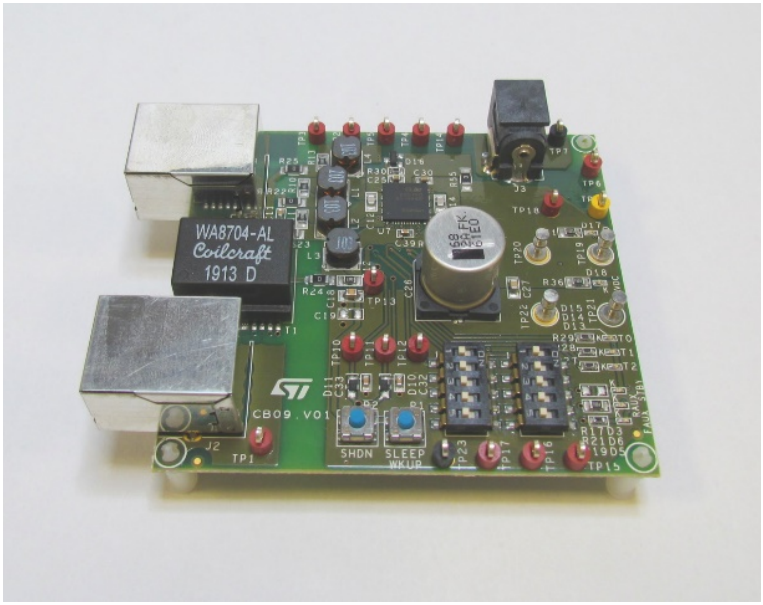
Electrical measurements are reported in order to show the capabilities of the reference device.

Description

The evaluation board is designed to allow the testing of the PM8805 features and to verify the behavior of the component. See PM8805 datasheet DS12813 Rev.2 for device description (see www.st.com).

The board is to be used as a functional block in a complete PD design, having all possible features available to implement a demanding application circuit.

Figure 1. Evaluation board



Features

- 74x66 mm (3x2.6 inch) P.C.B. dimension optimized to allow probe connection, component replacing, additional wiring.
- Data & power input plus Data output RJ45 Ethernet connectors joined to a PoE signal path transformer, to meet Gbit and IEEE Std. 802.3 requirements.
- Chassis ground plane connection, with 1.6 mm (65 mils) creepage distance to the Ethernet wire connections.
- Adequate components available for EMC compliance and circuit setting in critical working conditions.
- Classification resistors and dip switch available, for PD's Class and Type selection.
- Eight LEDs and two push-buttons placement, for PD's status display and setting.
- Single connector presence, for Rear or Frontal auxiliary source implementation.
- Return path of the output voltage sectioned by MOSFET, with control provided by the PG signal.
- Twenty two test points or turrets, for signals monitoring and board output connection.

1 Electrical schematic

Figure 2. **Electrical schematic - page 1**

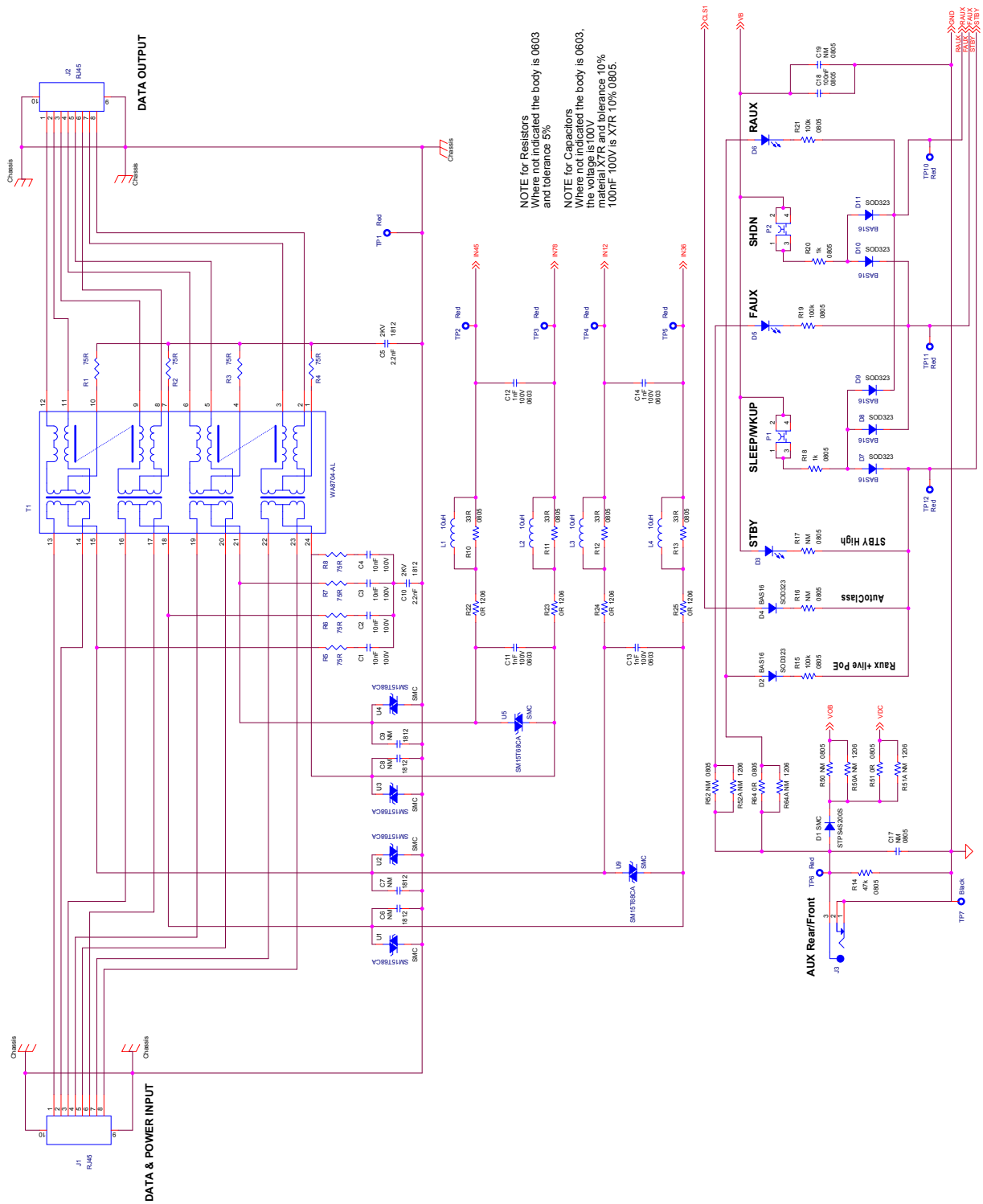
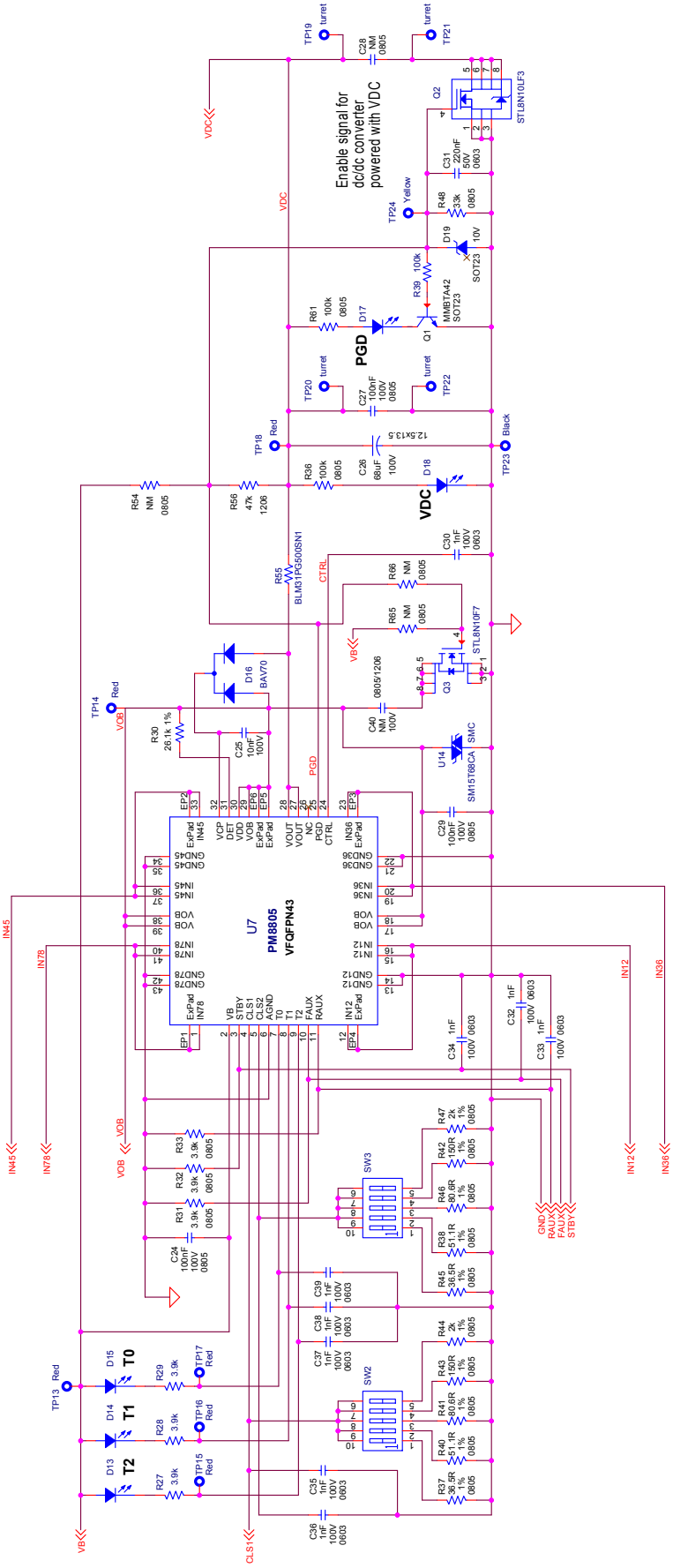


Figure 3. **Electrical schematic - page 2**



2 Component layout

Figure 4. **Component layout - top side**

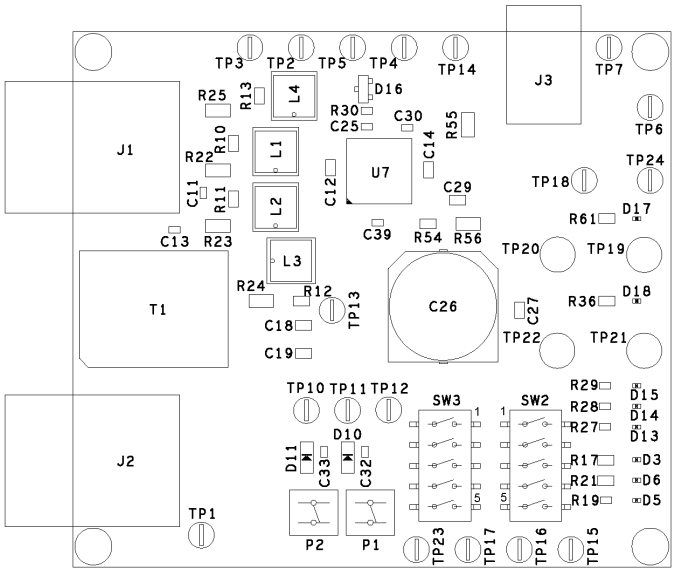
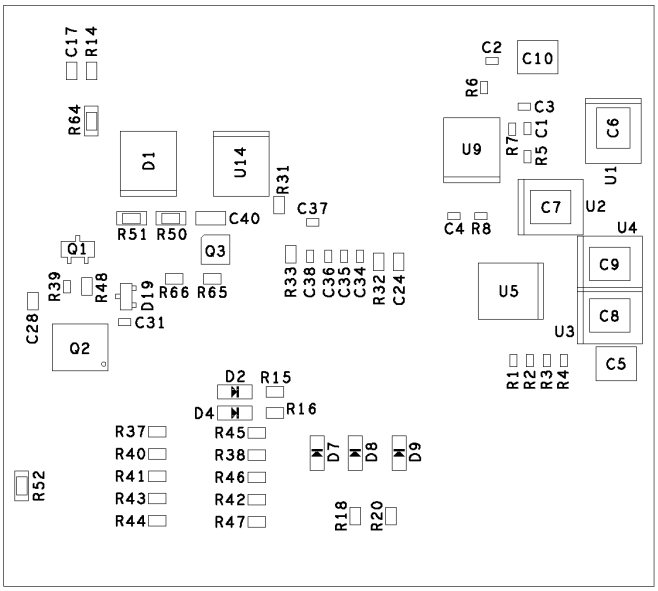


Figure 5. **Component layout - bottom side**



3 Board bill of material

Table 1. Board bill of material.

Q.ty	Reference designator	Value	Description	Package	Manufacturer code	Manufacturer
5	C1, C2, C3, C4, C25	10nF 100V X7R	SMT capacitor	Size 0603	-	Several
2	C5, C10	2.2nF 2kV X7R	SMT capacitor	Size 1812	C4532X7R3D222K130KA or equivalent	TDK
4	C6, C7, C8, C9	NM	SMT capacitor	Size 1812	-	-
2	C12, C14	1nF 100V COG (NP0)	SMT capacitor	Size 0805	-	Several
3	C17, C19, C40	NM	SMT capacitor	Size 0805	-	-
5	C18, C24, C27, C28, C29	100nF 100V X7R	SMT capacitor	Size 0805	-	Several
1	C26	68uF 100V	SMT capacitor	Diam. 12.5X13	EEEFK2A680AQ or equivalent	Panasonic
11	C11, C13, C30, C32, C33, C34, C35, C36, C37, C38, C39	1nF 100V X7R	SMT capacitor	Size 0603	-	Several
1	C31	220nF 16V X7R	SMT capacitor	Size 0603	-	Several
1	D1	STPS4S200S	4A - 200V power Schottky rectifier	SMC	STPS4S200S	STMicroelectronics
7	D2, D4, D7, D8, D9, D10, D11	BAS16	Silicon Switching Diode	SOD323	BAS16-03W or equivalent	Infineon
1	D3	STBY	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D5	FAUX	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D6	RAUX	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D13	T2	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D14	T1	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D15	T0	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D16	BAV70	Dual Switching Diode Common Cathode	SOT23	BAV70LT1G / T3G or equivalent	ON Semiconductor
1	D17	PGD	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright
1	D18	VDC	1.0X0.5mm SMD CHIP LED	Size 0402	KPHHS-1005MGCK or equivalent	Kingbright

Q.ty	Reference designator	Value	Description	Package	Manufacturer code	Manufacturer
1	D19	BZX84C10	350mW SURFACE MOUNT ZENER DIODE	SOT23	BZX84C10 or equivalent	Diodes Incorporated
1	J1	Data & Power input	Eight contact, Eight position shielded Jack		SS-7188S-A-NF or equivalent	Stewart Connector
1	J2	Data output	Eight contact, Eight position shielded Jack		SS-7188S-A-NF or equivalent	Stewart Connector
1	J3	AUX Rear/ Front	Receptacle for 6.3mm power jack, 2mm pin		RAPC722 or equivalent	Switchcraft
4	L1, L2, L3, L4	10uH	SMT Power Inductors – SD54 Series	SD54	SD54-103ML_x or equivalent	Coilcraft
1	P1	Sleep/WKUP	7914 4 mm SMD & Through-hole Sealed Key Switch	7914J	7914J-1-000E or equivalent	Bourns
1	P2	SHDN	7914 4 mm SMD & Through-hole Sealed Key Switch	7914J	7914J-1-000E or equivalent	Bourns
1	Q1	MMBTA42	Small signal NPN transistor	SOT23	MMBTA42 or equivalent	Several
1	Q2	STL8N10LF3	N-channel 100V, 25mΩ, 7.8A, MOSFET	PowerFLAT 5x6	STL8N10LF3	STMicroelectronics
1	Q3	STL8N10F7	N-channel 100V, 17mΩ, 8A, MOSFET	PowerFLAT 3.3x3.3	STL8N10F7	STMicroelectronics
8	R1, R2, R3, R4, R5, R6, R7, R8	75R	SMT resistor	Size 0603	-	Several
4	R10, R11, R12, R13	33R	SMT resistor	Size 0805	-	Several
1	R14	47K	SMT resistor	Size 0805	-	Several
4	R15, R21, R36, R61	100k	SMT resistor	Size 0805	-	Several
2	R16, R17	NM	SMT resistor	Size 0805	-	-
2	R18, R20	1K	SMT resistor	Size 0805	-	Several
2	R19, R39	100k	SMT resistor	Size 0603	-	Several
3	R27, R28, R29	3.9K	SMT resistor	Size 0603	-	Several
1	R30	26.1K 1%	SMT resistor	Size 0603	-	Several
3	R31, R32, R33	3.9k	SMT resistor	Size 0805	-	Several
2	R37, R45	35.6R 1%	SMT resistor	Size 0805	-	Several
2	R38, R40	51.1R 1%	SMT resistor	Size 0805	-	Several
2	R41, R46	80.6R 1%	SMT resistor	Size 0805	-	Several
2	R42, R43	150R 1%	SMT resistor	Size 0805	-	Several

Q.ty	Reference designator	Value	Description	Package	Manufacturer code	Manufacturer
2	R44, R47	2K 1%	SMT resistor	Size 0805	-	Several
1	R48	33K	SMT resistor	Size 0805	-	Several
5	R50, R52, R54, R65, R66	NM	SMT resistor	Size 0805	-	-
2	R51, R64	0R	SMT resistor	Size 0805	-	Several
	R55	50Ohm	Bead Impeder	Size 1206	BLM31PG500SN1	Murata
4	R22, R23, R24, R25	0R	SMT resistor	Size 1206	-	Several
1	R56	47K	SMT resistor	Size 1206	-	Several
2	SW2, SW3	A6S-5104-H	Slide DIP Switch		A6S-5104-H or equivalent	Omron
15	TP1, TP2, TP3, TP4, TP5, TP6, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	Red	Red bead terminal, diam. 1.32mm	Diam. 2,9 , Hole 1.6mm	20-313141 or equivalent	Vero Technologies
2	TP7, TP23	Black	Black bead terminal, diam. 1.32mm	Diam. 2,9 , Hole 1.6mm	20-2136 or equivalent	Vero Technologies
4	TP19, TP20, TP21, TP22	Turret	SOLDER TERMINAL TURRETS	2501	2501-2-00-80-00-00-07-0 or equivalent	MILL-MAX
1	TP24	Yellow	Yellow bead terminal, diam. 1.32mm	Diam. 2,9 , Hole 1.6mm	20-313141 or equivalent	Vero Technologies
1	T1	WA8704-AL	POE Signal Path Transformer		WA8704-ALD or equivalent	Coilcraft
7	U1, U2, U3, U4, U5, U9, U14	SM15T68CA	1500 W TVS Diode	SMC	SM15T68CA	STMicroelectronics
1	U7	PM8805	IEEE 802.3bt PoE-PD interface	VFQFPN 8X8X1.0 43L	PM8805TR	STMicroelectronics
4	-	-	Plastic support for P.C.B.	-	PST-6-01 or equivalent	Essentra Components
1	-	-	FR4 four layers P.C.B.	66x73.81 mm	-	-

4 P.C.B. layout

Figure 6. P.C.B. layout - top side

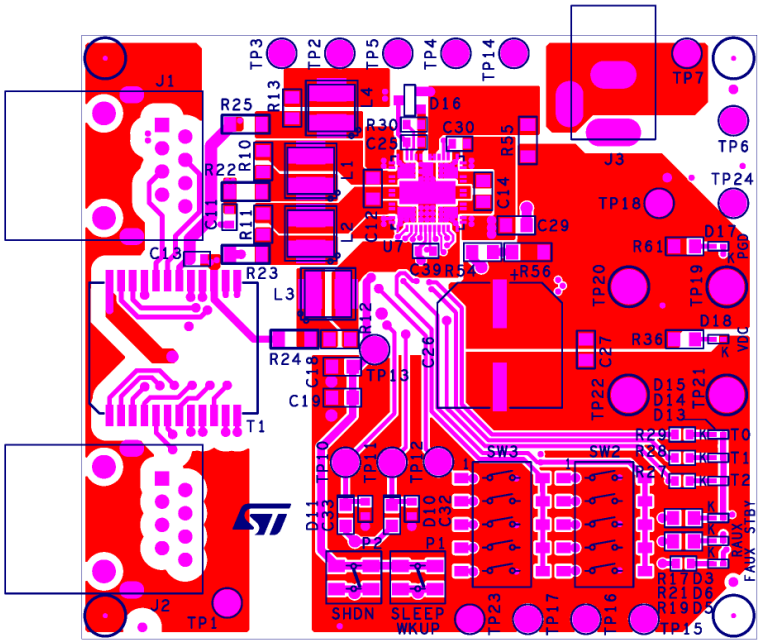


Figure 7. P.C.B. layout - layer 2

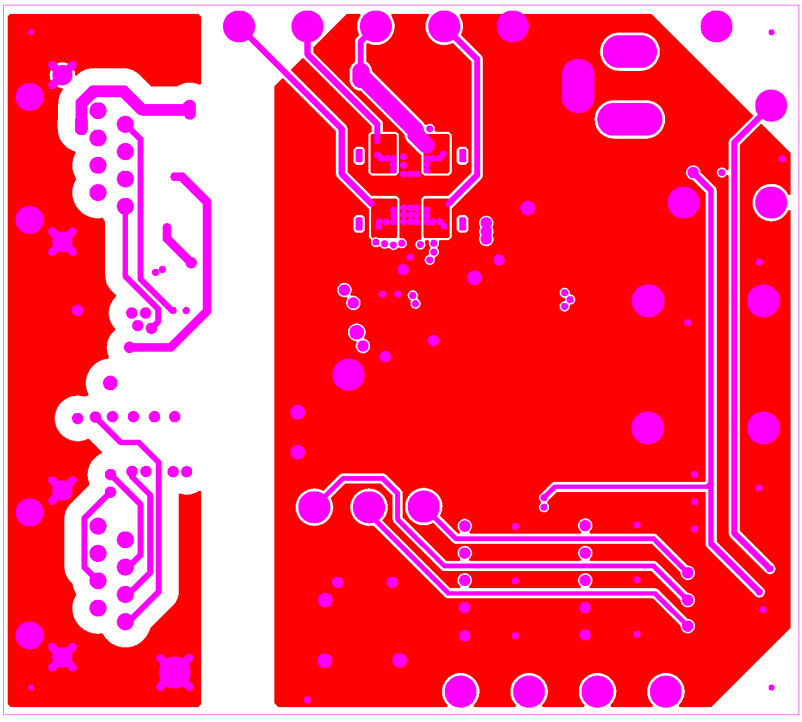


Figure 8. P.C.B. layout - layer 3

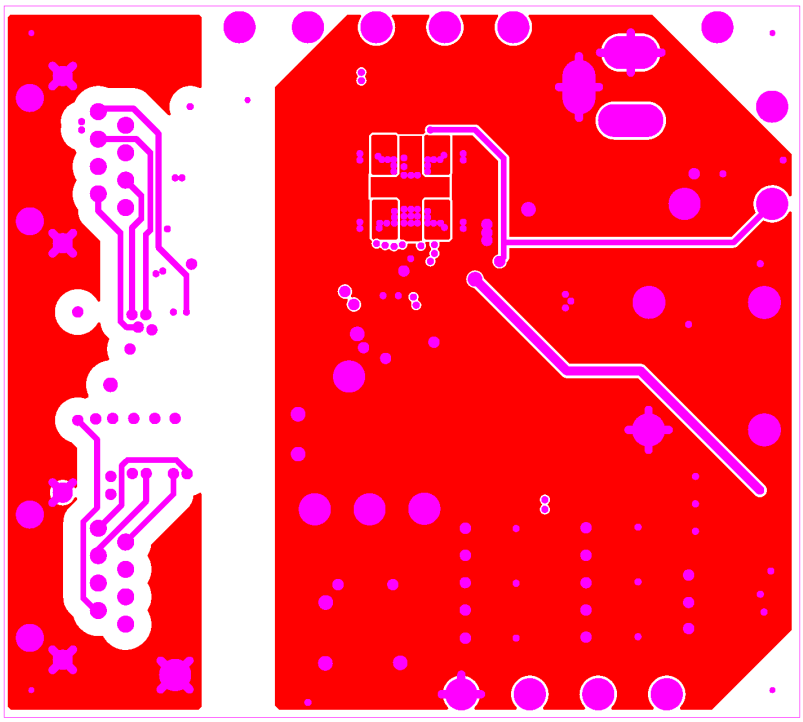
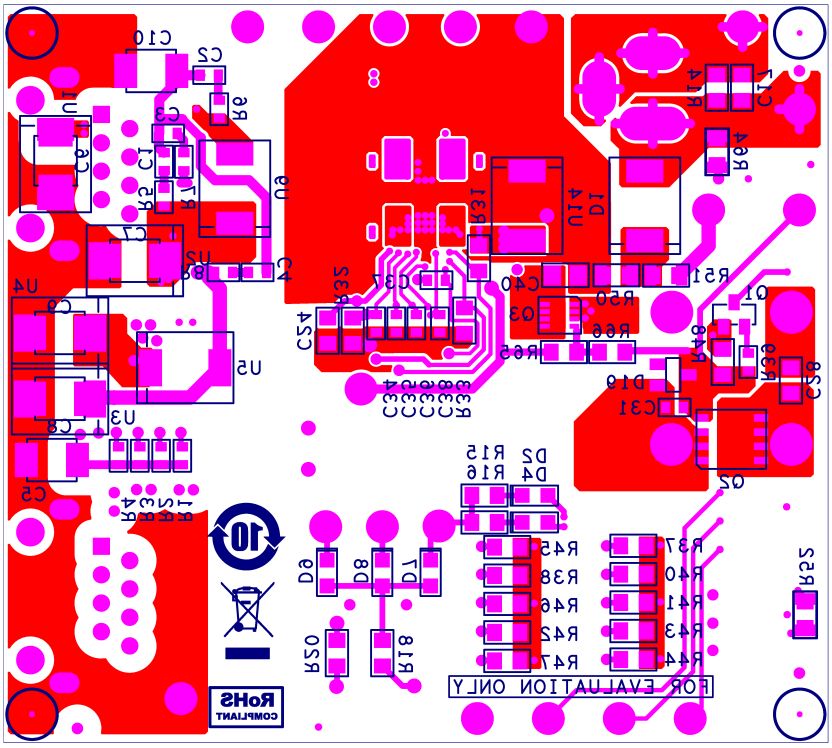


Figure 9. P.C.B. layout - bottom side



5 Board details

The following sections list the operative points available on the evaluation board, for testing and developing activities.

See Figure 2, Figure 3, Figure 4, Figure 5 and PM8805 datasheet DS12813 as reference on www.st.com.

5.1 Board connectors

This section provides a list of the connectors present on the board and their purpose:

Table 2. Board connectors

Reference designator	Type	Description
J1	RJ45	Data and Power input connector, satisfying IEEE Std. 802.3bt requirement, with metallic shield connected to Chassis ground plane.
J2	RJ45	Data output connector, satisfying IEEE Std. 802.3bt requirement, with metallic shield connected to Chassis ground plane.
J3	Jack	Auxiliary input connector, with 2 mm internal male pin, suitable for 6.3 mm bipolar power jack, configurable to perform Rear or Frontal auxiliary source.

5.2 Board test points and turrets

The following list explains the board test points function:

Table 3. Board test points and turrets

Reference designator	Type	Description
TP1	Red pin	Chassis ground connection
TP2, TP3, TP4, TP5	Red pins	Test points connected to the four input Ethernet Pairs, at the input bridges connection points, for the PM8805 inputs monitoring
TP6, TP7	Red / black pins	Monitoring points at J3 auxiliary input voltage
TP10	Red pin	RAUX signal (PM8805)
TP11	Red pin	FAUX signal (PM8805)
TP12	Red pin	STBY signal (PM8805)
TP13	Red pin	VB signal, internal reference voltage (PM8805)
TP14	Red pin	VOB voltage, internal active bridges positive output voltage (PM8805)
TP15, TP16, TP17	Red pins	T2, T1, T0 signals (PM8805)
TP18, TP19, TP20	Red pin and turrets	Board positive output voltage
TP21	Turret	Board output voltage return
TP22, TP23	Turret and black pin	GND signal, internal active bridges output voltage return (PM8805)
TP24	Yellow pin	PGD signal (PM8805)

5.3 Board signaling LEDs

The following is a list of LEDs present on the board:

Table 4. Board signaling LEDs

Reference designator	Function	Description
D3	(LED ON) = (STBY=1=active)	STBY signal monitor, this LED is ON if polarized through R17 path only. Use R17 pads, to implement the STBY signal driving and obtain the special operation condition, described in the PM8805 datasheet DS12813 on www.st.com
D5	(LED ON) = (FAUX=1=active)	FAUX signal monitor, this LED is ON if the Auxiliary Frontal input voltage is selected and present.
D6	(LED ON) = (RAUX=1=active)	RAUX signal monitor, this LED is ON if the Auxiliary Rear input voltage is selected and present.
D13, D14, D15	(LEDs ON) = (T2/T1/T0=0=NOT active). (LEDs OFF) = (T2/T1/T0=0=active).	T2, T1 and T0 signals monitors. These LEDs are ON if the relative PM8805 signals are NOT active. These LEDs are OFF if the relative PM8805 signals are active.
D17	(LED ON) = (PGD=1=active)	PGD monitor, this LED is ON if the PGD signal is active.
D18	(LED ON) = (VOUT=VDC=present)	VOUT=VDC voltage monitor, this LED is ON if the PM8805 output voltage (VOUT) is present. VDC is the recognition mark printed on the evaluation board.

5.4 Board push-buttons

The following push-buttons are present on the board:

Table 5. Board push-buttons.

Reference designator	Function	Description
P1	SLEEP/WKUP	Pushing this button, three signals are asserted at one, RAUX, FAUX and STBY. See DS12813 on www.st.com, for PM8805 behavior description.
P2	SHDN	Pushing this button, two signals are asserted at one, RAUX and FAUX. See DS12813 on www.st.com, for PM8805 behavior description.

5.5 Board dip switches

Two groups of five dip switches, SW2 and SW3 are foreseen on the board, to allow the selection of the classification resistors connected to the PM8805.

CLS1 and CLS2 classification pins connected to the necessary resistors value to GND, set up the PD class request, during classification process.

See datasheet DS12813 on www.st.com, for classification process understanding.

Looking at Figure 3 and Figure 4 , it is possible to verify dip switches operation and resistors correspondence.

Both figures report the position of switches 1 and 5 on SW2 and SW3.

5.6 Additional wires

Four 0 Ω resistors, R22, R23, R24, and R25, placed near the J1 connector, on the board top side, can be replaced by four insulated wires, to allow a probe insertion for current measurement.

6 Board electrical specifications

The following table reports the most important electrical specifications of the evaluation board.

Table 6. Board electrical specification.

Parameter	Description	Min.	Max.	Unit
Vin	Input voltage at J1 connector	35	57	V
Iin	Input current at J1 connector for each Ethernet Pair		1	A
Vout	Output voltage at TP19 and TP21 turrets	34	57	V
Iout	Output current at TP19 and TP21 turrets		2	A
Pout	Outpur power at TP19 and TP21, turrets		100	W
η%	Overall efficiency at Iout=2 A	97		%
VFront	Voltage at J3 connector as Frontal auxiliary input	35	57	V
IFront	Current at J3 connector as Frontal auxiliary input		2	A
VRear	Voltage at J3 connector as Rear auxiliary input	35	57	V
IRear	Current at J3 connector as Rear auxiliary input		2	A
Tamb	Operating ambient temperature	0	50	°C

7 Operation details

The following sections list the board functional capabilities, explaining the operative procedures.

Those features are obtained with dedicated circuitry or components, foreseen to tackle specific subjects of the application field.

See Figure 2, Figure 3, Figure 4, Figure 5 and PM8805 datasheet DS12813 on www.st.com as reference.

7.1 Input section

The input section is composed by the connectors J1, J2, and the coupling transformer T1.

A proper ground plane connected to the connectors shield is foreseen and it is designed with a creepage distance of 1.6 mm (65 mils), to be connected to the Protective Earth.

Use TP1 for clip connection to this copper plane.

7.2 Input lines circuitry

Four input lines are available, after the coupling transformer T1, to derive current from the four wire pairs of the Ethernet line.

The four input lines are connected to the eight input pins of the PM8805, through a dedicated circuitry.

This is to prevent the input abnormal electrical events, characteristic of the communication lines, to protect the Powered Device electrical circuit.

The following list explains the components' purpose:

- U1, U2, U3, U4, Transient Voltage Suppressors, to clamp input common mode overvoltage (voltage surge), between the four Ethernet wire pairs and the Chassis ground plane, usually connected to the Protective Earth conductor.
- U5, U9, TVSs, to clamp input differential mode overvoltage, between two Ethernet wire pairs.
- L1, L2, L3, L4, four inductors to limit the current through the PD electrical circuit, during common mode overvoltage transient (voltage surge).
- R10, R11, R12, R13, four dumping resistors, used along with previous inductors.
- C11, C12, C13, C14, four filtering capacitors, for high frequency, differential mode noise filtering.

The presence of these components allows the test of the board and the test of additional application circuits connected to the board output, which make up a complete PD circuitry.

It is possible to verify the PM8805 working condition, during the abnormal electrical transient application.

See Design tip DT0149 on www.st.com “Power over Ethernet application circuits, line surge analysis and treatment”, for a better understanding of the topic.

7.3 Rear/Front auxiliary input

The J3 connector can be configured to implement both Rear or Frontal auxiliary input.

- Rear auxiliary configuration; it is the normal setting present on the board:

  R51=0Ω and R50=N.M., to select the PM8805’s output voltage (Vout/VDC) as insertion point of the auxiliary input.

  R64=0Ω and R52=N.M., to select the Rear auxiliary configuration and the Maintaining Power Signature function, on the PM8805’s pins.
- Frontal auxiliary configuration; it is possible to apply this setting as follows:

  R50=0Ω and R51=N.M., to select the PM8805’s VOB voltage as insertion point of the auxiliary input.

  R52=0Ω and R64=N.M., to select the Frontal auxiliary configuration to the PM8805’s pins.

See the PM8805 datasheet DS12813 on www.st.com, for a correct learning of these features.

7.4 Board output

The Powered Devices must respect a proper timing before drawing current from the Ethernet line.

The circuitry following the PM8805 can start drawing current after the PDG signal assertion.

The PGD is an open collector, high active signal.

If the output voltage is obtained from TP20 and TP22 turrets, the following PD circuits must use the PGD signal, to enable the PD's operation. The PGD signal is available on TP24.

Using these output points, connected in parallel to C26=68µF, all the capacitance connected is charged using a controlled current, during startup phase.

If the output voltage is obtained from TP19 and TP21 turrets, the PD circuitry is supplied after the PDG assertion only, because the Q2 MOSFET is driven by this signal.

Using these output points, the capacitance present in the PD circuits, is not charged using a limited current, because the startup phase has already expired.

See the PM8805 datasheet DS12813 on www.st.com for a complete description of the startup phase.

7.5 VOB fast transient protection

The PM8805's VOB signal can be subjected to a very fast voltage transient, depending on the application circuit type and working condition.

If the voltage transient has a falling edge with an amplitude higher than 10 V and a duration lower than 1 µs, there is the possibility to have the PM8805's circuitry reset.

An example of these conditions is the presence of a common mode inductor along the output voltage path, without a proper capacitor on the VOUT pins.

The leakage inductance of the inductor can generate a voltage transient, when crossed by high and fast current peak.

Even without the common mode inductor, during an input line surge injection, the current flowing back through the C26 capacitor can generate a fast voltage transition, on VOUT and VOB.

If it is not possible to avoid the root cause of the VOB voltage transient, it is possible to limit the transition applying a ceramic capacitor on the VOB pins.

The capacitor should be large enough to be effective, but it must be considered that it is forbidden to have more than 100 nF between the input lines during the PD classification process. (This is a requirement of IEEE Std. 802.3bt standard).

The transistor Q3 is foreseen on the board to connect the C40 capacitor, between VOB and GND signals.

Connecting 1 µF, 100 V capacitor, after the assertion of PGD signal or the rising of VB voltage, it is possible to protect VOB, without influencing the PD classification procedure.

Q3 is always available on the board, C40=1 µF and R65 or R66 can be placed if necessary.

R65 supplies the Q3's gate bias from VB voltage.

R66 supplies the Q3's gate bias from PGD signal.

7.6 Noise reduction

The PD circuitry following the PM8805 interface can generate a lot of differential mode noise between VOUT/VDC and GND signals.

A small filter placed on R55 pads is used to reduce the high frequency noise reaching the PM8805's output section.

This bead impeder could be useful or not, depending on the application circuit condition.

Verify the effective necessity of this component, that is sometimes useful to avoid the circuitry reset during input line surge injection or during electrostatic discharge applied to the VDC voltage, on the output turrets.

8 Evaluation measurements

The following paragraphs report some measurements performed on the evaluation board, to show the performances of the PM8805 and of the board itself.

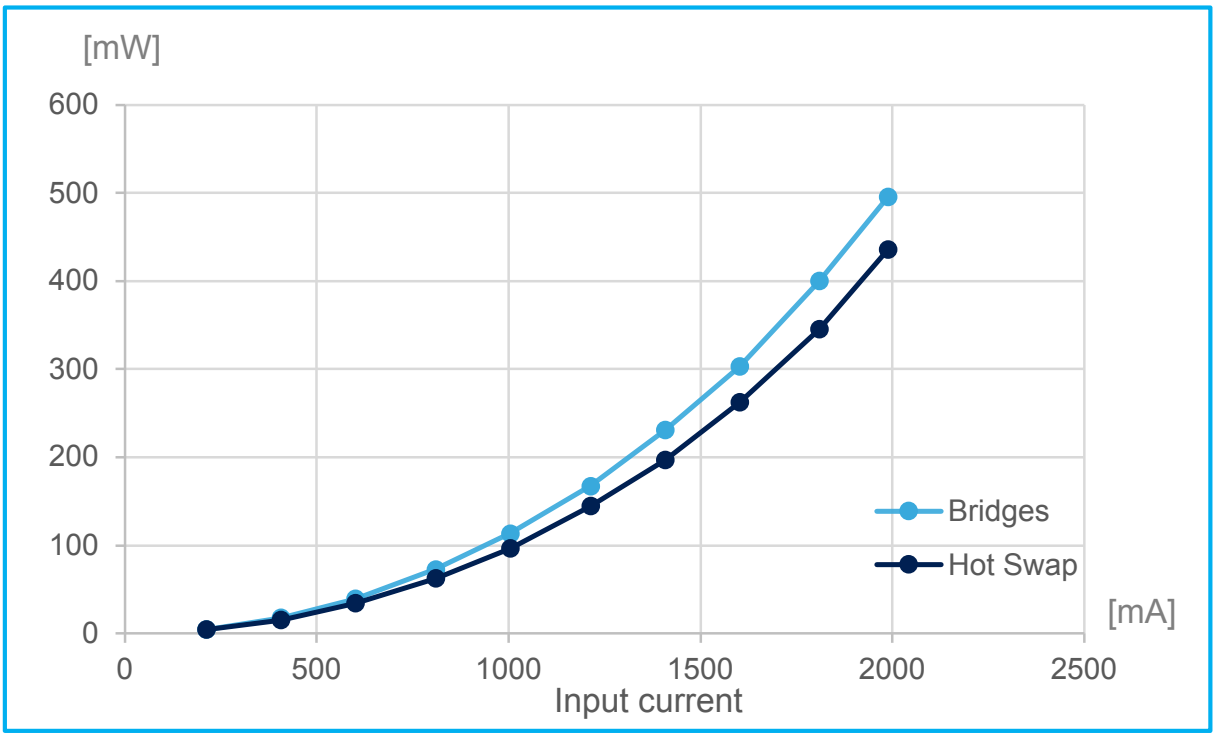
8.1 Power losses

The following figure reports the PM8805 power losses, during a steady-state functioning.

The causes of greater loss of the device are the voltage drops on the input bridges and the voltage drop on the hot swap switch.

Measurements were conducted taking care to obtain the device losses only.

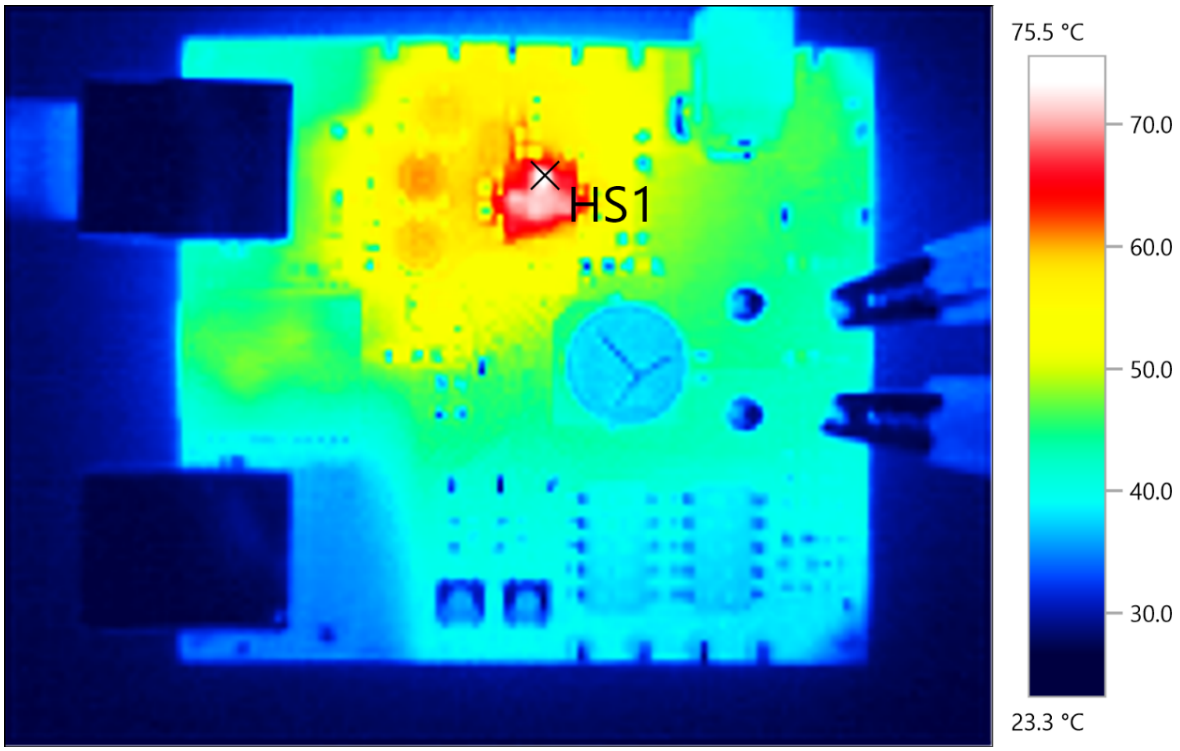
Figure 10. Input bridges and hot swap losses



8.2 Board thermal measurement

The following figure shows the board performance as heat dissipation capability and resulting temperature of the PM8805 device.

Figure 11. Board thermal image



Measurement conditions:

Tamb=23.3 °C, ambient temperature.

No cooling air flow.

Input=2 A, current flowing through the PM8805.

HS1=75.5 °C, PM8805 temperature.

8.3 Electro-magnetic compatibility

The following section reports the measurement conducted on the board, relative to the voltage surge application.

Tests are performed using a proper Coupling and Decoupling Network (CDN), following the specification present in the IEC 61000-4-5 standard.

Tests reported in this application note are conducted using the 1.2/50 µs surge, which is relative to the most common PoE application circuits that are connected to lines frequently classified as Unshielded and Symmetrical.

The scope of the test is to verify the presence of a failure risk, during the surge application.

Since the circuit foresees the presence of four TVS on the input lines (U1, U2, U3, U4), which limit the voltage transient amplitude on the board, a possible failure implies the presence of high currents flowing through the electrical paths.

It is very important to note that since the board output voltage is not isolated, there cannot be a ground connection of the output.

During the test, the ground connection was applied to the Chassis ground plane.

Considering the board circuitry, the most sensitive component is the PM8805, which can suffer high current flowing into its hot swap MOSFET.

To verify the amplitude of the current flowing through the PM8805, it is enough to measure the current flowing into the R55 bead impeder, which means the current flowing along the positive path of VOUT/VDC voltage.

The tests report a safe effect of ±4 kV surges, showing IOUT= -20 A, maximum current peak during the Surge injection, flowing into the VOUT pins.

The input bridges present in the PM8805 are composed by MOSFETs, which open when sensing a reverse current flowing inside.

This method introduces a little opening delay of the input bridges, which can result in around 2 µs, depending on the external circuitry and the effective reverse current shape.

That leads to high current flowing through the PM8805 during surge event, until the input bridges are opened.

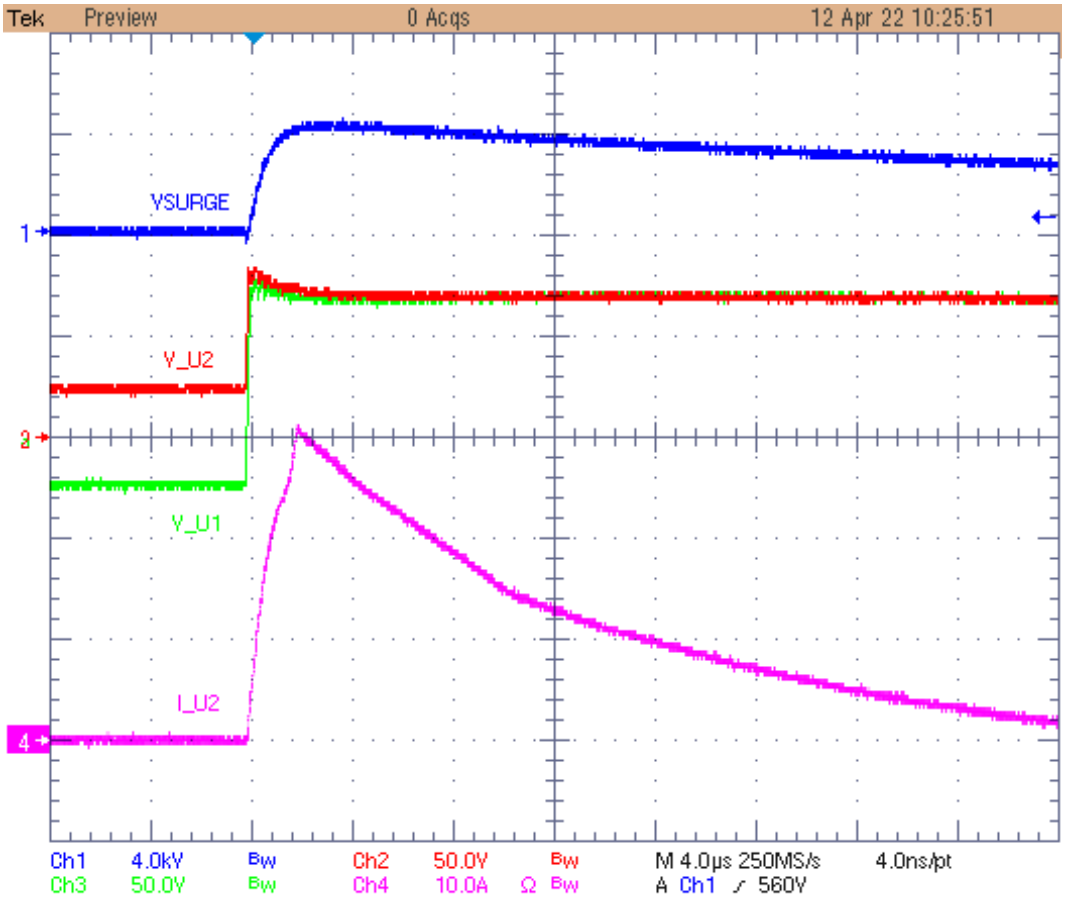
Four input inductors L1, L2, L3 and L4 limit that current and allow to sustain surge without failure.

The following two figures show the test results.

Notes:

- The presence of the four TVS' on the input lines, allows the injection of high voltage surge, even if the creepage distance maintained between input lines paths and the Chassis plane is 65 mils only.
- See design tip DT0149 “Power over Ethernet application circuits, line surge analysis and treatment”, to obtain more information on the subject.

Figure 12. +4 kV surge



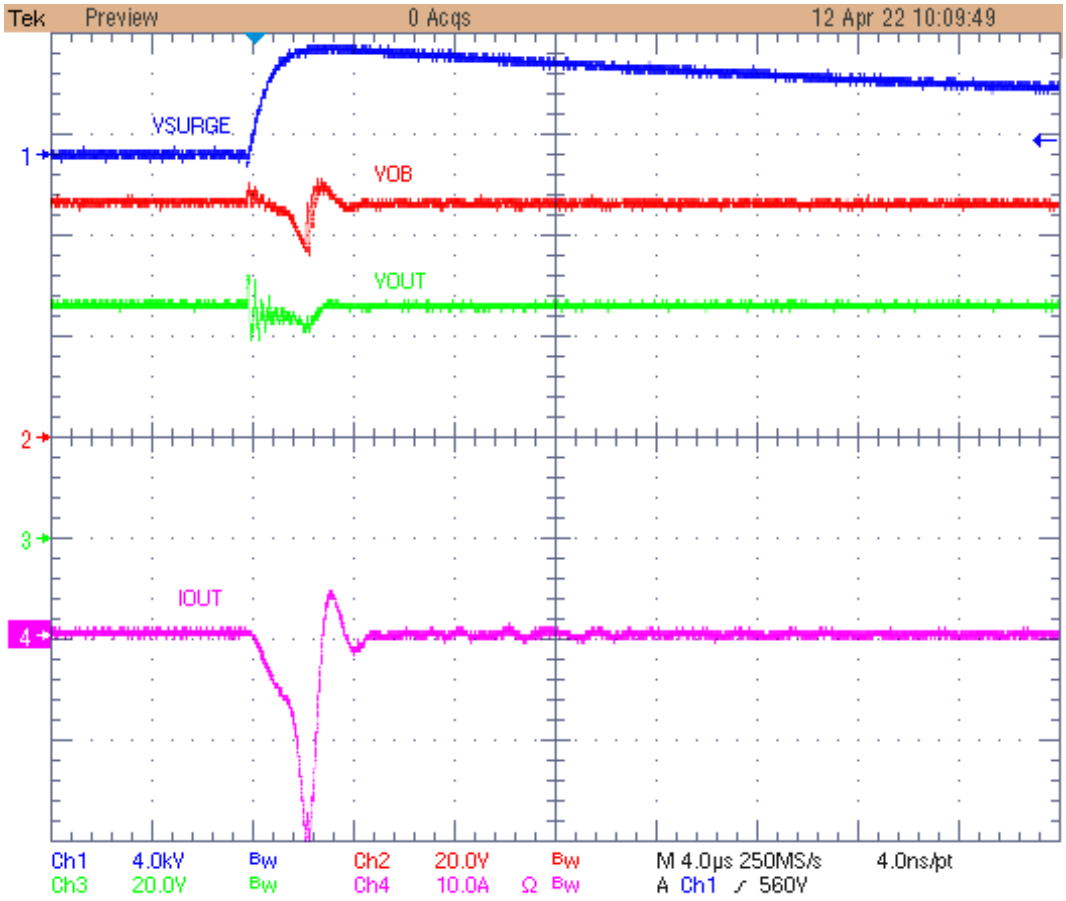
Ch1 blue trace, 4 kV/div, Surge voltage applied between input Ethernet lines and Chassis ground.

Ch2 red trace, 50 V/div, U2 voltage.

Ch3 green trace, 50 V/div, U1 voltage.

Ch4 purple trace, 10 A/div, U2 current.

Figure 13. **+4 kV surge**



Ch2 red trace, 20 V/div, PM8805 VOB voltage.

Ch3 green trace, 20 V/div, PM8805 VOUT voltage.

Ch4 purple trace, 10 A/div, PM8805 IOUT current.

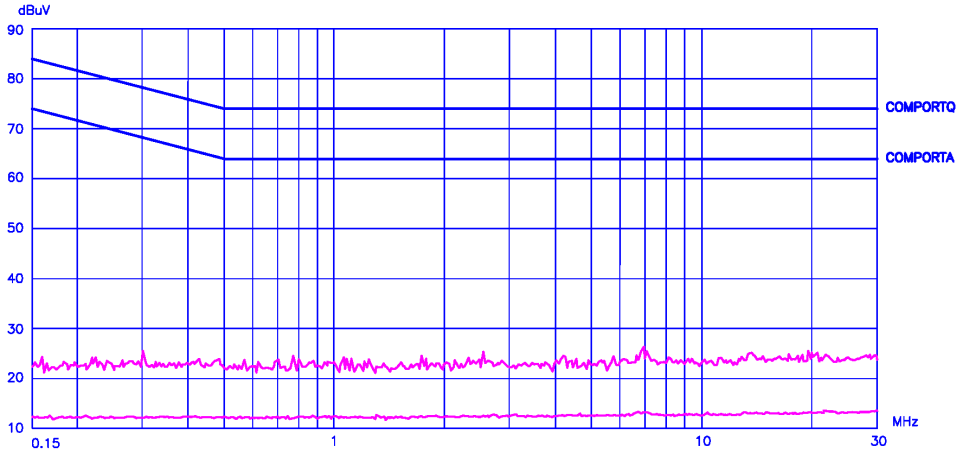
8.4 Electro-magnetic interferences

Conducted common mode disturbance.

The following figure reports the measurement carried out on the board, relative to the conducted common mode (asymmetric mode) disturbance at telecommunication ports, in the frequency range 0.15 MHz to 30 MHz, for class B equipment.

The measurement is performed using a proper Impedance Stabilization Network (ISN), following the specification present in the CISPR 22: 2008 and EN 55022: 2010 standards.

Figure 14. **Conducted common mode disturbance**



Measurement conditions:

Vinput= 48 V.

Iout= 2 A, resistive load.

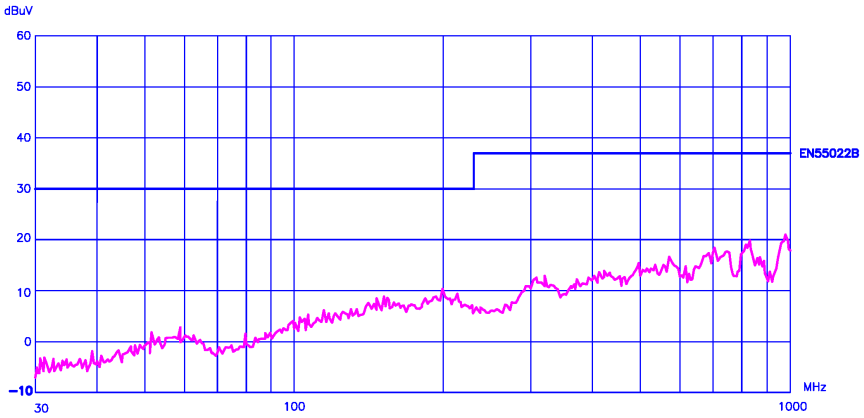
The previous figure demonstrates that the evaluation board with the PM8805 device does not add significant noise to the background level.

Radiated disturbance

The following figures report the measurement carried out on the board, relative to the radiated disturbance, in the frequency range 30 MHz to 1 GHz, for class B equipment.

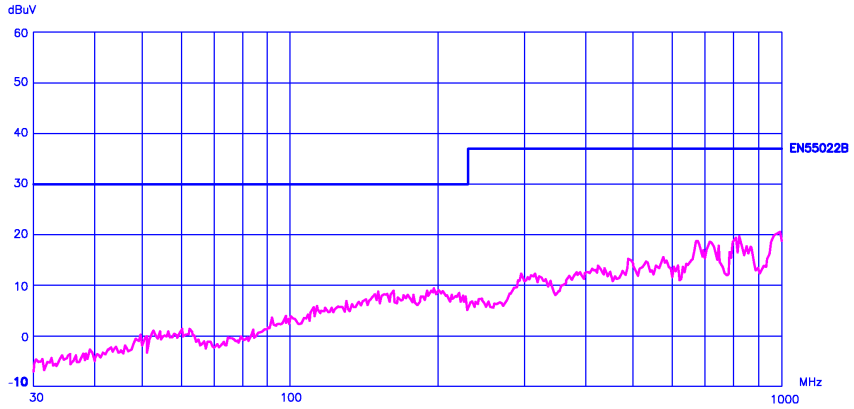
The measurement is performed following the specification present in the CISPR 22: 2008 and EN 55022: 2010 standards.

Figure 15. **Radiated disturbance, background noise level**



Measurement conditions: Evaluation board present but without input voltage.

Figure 16. Radiated disturbance, maximum load and input voltage condition



Measurement conditions:

Vinput= 57 V.

Iout= 2 A, resistive load.

The previous two figures show the radiated noise emissions of the evaluation board and of the PM8805 device, comparing the background noise level of the measurement equipment versus the board noise emission, with maximum output current and maximum input voltage.

The comparison demonstrates that the PM8805 and the board do not generate significant noise.

9 IEEE Std 802.3bt compliance

The Institute of Electrical and Electronics Engineers (who develops industry standards, to establish the functionality and interoperability of products and services) has created the IEEE Std 802.3 standard, to regulate the Ethernet local area networks functionality.

The 802.3 standard is also composed by its amendments or projects (identified by two character suffixes 802.3xx), which correct or expand particular topics.

The 802.3at Amendment 3, Data Terminal Equipment (DTE), Power via the Media Dependent Interface (MDI) Enhancements, includes changes to IEEE Std 802.3-2008, to augment the capabilities of 802.3 with higher power levels and improved power management information.

The 802.3bt Amendment 2, Physical Layer and Management Parameters for Power over Ethernet over 4 Pairs, increases the maximum power available for the Powered Device (PD), to the IEEE Std 802.3-2018, by utilizing all four pairs in the specified structured wiring plant.

This represents a substantial change to the capabilities of Ethernet with standardized power. The power classification information exchanged during negotiation is extended to allow meaningful power management capability. These enhancements solve the problem of higher power and more efficient standardized Power over Ethernet (PoE) delivery systems.

One of the principal characteristics of a PoE interface is to be compliant with a proper standard, widely recognized and adopted, to guarantee the correct functionality of the PD using it.

The PM8805 device is designed to be compliant with the IEEE Std 802.3bt specification, maintaining compatibility and interoperability with the previous 802.3at amendment.

The Ethernet Alliance organization (that is an industry consortium dedicated to the success and advancement of Ethernet technologies) is considered a reference in the Ethernet compass.

EA has defined a measurement method and test procedure to verify compliance to the 802.3at (Gen 1) and 802.3bt (Gen 2) amendments.

The Sifos Technologies (a Company developing and producing PoE test instruments and software) has developed dedicated instruments to verify PD compliance with the IEEE standards, referring to Ethernet Alliance test procedure.

The following measurement, performed using an up to date measurement system connected to the evaluation board, demonstrates the PM8805 compliance with the 802.3bt and 802.3at requirements.

Figure 17. IEEE Std 802.3bt Conformance Test report

	A	B	C	D	E	F	G	H	I	J	K	L
1	PDA-600 BT TEST REPORT			EA Cert. Status	Coverage:	ALT A	MDI	Type3 Phy	Software Version: 2.4.0.5		Sifos Technologies	
2	7/ 1/2022 5:59 PM					ALT B	MDI	Type4 Phy	PDA Firmware: 2.08			
3	Product Tested:				Color Key:			LLDP	Report Ver: 3.6			
4	EVL-POE007V1			PASS	PASS	FAIL	WARN	INFO	Serial Number 604A0050			
9	Detection											
10		Parameter	EA Test ID	Meas.	Units	Min.	Max.	Average	Low Lim.	High Lim.	P/F	
11		SigType	11.18.1	SINGLE	-	-	-	-	SINGLE	SINGLE	P	
12		Rdet_A	11.12.2	25.69	kohm	25.69	25.69	25.69	23.70	26.30	P	
13		Rdet_final_A	11.12.2	25.59	kohm	25.59	25.59	25.59	23.70	26.30	P	
14		Rdet_unpwr_A	11.13.1,11.18.1	>99.00	kohm	99.00	99.00	99.00	<12.00	>45.00	P	
15		Rdet_at_Vmin_A	11.12.2	25.29	kohm	25.29	25.29	25.29	23.70	26.30	P	
16		Rdet_at_Vmax_A	11.12.2	26.22	kohm	26.22	26.22	26.22	23.70	26.30	P	
17		Rdet_Voffset_A	11.12.2	1.2	VDC	1.2	1.2	1.2	0.0	1.9	P	
18		Cdet_A	11.12.1	0.10	uF	0.10	0.10	0.10	0.05	0.12	P	
19		Cdet_final_A	11.12.1	0.10	uF	0.10	0.10	0.10	0.05	0.12	P	
20		Rdet_B	11.12.3	25.78	kohm	25.78	25.78	25.78	23.70	26.30	P	
21		Rdet_final_B	11.12.3	25.71	kohm	25.71	25.71	25.71	23.70	26.30	P	
22		Rdet_unpwr_B	11.13.2,11.18.2	>99.00	kohm	99.00	99.00	99.00	<12.00	>45.00	P	
23		Rdet_at_Vmin_B	11.12.3	25.16	kohm	25.16	25.16	25.16	23.70	26.30	P	
24		Rdet_at_Vmax_B	11.12.3	25.70	kohm	25.70	25.70	25.70	23.70	26.30	P	
25		Rdet_Voffset_B	11.12.3	1.3	VDC	1.3	1.3	1.3	0.0	1.9	P	
26		Cdet_B	11.12.1	0.10	uF	0.10	0.10	0.10	0.05	0.12	P	
27		Cdet_final_B	11.12.1	0.10	uF	0.10	0.10	0.10	0.05	0.12	P	

Figure 18. **IEEE Std 802.3bt Conformance Test report**

	A	B	C	D	E	F	G	H	I	J	K	L
28		**Classification**										
29		ClassNum_A	11.27	8		8	8	-	8	8	P	
30		class_sig_EV1-2_min_A	11.27	39.5	mA	39.5	39.5	39.5	36.0	44.0	P	
31		class_sig_EV1-2_max_A	11.27	40.1	mA	40.1	40.1	40.1	36.0	44.0	P	
32		class_sig_EV3-5_min_A	11.27	27.9	mA	27.9	27.9	27.9	26.0	30.0	P	
33		class_sig_EV3-5_max_A	11.27	28.6	mA	28.6	28.6	28.6	26.0	30.0	P	
34		MarkI_A	11.33	0.50	mA	0.50	0.50	0.50	0.25	4.00	P	
35		Tclass_max_A	11.29	3.4	ms	3.4	3.4	3.4	0.2	5.0	P	
36		Iclass_EV1_at_Vmin_A	11.27	39.7	mA	39.7	39.7	39.7	36.0	44.0	P	
37		Iclass_EV1_at_Vmax_A	11.27	39.4	mA	39.4	39.4	39.4	36.0	44.0	P	
38		Class_Reset_A	11.27	1		1	1	-	1	1	P	
39		Autoclass	11.35	0		0	0	-	0	0	P	
40		Tacs	11.35	0.0	ms	0.0	0.0	0.0	0.0	0.0	P	
41		ClassNum_B	11.27	8		8	8	-	8	8	P	
42		class_sig_EV1-2_min_B	11.27	39.6	mA	39.6	39.6	39.6	36.0	44.0	P	
43		class_sig_EV1-2_max_B	11.27	40.1	mA	40.1	40.1	40.1	36.0	44.0	P	
44		class_sig_EV3-5_min_B	11.27	27.9	mA	27.9	27.9	27.9	26.0	30.0	P	
45		class_sig_EV3-5_max_B	11.27	28.4	mA	28.4	28.4	28.4	26.0	30.0	P	
46		MarkI_B	11.33	0.60	mA	0.60	0.60	0.60	0.25	4.00	P	
47		Tclass_max_B	11.29	3.4	ms	3.4	3.4	3.4	0.2	5.0	P	
48		Iclass_EV1_at_Vmin_B	11.27	39.6	mA	39.6	39.6	39.6	36.0	44.0	P	
49		Iclass_EV1_at_Vmax_B	11.27	39.6	mA	39.6	39.6	39.6	36.0	44.0	P	
50		Class_Reset_B	11.27	1		1	1	-	1	1	P	
51		**Power-Up / Down**										
52		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
53		Iinrush_init	11.51	81.6	mA	81.6	81.6	81.6	0.0	800.0	INFO	
54		Iinrush_tdel	11.51	126.500	mA	126.5	126.5	126.5	0.0	257.6	P	
55		Tinrush	11.51	50.0	ms	50.0	50.0	50.0	0.0	50.0	P	
56		Iinrush_init_A	11.51	38.8	mA	38.8	38.8	38.8	0.0	600.0	INFO	
57		Iinrush_tdel_A	11.51	62.100	mA	62.1	62.1	62.1	0.0	257.6	P	
58		Tinrush_A	11.51	50.0	ms	50.0	50.0	50.0	0.0	50.0	P	
59		Iinrush_init_B	11.51	40.4	mA	40.4	40.4	40.4	0.0	600.0	INFO	
60		Iinrush_tdel_B	11.51	65.800	mA	65.8	65.8	65.8	0.0	257.6	P	
61		Tinrush_B	11.51	50.0	ms	50.0	50.0	50.0	0.0	50.0	P	
62		Vrefl_A	11.66	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P	
63		Vrefl_B	11.66	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P	
64		Von	11.39	39.1	VDC	39.1	39.1	39.1	30.0	42.0	P	
65		Voff	11.41	30.2	VDC	30.2	30.2	30.2	30.0	42.0	P	
66		Vhyst		8.8	VDC	8.8	8.8	8.8	2.8	12.0	INFO	
67		Vport_ext_A	11.7	-1.0	VDC	-1.0	-1.0	-1.0	0.0	2.8	NA	
68		Vport_ext_B	11.7	-1.0	VDC	-1.0	-1.0	-1.0	0.0	2.8	NA	
69		**2 Pair Powered Type-1 PHY**			*PSE Emulation:*	On Time:	**120 sec**	Off Time:	**10 sec**	Vport:	**56.0**	
70		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
71		MinI_1	11.73	6.7	mA	6.7	6.7	6.7	0.0	258.5	P	
72		Vport_1	11.8	55.7	VDC	55.7	55.7	55.7	37.0	57.0	INFO	
73		Ppeak_1	11.52	12.04	W	12.04	12.04	12.04	0.0	14.4	P	
74		Pport_1	11.20,11.44*	11.95	W	11.95	11.95	11.95	0.0	13.0	P	
75		PeakViolation_1	11.52	0		0	0	-	0	0	P	
76		MPSViolation_1	11.73.1	0		0	0	-	0	0	P	
77		TcutWindowViolation_1	11.54	0		0	0	-	0	0	P	
78		DutyCycleViolation_1	11.54	0		0	0	-	0	0	P	
79		**2 Pair Powered Type-3 PHY**			*PSE Emulation:*	On Time:	**120 sec**	Off Time:	**10 sec**	Vport:	**43.5**	
80		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
81		MinI_2	11.73	4.3	mA	4.3	4.3	4.3	0.0	655.0	P	
82		Vport_2	11.8	43.5	VDC	43.5	43.5	43.5	42.5	57.0	INFO	
83		Ppeak_2	11.52	7.34	W	7.34	7.34	7.34	0.0	28.3	P	
84		Pport_2	11.20,11.44*	7.25	W	7.25	7.25	7.25	0.0	25.5	P	
85		PeakViolation_2	11.52	0		0	0	-	0	0	P	
86		MPSViolation_2	11.73.2	0		0	0	-	0	0	P	
87		TcutWindowViolation_2	11.54	0		0	0	-	0	0	P	
88		DutyCycleViolation_2	11.54	0		0	0	-	0	0	P	
89		**4 Pair Powered Type-3 PHY**			*PSE Emulation:*	On Time:	**120 sec**	Off Time:	**10 sec**	Vport:	**56.0**	
90		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
91		MinI_3	11.73	11.4	mA	11.4	11.4	11.4	0.0	958.7	P	
92		Vport-2P_3_A	11.8	55.7	VDC	55.7	55.7	55.7	42.5	57.0	INFO	
93		Vport-2P_3_B	11.8	55.8	VDC	55.8	55.8	55.8	42.5	57.0	INFO	
94		Ppeak_3	11.52	12.22	W	12.22	12.22	12.22	0.0	53.5	P	
95		Pport_3	11.20,11.44*	12.10	W	12.10	12.10	12.10	0.0	51.0	P	
96		PeakViolation_3	11.52	0		0	0	-	0	0	P	
97		MPSViolation_3	11.73.3	0		0	0	-	0	0	P	
98		TcutWindowViolation_3	11.54	0		0	0	-	0	0	P	
99		DutyCycleViolation_3	11.54	0		0	0	-	0	0	P	
100		**4 Pair Powered Type-4 PHY**			*PSE Emulation:*	On Time:	**300 sec**	Off Time:	**10 sec**	Vport:	**43.5**	
101		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
102		MinI_4	11.73	5.0	mA	5.0	5.0	5.0	0.0	1727.6	P	
103		Vport-2P_4_A	11.8	43.3	VDC	43.3	43.3	43.3	41.1	57.0	INFO	
104		Vport-2P_4_B	11.8	43.4	VDC	43.4	43.4	43.4	41.1	57.0	INFO	
105		Ppeak_4	11.52	7.42	W	7.42	7.42	7.42	0.0	74.9	P	
106		Pport_4	11.20,11.44*	7.35	W	7.35	7.35	7.35	0.0	71.3	P	
107		PeakViolation_4	11.52	0		0	0	-	0	0	P	
108		MPSViolation_4	11.73.3	0		0	0	-	0	0	P	
109		TcutWindowViolation_4	11.54	0		0	0	-	0	0	P	
110		DutyCycleViolation_4	11.54	0		0	0	-	0	0	P	
111		**4 Pair Powered LLDP**			*PSE Emulation:*	On Time:	**300 sec**	Off Time:	**10 sec**	Vport:	**52.0**	
112		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
113		**PD LLDP Protocol Characteristics**										
114		**Parameter**	**EA Test ID**	**Meas.**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**	
115			* also 11.52									
116		**NOTE**: *testing did not include LLDP, so PD Data Link Layer characteristics were not checked.*										

Revision history

Table 7. **Document revision history**

Date	Version	Changes
19-Sep-2022	1	Initial release.

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