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AN5817

Application note

L5965 External components sizing

Introduction

This document is intended to integrate the information provided in the L5965 product datasheet, in order to facilitate the correct BUCK and BOOST external components sizing into the different applicative conditions. A specific focus is reserved to external components like inductor, output capacitor and compensation network.

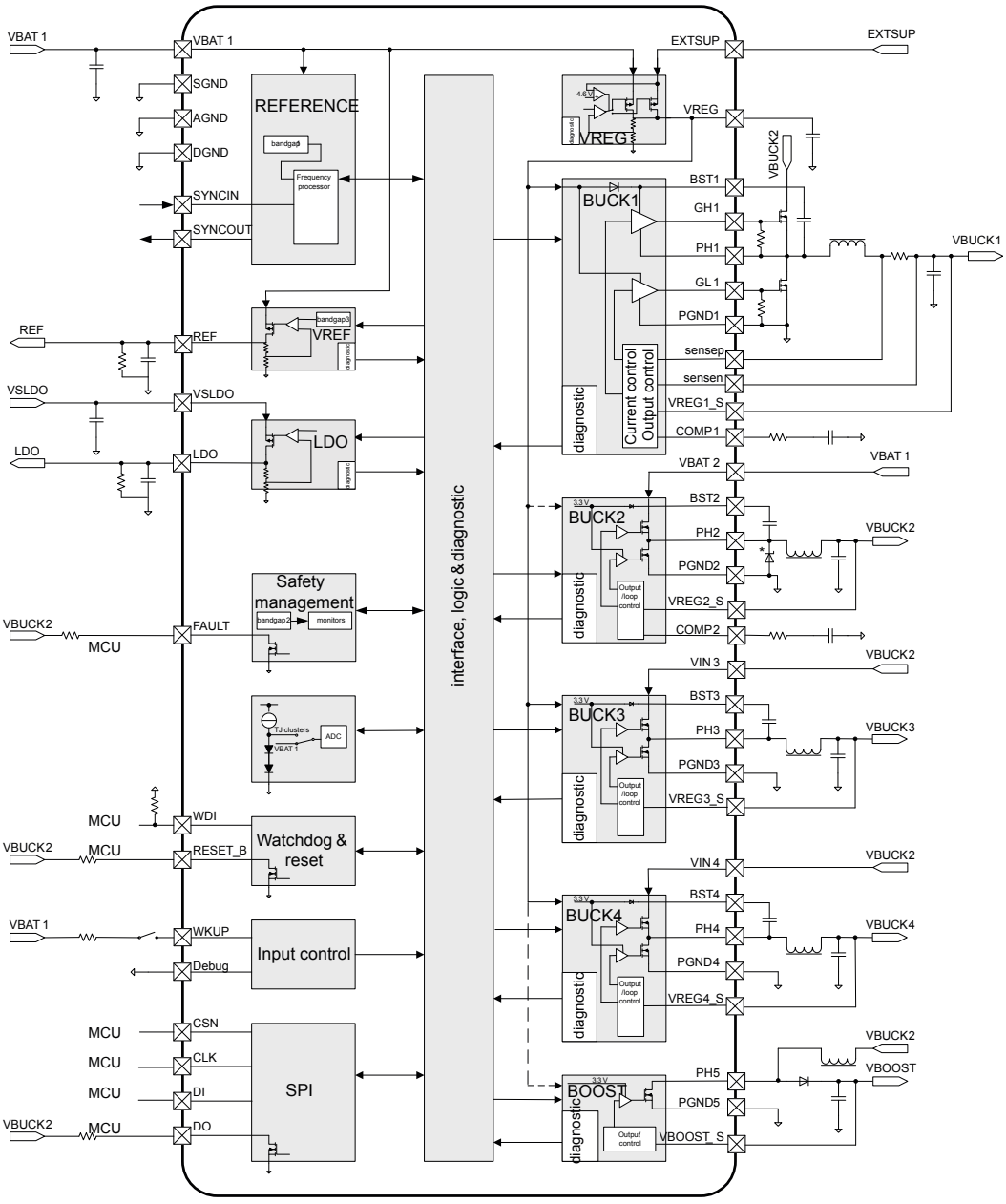
1 L5965 features

One of the main advantages in use a multi-regulator solution is the integration and scalability compared with a discrete solution. Figure 1 shows the L5965 functional block diagram to have the complete view of the device.

In the next chapters will be expressed the relationships to define the external components. Generally, the expressions define a minimum value for those components. To avoid poor dynamic behavior, it is recommended to not exceed too much (1.5 - 2 typically) the minimum value calculated if not specifically indicated.

Figure 1. Functional block diagram

Application example with BUCK2 as main buck.

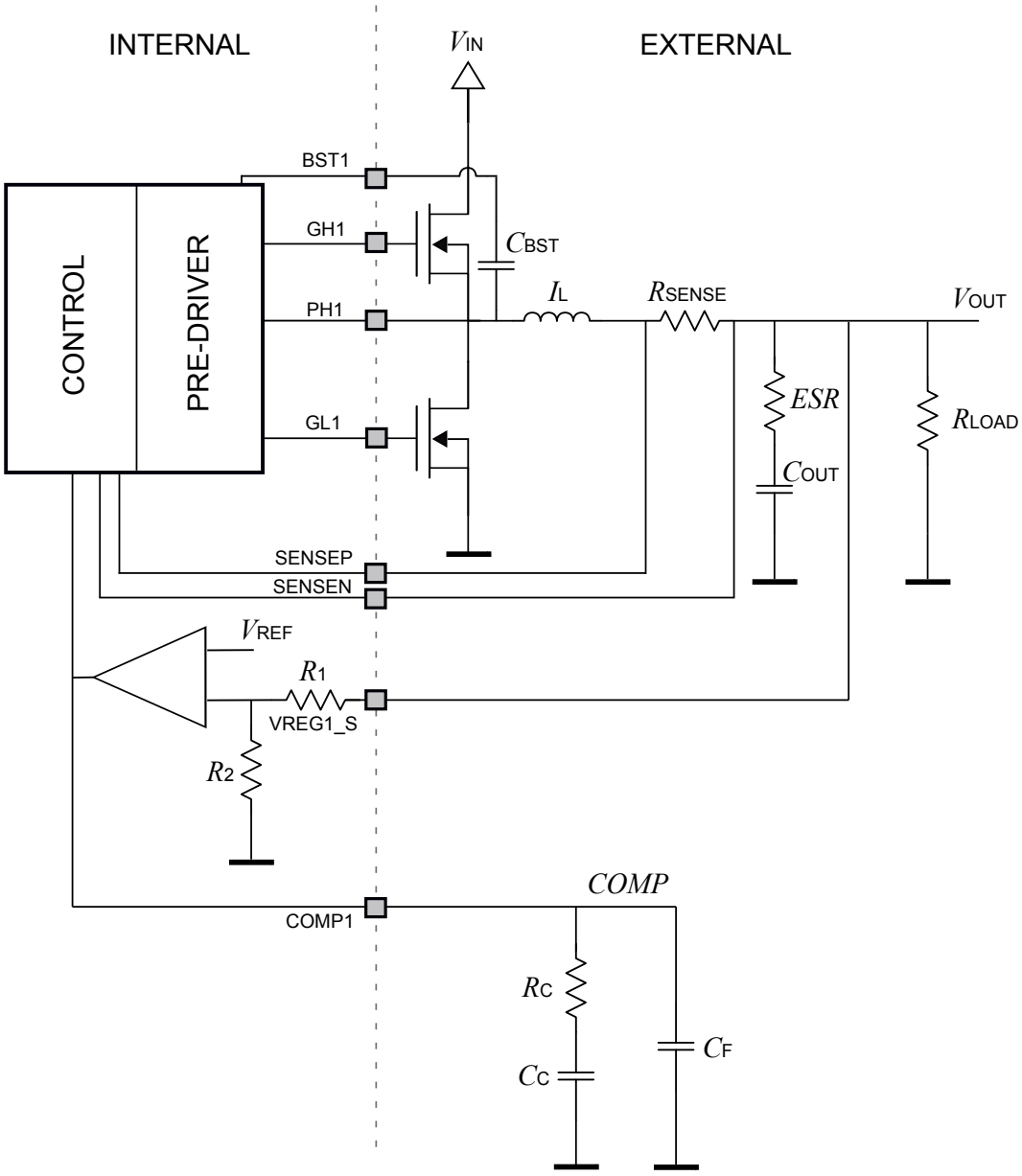


* A SCHOTTKY diode is needed. A 100 V, min 2 A forward current diode, is strongly suggested

2 BUCK1 components

BUCK1 is a controller. It is therefore necessary to provide the inductor current sense resistor and the power section (external mos) as well as the inductor, the output capacitor and the compensation network (*). The controller implements a peak current mode strategy.

Figure 2. BUCK1 Functional block diagram



Note: (*) An unproper external components choice, could activate the overcurrent flag at power-up. A read and clear of the register resets the flag.

2.1 R_{SENSE} choice

An external resistor senses the current through the inductor and reports this info to the device through two pins connection (sensp, sensn). R_{SENSE} value must be chosen so that the maximum forward peak current in the inductor generates a voltage (V_{SENSE}) across the sense pins big enough to trigger the current limitation.

The typical value of V_{SENSE} is 75 mV.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK\_LIM}} \quad (1)$$

Where a reasonable choice is $I_{PEAK\_LIM} = I_{L(PEAK)}$.

2.2 Output inductor

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. To achieve the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

As an example, the current ripple can be evaluated with the usage of the following equation:

$$I_{Ripple} = \Delta I_L = 0.3\, I_{OUT(MAX)} \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current.

Then, the inductor value can be estimated by the equation:

$$L = \frac{1}{F_{SW}\,\Delta I_L}\, V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (3)$$

Where F_{SW} is the switching frequency, $V_{IN(MAX)}$ is the maximum input voltage.

The peak current flowing in Inductor is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \quad (4)$$

If the Inductor value decreases, the peak current increases. The peak current need to be lower than the current limit of the device.

The inductor should have a saturation current higher than the device current limit.

In order to meet slope compensation, L needs to meet the following equation:

$$L > \frac{V_{OUT}}{2\, I_{slope}} \quad (5)$$

The I_{slope} is evaluated with equation:

$$I_{slope} = N\, 30\mu A\, f_{SW} \quad (6)$$

With $N = \frac{1000}{R_{sense}}$ coefficient coming for internal components and depends on the current mirror ratio.

2.3 Output capacitor

Output capacitors are selected to support load transients and output ripple current, as well as loop stability. The voltage ripple is related to the ripple current flowing into the inductor, an adequate output capacitor sizing can reduce the impact of current ripple.

$$\Delta V_{OUT(RIPPLE)} = \Delta I_L \left(ESR + \frac{1}{8\, f_{SW}\, C_{OUT}} \right) \quad (7)$$

Considering that the goal is to define the minimum output current to satisfy the desired max output ripple the equation become:

$$C_{OUT(MIN)} = \frac{\Delta I_L}{8\, f_{SW} \left(\Delta V_{OUT(RIPPLE)} - \Delta I_L\, ESR \right)} \quad (8)$$

If the capacitor is appropriately chosen, the ESR value will be quite low then the related term can be neglected with a simplification of the above equation.

The output capacitor is also important to sustain the output voltage during a load transient. In general, minimizing the ESR value and increasing the output capacitance results in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel, or by using higher quality capacitors.

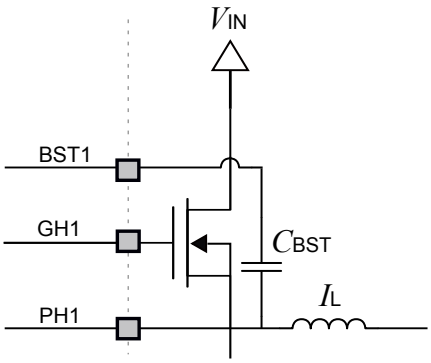
$$C_{OUT(MIN)} = \frac{L}{2} \frac{\left(I_{OUT(MAX)} - I_{OUT(MIN)} \right)^2}{MIN(V_{IN} - V_{OUT}\, ,\, V_{OUT})\, \Delta V_{OUT(MAX)}} \quad (9)$$

$\Delta V_{OUT(MAX)}$ max allowed transient output variation.

2.4 Bootstrap capacitor

The bootstrap capacitor is inserted between inductor (PH1 side) and BST1 pin as reported in Figure 3, a reasonable choice is 100 nF. The voltage rating of the capacitor is at least 9 V. The bootstrap capacitor should be a high-quality ceramic type with good temperature stability.

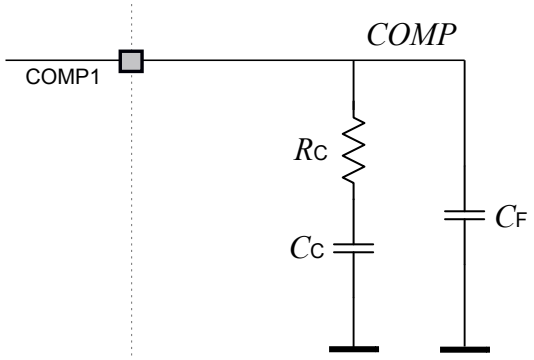
Figure 3. BUCK1 bootstrap capacitor



2.5 Compensation network

The compensation network components selection is crucial to ensure stability and good dynamic performance to the regulator. The loop control strategy as already stated is based on the peak current mode control, compatible with external RC compensation network. The error amplifier is a trans-conductance amplifier with large bandwidth, which is larger than the closed-loop one.

Figure 4. BUCK1 compensation network components



In Figure 4 are reported the external compensation network components. The basic regulator loop is modeled as a power modulator, an output feedback divider and an error amplifier. The loop transfer function is:

$$L_{(s)} = \frac{V_{REF}}{V_{OUT}} G_{MOD}(s)\, G_{EA}(s) \quad (10)$$

Where:

V_{REF} is the internal reference voltage equal to 0.8 V as defined in the specific implementation.

V_{OUT} is the converter output voltage.

$G_{MOD}(s)$ is the transfer function of the error amplifier, it forms a pole and zero, as expressed in the equation:

$$G_{MOD}(s) = \frac{g_{mMOD}\, R_{LOAD}\, (1 + sESR\, C_{OUT})}{(1 + sR_{LOAD}\, C_{OUT})} \quad (11)$$

g_{mMOD} for the BUCK1 converter it is related to the extremal sense resistor and internal partitioning ration.

$$g_{mMOD} = \frac{1}{10\ R_{sense}} \quad (12)$$

R_{LOAD} is obtained for the specific output voltage and current selection as:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} \quad (13)$$

The dominant pole is:

$$f_{pMOD} = \frac{1}{2\pi\, C_{OUT}\, (R_{LOAD} + ESR)} \quad (14)$$

The zero is:

$$f_{zMOD} = \frac{1}{2\pi\, C_{OUT}\, ESR} \quad (15)$$

$G_{EA}(s)$ is the transfer function of the buck converter from control to output. As reported in the equation It forms two poles and a zero.

$$G_{EA}(s) \simeq \frac{g_{mEA}\, r_o\, (1 + sR_C\, C_C)}{(1 + sr_o\, C_C)(1 + sR_C\, C_F)} \quad (16)$$

g_{mEA} is the trans-conductance of the error amplifier, 500 µs.

r_o is the output resistance of the error amplifier.

The zero is:

$$f_{zEA} = \frac{1}{2\pi\, C_C\, R_C} \quad (17)$$

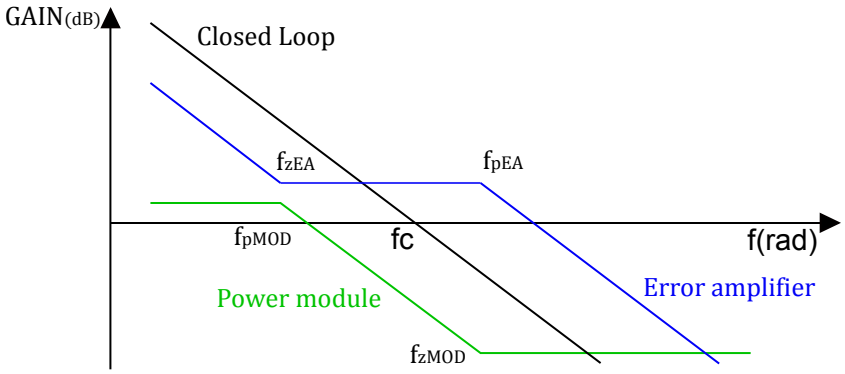
The first pole it can be considered at low frequency because r_o is very big, the second pole is:

$$f_{pEA} = \frac{1}{2\pi C_F R_C} \quad (18)$$

The choice to select the compensation values is to cancel the f_{pMOD} with f_{zEA} and the f_{zMOD} with f_{pEA}.

The second cancellation is necessary only if the f_{zMOD} is near to the crossover frequency f_c (see Figure 5).

Figure 5. BUCK1 simplified gain plot



The power modulator has a DC gain reported in equation:

$$GAIN_{MOD(DC)} = g_{mMOD}\ R_{LOAD} \quad (19)$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_c should be equal to 1.

Then:

$$\frac{V_{REF}}{V_{OUT}} GAIN_{MOD}\left(f_c\right) G_{EA}(f_c) = 1 \quad (20)$$

Where:

$$GAIN_{MOD}\left(f_c\right) = GAIN_{MOD(DC)} \frac{f_{pMOD}}{f_c} \quad (21)$$

$$G_{EA}(f_c) = g_{mEA}\ R_C \quad (22)$$

From Eq. (20):

$$R_C = \frac{V_{OUT}}{g_{mEA} V_{REF}\ GAIN_{MOD}(f_c)} \quad (23)$$

The procedure to follow step by step to define the external network components is:

1. Choose a suitable value for f_c, usually between $\frac{f_{SW}}{5}$ and $\frac{f_{SW}}{10}$.
2. Choose the V_{OUT} value within the selectable options.
3. Calculate the R_C value of with expression Eq. (23):

$$R_C = \frac{V_{OUT}}{g_{mEA} V_{REF}\ GAIN_{MOD}(f_c)} \quad (24)$$

4. Calculate C_C the value by forcing $f_{pMOD} = f_{zEA}$:

$$C_C = \frac{1}{2\pi f_{pMOD} R_C} \quad (25)$$

5. If f_{zMOD} is less than $5\ f_c$, add a second capacitor, C_F, by forcing $f_{zMOD} = f_{pEA}$:

$$C_F = \frac{1}{2\pi f_{zMOD} R_C} \quad (26)$$

2.6 Specific sizing example

In this example is considered to use the BUCK1 as pre-regulator. This leads to an assumption of $V_{IN} = 12\ V$ and $V_{OUT} = 5\ V$, $I_{OUT(MAX)} = 2\ A$ and $f_{SW} = 400\ kHz$.

$$\Delta I_L = 0.3\ I_{OUT(MAX)} = 0.6\ A \tag{27}$$

$$I_{PEAK\_LIM} = I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} = 2.3\ A \tag{28}$$

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK\_LIM}} = \frac{75\ mV}{2.3\ A} = 32\ m\Omega \tag{29}$$

Assuming $V_{IN(MAX)} = 18\ V$

$$L = \frac{1}{F_{SW}\,\Delta I_L}\ V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) = 15\ \mu H \tag{30}$$

This value needs to be checked with the respect of the absolute minimum due to I_{slope}.

$$I_{slope} = N\ 30\ \mu A\ f_{SW} = 0.34\ A/\mu s \tag{31}$$

$$L_{MIN} > \frac{V_{OUT}}{2\ I_{slope}} = 7.4\ \mu H \tag{32}$$

From this check it is confirmed the value of L previously calculated.

With a choice of 2.5% max variation for the output $\Delta V_{OUT(RIPPLE)} = 0.125\ V$.

$$C_{OUT(MIN)} = \frac{\Delta I_L}{8\ f_{SW}\ \left(\Delta V_{OUT(RIPPLE)} - \Delta I_L\ ESR\right)} = 1.5\ \mu F \tag{33}$$

A reasonable choice can be $C_{OUT} = 1.8\ \mu F$.

To complete the C_{OUT} evaluation is needed to take into account also the dynamic load current variation (see Eq. (9)). The example does not include this contribution for sake of clarity.

After chosen the inductor and capacitor values it is possible to define the compensation network, starting from the evaluation of f_{pMOD} and f_{zMOD}.

With $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = 2.5\ \Omega$ and $ESR = 0.01\ \Omega$

$$f_{pMOD} = \frac{1}{2\pi\ C_{OUT}\ (R_{LOAD} + ESR)} = 35\ \text{KHz} \tag{34}$$

$$f_{zMOD} = \frac{1}{2\pi\ C_{OUT}\ ESR} = 8.8\ MHz \tag{35}$$

With this previous info and defined the $f_c = 80\ KHz$ and $GAIN_{MOD(DC)} = 7.8$, the $GAIN_{MOD(f_c)}$ is:

$$GAIN_{MOD(f_c)} = GAIN_{MOD(DC)}\ \frac{f_{pMOD}}{f_c} = 3.4 \tag{36}$$

Last step is to evaluate the compensation values R_C, C_C:

$$R_C = \frac{V_{OUT}}{g_{mEA}\ V_{REF}\ GAIN_{MOD(f_c)}} = 3.7\ K\Omega \tag{37}$$

$$C_C = \frac{1}{2\pi\ f_{pMOD}\ R_C} = 1.23\ nF \tag{38}$$

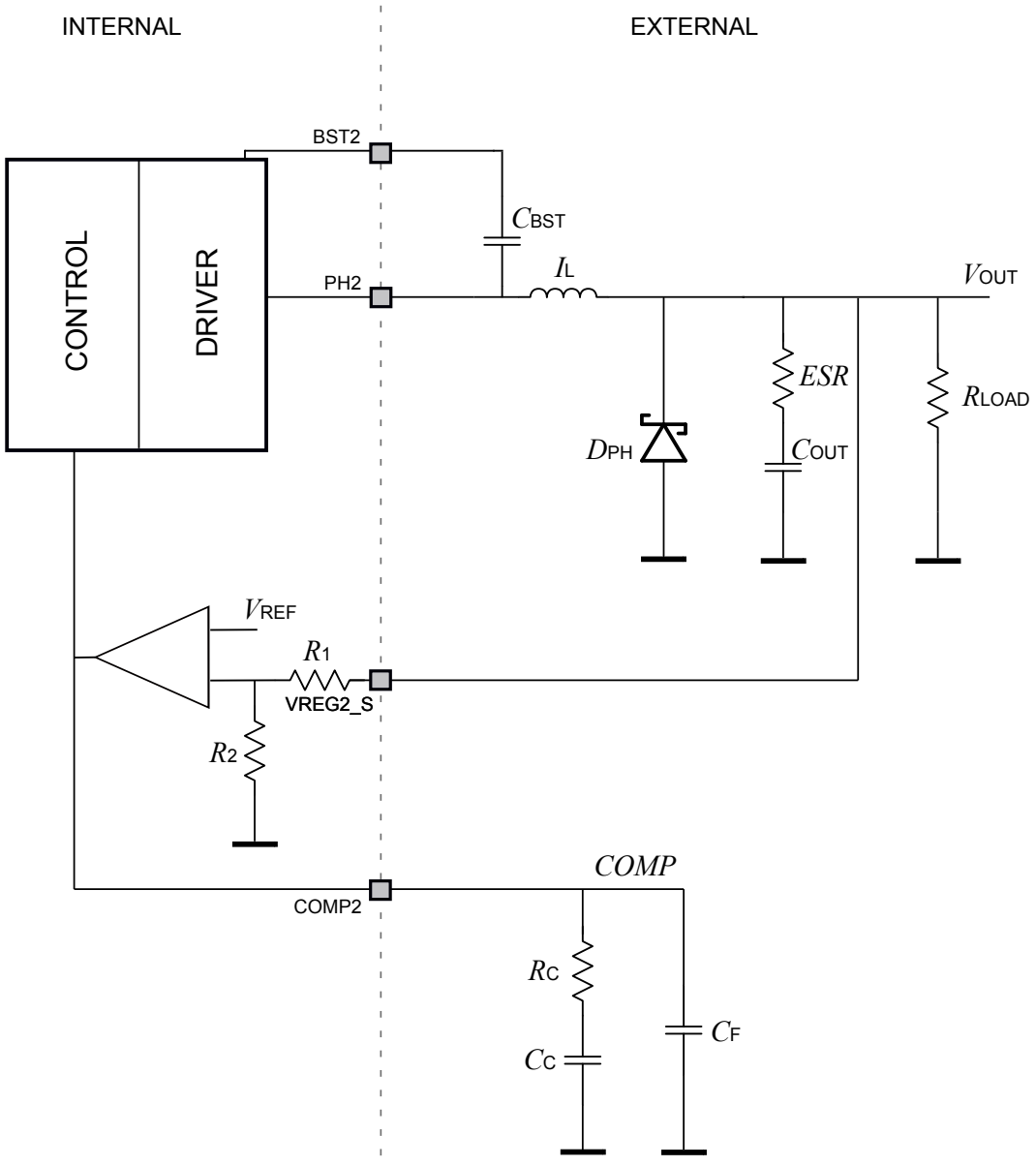
Finally, the optional extra capacitor C_F:

$$C_F = \frac{1}{2\pi\ f_{zMOD}\ R_C} = 4.9\ pF \tag{39}$$

3 BUCK2 components

BUCK2 is a converter. It is therefore necessary to provide the inductor, the output capacitor and the compensation network externally (see Figure 6) (*). The controller implements a peak current mode strategy.

Figure 6. BUCK2 Functional block diagram



Note: (*) An unproper external components choice, could activate the overcurrent flag at power-up. A read and clear of the register resets the flag.

3.1 Output inductor

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. To achieve the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

As an example, the current ripple can be evaluated with the usage of Eq. (40):

$$I_{Ripple} = \Delta I_L = 0.3\, I_{OUT(MAX)} \tag{40}$$

Where $I_{OUT(MAX)}$ is the maximum output current.

Then, the inductor value can be estimated by the equation:

$$L = \frac{1}{F_{SW}\,\Delta I_L}\, V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \tag{41}$$

Where F_{SW} is the switching frequency and $V_{IN(MAX)}$ is the maximum input voltage.

The peak current flowing through the inductor is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{42}$$

If the Inductor value decreases, the peak current increases. The peak current need to be lower than the current limit of the device.

The inductor should have a saturation current higher than the device current limit.

in order to meet slope compensation, L needs to meet the following equation:

$$L > \frac{V_{OUT}}{2\, I_{slope}} \tag{43}$$

The I_{slope} for BUCK2 is evaluated with equation:

$$I_{slope} = N\, 45\ \mu A\ f_{SW} \tag{44}$$

With $N = 5{*}4000$ coefficient coming for internal components and depends on the current mirror ratio.

3.2 Output capacitor

Output capacitors are selected to support load transients and output ripple current, as well as loop stability. The voltage ripple is related to the ripple current flowing into the inductor, an adequate output capacitor sizing can reduce the impact of current ripple.

$$\Delta V_{OUT(RIPPLE)} = \Delta I_L\left(ESR + \frac{1}{8\, f_{SW}\, C_{OUT}}\right) \tag{45}$$

Considering that the goal is to define the minimum output current to satisfy the desired max output ripple the equation become:

$$C_{OUT(MIN)} = \frac{\Delta I_L}{8\, f_{SW}\left(\Delta V_{OUT(RIPPLE)} - \Delta I_L\, ESR\right)} \tag{46}$$

If the capacitor is appropriately chosen, the ESR value will be quite low then the related term can be neglected with a simplification of the above equation.

The output capacitor is also important to sustain the output voltage during a load transient. In general, minimizing the ESR value and increasing the output capacitance results in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel, or by using higher quality capacitors.

$$C_{OUT(MIN)} = \frac{L}{2}\,\frac{\left(I_{OUT(MAX)} - I_{OUT(MIN)}\right)^2}{MIN(V_{IN} - V_{OUT}\,, V_{OUT})\,\Delta V_{OUT(MAX)}} \tag{47}$$

$\Delta V_{OUT(MAX)}$ max allowed transient output variation.

3.3 Bootstrap capacitor

A bootstrap capacitor must be connected between the BST2 and PH2 pins to provide a floating gate drive to the high-side MOSFET. For most applications 47 nF is sufficient. This should be a ceramic capacitor with a voltage rating of at least 6 V.

3.4 Compensation network

The compensation network components selection is crucial to ensure stability and good dynamic performance to the regulator. The loop control strategy as already stated is based on the peak current mode control, compatible with external RC compensation network. The error amplifier is a trans-conductance amplifier with large bandwidth, which is larger than the closed-loop one.

The basic regulator loop is modeled as a power modulator, an output feedback divider and an error amplifier. The loop transfer function is:

$$L_{(s)} = \frac{V_{REF}}{V_{OUT}} G_{MOD}(s)\, G_{EA}(s) \tag{48}$$

Where:

V_{REF} is the internal reference voltage equal to 1 V as defined in the specific implementation.

V_{OUT} is the converter output voltage.

$G_{MOD}(s)$ is the transfer function of the error amplifier, it forms a pole and zero, as expressed in the Eq. (49):

$$G_{MOD}(s) = \frac{g_{mMOD}\, R_{LOAD}\, (1 + sESR\, C_{OUT})}{(1 + sR_{LOAD}\, C_{OUT})} \tag{49}$$

g_{mMOD} for the BUCK2 is 2.2 s.

R_{LOAD} is obtained for the specific output voltage and current selection as:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} \tag{50}$$

The dominant pole is:

$$f_{pMOD} = \frac{1}{2\pi\, C_{OUT}\, (R_{LOAD} + ESR)} \tag{51}$$

The zero is:

$$f_{zMOD} = \frac{1}{2\pi\, C_{OUT}\, ESR} \tag{52}$$

$G_{EA}(s)$ is the transfer function of the buck converter from control to output. As reported in the equation It forms two poles and a zero.

$$G_{EA}(s) \backsimeq \frac{g_{mEA}\, r_o\, (1 + sR_C\, C_C)}{(1 + sr_o\, C_C)(1 + sR_C\, C_F)} \tag{53}$$

g_{mEA} is the trans-conductance of the error amplifier, 1 ms.

r_o is the output resistance of the error amplifier.

The zero is:

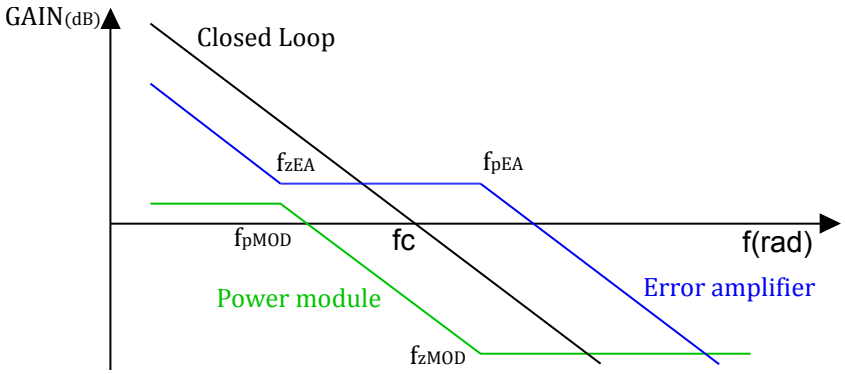
$$f_{zEA} = \frac{1}{2\pi\, C_C\, R_C} \tag{54}$$

The first pole it can be considered in the origin because r_o is very big, the second pole is:

$$f_{pEA} = \frac{1}{2\pi\, C_F\, R_C} \tag{55}$$

The choice to select the compensation values is to cancel the f_{pMOD} with f_{zEA} and the f_{zMOD} with f_{pEA}. The second cancellation is necessary only if the f_{zMOD} is near to the crossover frequency f_c (see Figure 7).

Figure 7. **BUCK2 simplified gain plot**



The power modulator has a DC gain reported in the Eq. (56):

$$GAIN_{MOD(DC)} = g_{mMOD}\ R_{LOAD} \tag{56}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_c should be equal to 1.

Then:

$$\frac{V_{REF}}{V_{OUT}} GAIN_{MOD}\left(f_c\right) G_{EA}(f_c) = 1 \tag{57}$$

Where:

$$GAIN_{MOD}\left(f_c\right) = GAIN_{MOD(DC)} \frac{f_{pMOD}}{f_c} \tag{58}$$

$$G_{EA}(f_c) = g_{mEA}\ R_C \tag{59}$$

Finally:

$$R_C = \frac{V_{OUT}}{g_{mEA} V_{REF}\ GAIN_{MOD}(f_c)} \tag{60}$$

The procedure to follow step by step to define the external network components is:

1. Choose a suitable value for f_c, usually between $\frac{f_{SW}}{5}$ and $\frac{f_{SW}}{10}$.
2. Choose the V_{OUT} value within the selectable options.
3. Calculate the value of R_C:

$$R_C = \frac{V_{OUT}}{g_{mEA} V_{REF}\ GAIN_{MOD}(f_c)} \tag{61}$$

4. Calculate the C_C value by forcing $f_{pMOD} = f_{zEA}$:

$$C_C = \frac{1}{2\pi f_{pMOD} R_C} \tag{62}$$

5. If f_{zMOD} is less than $5\ f_c$, add a second capacitor, C_F, by forcing $f_{zMOD} = f_{pEA}$:

$$C_F = \frac{1}{2\pi f_{zMOD} R_C} \tag{63}$$

3.5 PH diode

It is necessary to insert a Schottky diode between the BUCK2 phase and GND as close as possible to the device pins. The diode must ensure almost 2 A forward current and minimum 100 V for reverse voltage.

3.6 Specific sizing example

3.6.1 Example 1

In this example is considered to use the BUCK2 as pre-regulator. This leads to an assumption of $V_{IN} = 12\ V$ and $V_{OUT} = 5\ V$, $I_{OUT(MAX)} = 2\ A$ and $f_{SW} = 400\ kHz$.

$$\Delta I_L = 0.3\ I_{OUT(MAX)} = 0.6\ A \tag{64}$$

$$L = \frac{1}{F_{SW}\,\Delta I_L}\ V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) = 15\ \mu H \tag{65}$$

This value needs to be checked with the respect of the absolute minimum due to I_{slope}.

$$I_{slope} = N\ 45\ \mu A\ f_{SW} = 0.36\ A/\mu s \tag{66}$$

$$L_{MIN} > \frac{V_{OUT}}{2\ I_{slope}} = 7.0\ \mu H \tag{67}$$

From this check it is confirmed the value of L previously calculated.

With a choice of 2.5% max variation for the output $\Delta V_{OUT(RIPPLE)} = 0.125\ V$.

$$C_{OUT(MIN)} = \frac{\Delta I_L}{8\ f_{SW}\ \left(\Delta V_{OUT(RIPPLE)} - \Delta I_L\ ESR\right)} = 1.5\ \mu F \tag{68}$$

A reasonable choice can be $C_{OUT} = 1.8\ \mu F$.

To complete the C_{OUT} evaluation is needed to take into account also the dynamic load current variation (see Eq. (40)). The example does not include this contribution for sake of clarity.

After chosen the inductor and capacitor values it is possible to define the compensation network, starting from the evaluation of f_{pMOD} and f_{zMOD}.

With $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = 2.5\ \Omega$ and $ESR = 0.01\ \Omega$

$$f_{pMOD} = \frac{1}{2\pi\ C_{OUT}\ (R_{LOAD} + ESR)} = 35\ \text{KHz} \tag{69}$$

$$f_{zMOD} = \frac{1}{2\pi\ C_{OUT}\ ESR} = 8.8\ MHz \tag{70}$$

With this previous info and defined the $f_c = 80\ KHz$ and $GAIN_{MOD(DC)} = 5.5$, the $GAIN_{MOD(f_c)}$ is:

$$GAIN_{MOD(f_c)} = GAIN_{MOD(DC)}\ \frac{f_{pMOD}}{f_c} = 2.4 \tag{71}$$

Last step is to evaluate the compensation values R_C, C_C:

$$R_C = \frac{V_{OUT}}{g_{mEA}\ V_{REF}\ GAIN_{MOD(f_c)}} = 2.1\ K\Omega \tag{72}$$

$$C_C = \frac{1}{2\pi\ f_{pMOD}\ R_C} = 2.16\ nF \tag{73}$$

Finally, the optional extra capacitor C_F:

$$C_F = \frac{1}{2\pi\ f_{zMOD}\ R_C} = 8.61\ pF \tag{74}$$

3.6.2 Example 2

In this example is considered to use the BUCK2 as post-regulator. This leads to an assumption of $V_{IN} = 5\ V$ and $V_{OUT} = 1.5\ V$, $I_{OUT(MAX)} = 2\ A$ and $f_{SW} = 2.4\ MHz$.

$$\Delta I_L = 0.3\ I_{OUT(MAX)} = 0.6\ A \tag{75}$$

$$L = \frac{1}{F_{SW}\,\Delta I_L}\ V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) = 0.66\ \mu H \tag{76}$$

This value needs to be checked with the respect of the absolute minimum due to I_{slope}.

$$I_{slope} = N\ 45\ \mu A\ f_{SW} = 2.16\ A/\mu s \tag{77}$$

$$L_{MIN} > \frac{V_{OUT}}{2\ I_{slope}} = 0.35\ \mu H \tag{78}$$

From this check is chosen the value $L = 1.2\ \mu H$.

With a choice of 2.5% max variation for the output $\Delta V_{OUT(RIPPLE)} = 0.0375\ V$.

$$C_{OUT(MIN)} = \frac{\Delta I_L}{8\ f_{SW}\ \left(\Delta V_{OUT(RIPPLE)} - \Delta I_L\ ESR\right)} = 1\ \mu F \tag{79}$$

A reasonable choice can be $C_{OUT} = 1.8\ \mu F$.

To complete the C_{OUT} evaluation is needed to take into account also the dynamic load current variation (see Eq. (40)). The example does not include this contribution for sake of clarity.

After chosen the inductor and capacitor values it is possible to define the compensation network, starting from the evaluation of f_{pMOD} and f_{zMOD}.

With $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = 0.75\ \Omega$ and $ESR = 0.01\ \Omega$

$$f_{pMOD} = \frac{1}{2\pi\ C_{OUT}\ (R_{LOAD} + ESR)} = 116\ \text{KHz} \tag{80}$$

$$f_{zMOD} = \frac{1}{2\pi\ C_{OUT}\ ESR} = 8.8\ MHz \tag{81}$$

With this previous info and defined the $f_c = 480\ KHz$ and $GAIN_{MOD(DC)} = 1.65$, the $GAIN_{MOD(f_c)}$ is:

$$GAIN_{MOD(f_c)} = GAIN_{MOD(DC)}\ \frac{f_{pMOD}}{f_c} = 0.4 \tag{82}$$

Last step is to evaluate the compensation values R_C, C_C:

$$R_C = \frac{V_{OUT}}{g_{mEA}\ V_{REF}\ GAIN_{MOD(f_c)}} = 3.75\ K\Omega \tag{83}$$

$$C_C = \frac{1}{2\pi\ f_{pMOD}\ R_C} = 0.37\ nF \tag{84}$$

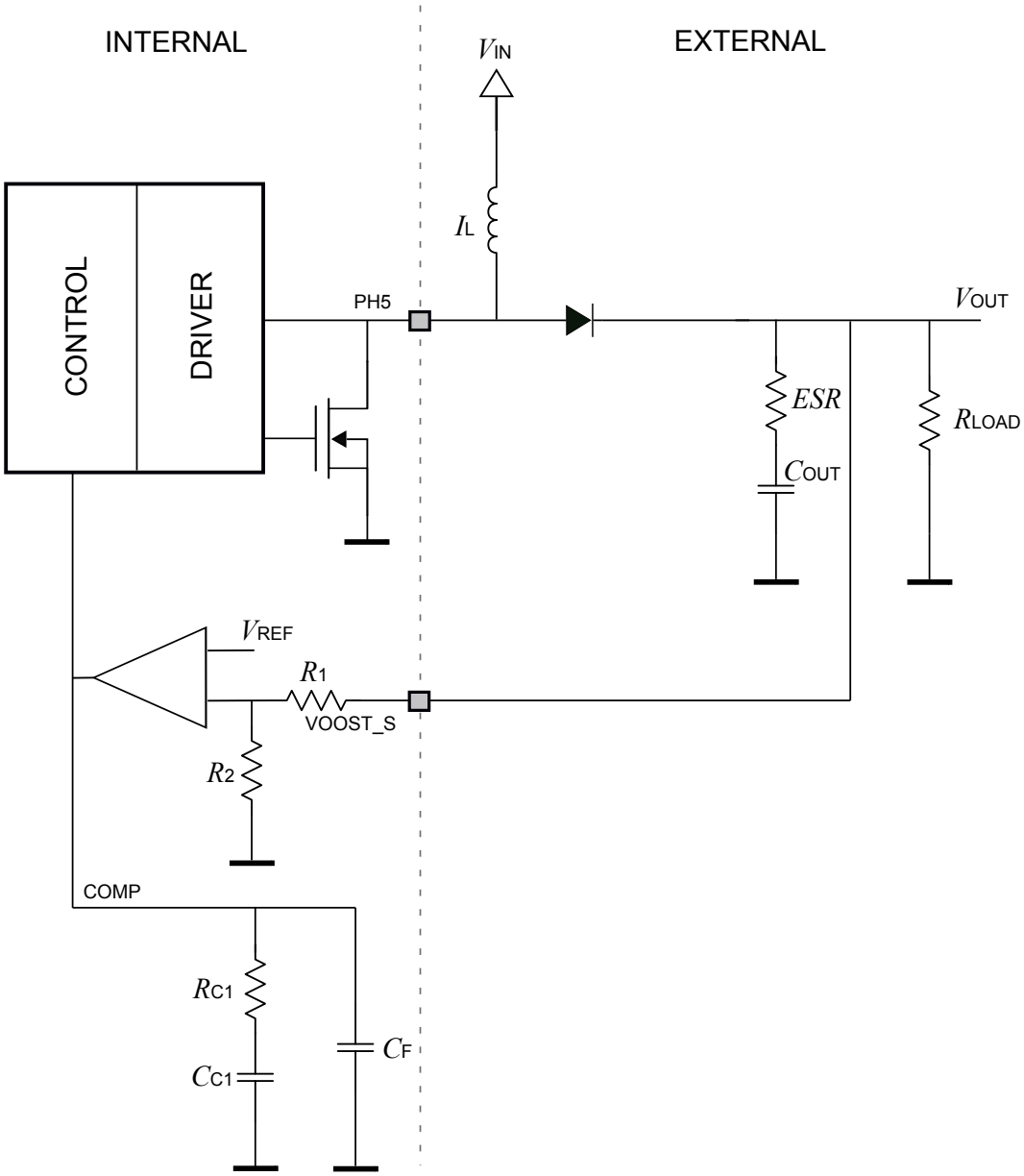
Finally, the optional extra capacitor C_F:

$$C_F = \frac{1}{2\pi\ f_{zMOD}\ R_C} = 4.82\ pF \tag{85}$$

4 BOOST components

BOOST controller integrates the compensation network, it is then needed to provide externally only the diode, the inductor and the output capacitor. The controller implements a peak current mode strategy. The implementation block diagram is reported in Figure 8.

Figure 8. BOOST Functional block diagram



4.1 Output inductor

The inductor value depends on the allowed ripple current in the coil, directly related to V_{IN}, V_{OUT} and f_{SW}.

In the specific Boost case, the maximum inductor value acceptable is limited by RHP zero value. The RHP (Right-Half-Plane) zero limits the cross frequency and is evaluated with the following equation:

$$f_{Z,\,RPH} = \frac{R_{LOAD}\left(\frac{V_{IN}}{V_{OUT}}\right)^2}{2\pi L} \tag{86}$$

From this, it is possible to obtain the inductor value for a specific $f_{Z,\,RPH}$ choice, for example with $f_{Z,\,RPH} = \frac{f_{SW}}{\pi}$ the L is reported in equation:

$$L = \frac{V_{IN}(1-D)}{2\,I_{LOAD}\,f_{SW}} \tag{87}$$

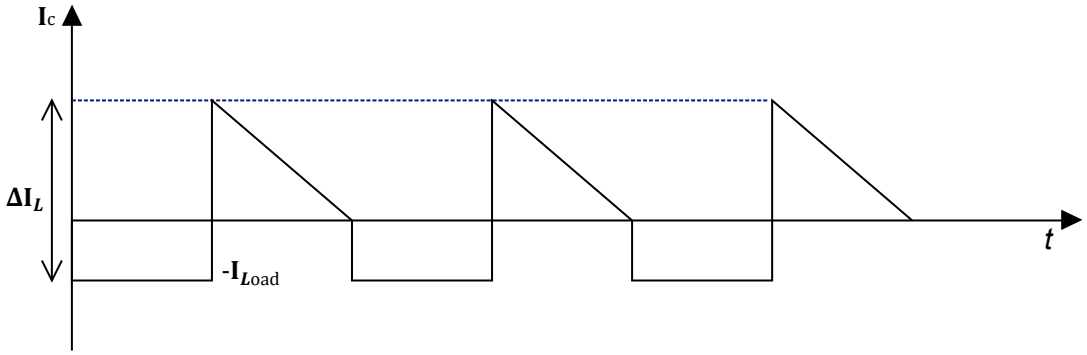
With $D = 1 - \frac{V_{IN}}{V_{OUT}}$ phase duty-cicle.

This result is obtained with the choice of a specific ΔI_L reported in equation:

$$\Delta I_L = \frac{2\,D}{(1-D)}\,I_{LOAD} \tag{88}$$

That results in the condition of zero current (see Figure 9) on output capacitor when the low side turn ON.

Figure 9. BOOST output capacitor ripple current



4.2 Output capacitor

The output capacitor choice directly impacts on two important aspects, the transient response and the output static ripple. The assumption made here is to simplify the overall system response by cancel the zero defined by the compensation network with the main pole generated with the external components choice.

The two frequencies, the zero f_{ZC} and the pole f_{P1} are evaluated with the following equations:

$$f_{ZC} = \frac{1}{2\pi R_{C1} C_{C1}} \tag{89}$$

$$f_{P1} = \frac{\left((1-D)^3 \frac{\left(0.5 + \frac{S_e}{S_n}\right)}{L\,C_L\,f_{sw}} + \frac{2}{R_L\,C_L}\right)}{2\pi} \tag{90}$$

In which $C_{C1} = 240\,pF$ and $R_{C1} = 42\,K\Omega$ are the capacitor and the resistor of the internal compensation network. Instead, S_e is the slope compensation coefficient in the specific implementation defined as $S_e = 0.528\,A/\mu s$ and S_n in the inductance current slope during ON phase evaluated with the equation:

$$S_n = \frac{V_{IN} - \frac{(ESR_L + R_{SW})}{1-D} I_{OUT}}{L} \tag{91}$$

In which R_{SW} is the total equivalent ON resistance (0.7 Ω) and ESR_L is the equivalent series resistance related to the chosen inductor.

The following equation, to evaluate the minimum value for the output capacitor, is obtained forcing the condition $f_{ZC} = f_{P1}$:

$$C_{OUT} = R_{C1}C_{C1}\left((1-D)^3 \frac{\left(0.5 + \frac{S_e}{S_n}\right)}{L\, f_{sw}} + \frac{2}{R_L} \right) \quad (92)$$

As a final check is it possible to compute the output static ripple $V_{OUT(Ripple)}$ with the following equation to confirm that it is in the acceptable range for the specific application case.

$$V_{OUT(Ripple)} = \frac{I_{OUT}\, D}{C_{OUT}} \frac{1}{f_{SW}} \quad (93)$$

To improve the overall performance, it is good practice to choose output capacitors with low ESR.

As a direct implication of the BOOST inner compensation, which is fixed, the maximum acceptable output capacitor needs to be selected based on compensation, bandwidth and phase margin.

4.3 Output diode

The reverse voltage of selected diode needs to be at least $1.25\, V_{OUT}$ of the boost.

The peak current rating of the diode must be greater than the maximum inductor current.

To reduce the power losses, it is a good practice to choose a Schottky diode. The power dissipation of the diode is estimated with the equation:

$$P_{D(MAX)} = V_{FD}\, I_{OUT} \quad (94)$$

In which V_{FD} is diode forward drop voltage.

4.4 Input capacitor

The input capacitor is chosen based on $V_{IN(Ripple)}$ and can be calculated as below.

$$C_{IN} > \frac{I_{RIPPLE}}{4\, V_{IN(Ripple)}\, f_{SW}} \quad (95)$$

$$ESR > \frac{V_{IN(Ripple)}}{2\, I_{IN(Ripple)}} \quad (96)$$

4.5 Specific sizing example

Considering a configuration in which the BOOST output voltage it is $V_{OUT} = 5\,V$ and the input voltage $V_{IN} = 3.3\,V$, it is provided by a pre-regulator. With the output voltage chosen the current in the inductor is limited to $I_{lim} = 0.6\,A$ that defines also the maximum output current as calculated in equation:

$$I_{OUT(MAX)} = I_{lim}\frac{(1-D)}{(1+D)} \quad (97)$$

In the case under analysis $D = 1 - \frac{V_{IN(MIN)}}{V_{OUT}} = 1 - \frac{3}{5} = 0.4$

As result $I_{OUT(MAX)} = 257\,mA$

With this info:

$$L = \frac{V_{IN}\,(1-D)}{2\,I_{LOAD}\,f_{SW}} = 1.45\,\mu H \quad (98)$$

A reasonable choice can be $L = 1.5\,\mu H$

With L value assigned the S_n can be calculated with Eq. (91):

$$S_n = 1.8\,A/\mu s \quad (99)$$

The minimum capacitance value $C_{OUT(MIN)} = R_{C1}C_{C1}\left((1-D)^3\frac{\left(0.5+\frac{S_e}{S_n}\right)}{L\,f_{sw}} + \frac{2}{R_L}\right) = 1.36\,\mu F$

A reasonable choice can be $C = 1.8\,\mu F$

Output voltage ripple can be evaluated for the chosen values considering equation:

$$V_{OUT(Ripple)} \approx 23\,mV \quad (100)$$

5 BUCK3 and BUCK4 components

BUCK3 and BUCK4 have an inner compensation. Below are the recommendations for selecting the external inductor and capacitors.

5.1 Output inductor and capacitor

Recommended value for inductor is:

- 2.2 µH if output voltage > 1.2 V
- 1.5 µH if output voltage ≤ 1.2 V

Recommended value for output capacitor is in the range 4.7 µF ~ 20 µF.

Inductor current/output voltage ripple can be evaluated using relations available for BUCK2 considering $f_{SW} = 2.4\,MHz$

5.2 Bootstrap capacitor

A bootstrap capacitor must be connected between the BSTx and PHx pins to provide a floating gate drive to the high-side MOSFET. For most applications 47 nF is sufficient. This should be a ceramic capacitor with a voltage rating of at least 6 V.

5.3 Input capacitor

Buck converters show a pulsating current on their input. The device requires a low-ESR input capacitor to prevent large voltage transients that can cause misbehavior of the device or interference with other circuits in the system. An input capacitor of 4.7 µF ~ 10 µF is sufficient for BUCK3 and BUCK4.

6 Conclusion

The present application note is intended to explain and facilitate the correct BUCK and BOOST external components sizing into the different applicative conditions. The main info to highlight is to keep the selected value close to the calculated one due to high impact of external components on the stability of the overall system.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
19-Oct-2022	1	Initial release.

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