RHFAD128 operating description

Introduction

The aim of this application note is to explain the principle of the RHFAD128 SAR conversion mechanism and how to program the SPI interface.

The last part of the document describes a typical user application.

The following items are described in this document:

- The SAR ADC algorithm principle
- SPI programming
- The power supply
- The input op amp
- The input filter

The RHFAD128 description

The RHFAD128 is specifically designed to withstand ionizing doses and heavy ions in space applications through a proven, high-end, CMOS technology.

This device is a low-power multiplexed, eight-input, pure CMOS, 12-bit analog-to-digital converter specified for 50 ksps to 1 Msps conversion. The architecture is based on successive approximation register with internal track-and-hold. The output serial data is straight binary and is compatible with SPI.

The analog and digital power supplies operate from 2.7 V to 3.6 V, drawing a maximum current consumption of only 2 mA. The RHFAD128 can operate over a large temperature range of -55°C to +125°C and it is housed in a hermetic ceramic Flat-16 package.

Table 1. Acronym list

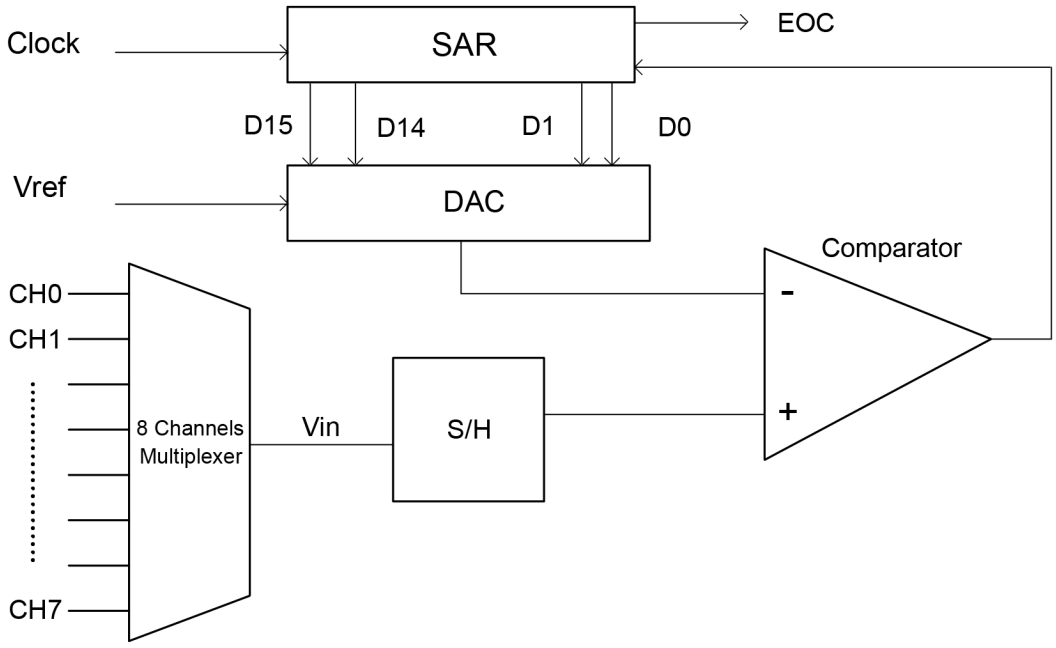
Acronym	Meaning
ADC	Analog to digital converter
SAR	Successive appoximation register
Op amp	Operational amplifier
SPI	Serial protocol interface
DAC	Digital to analog cconverter
EOC	End of conversion
DIN	Data in
DOUT	Data out
CS	Chip select
SS	Slave select
MOSI	Master out slave in
MISO	Master in slave out
SCLK	Serial clock
MSB	Most-significant bit
LSB	Least-significant bit
INL	Integral nonlinearity
DNL	Differential nonlinearity
S/H	Sample and hold

1 RHFAD128 operation

1.1 SAR algorithm principle

Figure 1 shows a standard ADC SAR block diagram.

Figure 1. A theoretical SAR ADC diagram



The SAR principle is to basically compare the reference voltage to the input voltage applied to an input channel using the dichotomy method (Figure 2).

Figure 2. An ideal SAR ADC conversion mechanism for Vin = 2 V

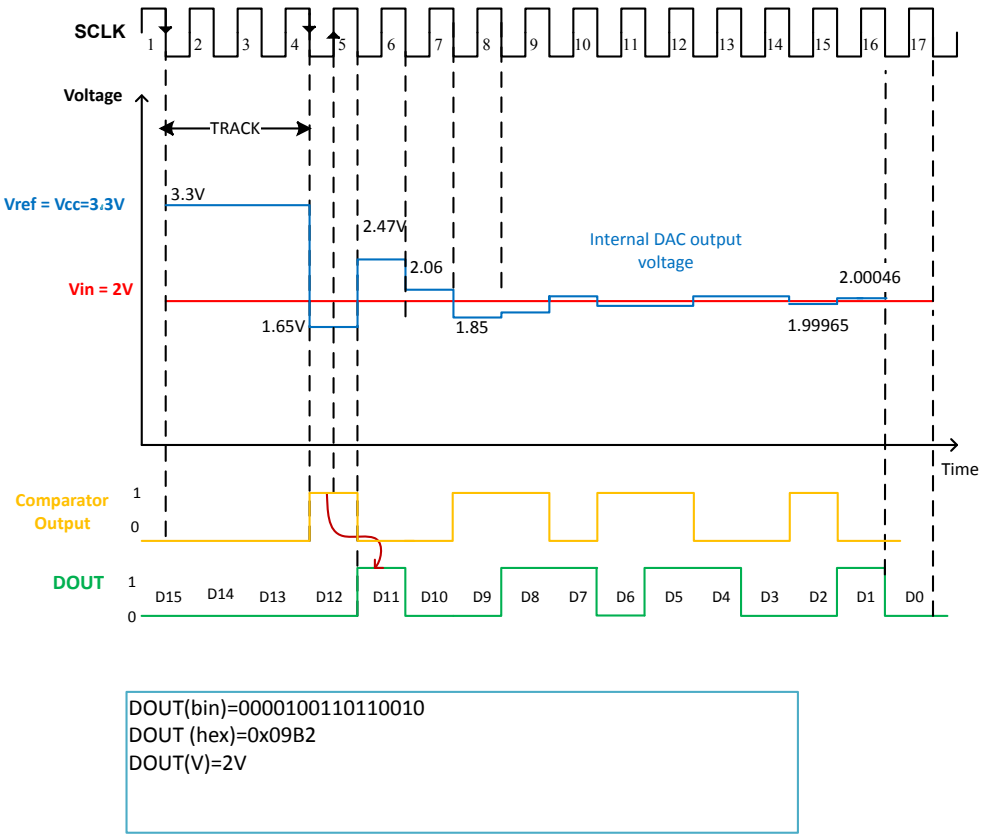


Figure 2 timing diagram shows an example of the conversion of a 2 V analog voltage applied to an ADC input channel. The analog supply voltage is AVcc = 3.3 V. It is also the internal reference voltage Vref.

The digital result code is read through the SPI DOUT signal.

It is important to note that the comparator compares its input at the clock falling edge, while the SAR DOUT is read at clock rising edge.

The data conversion is split in 2 phases:

a) The Tracking/Sampling phase

For the 3 first clock cycles, the Sample & Hold circuit records the value of Vin selected by the multiplexer and keeps it constant at the comparator positive input during the rest of the S/H cycle.

During this phase, all the first four bits of DOUT are set to low level, and the other 12 bits are undefined.

b) The Evaluation phase

During the thirteen other clocks cycles, the comparator compares the Vin with the DAC output. At the 4th clock cycle, the successive approximation algorithm begins.

- Step 1: The DAC is set to midscale Vref/2 = 1.65 V

The comparator determines whether the Vin is greater to or less than the DAC output, the comparator output = “1”.

At the next clock cycle, the SAR sets the register MSB bit, D11 = “1”.

- Step 2: The DAC is set to Vref/2 +Vref/4 = 3Vref/4 = 2.47 V

The comparator determines whether the Vin is greater to or less than the DAC output, the comparator output = “0”.

At the next clock cycle, the SAR sets the next bit D10 = "0".

- Step 3: The DAC is set to 3Vref/4 - Vref/8 = 5Vref/8 = 2.06 V

The comparator determines whether the Vin is greater or less than the DAC output, the comparator output = “0”.

At the next clock cycle, the SAR sets the next bit D9 = “0”

- Step 4: The DAC is set to 5Vref/8 - Vref/16 = 9Vref/16 = 1.85 V

The comparator determines whether the Vin is greater or less than the DAC output, the comparator output= “1”.

At the next clock cycle, the SAR sets the next bit D8 = 1.

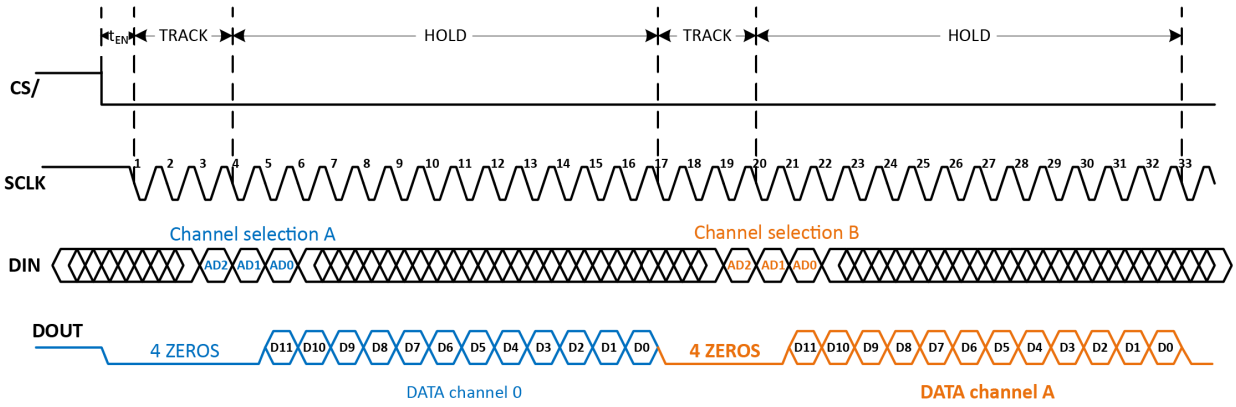
The process continues until all the bit values have been determined. The algorithm continues up to Step 12 with the result as close to VIN as possible with the best resolution.

At the end of the conversion process, a logic signal (EOC) is asserted.

1.2 SPI interface and device programming

The protocol is described in the operational timing diagram presented in Figure 3.

Figure 3. SPI interface timing diagram in single ended input



The RHFAD128 SPI naming convention is:

1. **DIN** is the signal usually named **MOSI** (Master Output Slave Input):

This signal is used to transfer to the slave the next channel number to be read.

The **DIN** signal changes on the falling edge of the clock and the data is read on the rising edge of the clock.

Table 2 shows the control register coding for the eight input channels as presented in the product datasheet.

Table 2. Control register bits

Bit#	7 (MSB)	6	5	4	3	2	1	0
Single-ended mode	Any code except 11		ADD2	ADD1	ADD0	Any code except 001		
Differential mode	1	1	0	ADD1	ADD0	0	0	1

The following two tables show an example of code to program in **DIN** to select the corresponding channel.

Table 3. Single input channel coding

Channel	Hexadecimal code
Channel 0 (default)	0x00
Channel 1	0x08
Channel 2	0x10
Channel 3	0x18
Channel 4	0x20
Channel 5	0x28
Channel 6	0x30
Channel 7	0x38

Table 4. Differential input channel coding

Channel	Hexadecimal code
Channel 0 - Channel 1	0xC1
Channel 2 - Channel 2	0xC9
Channel 4 - Channel 5	0xD1
Channel 6 - Channel 7	0xD9

Warning: When only one address code is programmed in DIN, DOUT reads the channel_0 by default. To read the Channel_x, it's address must be programmed twice or more.

For example, to read the Channel_3: DIN = 0x1800, 0x1800

2. **DOUT** is the signal usually named **MISO** (Master Input Slave Output):

This signal is used to transfer to the master the data digitalized from the analog signal present on the channel that has been selected.

The **DOUT** signal changes on the falling edge of the clock and the data is read on the rising edge of the clock.

DOUT is generated by the ADC, the data is set on the bus on the falling edge of the clock.

DOUT is set on a 16-bit frame for 12-bit information presented in natural binary format. The frame starts with 4 bits set to 0 and then the 12-bit conversion data is sent on the interface. When the frame does not start with 4 bits set to 0, the data is not correct. It is then important to restart the device, the master must set the SS signal to high level, stop the clock, and then make a new request to the ADC (sent SS low, sent the clock, sent **DIN**, received the correct answer on the second reading of the bus if the address does not represent Channel 0)

In continuous mode, the reading of the data on **DOUT** starts on the rising edge of the 17^{th} clock; the falling edge of the 16^{th} clock is the startup for counting the new number of clocks.

3. **SCLK** is the clock provided by the master to the RHFAD128:

This clock is used internally to sample the signal.

As the SPI interface runs on a 16-bit word, the internal sampling is clocked by **SCLK** divided by 16 (for 1 Msps use a 16 MHz clock)

The clock controls the acquisition and data transfer times.

This **SCLK** clock must be generated to program and read the data. In continuous mode, the clock must be an integer number multiple of 16 clocks to be able to make continuous measurements. In Burst mode, a frame of 2 x 16 clocks must be sent to read the predefined channel, because the first reading is done on channel 0 by default.

4. **nCS** (negative Chip Select) is directly linked to the slave selection line generally named SS (Slave Select):

nCS is a signal active on a low logic voltage.

nCS selects the chip that communicates on the SPI physical interface; **nCS** is also used by the RHFAD128 as a Power ON signal to start the internal state machine. It drives the track and hold of the selected channel to measure the analog signal present at the input and samples the analog signal to provide a digital word.

When **nCS** is high, the device **DOUT** is in high impedances and the clock is internally off.

When **nCS** is low, the clock arrives on the **SLCK** pin of the device and the chip is ready to convert using DIN to select the channel and **DOUT** to transfer the data to the processor with MSB first.

Moreover, the device can run in continuous mode or in burst mode.

- Continuous mode: the nCS is kept low and the clock is never stopped. The device takes the first 16 clocks to do the acquisition (track period) and the data transfer (hold period) and then the sequence is reproduced on the next 16 clocks till the nCS is set to low. Continuous mode provides the most important throughput.
- Burst mode: after 16 clocks, the nCS signal goes high (when channel 0 is the channel to be read, otherwise, the nCS must be set high after 32 clock cycles to read one of the other 7 channels (channel selection is sent during the first 16 clock cycles on DIN), the device is stopped and ready to make another conversion when the chip going to be selected. This burst mode minimizes consumption of the device.

The consumption is averaged thanks to the shutdown after the conversion.

1.3 ADC coding and maximum scaling value

The converted input voltage appears on the SPI interface in a 12-bit natural binary code format. The LSB (quantum) of the conversion is directly linked to the analog voltage that supplies the ADC.

$$LSB = \frac{AVCC}{2^{12}} = \frac{AVCC}{4096} \quad (1)$$

Typically, the LSB for 3.3 V analog supply is rounded to 0.806 mV.

The transition between the code 0x00 and 0x01 has a difference step of ½ LSB and then the difference between each code is 1 LSB.

To avoid noise issues, it is possible to use the analog power supply to also supply the sensor (temperature sensors, Wheatstone bridges, current front-end amplifiers, etc.).

2 Application design and information

This paragraph gives the main guidelines to the application designer to do a high quality ADC acquisition design. Figure 4, Figure 5 and Figure 6 are typical applications of the RHFAD128 data converter in different power supply configurations.

Figure 4. RHFAD128 typical application with two external power supplies

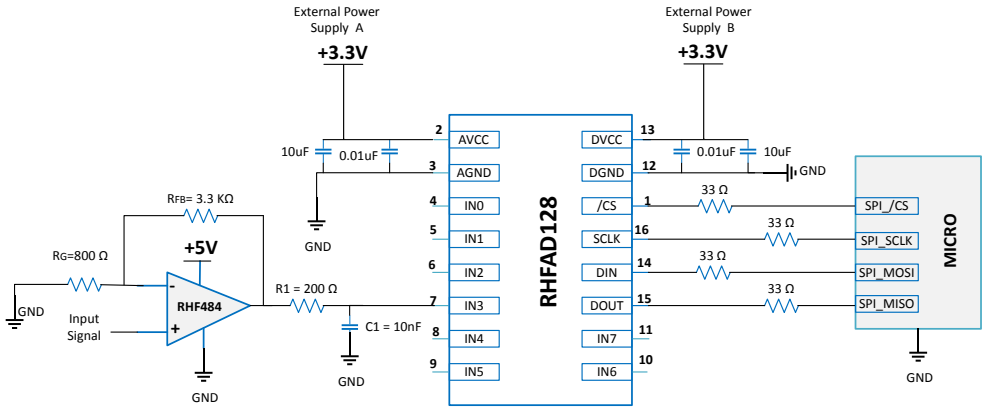


Figure 5. RHFAD128 typical application with one power supply

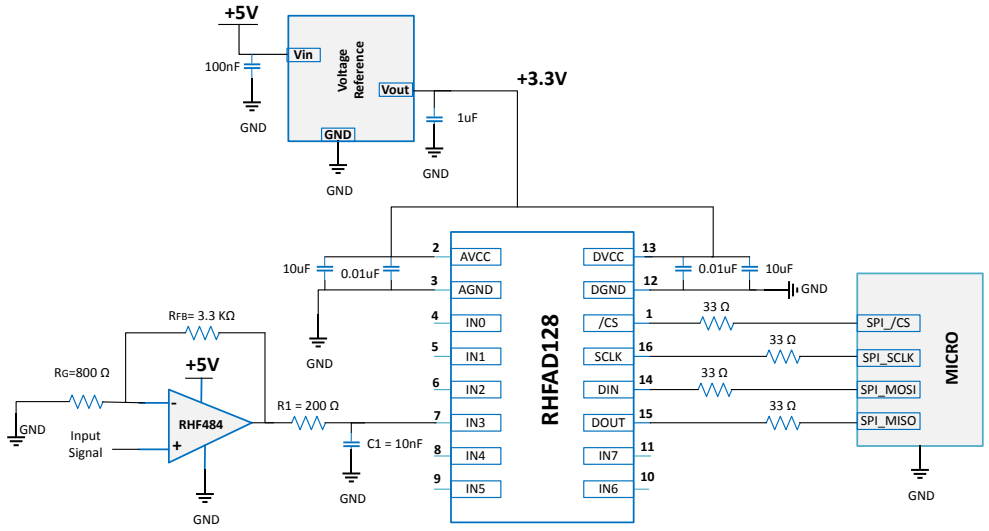
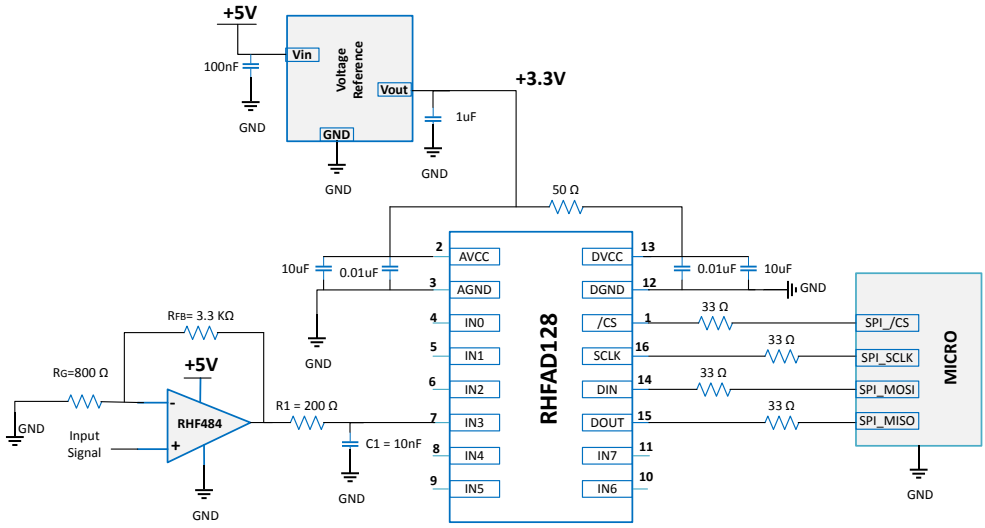


Figure 6. RHFAD128 typical application with one power supply and 50 ohm resistor



2.1 The power supplies

The RHFAD128 reference voltage is managed directly by the analog power supply.

Therefore, it is crucial to supply the device from a stable power supply.

In this section, we compare the device performances using different ways to supply the analog power domain and the digital power domain.

In Figure 5 and Figure 6, the 3.3 V power supply is provided by a high precision voltage reference with the following specification:

- Output voltage accuracy 0.05% to 0.25%
- Line regulation 5 ppm/V
- Load regulation 25 ppm/mA
- Very low output voltage noise (< 7 µVp-p)

For the decoupling capacitor, 100 nF and 1 µF have been placed at the input and output of the Vref, respectively.

The analog power supply AVCC and DVCC can vary from 2.7 V to 3.6 V.

The AVCC is also used as the voltage reference and the quantum is dependent on this voltage. This voltage should therefore be stable and well decoupled by 2 ceramic capacitors, one of 10 µF and one 0.01 µF, placed as close as possible to the RHFAD128 device.

The AVDD is the voltage used for communication with the microcontroller via SPI interface. This voltage must be also well decoupled to the ground with a 10 µF capacitor in parallel with a 0.01 µF capacitor.

For all capacitors, decoupling capacitors, and input filtering capacitors, the preferred technology is ceramic X7R-25 V.

The ground is important and must be a real voltage reference with minimum impedance. Therefore, for this ADC design, the recommendation is to have only one ground plane. It is also recommended to separate the analog power supply plan from the digital power supply plan. This helps to achieve better performance and to limit the digital noise propagation.

When SPI communication starts at a fast clock frequency, the digital power supply brings some noise to the analog power supply. As this is also used by the ADC as its internal reference voltage, the noise can disturb the conversion accuracy.

Therefore, it is strongly recommended to place a 50 Ω resistor as isolator (filter) between the 2 power domains when the same power supply is used to supply AVCC and AVDD.

The following tables show the device performances in terms of linearity in the different configurations:

- The AVCC and DVCC are supplied by 2 different external power supplies (see Figure 4)
- The AVCC and DVCC are supplied by the same power supply without the separator resistance (see Figure 5)
- The AVCC and DVCC are supplied by the same power supply with the separator resistance (see Figure 6)

The table below shows the performance difference in linearity between the 3 configurations.

Table 5. Linearity performance

VA = VD = 3.3 V, FSCLK = 16 MHz, Fs = 1 MHz, Fin = 40 KHz				
Configuration	DNL_max	DNL_min	INL_max	INL_min
Figure 4	0.4	-0.43	0.3	-0.6
Figure 5	0.7	-0.43	0.5	-0.7
Figure 6	0.4	-0.3	0.3	-0.6
Performance enhancement (%)	42.85714	30.23256	40	14.28571

Note: *Performance enhancement = 100 * (0.7 - 0.4) / 0.7*

Using the separator resistance and the recommended decoupling capacitor, the DNL and the INL have the same level of performance as the device using 2 different power supplies. The following figures (Figure 7 and Figure 8) also show the DNL distribution vs. the output code.

Figure 7. **DNL @ AVCC and DVCC connected to same power supply**

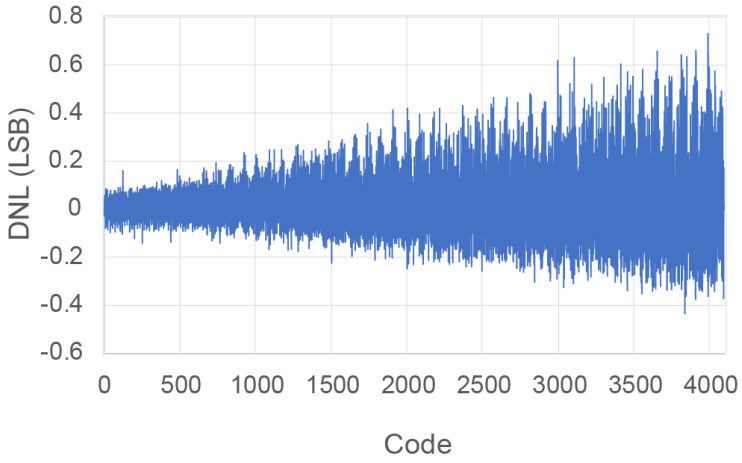
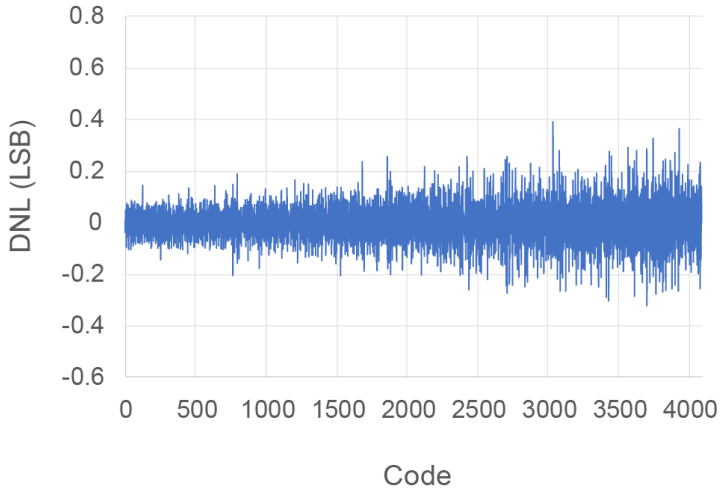


Figure 8. **DNL @ AVCC and DVCC separated by 50 Ω resistance**



2.2 Analog inputs and analog front-end constraints

The RHFAD128 inputs run from 0 to AVCC voltage (rail to rail voltage). This input voltage should not be above the supply voltage because the ADC input is saturated, and the output code is 0x0FFF.

The added front-end RHFAD128 extracts the desired analog signal from a physical parameter and then amplifies and filters it.

2.2.1 The input signal amplifier

To drive the RHFAD128, an operational amplifier can be placed at the beginning of the signal acquisition chain. Depending to the user application, the op amp can perform one or more of the following functions:

- Boost the input signal amplitude
- Buffer the signal
- Current sensing
- Extract a differential signal from common mode noise (for high side current measurement, be careful of the op amp common mode voltage).

As the RHFAD128 LSB = 806 µV for AVDD = 3.3 V, the op amp must has a smaller offset error to reduce the measurement errors.

In our application schematic (Figure 4), the ST rad-hard precision quad amp, RHF484, is used in non-inverting configuration.

Its offset error Vio = 60 µV typical.

The external op amp resistors, RG and RFB, should be chosen by the user for the op amp gain-setting according to their application.

For our example, we chose a Gain = 5.

The simplest gain expression has been used:

Gain = $1 + R_{FB} / R_G$

With: R_{FB} = 3.3 kΩ, 0.1%

R_G = 800 Ω, 0.1%

2.2.2 Settling time and input filter

During the track period, the capacitance seen typically has a value of 45 pF. The front end of the application must take this value into account to be sure that the RHFAD128 measures the right input voltage.

To achieve correct conversion, the sampling capacitor must be charged to ½ LSB within the acquisition time.

This timing is called the settling time.

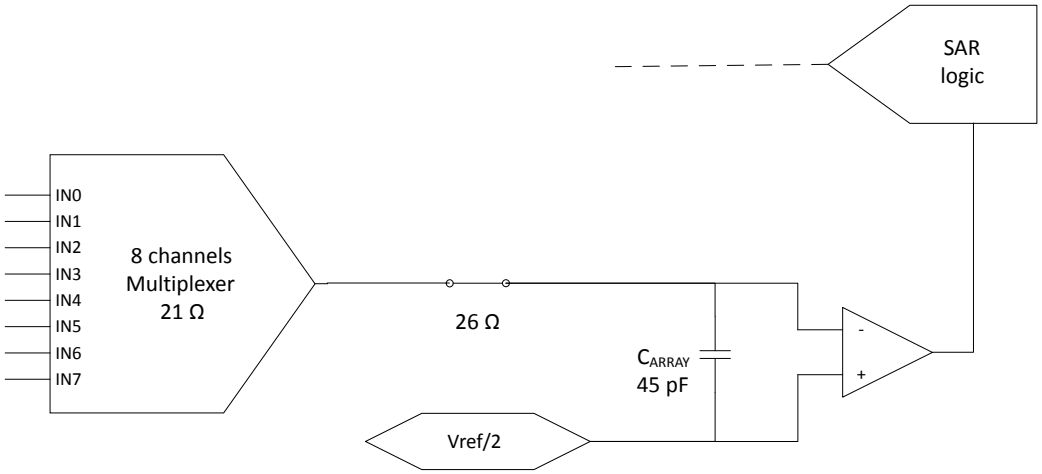
In the other words, the settling time is defined as the time it takes for the converter to settle within some specified amount of the final value (± 0.5 LSB).

Figure 9 is the equivalent schematic of the internal sampling element.

The total internal input impedance of the ADC consists of:

- The multiplexer internal resistance = 21 Ω
- The S/H element internal serial resistance = 26 Ω

Figure 9. Internal equivalent impedance



This equivalent input impedance is:
Zin = 21 Ω + 26 Ω + R1
R1 is the external RC filter resistance as shown in the application schematic, Figure 4.
To sample the input signal with 1 LSB accuracy the SCLK frequency must be lower:

$$F_{SCLK}(MHz) \leq \frac{11000}{R_1 + 47} \quad (2)$$

If C1 input capacitor is used with R1, then SCLK must be lower than:

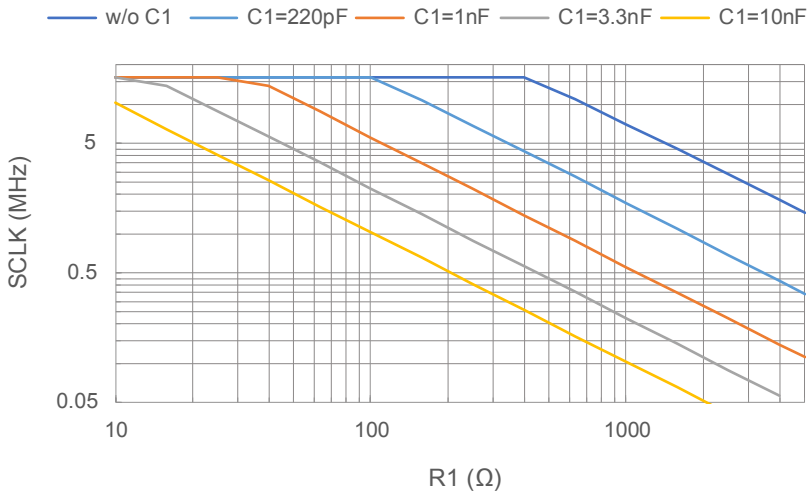
$$F_{SCLK}(MHz) \leq \frac{3 \cdot (d-b) \cdot 10^6}{2a \cdot ln\left[\frac{d}{2048 \cdot (\mathrm{d} + \mathrm{b} - 2R_1C_1)}\right]} \quad (3)$$

$a = 2115 \cdot R_1C_1$, $b = R_1C_1 + 45 \cdot R_1 + 2115$,$d = \sqrt{b^2 - 4a}$, $R_n(\Omega), C_n\,(pF),\ F_{SCLK}(MHz)$

Note: The factors 11000 and 1542 are internal characteristics of the device.

Figure 10 shows the clock frequency versus the input resistance R1 for different capacitor C1 values.
R1 = 200 Ω and C1= 10 nF is a good combination of RC filter for a clock frequency of around 500 kHz.

Figure 10. **SCLK vs. input filter resistance R1**



Revision history

Table 6. **Document revision history**

Date	Version	Changes
29-Jul-2022	1	Initial release.

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