Low-THD 350W CCM PFC pre-regulator based on L4986

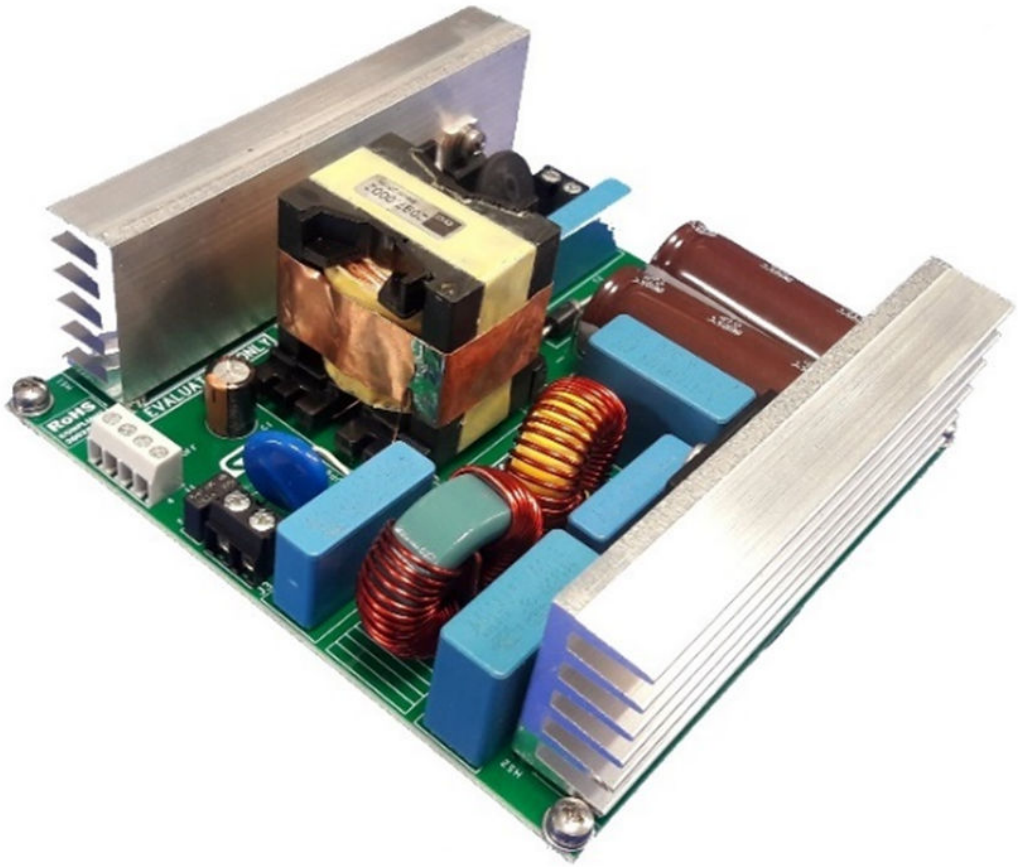
Introduction

This application note describes the demonstration board EVL4986-350W based on the new L4986 continuous conduction mode (CCM) power factor controller (PFC), and presents the main results of its bench evaluation. The board implements a 350W, wide-range input PFC pre-regulator, suitable for all SMPS from 150 W to several kW, which must comply with IEC61000-3-2 and JEITA-MITI standards.

Thanks to patented control embedded on the L4986, the design features very low input current distortion (THD) in all operating conditions, and highly limited number of external components, as the high-voltage start-up circuit and the X-cap discharge circuits are embedded in the L4986.

The L4986 includes an adjustable power good input (PG_IN), suitable for monitoring the PFC output voltage and driving a logic signal from an open drain pin (PG_OUT).

Figure 1. EVL4986-350W demonstration board



1 Main characteristics and circuit description

The main characteristics of the evaluation board are listed below:

- Input mains range: 90-265 Vac (45/65 Hz)
- Regulated output voltage (V_{OUT}): 400 Vdc
- Rated output power (P_{OUT_MAX}): 350 W
- Input current distortion (THD): < 10% from full load to 20% load
- Power Factor (PF): > 0.9 from full load to 20% load
- Converter efficiency peak (η): 97.8%
- Power good output signal (PGOOD)
- Switching frequency (F_{SW}): 65 kHz
- Mains harmonics: meets EN61000-3-2 Class-D and JEITA-MITI Class-D
- EMI: according to EN55022 Class-B
- PCB: single-sided, 70 µm, FR-4, 105 x 75 mm

The power stage of the Power Factor Converter (PFC) is a traditional boost converter, connected to the output of the bridge rectifier D3. It consists of a boost inductor L1, power switch MOSFET Q2 (Q1 is not mounted), output diode D1, and output capacitance formed by parallel electrolytic capacitors C3 and C4.

To meet EMC standards, the board is equipped with an input EMI filter to reduce the switching noise from the boost stage. L3 filters the common-mode emissions, while L2, C6, C7 reduce the differential-mode emissions.

The 300 V varistor RV1, connected between the line and the neutral, protects the circuit against high input voltage transients, while the fuse F1 disconnects the mains in case of short-circuit.

The NTC resistor, R1, in series with the output diode, limits the inrush current when the converter is plugged. The by-pass diode, D2, pre-charges the output capacitors to limit the current rushing into the boost inductor/output diode.

The L4986 embeds high-voltage start-up circuitry that charges the VCC pin (#1) up to the V_{CC_ON} threshold, sourcing a constant current I_{HV_ON} (7mA typ). The 800 V high-voltage start-up block includes circuitry to discharge the X-capacitors of the EMI filter to a safe level. This allows the unit to meet safety regulations such as IEC 61010-1 and IEC 62368-1 without using the traditional discharge resistor in parallel with the X-capacitors.

The resistors R25, R26, R27 with R19//R23 and R20//R21 are dedicated to sensing the output voltage and delivering the inverting input of the error amplifier (FB, pin #7) the feedback information necessary to keep the output voltage regulated. The components C16, R24 and C18, connected between COMP pin (#8) and ground, form the error amplifier compensation network to maintain the required loop stability.

The inductor peak current is sensed by resistors R2//R3//R4 placed in series with the ground return and the derived signal is fed into the current sense pin (CS, #4) of the L4986 via the resistor R16, used to optimize THD performance in CCM operation. A small filter capacitor C11 is connected between CS pin and ground.

The evaluation board provides a power good logic signal at connector J1 (PGOOD output signal; open drain pulled up to VCC voltage through R14 and active low) with a programmable threshold (V_{OUT_PGOFF}) through the resistors R19//R23 and R20//21.

A remote on/off control input is present at connector J1 (EBM input). Forcing 3.3V/5V at the EBM input, the FB pin (#7) is tied below the $V_{FB\_FF/EBM}$ threshold (0.5 V typ.) and the L4986 immediately stops switching activity and reduces its power consumption. The operation is restarted once the FB pin is released (EBM input tied to ground or lift floating).

A disable function is also provided, forcing 3.3V/5V at the ON/OFF input of the J1 connector. Once the COMP pin is released (ON/OFF input tied to ground or lift floating), the device restarts operation through soft start.

Figure 2. EVL4986-350W evaluation board schematic

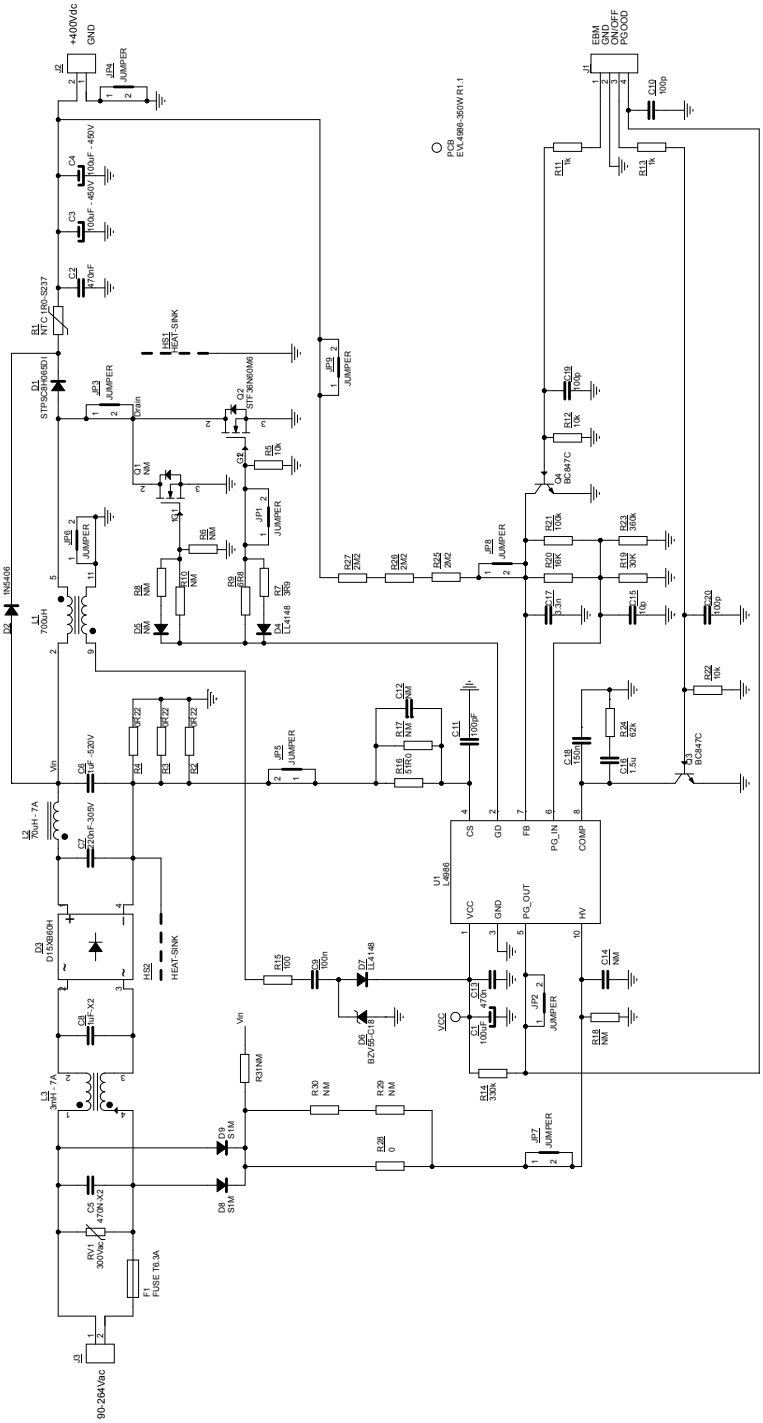


Table 1. EVL4986-350W evaluation board connectors

Schematic Reference	Description
J1	Input/output signal: 1. EBM (external burst-mode input) 2. GND (signal ground) 3. ON/OFF (enable/disable input) 4. PGOOD (Power good output)
J2	DC regulated output voltage

Schematic Reference	Description
J3	AC input voltage

Figure 3. EVL4986-350W PCB component placement (top side)

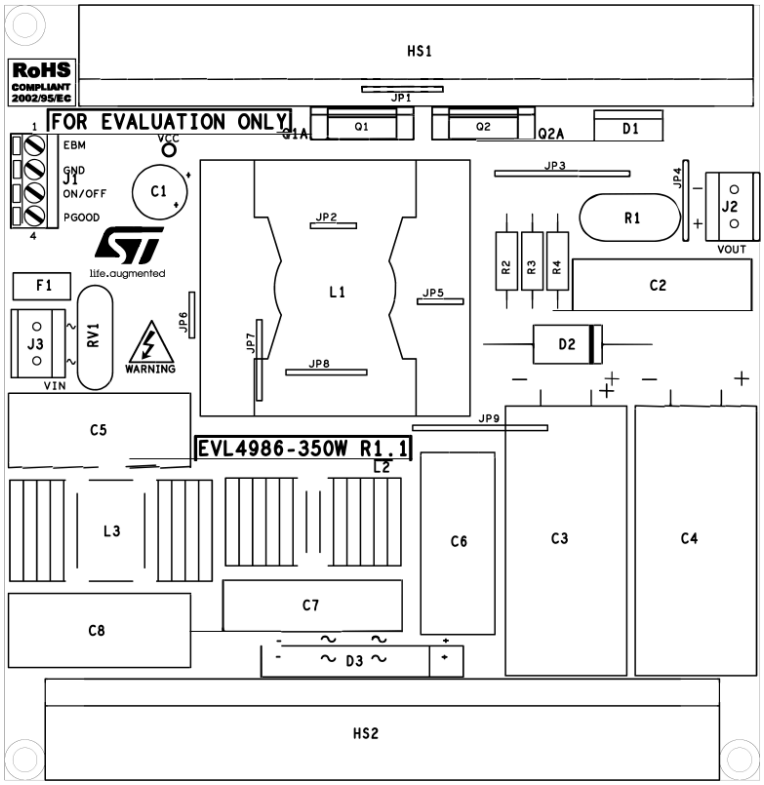


Figure 4. **EVL4986-350W PCB component placement (bottom side)**

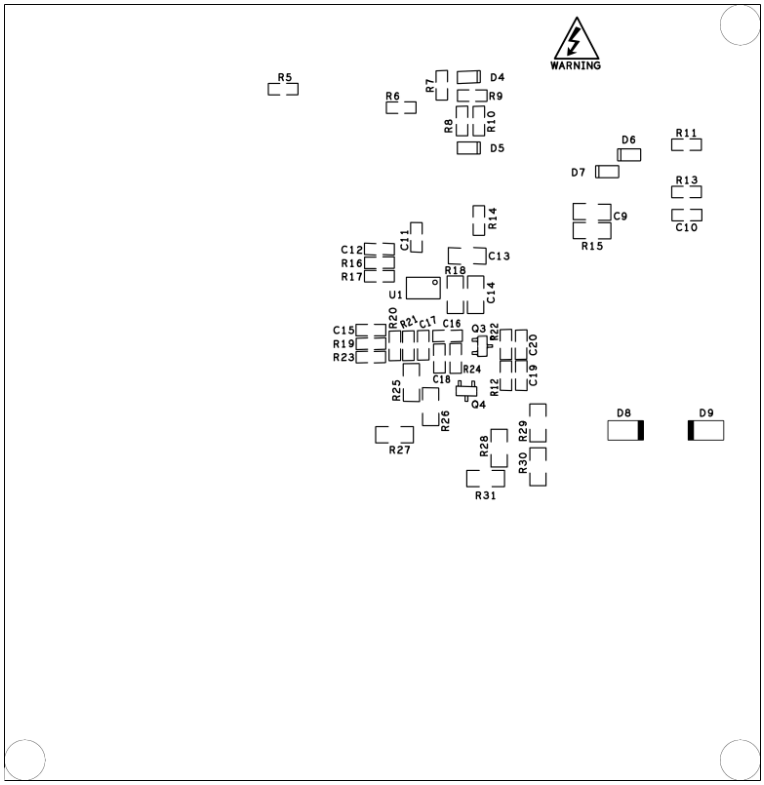


Figure 5. **EVL4986-350W PCB layout (top side)**

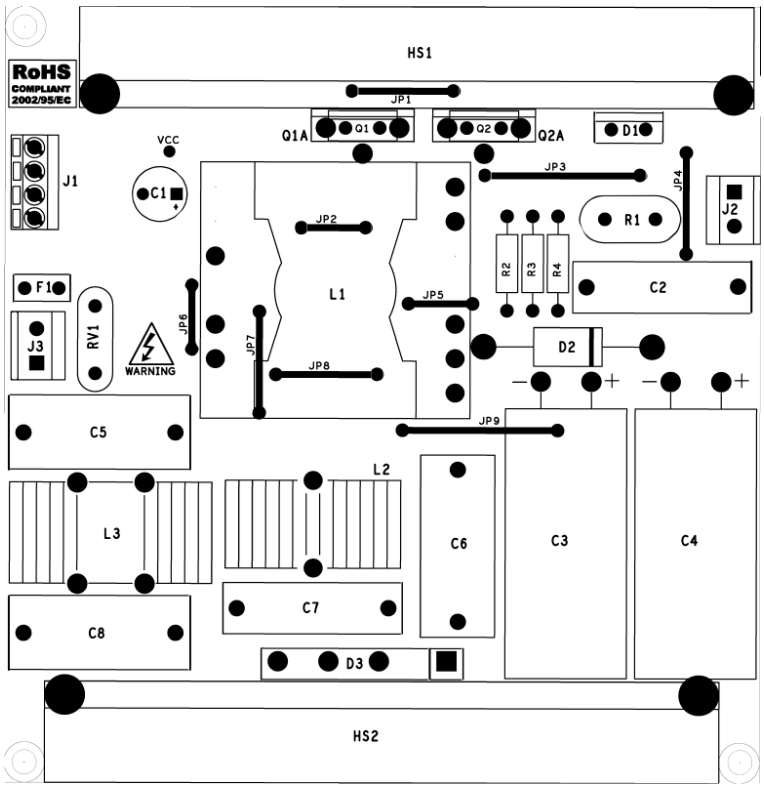
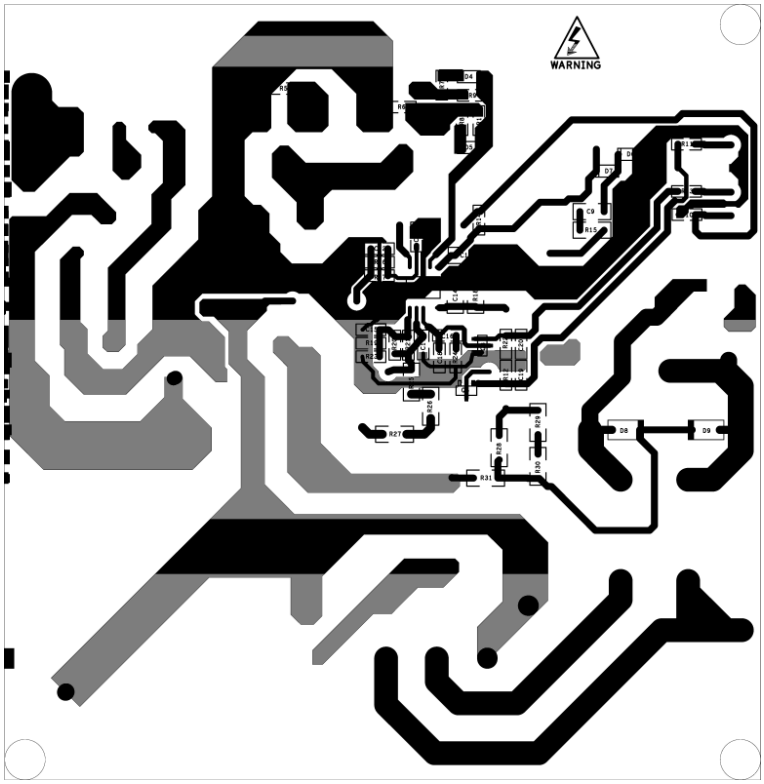


Figure 6. **EVL4986-350W PCB layout (bottom side)**



2 Test results and main waveforms

The following sections show the main results of the EVL4986-350W evaluation board in terms of performances and waveforms at nominal input voltages and/or various load conditions.

2.1 Line and load regulation

The desired output voltage (V_{OUT} = 400V), is set through the partitioning resistors connected between the output voltage V_{OUT} and the FB pin (#7):

$$V_{OUT} = V_{REF}\left(1 + \frac{R_{FB\_H}}{R_{FB\_L1} + R_{FB\_L2}}\right) \quad (1)$$

Where V_{REF} is the internal reference voltage (2.5V typ.), R_{FB_L1} = R19//R23, R_{FB_L2} = R20//R21, R_{FB_H} = R25 + R26 + R27.

Considering R_{FB_H} = 3x2.2 MΩ = 6.6 MΩ, to limit the power dissipation of the whole resistor divider to 25 mW, the output voltage can be set by the R_{FB_L} (R_{FB_L1} + R_{FB_L2}) resistor:

$$R_{FB\_L} = R_{FB\_L1} + R_{FB\_L2} = R_{FB\_H}\frac{V_{REF}}{V_{OUT} - V_{REF}} = 6600k\Omega\,\frac{2.5V}{400V - 2.5V} = 41.5\ k\Omega \quad (2)$$

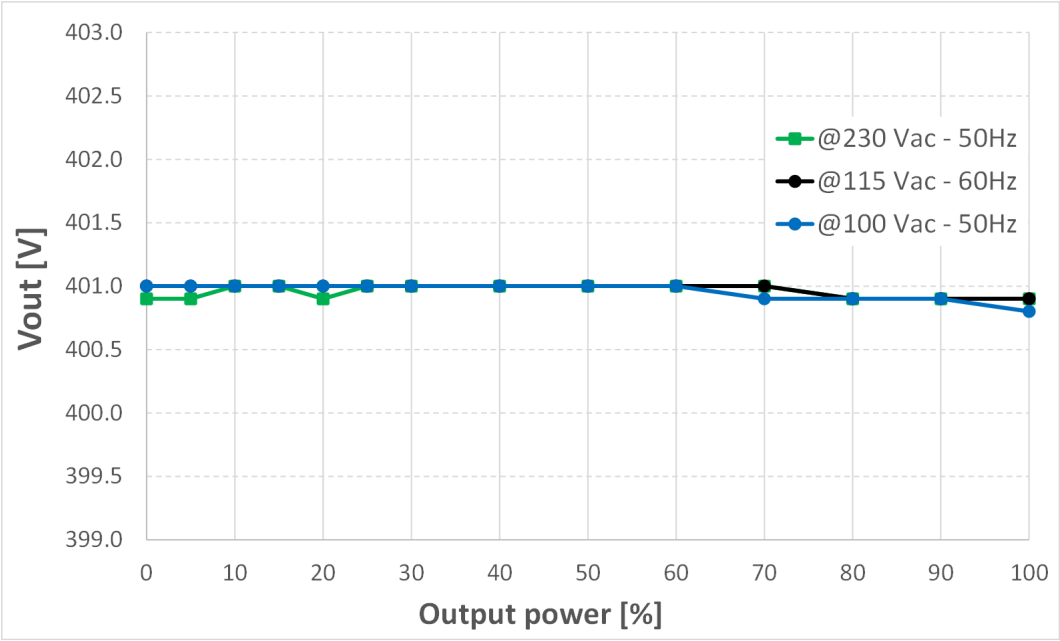
Where the value of resistor R_{FB_L1} is selected as 13.7kΩ according to the desired output power good threshold (V_{OUT_PGOFF}) - see Section 2.16 Power Good signal (PGOOD).

Therefore:

$$R_{FB\_L2} = R_{FB\_L} - R_{FB_{L1}} = 41.5\ k\Omega - 13.7\ k\Omega = 27.8\ k\Omega \quad (3)$$

Figure 7 shows the average output voltage, measured across the J2 connector, versus the output power for the nominal input voltages. The results confirm that the output voltage is well regulated, regardless of the input and output load conditions.

Figure 7. Output voltage versus AC line and output load



2.2 Power Factor and Total Harmonic Distortion

Figure 8 and Figure 9 show the total harmonic distortion of the input current (THD) and the power factor (PF) versus the nominal input voltages at different load conditions. The results confirm that the new control integrated in the L4986 device is able to achieve very low THD in all operating conditions.

Figure 8. **Total Harmonic Distortion (THD) versus output load**

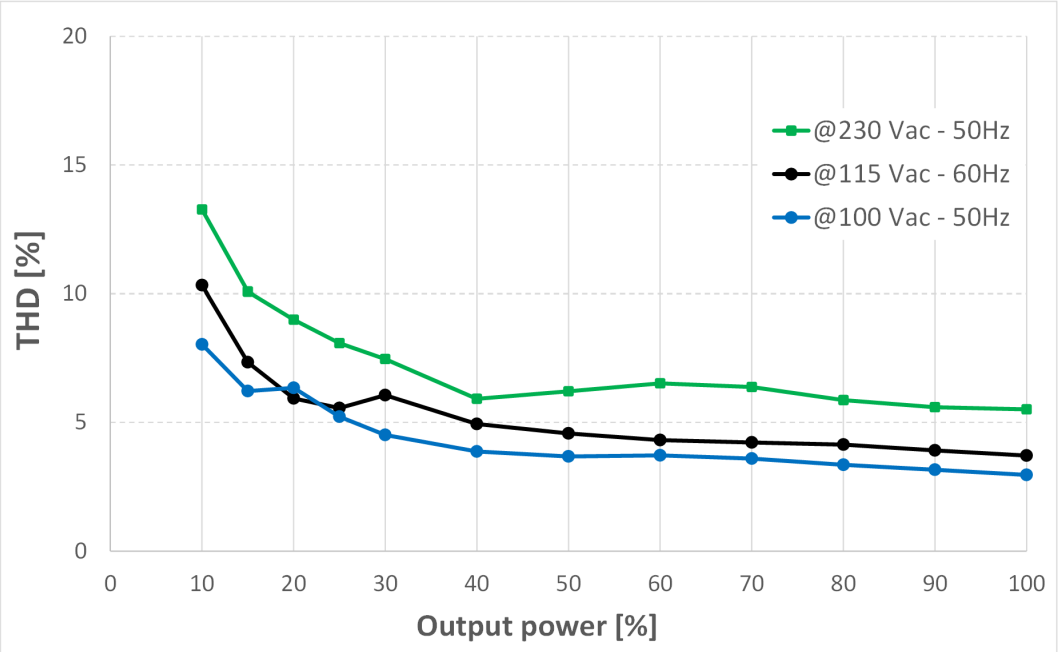
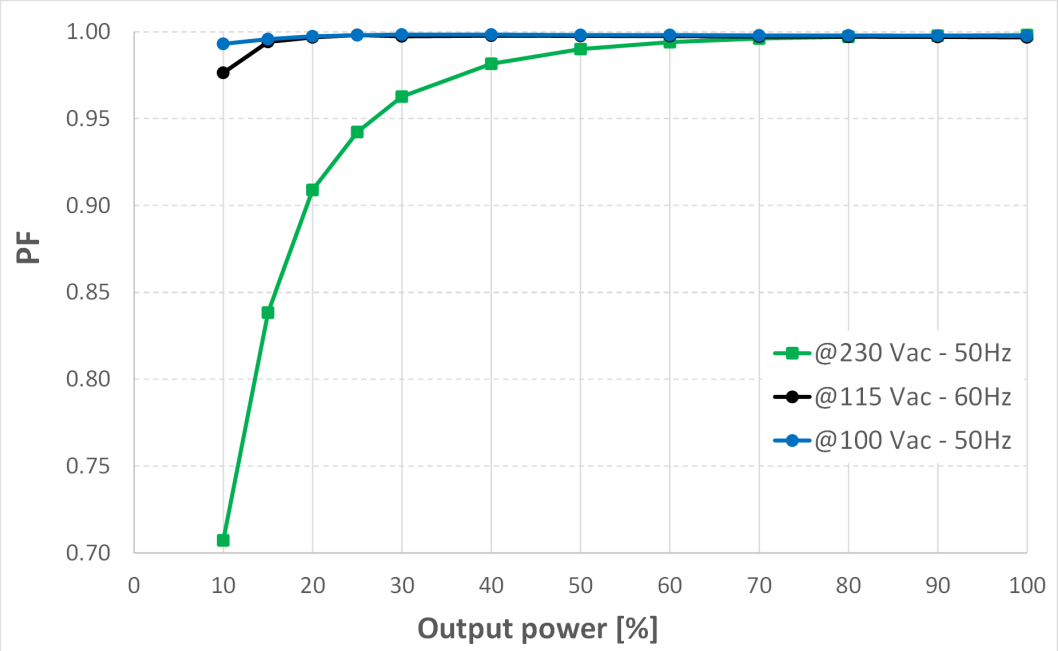


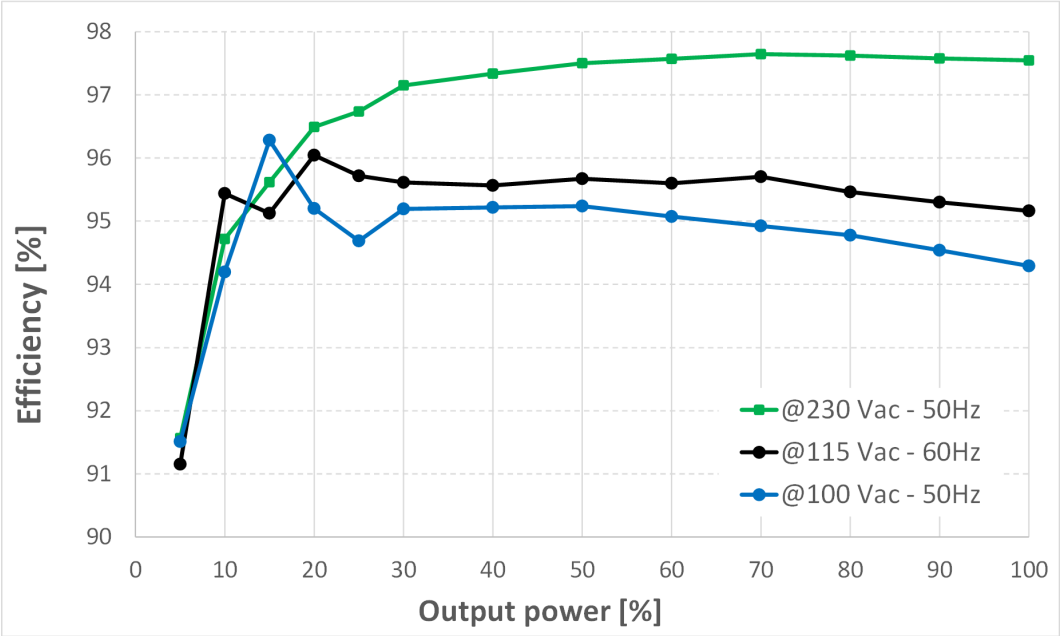
Figure 9. **Power Factor (PF) versus output load**



2.3 Converter efficiency

Figure 10 shows the efficiency of the converter at the nominal input voltages versus the output power. At full load, the converter's efficiency is about 94.3% at 100 Vac and 97.5% at 230 Vac.

Figure 10. **Converter efficiency**



Note: The self-supply consisting of auxiliary inductor windings (#9, #11) and by R15, C9, D6, D7 is not designed to support no-load condition.

To measure the input power consumption in no-load condition ($P_{IN\_NO\ LOAD}$), supply the L4986 device with an external power supply (e.g., 16V) using the dedicated VCC input connector.

The following figures show the converter efficiency according to ES-2 test conditions.

Figure 11. **Converter "spot" efficiency**

according to ES-2 test conditions

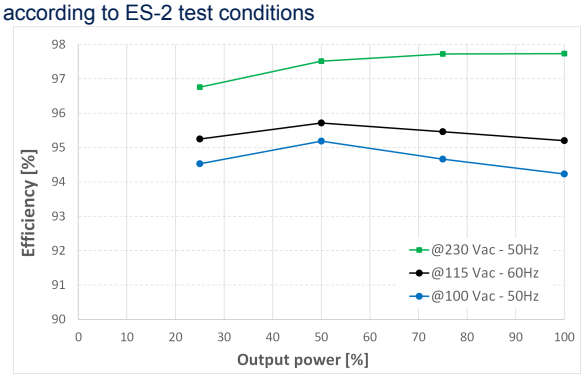
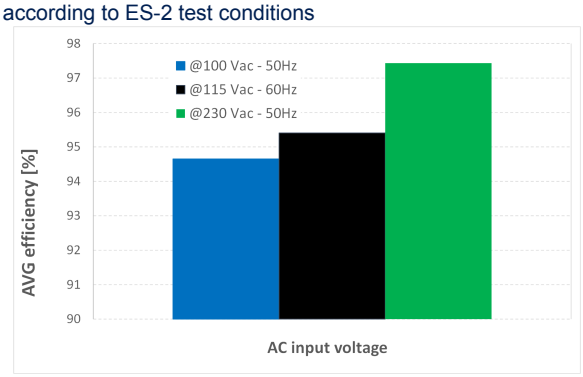


Figure 12. **Converter "average" efficiency**

according to ES-2 test conditions



2.4 Harmonics content

One of the main purposes of a PFC pre-regulator is the correction of input current distortion to ensure harmonics content remains within the limits of the relevant regulations.

This evaluation board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI class-D, at both the nominal input voltage mains, as shown in the following figures.

Figure 13. Harmonics content at full load (100 AC – 50 Hz)

Pout = 350 W

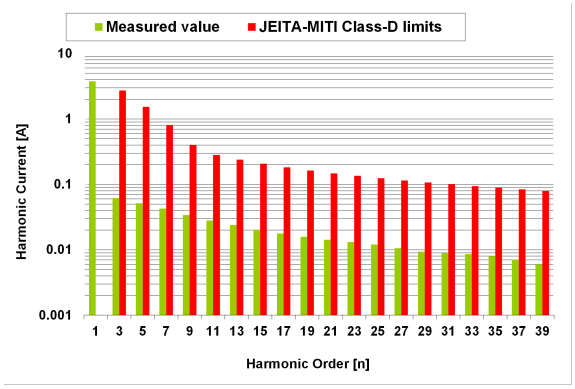
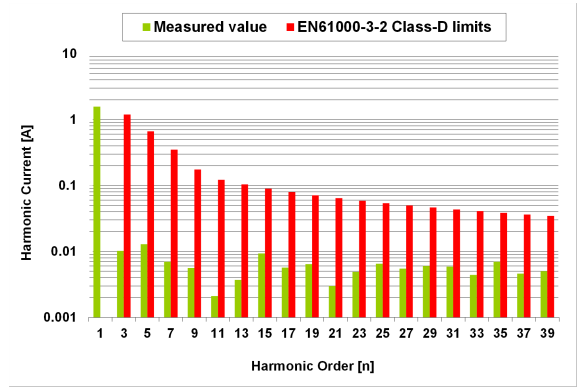


Figure 14. Harmonics content at full load (230 AC – 50 Hz)

Pout = 350 W



The converter was also tested at 20% of the full load to highlight the performance in all operating conditions.

Figure 15. Harmonics content at 20% load (100 AC – 50 Hz)

Pout = 70 W

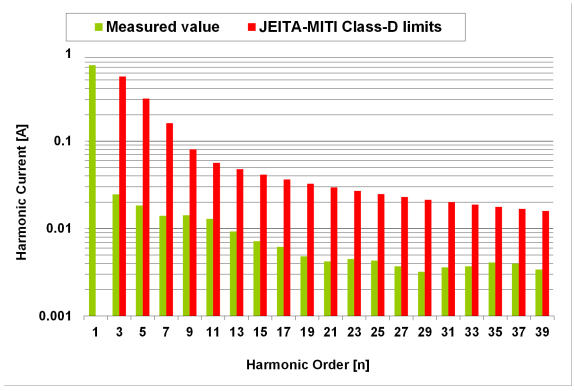
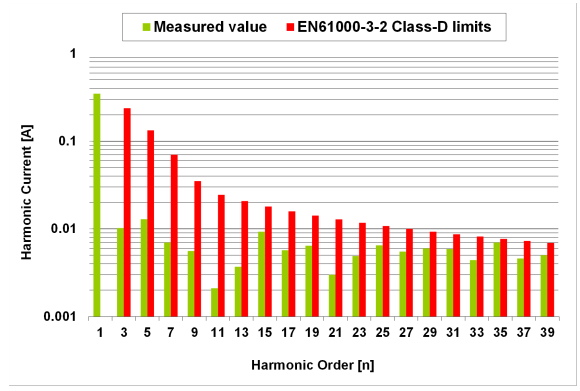


Figure 16. Harmonics content at 20% load (230 AC – 50 Hz)

Pout = 70 W



2.5 Start-up

Figure 17 and Figure 18 show the main voltage waveforms during the converter power-up.

As soon as the HV pin voltage (which is proportional to the rectified AC line voltage through D8 and D9 diodes) is higher than the start-up threshold (V_{start} = 29 V typ.), the internal high voltage current generator (I_{HV_ON} = 7 mA typ.) charges the VCC capacitor (C_1 = 100 µF) up to the IC turn-on threshold (V_{CC_ON}=14V typ). The resulting VCC rise time ($T_R = C_1.V_{CC\_ON}/I_{HV\_ON}$) is about 200 ms, as highlighted in the figures below.

Figure 17. Start-up voltage waveforms (115Vac)

CH1=HV pin#10, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2

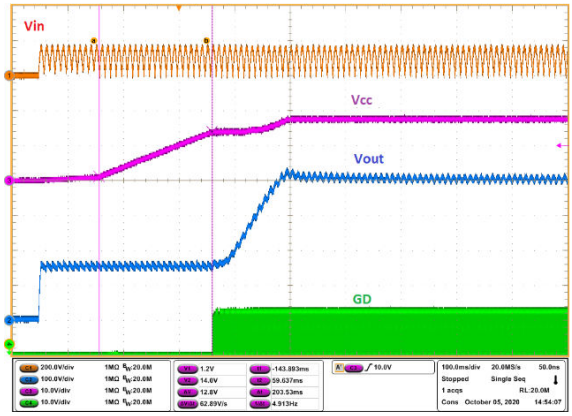
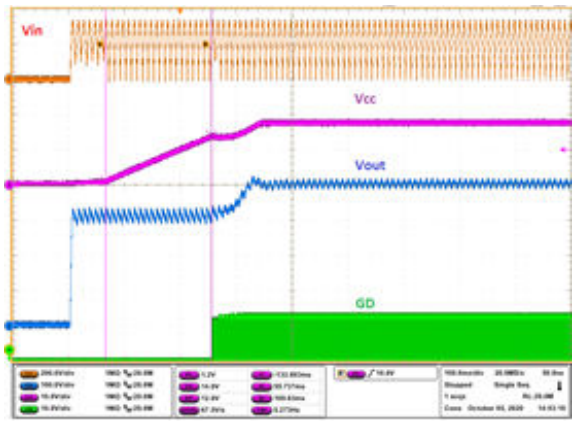


Figure 18. Start-up voltage waveforms (230Vac)

CH1=HV pin#10, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2



Once the VCC pin voltage reaches the V_{CC_ON} threshold, the device checks that the AC input voltage is higher than the brown-in threshold (V_{HV_PKBI}=115V typ.) and then starts the soft start, as shown in Figure 19 to Figure 22 (which highlight the inductor current and current sense waveforms for different load conditions).

Figure 19. Start-up at full load (115Vac)

CH1=HV pin#10, CH2=CS pin#4, CH3=IL, CH4=Vout

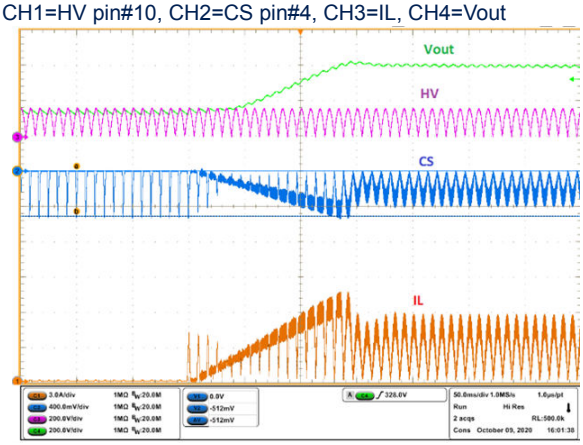


Figure 20. Start-up at full load (230Vac)

CH1=HV pin#10, CH2=CS pin#4, CH3=IL, CH4=Vout

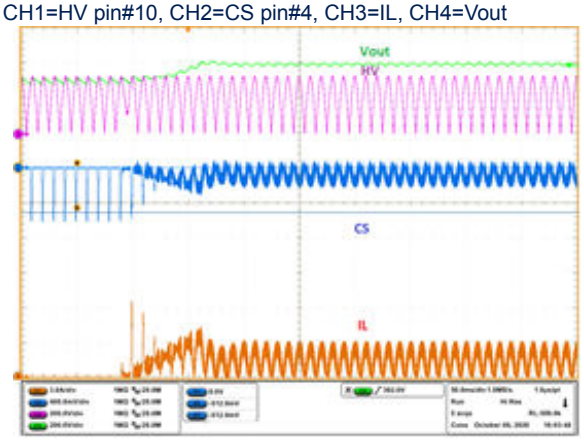


Figure 21. Start-up at light load (115Vac)

CH1=HV pin#10, CH2=CS pin#4, CH3=IL, CH4=Vout

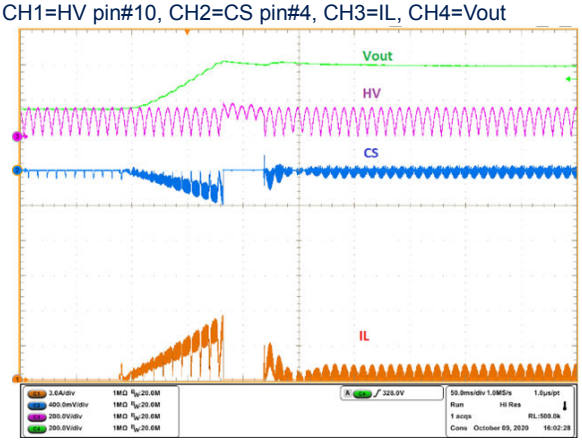
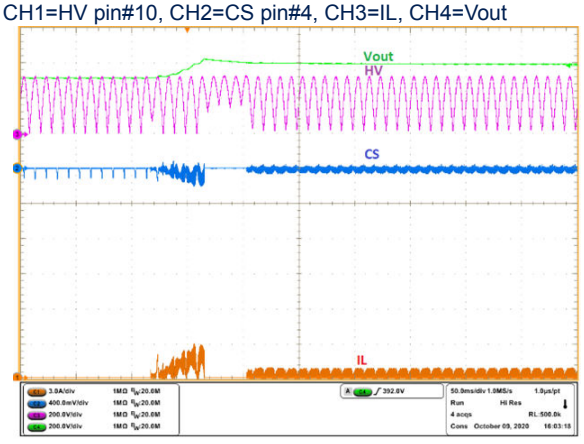


Figure 22. Start-up at light load (230Vac)

CH1=HV pin#10, CH2=CS pin#4, CH3=IL, CH4=Vout



Note: If the AC input voltage is below the brown-in threshold when the VCC voltage reaches the turn-on threshold (V_{CC_ON}), the controller does not start up. In this case, a recycle of the VCC voltage between the turn-off threshold (V_{CC_OFF}) and turn-off threshold (V_{CC_ON}) is required to start up the converter.

2.6 Steady-state operation

The following sections provide the main waveforms of the converter in steady-state operation.

2.6.1 Input Current

Figure 23 to Figure 28 show the input current waveforms of the converter for different input and output load conditions. The waveforms confirm that the new patented control integrated in the controller [1] is able to achieve sinusoidal input current (extremely low THD), regardless of the operating conditions (input or output load).

Figure 23. Steady-state – input current at full load (115Vac)

CH1=Iin, CH2=Vin

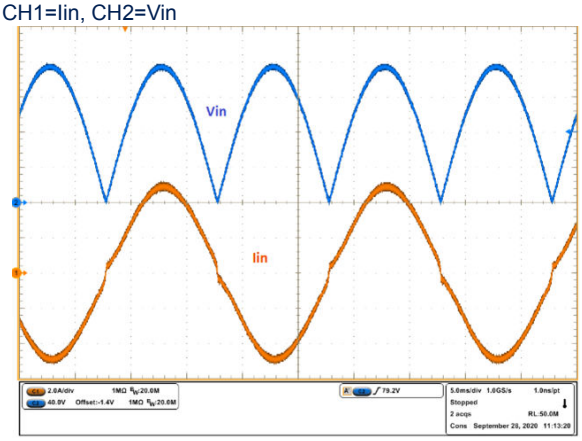


Figure 24. Steady-state – input current at full load (230Vac)

CH1=Iin, CH2=Vin

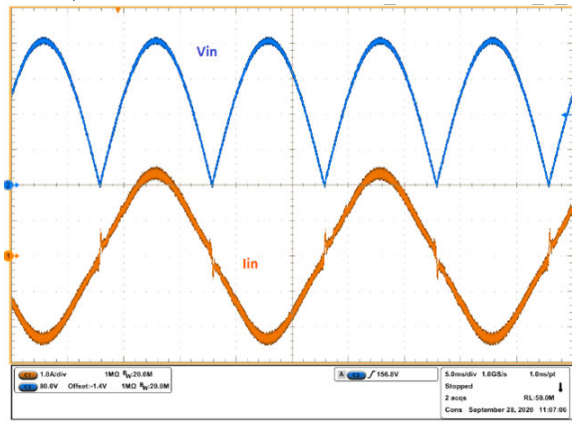


Figure 25. Steady-state - input current at 50% load (115Vac)

CH1=Iin, CH2=Vin

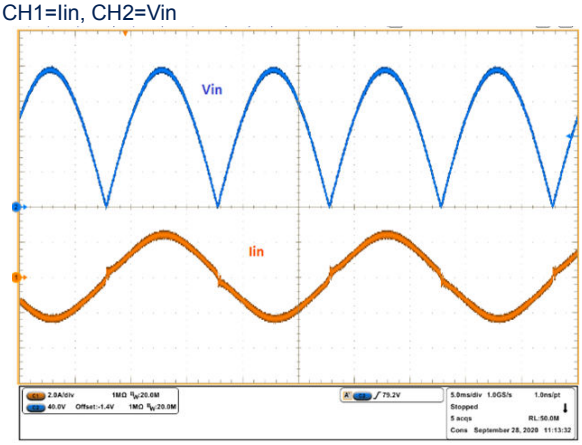


Figure 26. Steady-state - input current at 50% load (230Vac)

CH1=Iin, CH2=Vin

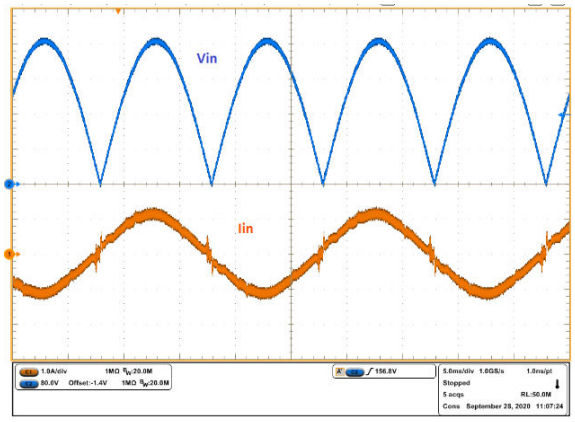


Figure 27. Steady-state - input current at 20% load (115Vac)

CH1=Iin, CH2=Vin

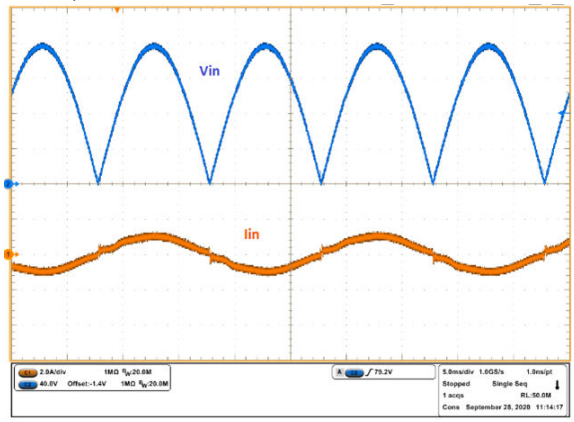
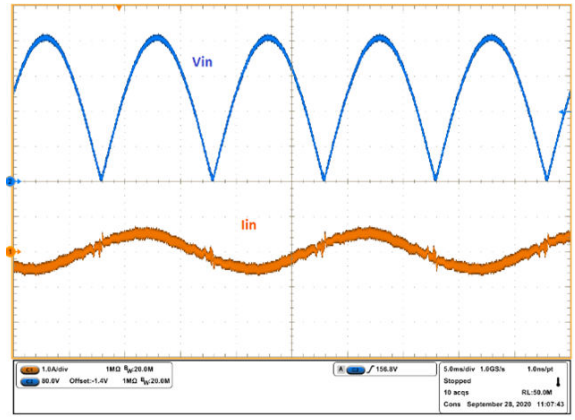


Figure 28. Steady-state - input current at 20% load (230Vac)

CH1=Iin, CH2=Vin



2.6.2 Switching frequency

The following figures show the waveforms of the boost inductor current (L1) for different input/output load conditions and the switching frequency on the peak and near zero-crossing of the sinusoid.

The waveforms confirm that the new off-time generator [2] integrated in the controller is able to achieve near fixed switching frequency, regardless of the operating conditions (input or output load).

Figure 29. Steady-state - Switching frequency at full load (115Vac)

CH1=IL, CH2=Vdrain, CH3=Vin, CH4=GD pin#2

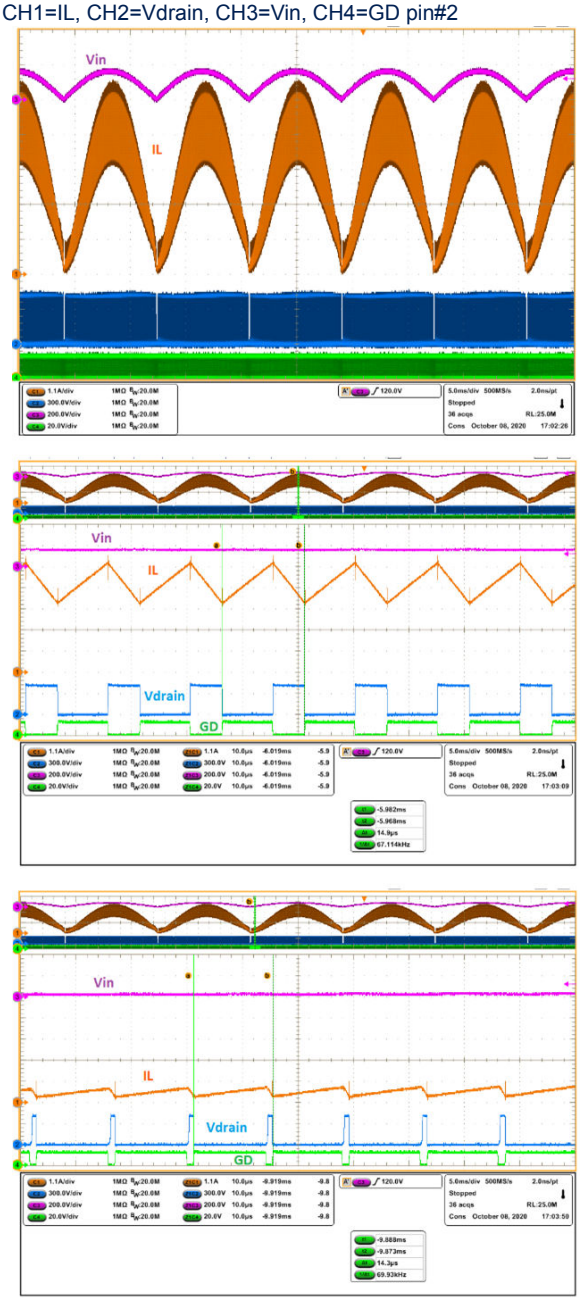


Figure 30. Steady-state - Switching frequency at full load (230Vac)

CH1=IL, CH2=Vdrain, CH3=Vin, CH4=GD pin#2

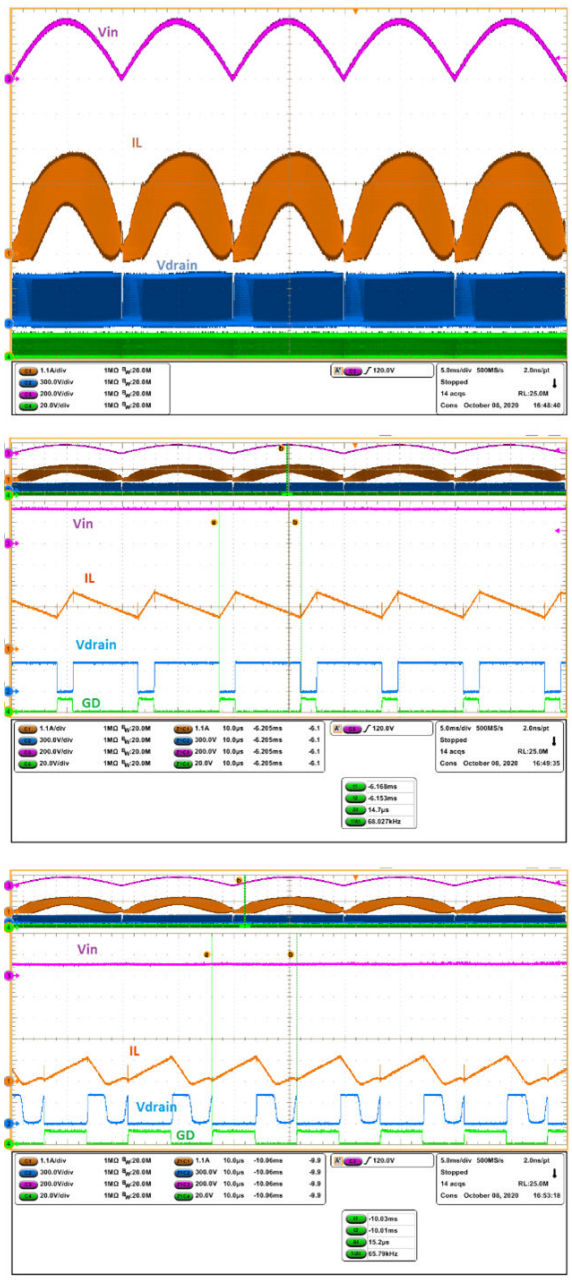


Figure 31. Steady-state - Switching frequency at 10% load (115Vac)

CH1=IL, CH2=Vdrain, CH3=Vin, CH4=GD pin#2

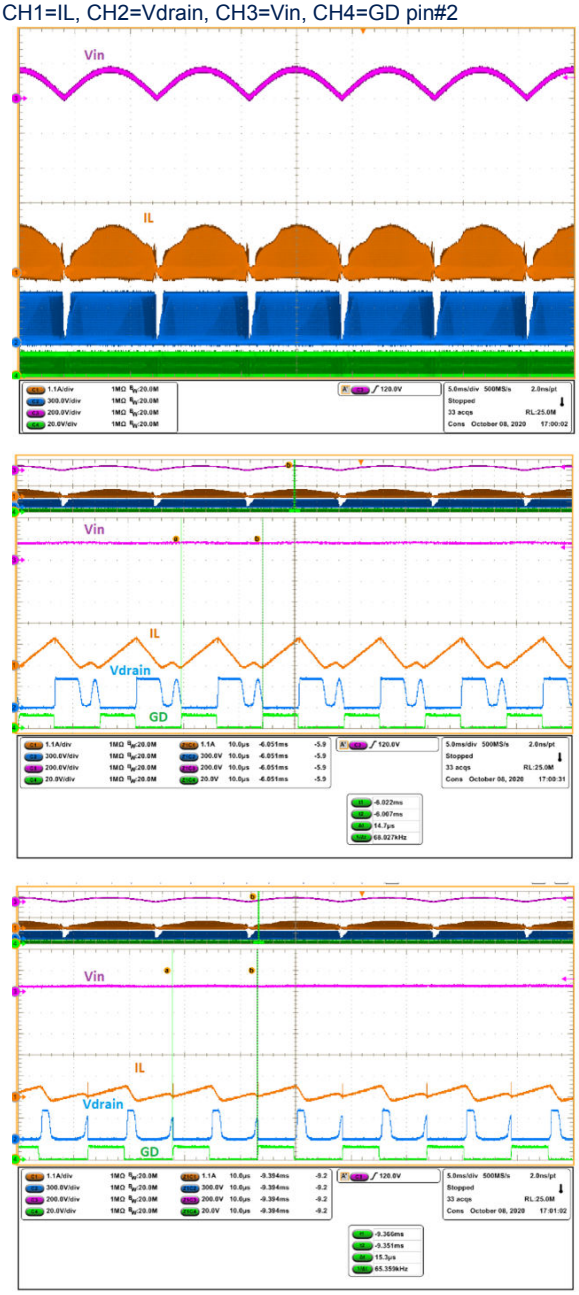
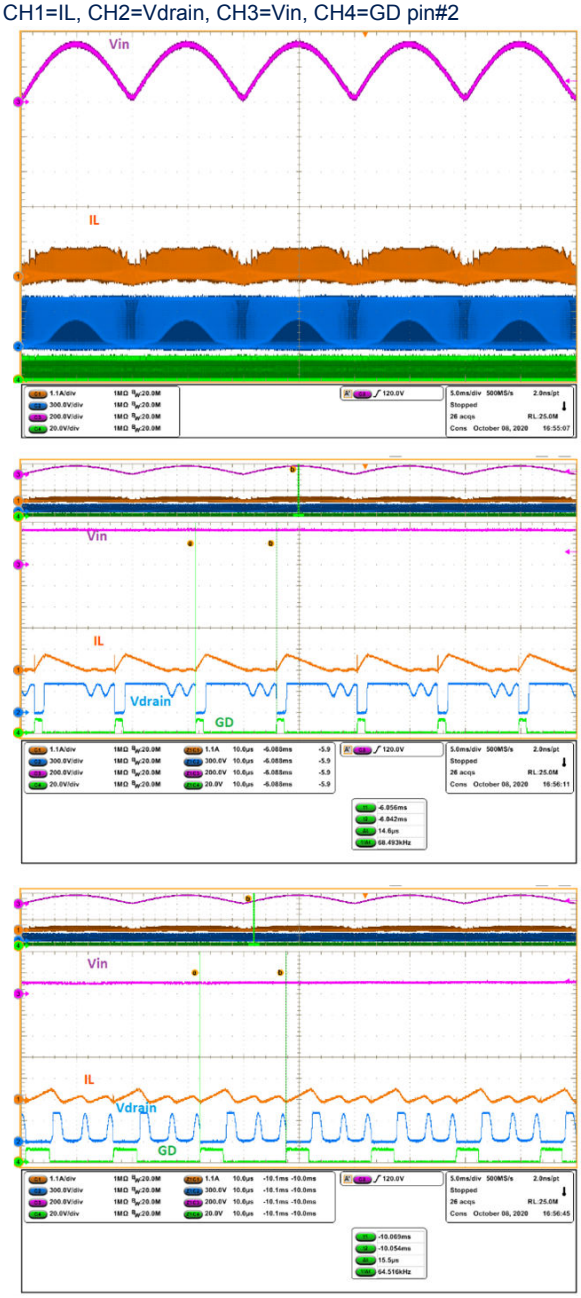


Figure 32. Steady-state - Switching frequency at 10% load (230Vac)

CH1=IL, CH2=Vdrain, CH3=Vin, CH4=GD pin#2



2.7 Load variation

Figure 33 to Figure 36 show the output voltage variation due to a load change.

Figure 33. Load variation - From 100% to 0% load (115Vac)

CH1=Iin, CH2=Vout, CH3=COMP pin#8, CH4=GD pin#2

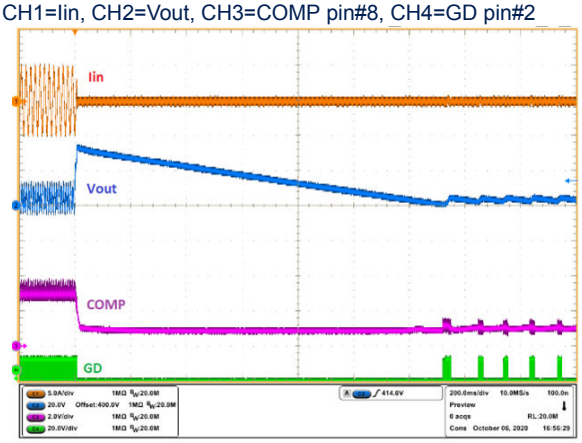


Figure 34. Load variation - From 100% to 0% load (230Vac)

CH1=Iin, CH2=Vout, CH3=COMP pin#8, CH4=GD pin#2

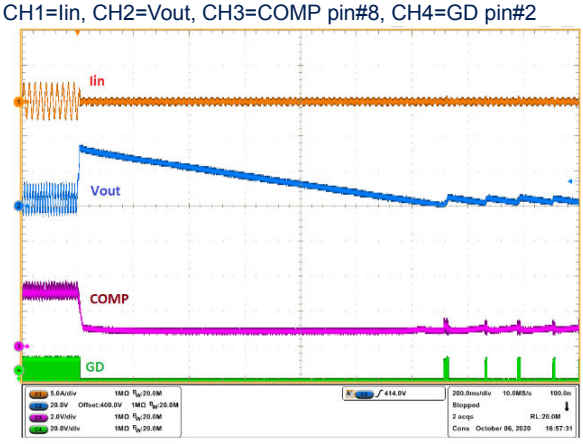


Figure 35. Load variation - From 10% to 100% load (115Vac)

CH1=Iin, CH2=Vout, CH3=COMP pin#8, CH4=GD pin#2

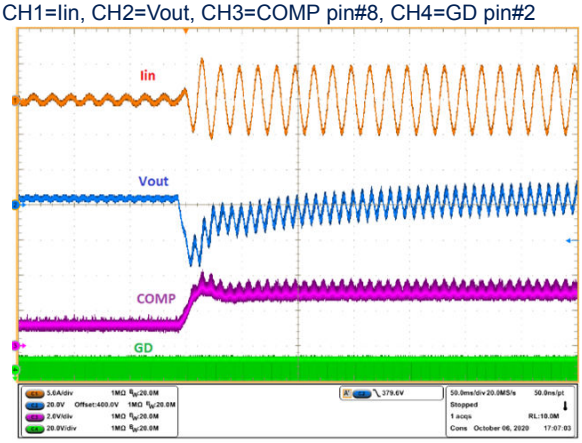
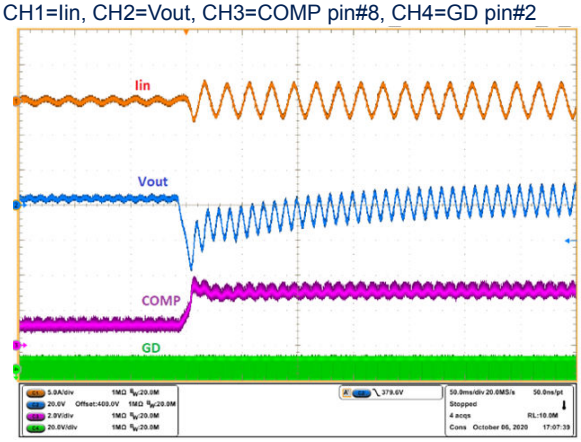


Figure 36. Load variation - From 10% to 100% load (230Vac)

CH1=Iin, CH2=Vout, CH3=COMP pin#8, CH4=GD pin#2



2.8 Light load - burst mode operation

At light-load conditions, the converter maintains output voltage regulation by implementing burst-mode operation (the device enters burst mode once the COMP pin is below the threshold V_{COMP_S} = 1.0V typ), as shown in the following figures.

Figure 37. Light load operation (115Vac)

CH1=COMP pin#8, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2

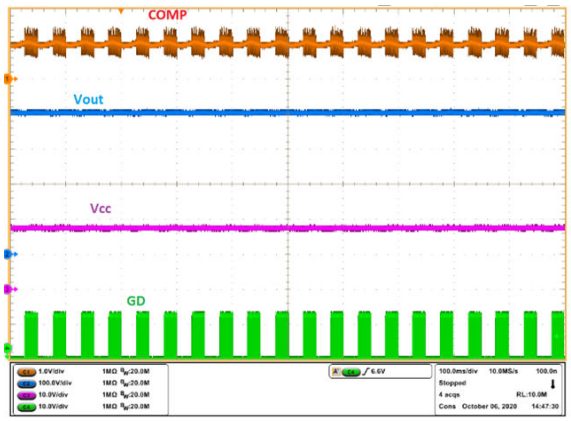
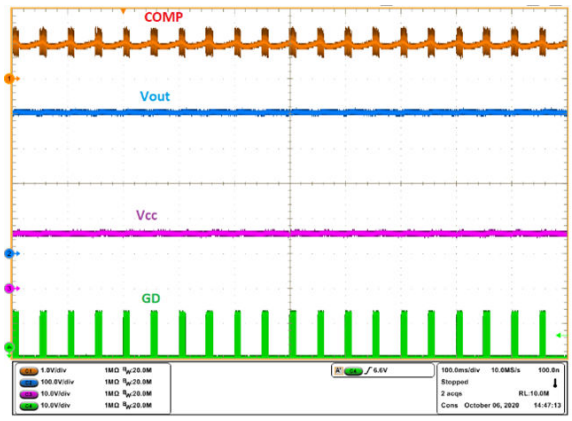


Figure 38. Light load operation (230Vac)

CH1=COMP pin#8, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2

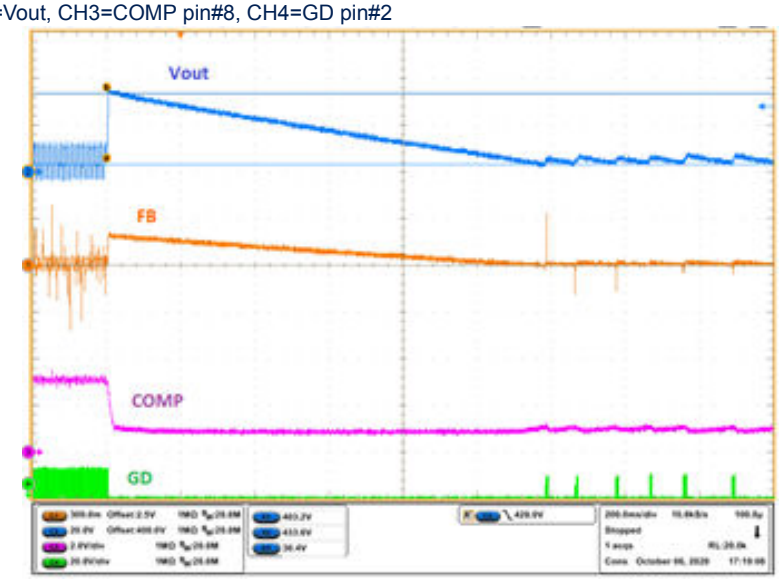


2.9 Overvoltage protection (OVP)

If the output voltage monitored through the FB pin rises higher than 107% of the regulated voltage, the controller turns off the power MOSFET (GD=0) until the voltage is close to the desired value (102% of the target value), as shown in the figure below.

Figure 39. Overvoltage protection (OVP)

CH1=FB pin#7, CH2=Vout, CH3=COMP pin#8, CH4=GD pin#2



2.10 XCAP discharge

Figure 40 to Figure 43 show converter power off, where the XCAP capacitors (C5 = 0.47 µF, C8 = 1 µF) are discharged by the internal high voltage current generator (I_{HV_DIS} = 5mA min.) after the detection time (T_{DETEC_XCAP} = 64 ms typ.).

Figure 40. XCAP discharge - detection time (115Vac)

CH1=Vac, CH2=HV pin#10, CH3=VCC pin#1, CH4=GD pin#2

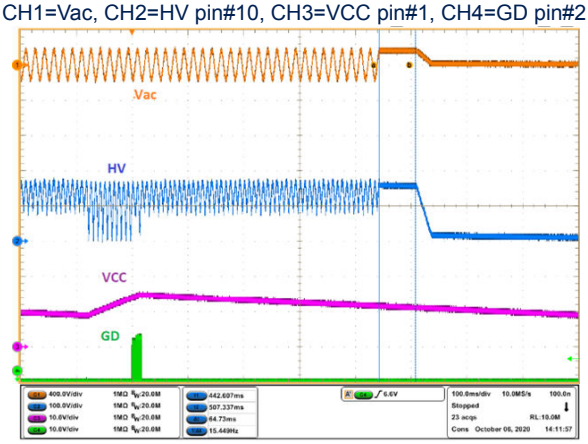


Figure 41. XCAP discharge - detection time (230Vac)

CH1=Vac, CH2=HV pin#10, CH3=VCC pin#1, CH4=GD pin#2

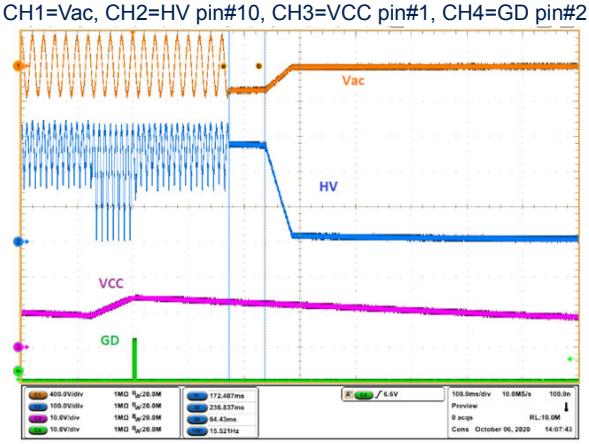


Figure 42. XCAP discharge - discharge time (115Vac)

CH1=Vac, CH2=HV pin#10, CH3=VCC pin#1, CH4=GD pin#2

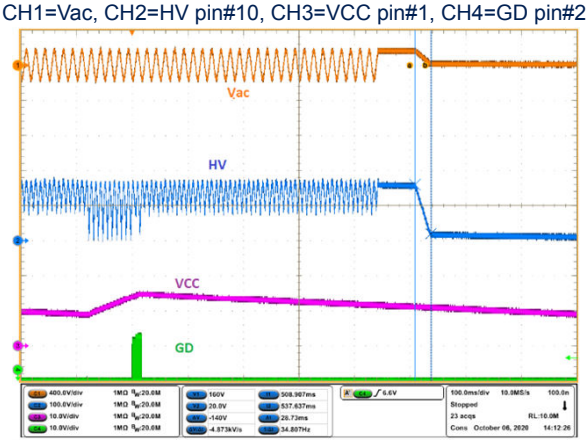
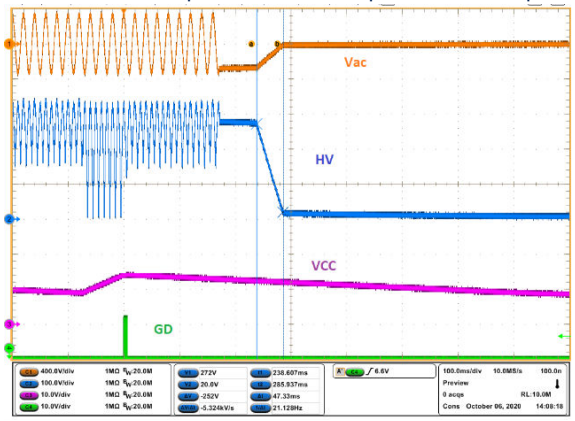


Figure 43. XCAP discharge - discharge time (230Vac)

CH1=Vac, CH2=HV pin#10, CH3=VCC pin#1, CH4=GD pin#2



Note: A DC input voltage is not allowed.

2.11 Mains dip

The evaluation board was also tested for the mains voltage dip at full load, as shown in the following figures (which also highlight the PG_OUT behavior).

Figure 44. Mains dip 0% - 1 cycle (115Vac)

CH1=PG_OUT pin#5, CH2=Vout, CH3=Vac, CH4=GD pin#2

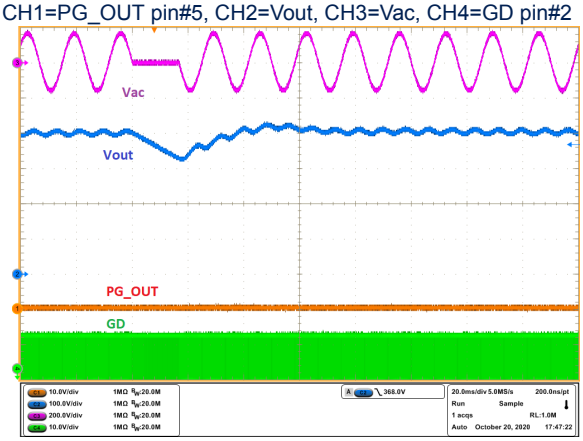


Figure 45. Mains dip 0% - 1 cycle (230Vac)

CH1=PG_OUT pin#5, CH2=Vout, CH3=Vac, CH4=GD pin#2

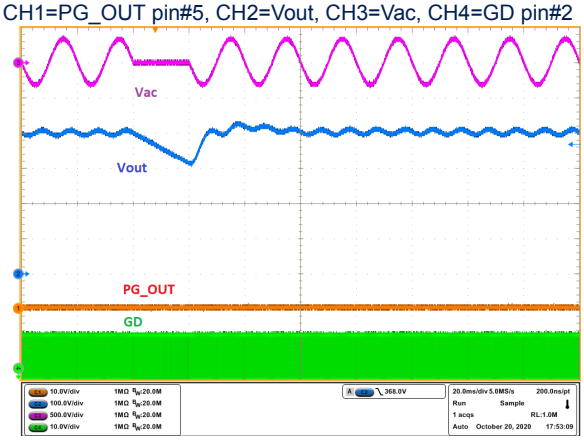


Figure 46. Mains dip 40% - 10 cycles (115Vac)

CH1=PG_OUT pin#5, CH2=Vout, CH3= Vac, CH4=GD pin#2

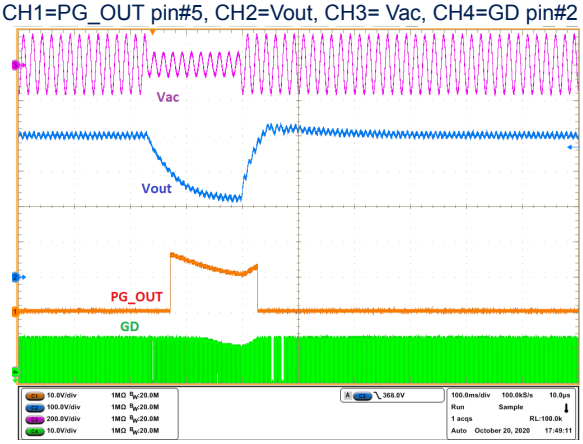


Figure 47. Mains dip 40% - 10 cycles (230Vac)

CH1=PG_OUT pin#5, CH2=Vout, CH3= Vac, CH4=GD pin#2

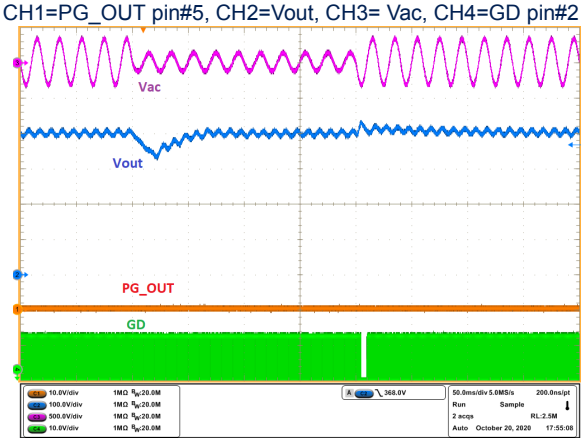


Figure 48. Mains dip 70% - 25 cycle (115Vac)

CH1=PG_OUT pin#5, CH2=Vout, CH3=Vac, CH4=GD pin#2

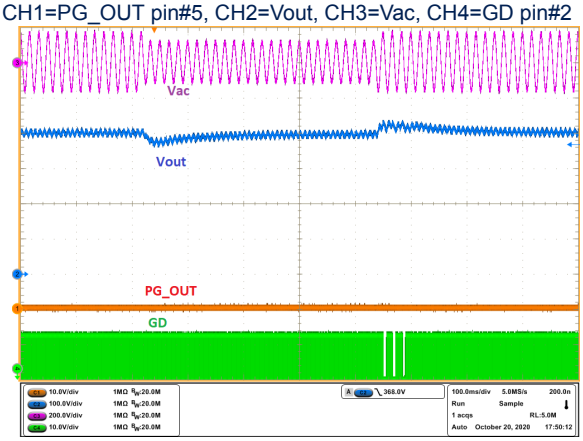
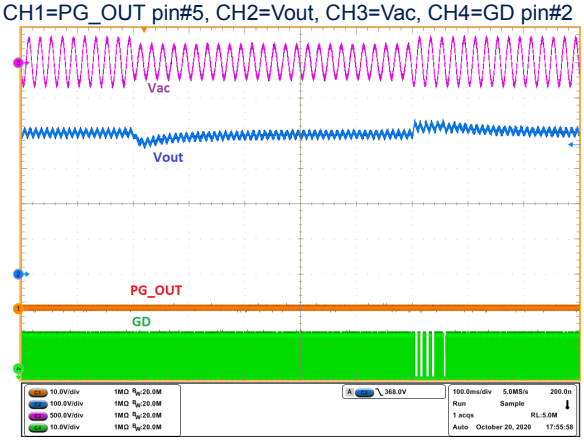


Figure 49. Mains dip 70% - 25 cycle (230Vac)

CH1=PG_OUT pin#5, CH2=Vout, CH3=Vac, CH4=GD pin#2

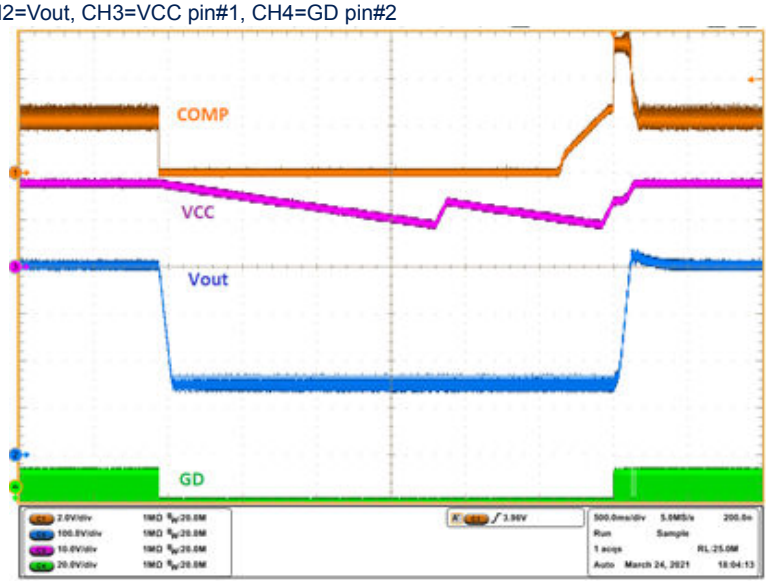


2.12 Disable

The device can be disabled by forcing the COMP pin below the threshold V_{COMP_DIS} (0.7 V typ.) and it restarts once the COMP pin is released and VCC voltage reaches the V_{CC_ON} threshold (14.0 V typ.), as shown in the figure below.

Figure 50. Disable

CH1=COMP pin#8, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2

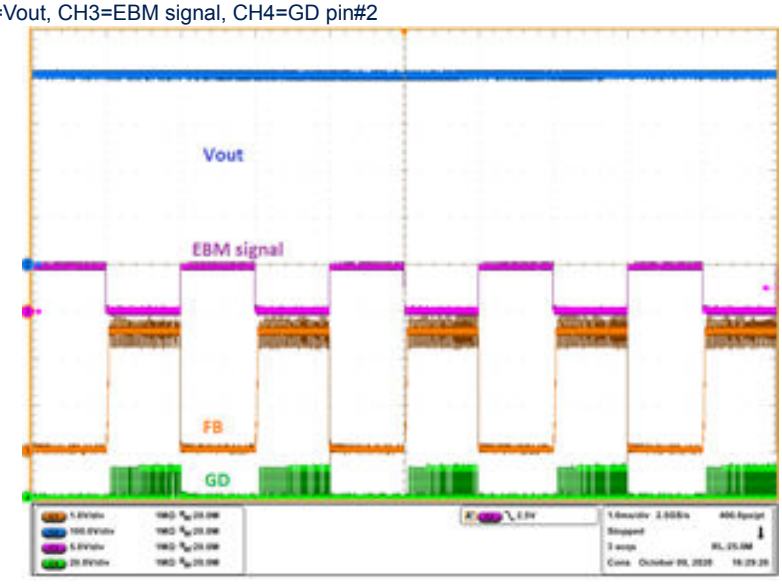


2.13 External burst mode (EBM)

Forcing the FB pin below the $V_{FB\_FF/EBM}$ threshold (0.5V typ), the device immediately stops operation, reduces its power consumption, and forces the COMP pin into “high-impedance”. As soon as the FB pin is released, the device restarts operation (without implementing soft start).

Figure 51. External burst mode

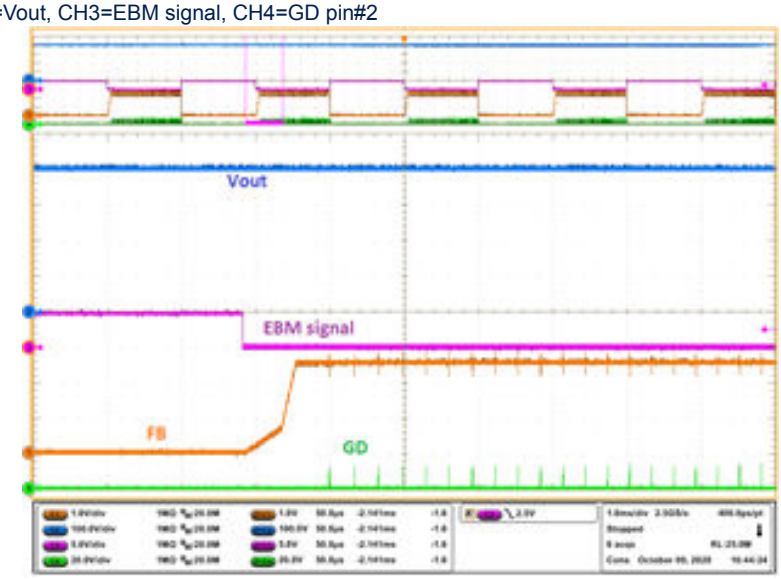
CH1=FB pin#7, CH2=Vout, CH3=EBM signal, CH4=GD pin#2



As soon as the device enters the EBM state, a weak pullup current I_{FB_EBM} (100 µA typ.) is sourced from the FB pin in order to speed up the FB voltage rising edge when the external pull down is released. In addition, once the FB voltage exceeds $V_{FB\_FF/EBM}$ + 50 mV, the I_{FB_EBM} current of 100 µA is increased to 1 mA, until the FB pin voltage reaches the final target of 2.5 V (internal V_{REF}), as shown in the figure below.

Figure 52. External burst mode - exit

CH1=FB pin#7, CH2=Vout, CH3=EBM signal, CH4=GD pin#2



2.14 Output overload

Figure 53 and Figure 54 show the main waveforms in the event of an output overload during normal operation. The input power is limited by the overcurrent protection (OCP), which turns off the power switch as soon as the CS rises above the V_{CS_OCP1} threshold (-0.49 V typ.).

Figure 53. Output overload (a)

CH1=COMP pin#8, CH2=Vout, CH3=CS pin#4, CH4=GD pin#2

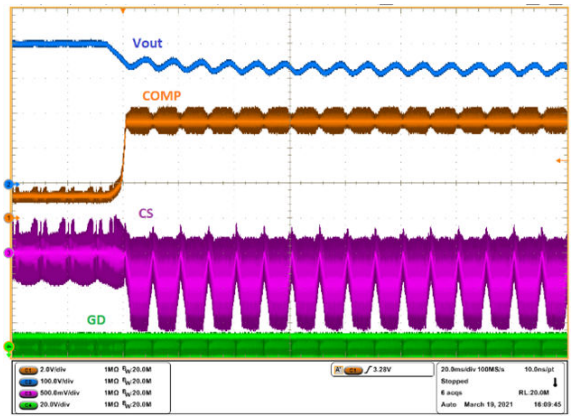
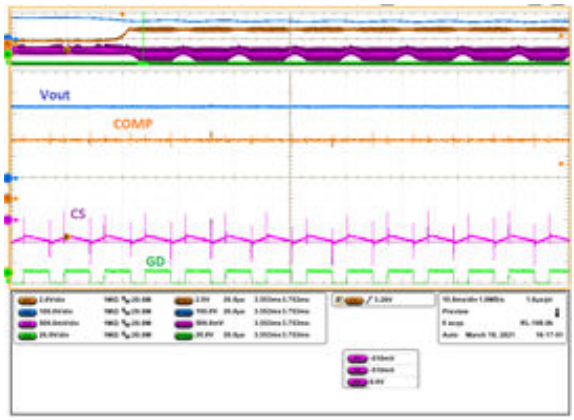


Figure 54. Output overload (b)

CH1=COMP pin#8, CH2=Vout, CH3=CS pin#4, CH4=GD pin#2



2.15 Line variation

The following figures show the main converter waveforms after a variation of the line input voltage at full load and light load.

Figure 55. Line variation – "Low line" and full load (90Vac to 140Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

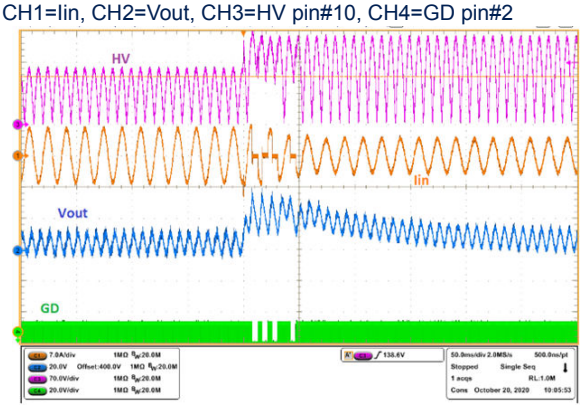


Figure 56. Line variation – "Low line" and full load (140Vac to 90Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

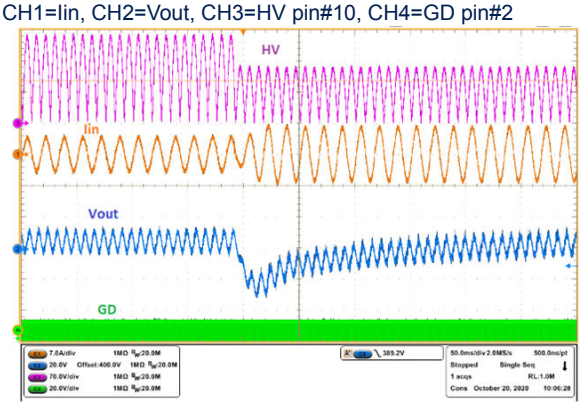


Figure 57. Line variation – "Low line" and 10% load (90Vac to 140Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

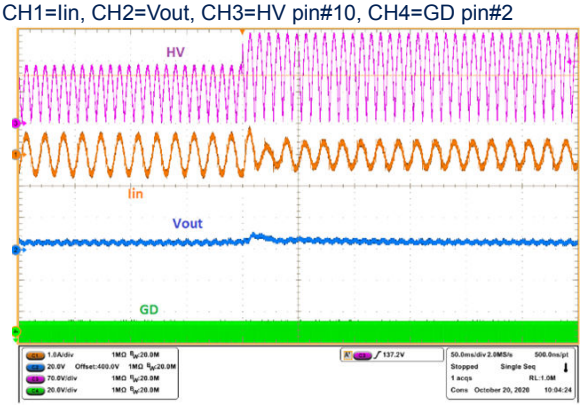


Figure 58. Line variation – "Low line" and 10% load (140Vac to 90Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

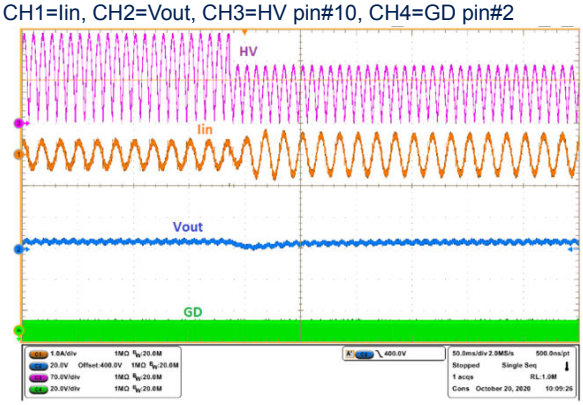


Figure 59. Line variation – "High-line" and full load (175Vac to 265Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

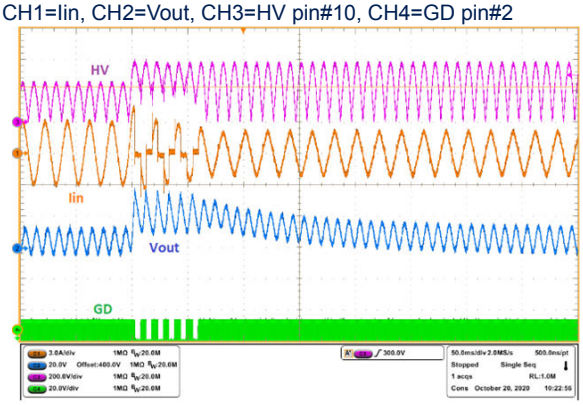


Figure 60. Line variation – "High-line" and full load (265Vac to 175Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

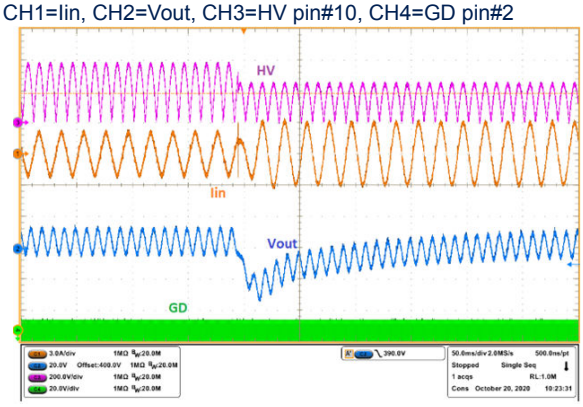


Figure 61. Line variation – "High-line" and 10% load (175Vac to 265Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

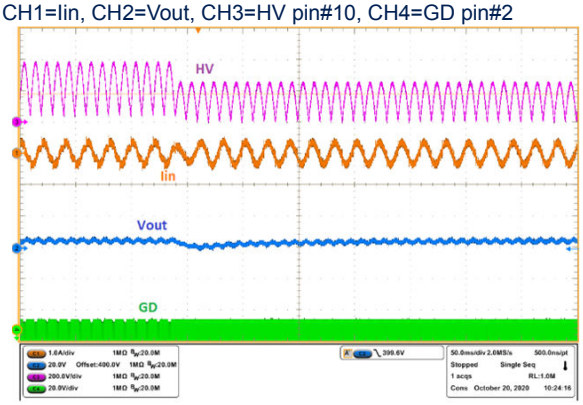
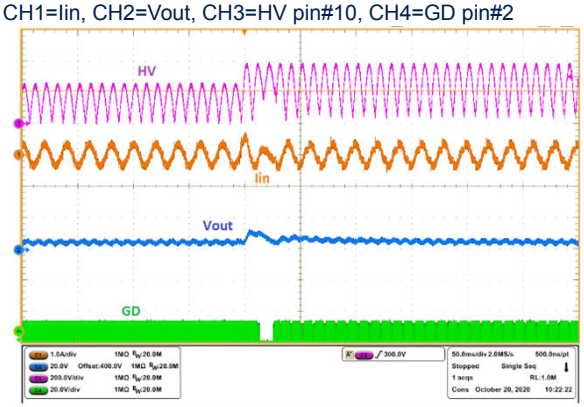


Figure 62. Line variation – "High-line" and 10% load (265Vac to 175Vac)

CH1=Iin, CH2=Vout, CH3=HV pin#10, CH4=GD pin#2

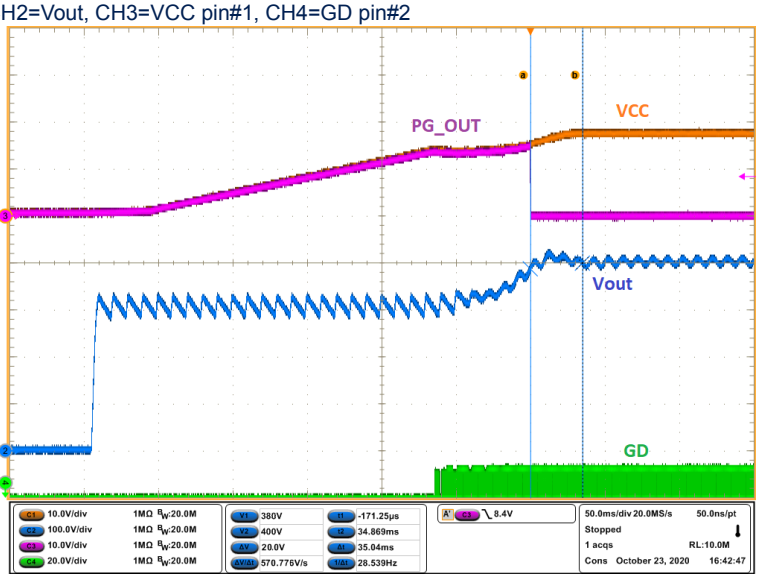


2.16 Power Good signal (PGOOD)

The L4986 provides programmable power good functionality by monitoring the PFC output voltage through the PG_IN pin and driving the PG_OUT pin (open drain pin, active low) accordingly. At start-up, once the output voltage reaches 95% of the programmed value, the PG_OUT pin is pulled-low (which is externally pulled-up to VCC pin through R14 resistor), as shown in the following figure.

Figure 63. Power Good - start-up

CH1=PG_OUT pin#5, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2



The voltage at the PG_IN pin is then:

$$V_{PG\_IN} = V_{OUT} \frac{R_{FB\_L1}}{R_{FB\_H} + R_{FB\_L}} \quad (4)$$

Once the PG_IN pin voltage is lower than the internal threshold V_{PGOOD_OFF} (1.25V typ) ,/the PG_OUT pin is released. As a result, the desired output voltage threshold V_{OUT_PGOFF} (e.g., 300V) can be set by selecting the R_{FB_L1} resistor:

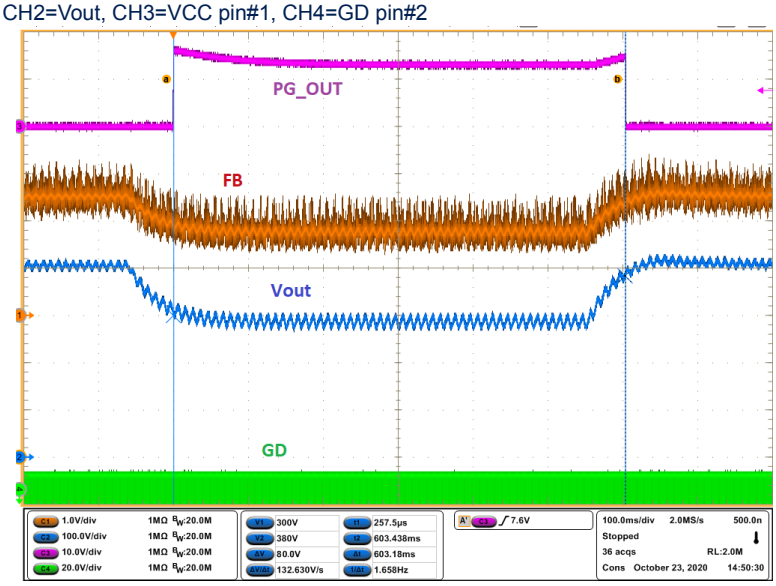
$$R_{FB\_L1} = \frac{V_{PGOOD\_OFF}}{V_{OUT\_PGOFF}}(R_{FB\_H} + R_{FB\_L}) = \frac{2.5V}{300V}(6600k\Omega + 41.5k\Omega) = 27.7k\Omega \quad (5)$$

R_{FB_L2} is therefore:

$$R_{FB\_L2} = R_{FB\_L} - R_{FB_{L1}} = 41.5\ k\Omega - 27.7\ k\Omega = 13.8\ k\Omega \quad (6)$$

Figure 64. Power Good - temporary over current

CH1=PG_OUT pin#5, CH2=Vout, CH3=VCC pin#1, CH4=GD pin#2



3 Thermal measurements

In order to verify design reliability, thermal mapping was performed using an IR camera. Figure 65 to Figure 68 show thermal measurements of the on-board components at nominal input voltages and full load. Some pointers visible on the pictures placed across key components show the relevant temperature.

The ambient temperature during measurements was 25°C.

Figure 65. Thermal measurements at 115Vac - full load (top side)

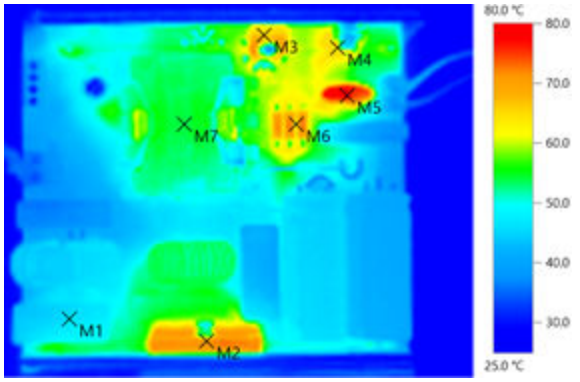


Figure 66. Thermal measurements at 115Vac - full load (bottom side)

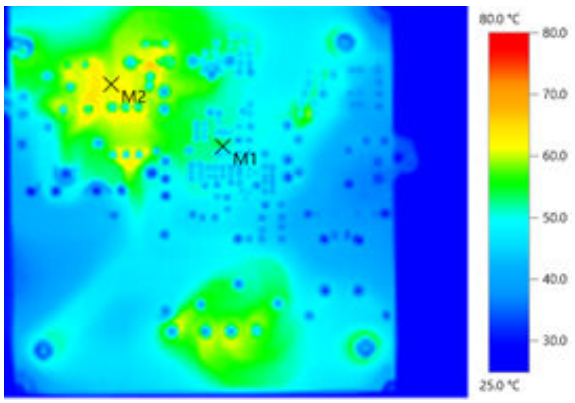


Figure 67. Thermal measurements at 230Vac - full load (top side)

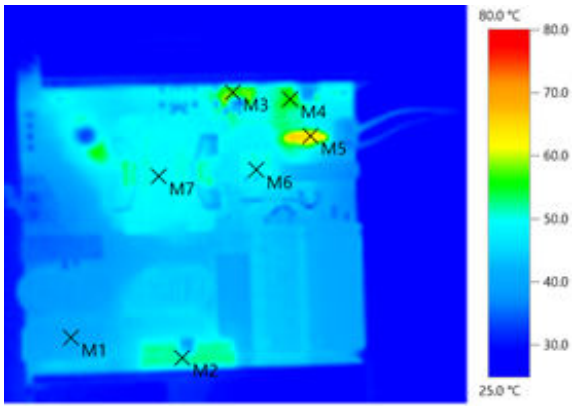


Figure 68. Thermal measurements at 230Vac - full load (bottom side)

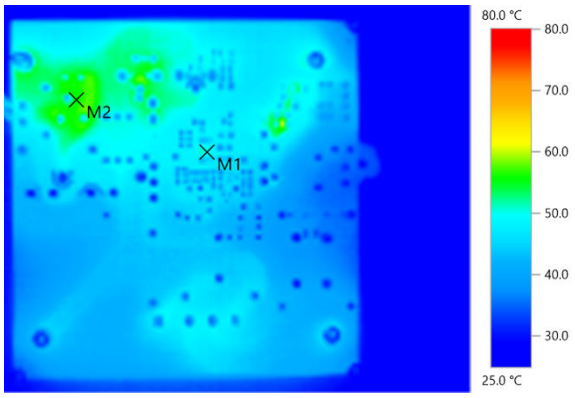


Table 2 and Table 3 provide the correlation between the measured points and components for both thermal maps.

Table 2. Measured temperature - PCB top side

Point	Part no.	Component	Temperature at 115Vac	Temperature at 230Vac
M1	L3	Input common choke	45.7	40.5
M2	D3	Bridge diode	71.1	51.7
M3	Q2	Power switch	66.7	57.6
M4	D1	Output diode	64.1	56.3
M5	NTC1	NTC resistor	76.9	63.8
M6	R2, R3, R4	Current sense resistors	64.9	49.7
M7	L1	Boost inductor	54.0	48.9

Table 3. **Measured temperature - PCB bottom side**

Point	Part no.	Component	Temperature at 115Vac	Temperature at 230Vac
M1	U1	IC controller (L4986A)	52.1	48.7
M2	-	PCB copper	60.1	55.5

4 Conducted emission pre-compliance test

Figure 69 and Figure 70 show the measurements of the conducted noise at full load and nominal mains voltages, with the “peak” setup. The limits shown on the diagrams relate to EN55022 Class-B, which is the most common standard for European equipment using a two-wire mains connection.

Figure 69. Full load at 115Vac

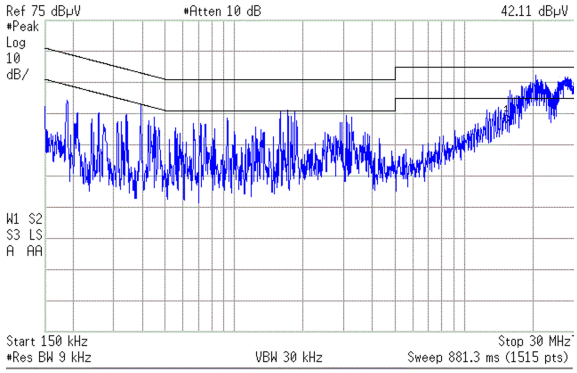
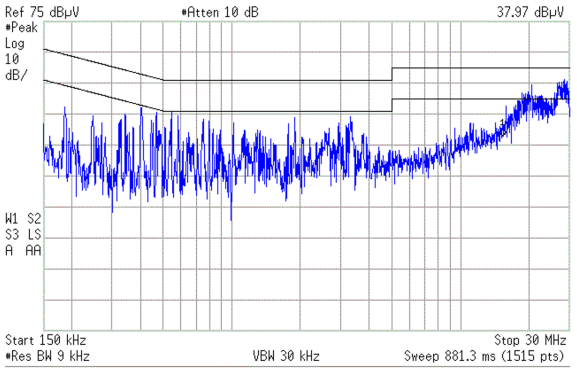


Figure 70. Full load at 230Vac (right)



5 Boost inductor specification

The main characteristics of the Boost inductor are:

- Primary inductance (pin 5-2): 700 µH ±15% @1 kHz - 0.25 V
- Core type: PQ35/35-PC44 or equivalent (center-leg gapped)
- Operating frequency range: 60-135 kHz
- Maximum primary rms current: 3.5 A
- Maximum primary peak current: 7.5 A
- Maximum temperature rise: 45°C
- Maximum operating ambient temperature: 60°C
- Coil former type: vertical, 6+6 pins (pin 12 is removed)
- Unit finishing: varnished
- External copper shield: not insulated, wound around the ferrite core and including the coil former; it is connected to pin 11 by a soldered solid wire.

Figure 71. Boost inductor – electrical diagram

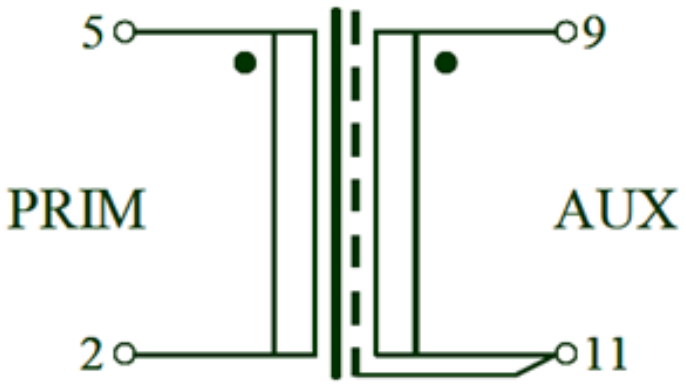
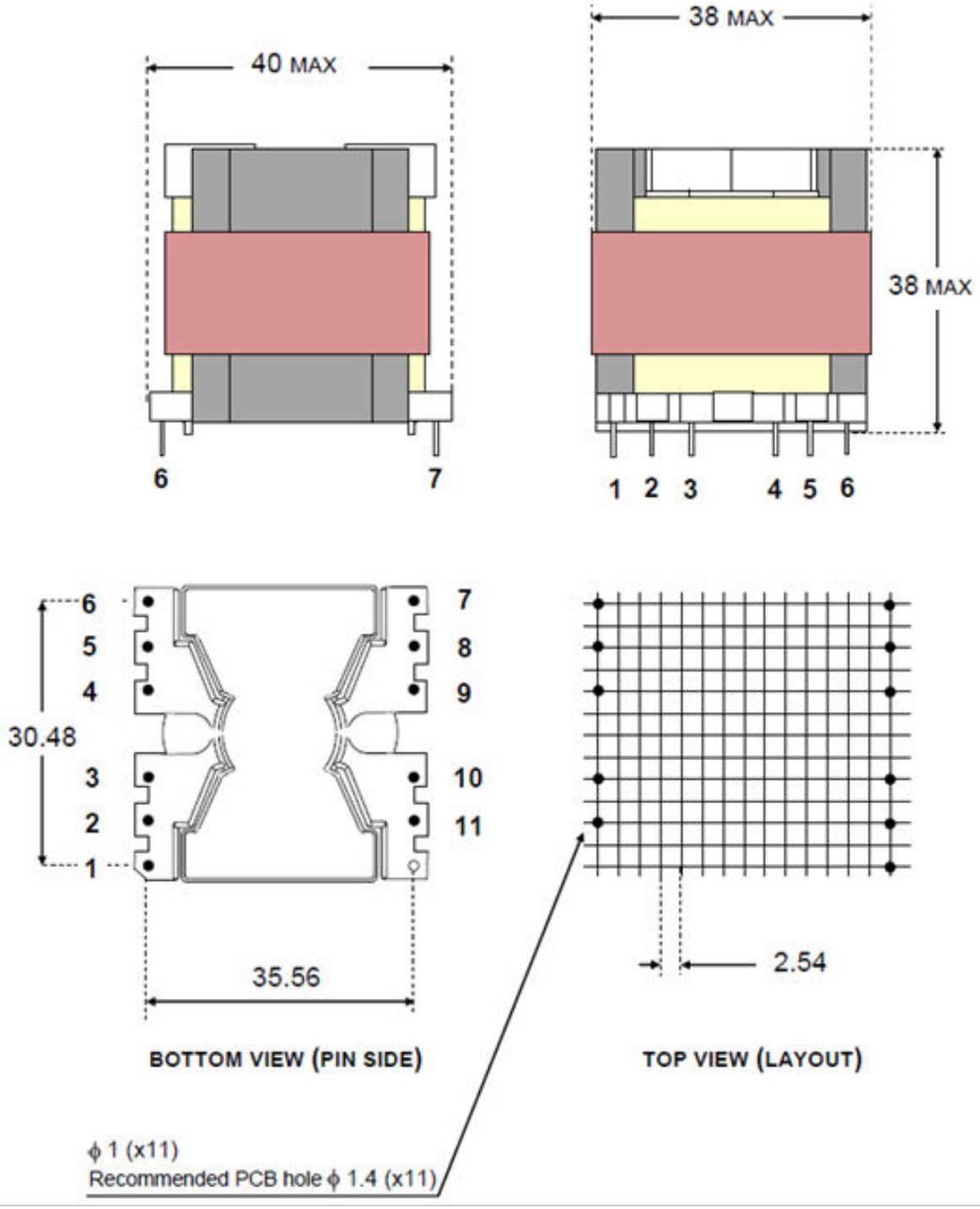


Table 4. Boost Inductor - winding characteristic

Windings	Start pins	End pins	Number of turns	Wire type	Wire diameter
PRIM	5	2	70	Single – G2	Litz 0.2Ø x 30
AUX	9	11	5 (spaced)	Litz – G2	0.28Ø

Figure 72. **Boost inductor – mechanical drawing**



6 Bill of materials

Table 5. EVL4986-350W evaluation board BOM

NM = not mounted

Sch. Ref.	Part no.	Case	Description	Supplier
C1	100µF	Rad. 8X11.5 mm	Electrolytic capacitor, 105°C - 50V	-
C2	470nF	6X26.5 mm	Film capacitor, 630V - B32673P6474K000	EPCOS
C3	100µF	Rad. 18X40 mm	Electrolytic capacitor, 105°C - 450V - EKXG451ELL101MM40S	UNITED CHEMICON
C4	100µF	Rad. 18X40 mm	Electrolytic capacitor, 105°C - 450V - EKXG451ELL101MM40S	UNITED CHEMICON
C5	470nF	8.5X26.5 mm	Film capacitor, X2 - B32923C3474M000	EPCOS
C6	1µF	10.5X26.5 mm	Film capacitor, 520V - B32673Z5105	EPCOS
C7	220nF	7.5X26.5 mm	Film capacitor, 305V - B32933A3224	EPCOS
C8	1µF	11X26.5 mm	Film capacitor, X2 - B32923C3105	EPCOS
C9	100nF	SMD 1206	Ceramic capacitor, 100V	-
C10	100pF	SMD 0805	Ceramic capacitor, X7R - 25V	-
C11	100pF	SMD 0805	Ceramic capacitor, X7R - 25V	-
C12	NM	-	-	-
C13	470nF	SMD 1206	Ceramic capacitor, X7R - 50V	-
C14	NM	-	-	-
C15	10pF	SMD 0805	Ceramic capacitor, X7R - 25V	-
C16	1.5µF	SMD 0805	Ceramic capacitor, X7R - 25V	-
C17	3.3nF	SMD 0805	Ceramic capacitor, COG - 25V	-
C18	150nF	SMD 0805	Ceramic capacitor, X7R - 25V	-
C19	100pF	SMD 0805	Ceramic capacitor, X7R - 25V	-
C20	100pF	SMD 0805	Ceramic capacitor, X7R - 25V	-
D1	STPSC8H065DI	TO-220AC Ins.	Schottky diode, 8A/650V SiC	STMICROELECTRONICS
D2	1N5406	DO-201	Rectifier diode	-
D3	D15XB60H	DWG	Bridge rectifier, 600V-15A	SHINDENGEN
D4	LL4148	MINIMELF	Signal diode	-
D5	NM	MINIMELF	-	-
D6	BZV55-C18	MINIMELF	Zener diode, 18V - 5%	-
D7	LL4148	MINIMELF	Signal diode	-
D8	S1M	SMA	Diode rectifier, 1000V-1A	-
D9	S1M	SMA	Diode rectifier, 1000V-1A	-
F1	6.3A	4x8.5mm P5.08mm	Fuse, 392/TE5 - Time delay	LITTELFUSE
HS2	HEAT-SINK	DWG	Heat sink for D3	TECNOAL
HS1	HEAT-SINK	DWG	Heat sink for Q1, Q2 & D1	TECNOAL
J1	Signal Connector	SIP 4P p3.5	PCB screw terminal - 4	LUMBERG
J2	Power Connector	SIP 2P p5.08	PCB screw terminal - 2	WEIDMULLER
J3	Power Connector	SIP 2P p5.08	PCB screw terminal - 2	WEIDMULLER

Sch. Ref.	Part no.	Case	Description	Supplier
JP1	Shorted	Wire	Isolated wire jumper	-
JP2	Shorted	Wire	Isolated wire jumper	-
JP3	Shorted	Wire	Isolated wire jumper	-
JP4	Shorted	Wire	Isolated wire jumper	-
JP5	Shorted	Wire	Isolated wire jumper	-
JP6	Shorted	Wire	Isolated wire jumper	-
JP7	Shorted	Wire	Isolated wire jumper	-
JP8	Shorted	Wire	Isolated wire jumper	-
JP9	Shorted	Wire	Isolated wire jumper	-
L1	700µH	DWG	PFC inductor - 2097.0002	AQ MAGNETICA
L2	70µH - 7A	DWG	DM Inductor - 1119.0013	AQ MAGNETICA
L3	3mH - 7A	DWG	EMI filter inductor - 1606.0007	AQ MAGNETICA
Q1	NM	TO-220FP	-	-
Q2	STF36N60M6	TO-220FP	N-CHANNEL Power MOSFET	STMICROELECTRONICS
Q1a	NM	TO-247	-	-
Q2a	NM	TO-247	-	-
Q3	BC847C	SOT23	BJT - NPN transistor	-
Q4	BC847C	SOT23	BJT - NPN transistor	-
RV1	300Vac	Rad. 15x5 p7.5mm	Metal Oxide Varistor, 300V - B72214S0301K101	EPCOS
R1	1R0	Rad. 15x7 p7.5mm	NTC resistor, B57237S0109M000	EPCOS
R2	0R22	PTH	Metal film resistor, 1W - 5%	KOA SPEER
R3	0R22	PTH	Metal film resistor, 1W - 5%	KOA SPEER
R4	0R22	PTH	Metal film resistor, 1W - 5%	KOA SPEER
R5	10K	SMD 0805	Resistor, 1/8W - 5%	-
R6	NM	SMD 0805	-	-
R7	3R9	SMD 0805	Resistor, 1/8W - 5%	-
R8	NM	SMD 0805	-	-
R9	6R8	SMD 0805	Resistor, 1/8W - 5%	-
R10	NM	SMD 0805	-	-
R11	1k	SMD 0805	Resistor, 1/8W - 5%	-
R12	10K	SMD 0805	Resistor, 1/8W - 5%	-
R13	1k	SMD 0805	Resistor, 1/8W - 5%	-
R14	330k	SMD 0805	Resistor, 1/8W - 5%	-
R15	100	SMD 1206	Resistor, 1/8W - 5%	-
R16	51R0	SMD 0805	Resistor, 1/8W - 1%	-
R17	NM	SMD 0805	-	-
R18	NM	SMD 1206	-	-
R19	30k	SMD 0805	Resistor, 1/8W - 1%	-
R20	16k	SMD 0805	Resistor, 1/8W - 1%	-

Sch. Ref.	Part no.	Case	Description	Supplier
R21	100k	SMD 0805	Resistor, 1/8W - 1%	-
R22	10K	SMD 0805	Resistor, 1/8W - 5%	-
R23	360K	SMD 0805	Resistor, 1/8W - 5%	-
R24	62k	SMD 0805	Resistor, 1/8W - 1%	-
R25	2M2	SMD 1206	Resistor, 1/8W - 1%	-
R26	2M2	SMD 1206	Resistor, 1/8W - 1%	-
R27	2M2	SMD 1206	Resistor, 1/8W - 1%	-
R28	0	SMD 1206	Resistor, 1/8W - 5%	-
R29	NM	SMD 1206	-	-
R30	NM	SMD 1206	-	-
R31	NM	SMD 1206	-	-
VCC	Test Point	-	Strip contact - 1	SAMTEC
U1	L4986A	SSOP10	CCM PFC controller	STMICROELECTRONICS
Z1	EVL4986-350W R1.1	-	Printed circuit board	-

7 References

[1] L4986 datasheet - www.st.com

[2] G. Gritti, “Novel Adaptive Pulse Width Modulator provides Quasi-Fixed Switching Frequency in Constant On/Off-Time controlled regulators”, Applied Power Electronics Conference and Exposition, 2018. APEC '18, Conference Proceedings 2018, pp. 760-766, March 2018.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
03-Dec-2021	1	Initial release.
28-Sep-2023	2	Updated Table 5 (D1 part number, U1 case).

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