Getting started with STM32H5 MCU hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features. Examples of these features are power supply, clock management, reset control, boot mode settings and debug management.

This document details how to use the STM32H5 series microcontrollers (MCUs) and describes the minimum hardware resources required to develop an application using these MCUs. Detailed reference design schematics are given in this document with the description of the main components, interfaces and modes.

For additional information, refer to the product datasheets and reference manuals available on www.st.com.

1 General information

This document applies to the STM32H5 series Arm®-based microcontrollers.

Note: Arm® is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Power supply management

2.1 Power supplies

The STM32H5 series requires a 1.71 V to 3.6 V operating voltage supply V_{DD}.

Several independent supplies can be provided for specific peripherals. Those supplies must not be provided without a valid operating supply on the VDD pin.

- **V_{DD}** = 1.71 V to 3.6 V.
  V_{DD} is the external power supply for the I/Os that is, the internal regulator and the system analog such as reset, power management, and internal clocks. It is provided externally through the VDD pins.
- **V_{DDA}** = 1.62 V ADCs / 1.8 V DAC), 2.1 V (VREFBUF) to 3.6 V for STM32H523/H533/H562/H563/H573 devices.
- **V_{DDA}** = 1.62 V (ADC, COMP) / 1.8 V (DAC) or 2.0 V (OPAMP) to 3.6 V for STM32H503 devices.
- V_{DDA} is the external analog power supply for A/D converters, D/A converters, and voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage and must be connected to V_{DD} when these peripherals are not used.
- **V_{DDSMPS}** = 1.71 V to 3.6 V
  V_{DDSMPS} is the external power supply for the SMPS step-down converter. It is provided externally through VDDSMPS supply pin, and must be connected to the same supply as VDD pin.
- **V_{LXSMPS}** is the switched SMPS step-down converter output.
- **V_{DDUSB}** = 3.0 V to 3.6 V
  V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage and must preferably be connected to V_{DD} when the USB is not used.
- **V_{DDIO2}** = 1.08 V to 3.6 V
  V_{DDIO2} is the external power supply for:
  - 10 I/Os (PD6, PD7, PG9:14, PB8, PB9) only available for STM32H523/H533/H562/H563/H573 devices
  - 9 I/Os (PA8, PA9, PA15, PB3:8) only available for STM32H503 devices

Note:

- *The SMPS power supply pins are available only on a specific package with SMPS step-down converter option:*
  - *V_{DDSMPS}, V_{LXSMPS} only available for STM32H563/H573 devices.*
  - *V_{DDUSB} pin is only available on STM32H523/H533/H562/H563/H573 devices.*

The V_{DDIO2} voltage level is independent from the V_{DD} voltage and must preferably be connected to V_{DD} when those pins are not used.

- **V_{CAP}** = 1.0 V to 1.35 V: digital core domain supply. This power supply is independent from all the other power supplies:
  - When the voltage regulator is enabled, VCORE is delivered by the internal voltage regulator.
  - When the voltage regulator is disabled, VCORE is delivered by an external power supply through VCAP pin, or by the switched mode power supply.
- **V_{BAT}** = 1.2 V to 3.6 V
- – V_{BAT} is the power supply when V_{DD} is not present through power switch for RTC (real-time clock), external clock 32 kHz oscillator, backup registers and optionally backup SRAM
- **VREF-, VREF+**:
  VREF+ is the input reference voltage for ADCs and DACs.
  For STM32H523/H533/H562/H563/H573 devices, it is also the output of the internal voltage reference buffer when enabled. VREF+ can be grounded when ADC and DAC are not active.
  The internal voltage reference buffer supports four output voltages, that are configured with the VRS bit in the VREFBUF_CSR register:
  - VREF+ ~1.8 V. This requires $V_{DDA} \geq 2.1$ V
  - VREF+ ~2.048 V. This requires $V_{DDA} \geq 2.4$ V
  - VREF+ ~2.5 V. This requires $V_{DDA} \geq 2.8$ V

For STM32H5xx devices, VREF- and VREF+ pins are not available on all packages. When these are not available, they are bonded to VSSA and VDDA, respectively.

When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled. VREF- must always be equal to VSSA.

For STM32H503 devices, independent VREF- and VREF+ pins are not available. They are bonded to VSSA and VDDA, respectively.

Figure 1, Figure 2 and Figure 3 show the power supply overview of STM32H523/H533/H562/H563/H573 and STM32H503 devices.

Figure 1. STM32H503 power-supply overview with LDO

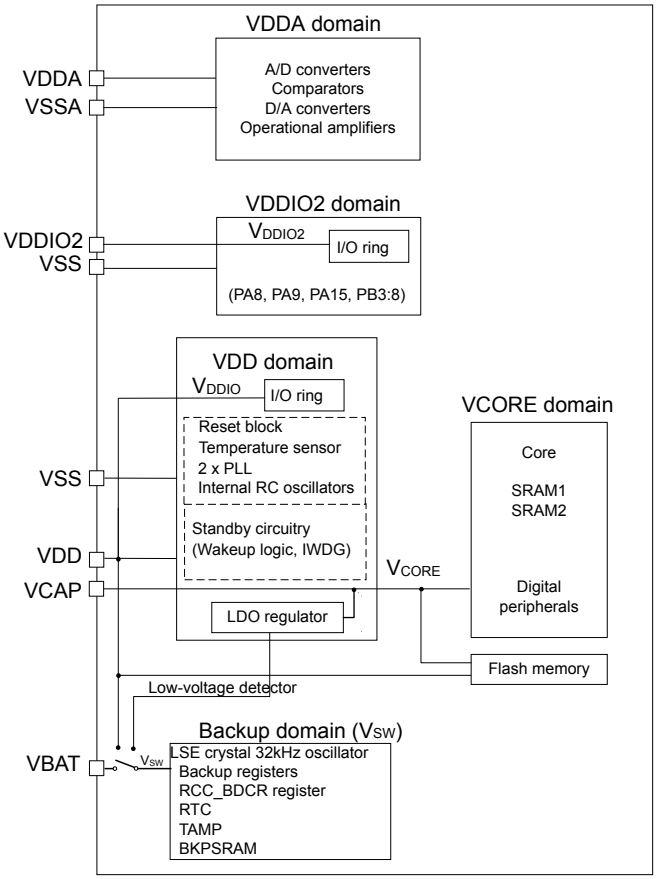


Figure 2. STM32H523/H533/H562/H563/H573 power-supply overview with LDO

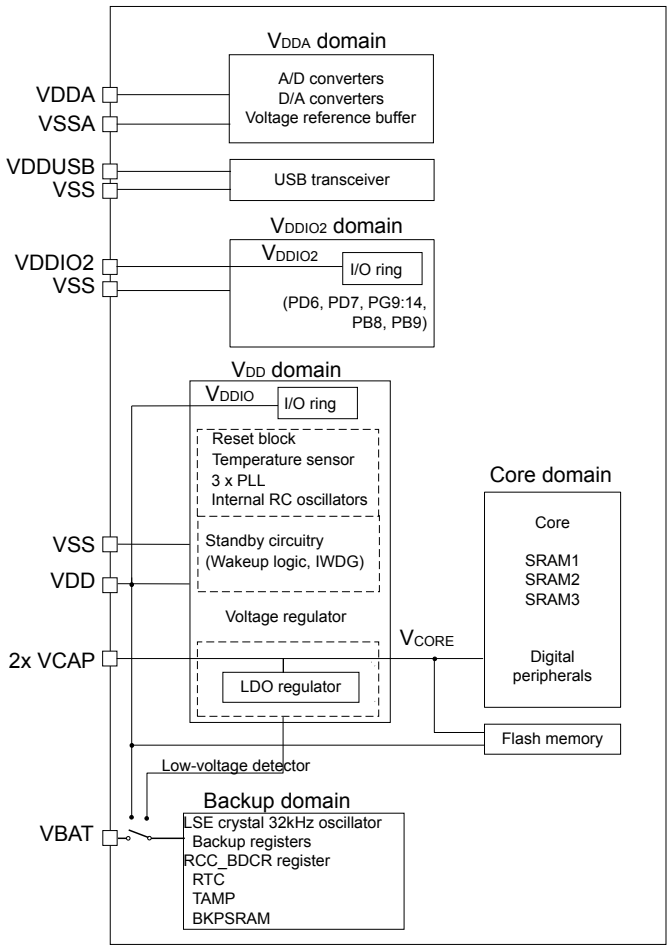
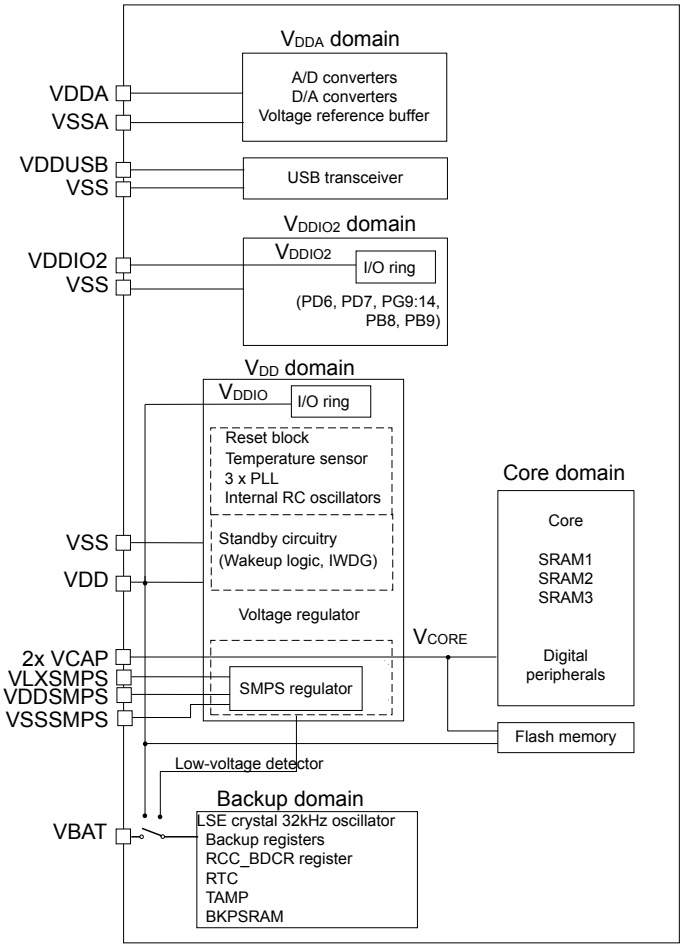


Figure 3. **STM32H563/H573 power-supply overview with SMPS**



2.1.1 Independent analog peripherals supply

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply that can be separately filtered and shielded from noise on the PCB.

The analog peripherals voltage supply input is available on a separate VDDA pin. An isolated supply ground connection is provided on VSSA pin. The V_{DDA} supply voltage can be different from V_{DD}.

The presence of V_{DDA} must be checked before enabling any of the analog peripherals supplied by V_{DDA} (A/D converter, D/A converter, voltage reference buffer). Power supply level monitoring is available on VDDA via AVDO bit in PWR_VMSR register. When a single supply is used, VDDA can be externally connected to VDD through the external filtering circuit in order to ensure a noise-free V_{DDA} reference voltage.

ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to VREF+, a separate reference voltage lower than V_{DDA}.

V_{REF+} is the highest voltage, represented by the full-scale value, for an analog input (ADC) or output (DAC) signal. V_{REF+} can be provided either by an external reference of by an internal buffered voltage reference (VREFBUF). The internal voltage reference can output a configurable voltage: 1.8 V, 2.048 V or 2.4 V. The internal voltage reference can also provide the voltage to external components through VREF+ pin.

For more details, refer to the device datasheet and to the reference manual.

Note:
- *The ADC and DAC reference voltage is available only on STM32H523/H533/H562/H563/H573 devices.*
- *For STM32H523/H533/H562/H563/H573 devices, the VREF+ and VREF- pins are not available on all packages (connected internally respectively to VDDA and VSSA). Do not enable the internal voltage reference buffer when an external power supply is applied to the VREF+ pin.*
- *Reference buffer supplied by VDDA are only available for STM32H523/H533/H562/H563/H573 devices.*

2.1.2 Independent I/O supply rail

Some I/Os are supplied from a separate supply rail. The power supply for this rail can range from 1.08 V to 3.6 V and is provided externally through the VDDIO2 pin. The VDDIO2 voltage level is completely independent from VDD or VDDA.

The VDDIO2 pin is available only for some packages. Refer to the pinout diagrams or tables in the related device datasheet for I/O list(s). The power supply level monitoring is available on VDDIO2 via VDDIO2RDY bit in PWR_VMSR register.

Note:
- *I/Os: PD6, PD7, PG9:14, PB8, PB9 supplied for STM32H523/H533/H562/H563/H573 devices.*

2.1.3 Independent USB transceivers supply

The USB transceivers are supplied from a separate V_{DDUSB} power supply pin. V_{DDUSB} range is from 3.0 V to 3.6 V and is completely independent from V_{DD} or V_{DDA}. The power supply level monitoring is available on VDDUSB via USB33RDY bit in PWR_VMSR register.

Note: The independent USB transceivers supply is available only onSTM32H523/H533/H562/H563/H573.

2.1.4 Backup domain

To retain the content of the backup registers and supply the RTC function when V_{DD} is turned off, the VBAT pin can be connected to an optional backup voltage supplied by a battery or by another source. The VBAT pin powers the RTC unit, the LSE oscillator, and the PC13 to PC15 and PI8 I/Os (PI8 is only available on STM32H562/H563/H573 devices), allowing the RTC to operate even when the main power supply is turned off. The backup SRAM is optionally powered by the VBAT pin when the BREN bit is set in the PWR backup domain control register (PWR_BDCR). The power-down reset embedded in the reset block controls the switch to the V_{BAT} supply.

Caution:
- During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a PDR (power-down reset) has been detected, the power switch between V_{BAT} and V_{DD} remains connected to VBAT pin.
- During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (refer to the datasheet for $t_{RSTTEMPO}$ value) and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into VBAT through an internal diode connected between VDD and the power switch (VBAT). If the power supply or battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin.

If no external battery is used in the application, it is recommended to connect VBAT externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

When the backup domain is supplied by VBAT (analog switch connected to VBAT), the following pins are available:

- PC13, PI8, PC14 and PC15, that can be configured by RTC or LSE
- PC13, PI8, PA0, PA1 and PA2 (PI8, PA1 and PA2 are only available on STM32H562/H563/H573 devices) when they are configured by TAMP peripheral as tamper pins

Note: Because the analog switch can transfer only a limited amount of current, the use of GPIO PC13 and PI8 (only available on STM32H562/H563/H573 devices) in output mode is restricted. The speed must be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source for instance to drive an LED. Current limit for PC14 and PC15 is described in product datasheet.

PI8 is not available on all devices. Refer to the product associated datasheet.

Backup domain access

After a system reset, the backup domain (RCC backup domain control register RCC_BDCR, RTC registers, TAMP registers, backup registers and backup SRAM) is protected against possible unwanted write accesses. To enable access to the backup domain, set the DBP bit in the PWR disable backup domain control register (PWR_DBPR) to enable access to the backup domain.

The Backup domain includes up to 4 Kbytes of backup RAM accessible in 32-, 16-, or 8-bit data mode. The backup RAM is supplied from the backup regulator in the Backup domain. When the backup regulator is enabled through BREN bit in the PWR_BDCR, the backup RAM content is retained even in Standby and/or VBAT mode (it can be considered as an internal EEPROM if VBAT is always present).

The backup regulator can be ON or OFF depending whether the application needs the backup RAM function in Standby or VBAT modes. The backup RAM is read protected and mass erased when a tamper event occurs, this prevents confidential data (such as a cryptographic private key) from being accessed.

The backup RAM can be erased in two ways:

- through the flash interface after a full product state regression
- after a tamper event

V_{BAT} battery charging

When V_{DD} is present the external battery can be charged on VBAT through an internal resistance. The V_{BAT} charging is done either through a 5 kΩ resistor or through a 1.5 kΩ resistor depending on the VBRS bit value in the PWR_BDCR register. The battery charging is enabled by setting VBE bit in the PWR_BDCR register. It is automatically disabled in VBAT mode.

2.1.5 Voltage regulator

Linear voltage regulator (LDO) is enabled on power-on reset. To supply the V_{CORE} from the external source, it is possible to disable the regulator by setting BYPASS bit in the PWR_SCCR register. The BYPASS bit is written once after power-on reset. The written-once mechanism locks the register and any further write access is ignored. The system must be power cycled before writing a new value. When V_{CORE} is supplied from an external source, the externally applied voltage level must be reflected in the VOSx bits in the PWR_VOSCR register.

The STM32H562/H563/H573 devices embed two internal regulators, one LDO or one SMPS to provide the digital peripherals, SRAMs (SRAM1/2/3) and the embedded flash memory.

Depending on the package configuration, the regulator is selected by the hardware (SMPS and LDO regulators are exclusively selected).

Note: The SMPS regulator is available only on STM32H563/H573 devices.

Dynamic voltage scaling

The STM32H5 series support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the maximum operating frequency of the system.

Both regulators (LDO or SMPS) provides four different voltages (voltage scaling) and operates in Stop modes.

The main regulator operates in the following ranges:

- VOS0 (1.35 V, 250 MHz)
- VOS1 (1.2 V, 200 MHz)
- VOS2 (1.1 V, 150 MHz)
- VOS3 (1.0V, 100 MHz)

Embedded voltage regulator operating modes

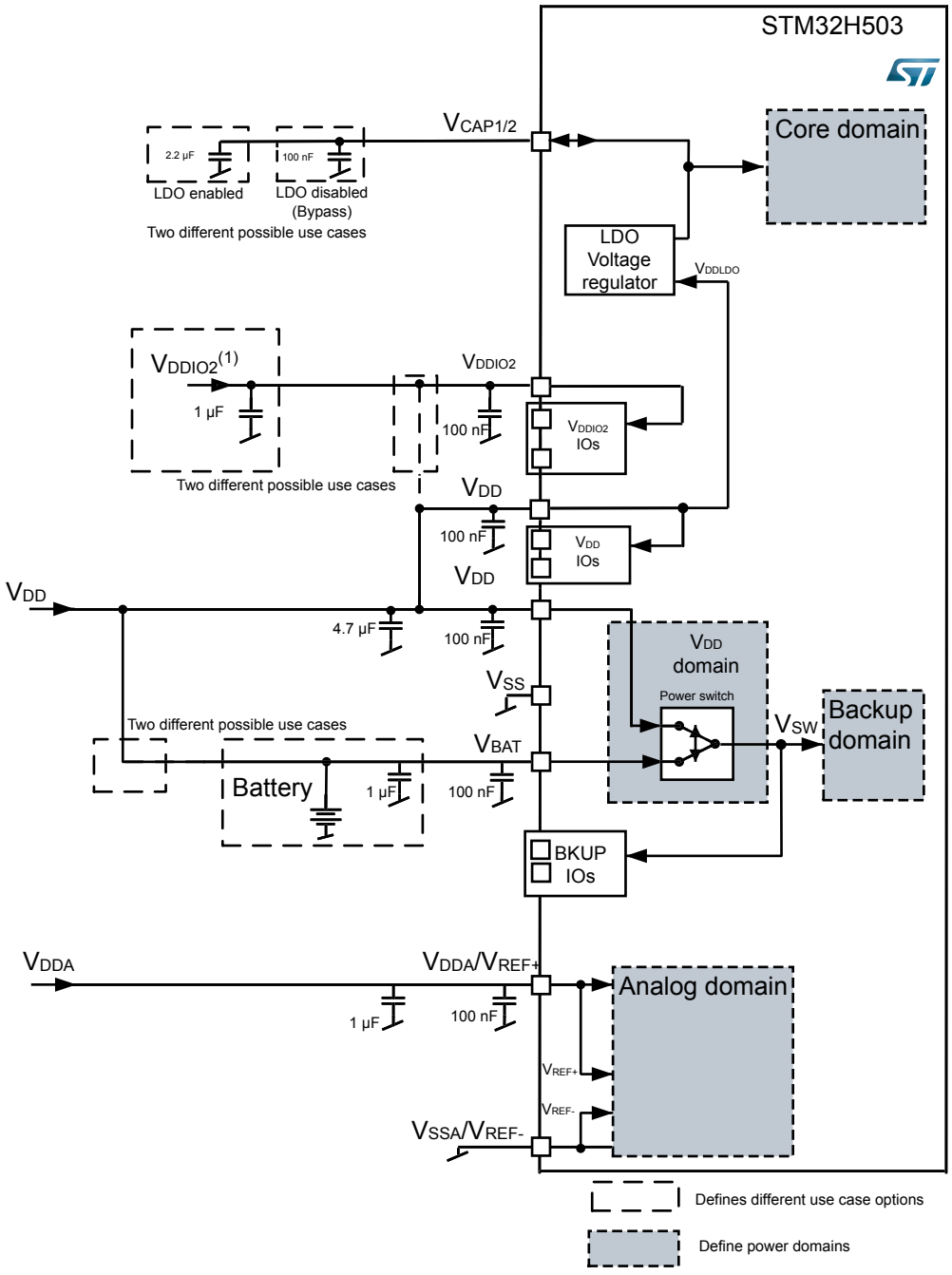
There are three different power modes:

- **Run mode**
  The voltage regulator (LDO or SMPS) provides full power to the VCORE domain (core, memories, and digital peripherals). The regulator output voltage either LDO or SMPS can be scaled by the software to different voltage levels (VOS0, VOS1, VOS2, and VOS3) that are configured through the VOS bits in the PWR voltage-scaling control register (PWR_VOSCR). The VOS voltage scaling allows optimization of the power consumption when the system is clocked below the maximum frequency. By default, VOS3 is selected after system reset. VOSx bits can be changed on-the-fly to adapt to the required system performance.
- **Stop mode**
  The voltage regulator (LDO or SMPS) supplies the VCORE domain to retain the content of registers and internal memories. The regulator level is selected through the SVOS bits in the PWR power mode control register (PWR_PMCR). Stop mode power consumption can be further reduced using SVOS (lower voltage level than VOS3) and even further with SVOS5.
- **Standby mode**
  The regulator (LDO or SMPS) is OFF and the VCORE domains are powered down. The content of the registers and memories is lost except for the Standby circuitry and the backup domain.

2.2 Power supply schemes

The following figures show the power supply schemes for STM32H503 and STM32H523/H533/H562/H563/H573.

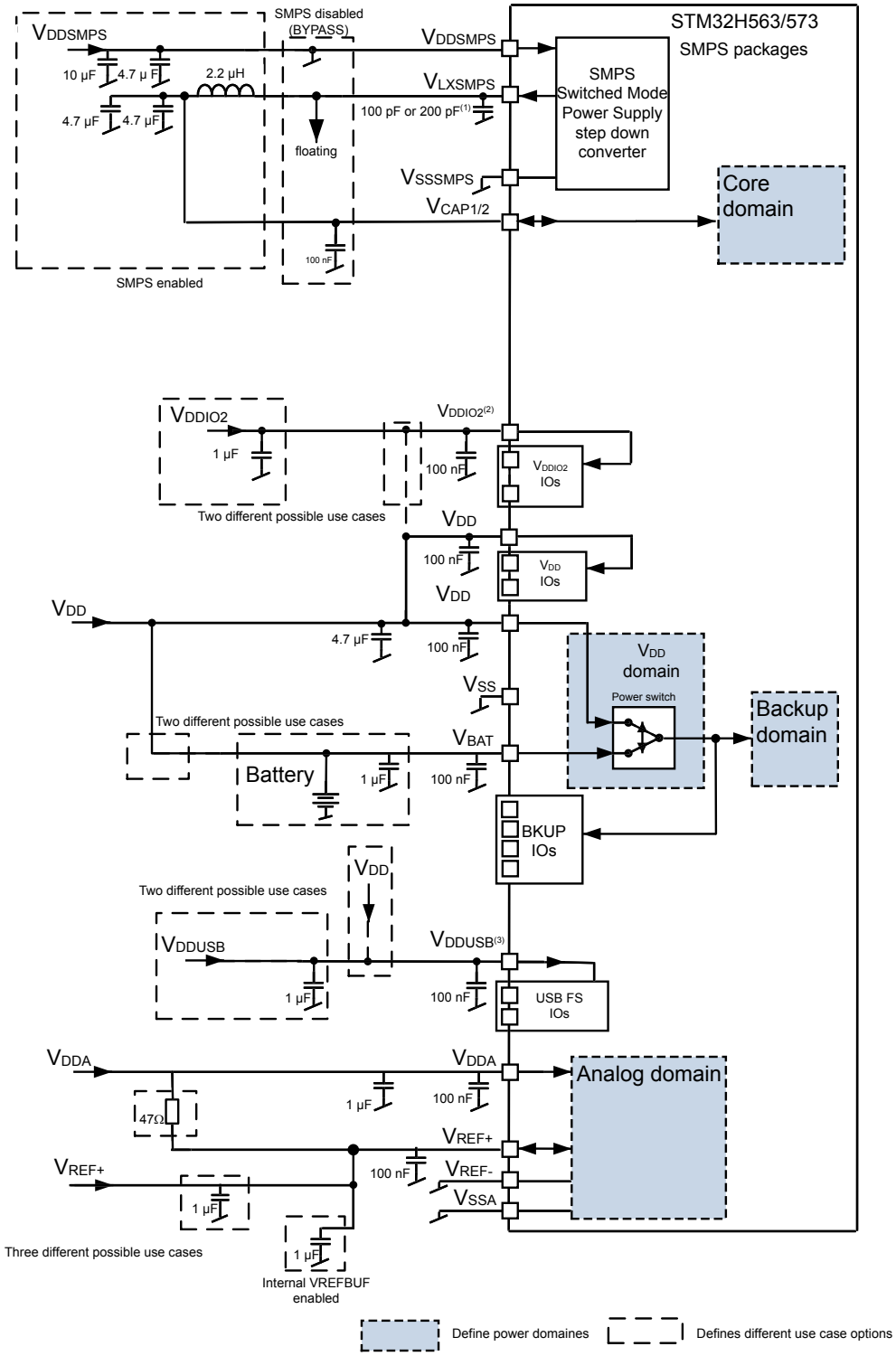
Figure 4. STM32H503 power-supply scheme



1.: Dedicated V_{DDIO2} supply pin is only available on WLCSP25 package; it represents the external power supply for nine I/Os (PA8, PA9, PA15, and PB[3:8]). On packages without V_{DDIO2} pin, those I/Os are supplied by V_{DD}.

Caution: If there are two VCAP pins (such as LQFP64 package), each pin must be connected to a 2.2 µF (typical) capacitor (for a total approximately 4.4 µF). If only one VCAP pin is available, then it must be connected to a 4.7 µF capacitor.

Figure 5. STM32H563/H573 power-supply scheme with SMPS



(1) 220 pF ceramic capacitor for LQFP packages. 100 pF ceramic capacitor for BGA packages (2) Dedicated supply for PD6, PD7, PG9:14, PB8, PB9 IOs. On packages without VDDIO2 pin, those I/Os are supplied by VDD.
(3) This pin is internally tied to VDD when it is not present in some specific packages. In consequence, the VDD supply level must be compliant with VDDUSB if the USB is used for these packages

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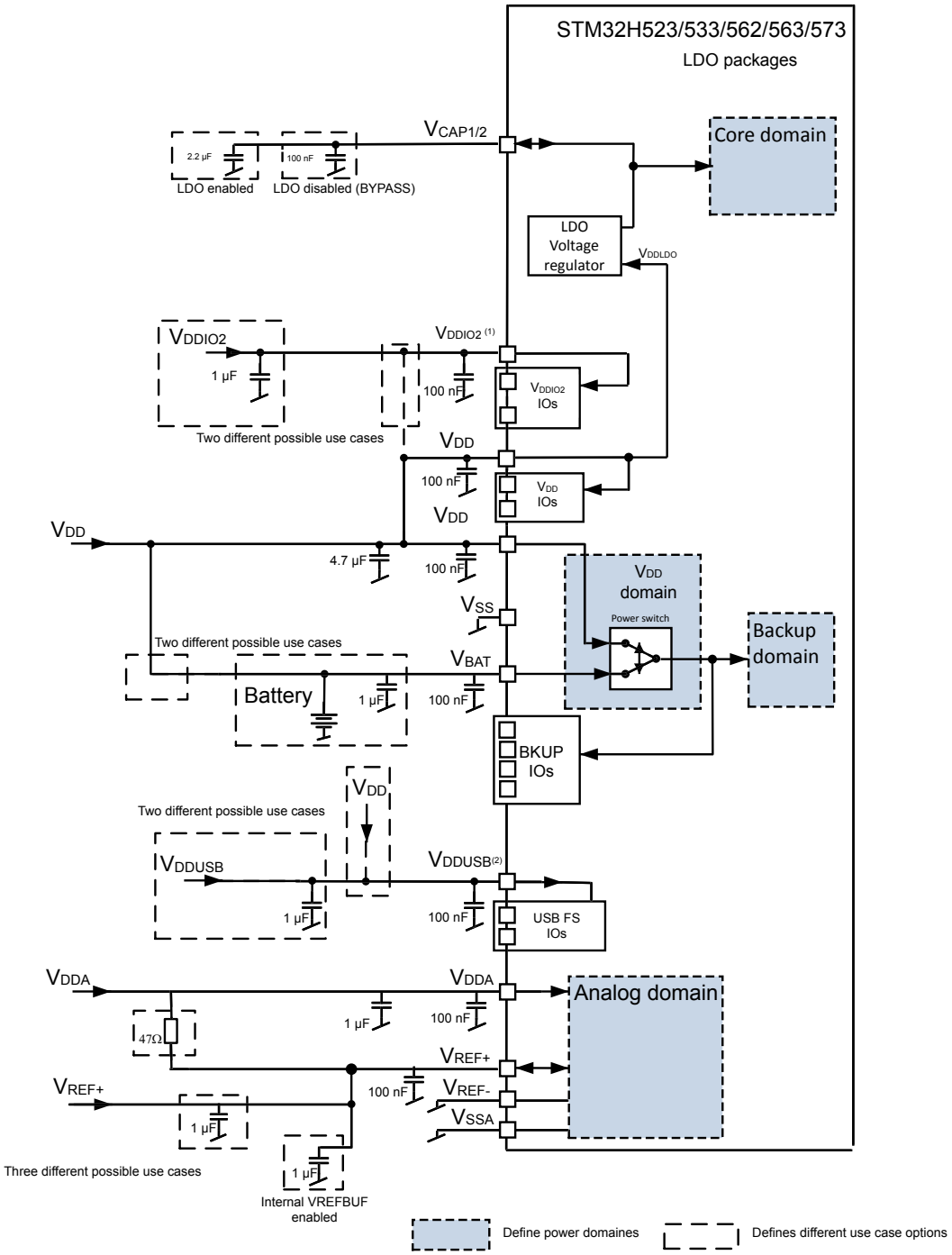
Figure 6. STM32H523/H533/H562/H563/H573 power-supply scheme with LDO



(1) Dedicated supply for PD6, PD7, PG9:14, PB8, PB9 IOs. On packages without VDDIO2 pin, those I/Os are supplied by VDD.
(2) This pin is internally tied to VDD when it is not present in some specific packages. In consequence, the VDD supply level must be compliant with VDDUSB if the USB is used for these packages

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Note: The 47-ohm resistor provides a possible solution to generate V_{REF+} from V_{DDA} at reduced cost. This resistor effectively allows filtering of V_{REF+} compared to V_{DDA} but with a quite relative efficiency.

2.3 Power supply sequence between VDDA, VDDUSB, VDDIO2, and VDD

2.3.1 Power supply isolation

The devices feature a reset system that ensures the main power supply (V_{DD}) has reached a valid operating range before releasing the MCU reset.

This reset system is also in charge of isolating the independent power domains: V_{DDA}, V_{DDUSB}, V_{DDIO2}, and V_{DD}. This reset system is supplied by V_{DD} and is not functional before V_{DD} reaches a minimal voltage (1 V in worse-case conditions).

In order to avoid leakage currents between the available supplies and V_{DD} (or ground), V_{DD} must be provided first to the MCU and released last with tolerance during power down (see Section 2.3.3).

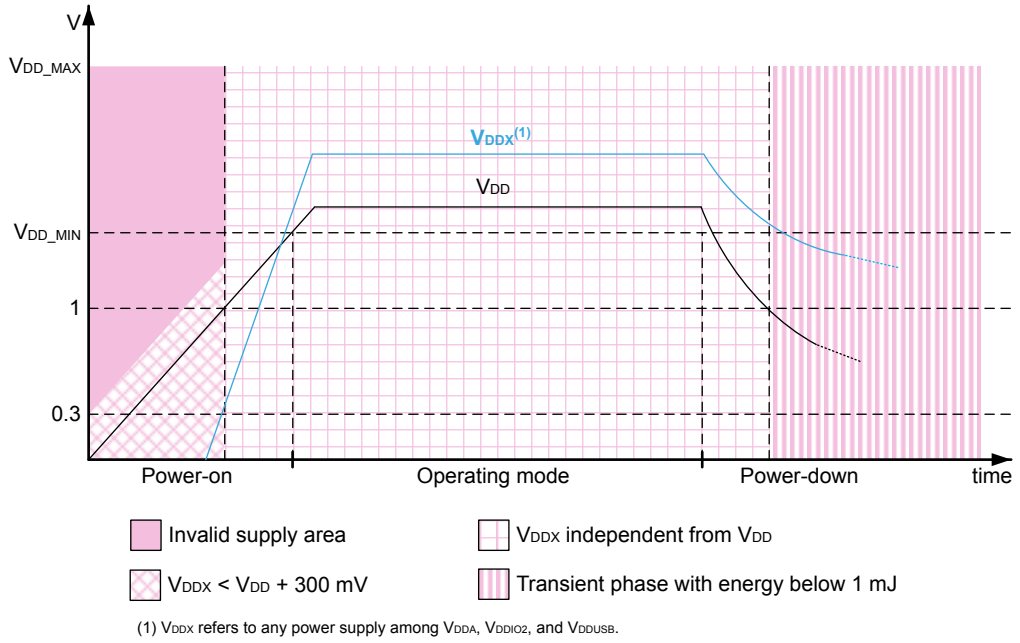
2.3.2 General requirements

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

Note: V_{DDUSB} power supply is only for STM32H523/H533/H562/H563/H573 devices.

Figure 7. Power-up/down sequence



Note: V_{DDX} refers to any power supply among V_{DDA}, V_{DDUSB}, and V_{DDIO2}.

2.3.3 Particular conditions during power-down phase

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase (see Figure 7).

2.4 Reset and power-supply supervisor

2.4.1 Power-on reset (POR), power-down reset (PDR) and Brownout reset (BOR)

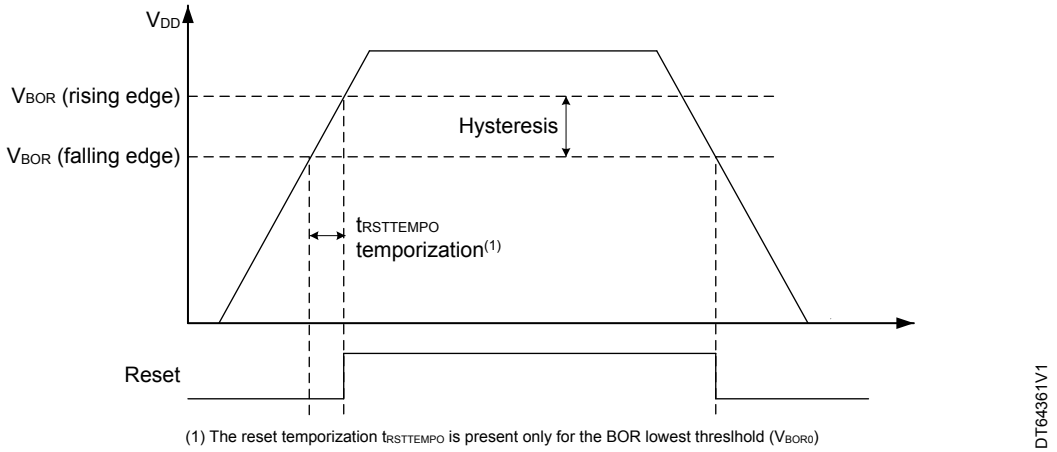
The devices have an integrated power-on reset (POR) and power-down reset (PDR), coupled with a Brownout reset (BOR) circuitry. The BOR is by default disabled and can be enabled by setting BORH_EN option bit to 1. The BOR monitors the backup domain supply voltage that is, VDD when present, VBAT otherwise.

The BOR thresholds can be selected through option bytes.

During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified VBORx threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the VBORx upper limit, the device reset is released and the system can start.

For more details on the Brownout reset thresholds, refer to the electrical characteristics section in the datasheet.

Figure 8. Brownout reset waveform



(1) The reset temporization $t_{RSTTEMPO}$ is present only for the BOR lowest threslhold (V_{BOR0})

2.4.2 Programmable voltage detector (PVD)

The PVD can be used to monitor the VDD power supply by comparing it to a threshold selected by the PLS[2:0] bits in the PWR voltage monitor control register (PWR_VMCR). The PVD can also be used to monitor a voltage level on the PVD_IN pin. In this case PVD_IN voltage is compared to the internal VREFINT level. The PVD is enabled by setting the PVDE bit in PWR voltage monitor control register (PWR_VMCR).

A PVDO flag is available in the PWR voltage monitor status register (PWR_VMSR) to indicate if VDD or PVD_IN voltage is higher or lower than the PVD threshold. This event is internally connected to the EXTI and can generate an interrupt, provided it has been enabled through the EXTI registers.

The rising/falling edge sensitivity of the EXTI line must be configured according to PVD output behavior that is, if the EXTI line is configured to rising edge sensitivity, the interrupt is generated when VDD or PVD_IN voltage drops below the PVD threshold. As an example, the service routine could perform emergency shutdown.

2.4.3 Analog voltage detector (AVD)

The AVD can be used to monitor the VDDA supply by comparing it to a threshold selected by the ALS[1:0] bits in the PWR voltage monitor control register (PWR_VMCR). The AVD is enabled by setting the AVDEN bit in PWR voltage monitor control register (PWR_VMCR). An AVDO flag is available in the PWR voltage monitor status register (PWR_VMSR) to indicate whether VDDA is higher or lower than the AVD threshold.

This event is internally connected to the EXTI and can generate an interrupt if enabled through the EXTI registers. The AVDO interrupt can be generated when VDDA drops below the AVD threshold and/or when VDDA rises above the AVD threshold depending on EXTI rising/falling edge configuration. As an example the service routine could indicate when the VDDA supply drops below a minimum level.

2.4.4 System reset

A system reset sets all registers to their reset values except the reset flags in RCC reset status register (RCC_RSR) and the registers in the backup domain.

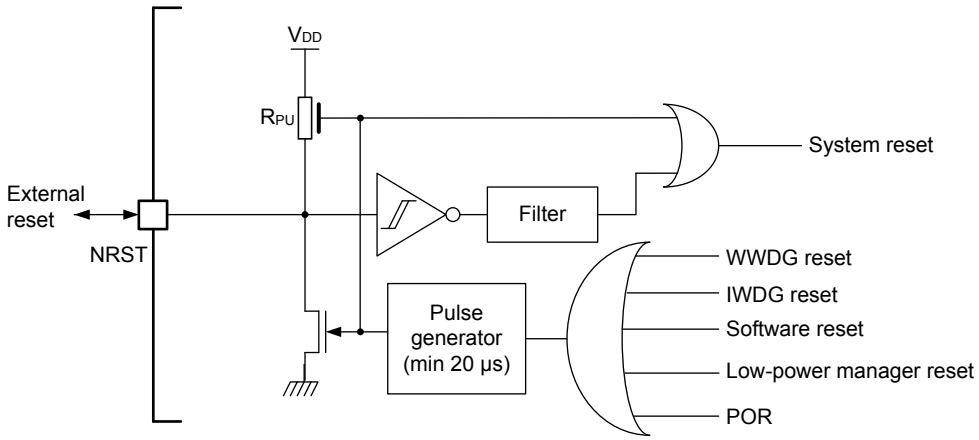
A system reset is generated when one of the following events occurs:

- a low level on the NRST pin (external reset)
- a window watchdog event (WWDG reset)
- an independent watchdog event (IWDG reset)
- a software reset (SW reset)
- a low-power mode security reset
- a Brownout reset

These sources act on the NRST pin and this pin is always kept low during the delay phase. The reset service routine vector is selected depending on the product state, on Boot option bytes or on both.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low. In case on an internal reset, the internal pull-up RPU is deactivated in order to save the power consumption through the pull-up resistor.

Figure 9. Simplified diagram of the reset circuit



2.4.5 Bypass mode

The power management unit is configurable by software with the option to bypass. When bypassed, the core power supply should be provided through VCAPx pins connected together.

In Bypass mode, the internal voltage scaling is not managed internally, and the external voltage value (1.0 to 1.3 V) must be consistent with the targeted maximum frequency (see the applicable datasheet for the actual VOS level).

In Stop mode, it can be lowered to 1.0 V (see the applicable datasheet for the actual SVOS level).

In Bypass mode, the external voltage must be present at the same time as VDD. To avoid conflict with the LDO, the external voltage must be kept above 1.15 V until the LDO is disabled by software.

When operating in Bypass mode, the application must adjust VOS, using bits VOS[1:0] in PWR_VOSCR register. VOS[1:0] must be set according to the external provided core voltage level and related performance. To adjust the VOS level, the software must select sequentially the intermediate levels.

When increasing the performance:

- First, voltage scaling must be incremented (for example when changing from VOS3 to VOS0, lower levels must be selected in the VOS[1:0] bits: VOS2, VOS1, and then VOS0).
- The external voltage can be increased.
- The system frequency can be increased.

When decreasing the performance:

- The system frequency must be decreased.
- The external voltage must be decreased.
- The voltage scaling can be decremented (for example when changing from VOS1 to VOS3, lower levels must be selected in the VOS[1:0] bits: VOS2, and then VOS3).

2.4.6 Backup domain reset

A backup domain reset is generated when one of the following events occurs:

- a software reset, triggered by setting the BDRST bit in RCC_BDCR register
- a V_{DD} or V_{BAT} power on, if both supplies have previously been powered off

A backup domain reset affects the LSE oscillator, the RTC, the backup registers, the backup SRAM, all secrets protected by tamper and the RCC_BDCR register.

3 Clock

The following clock sources can be used to drive the system clock (SYSCLK):

- HSI: high-speed internal 64 MHz RC oscillator clock
- CSI: multi-speed internal RC oscillator clock
- HSE: high-speed external crystal or clock, from 4 MHz to 50 MHz
- PLL1 clock

The HSI is used as a system clock source after startup from reset, configured at 32 MHz.

The devices have the following additional clock sources:

- LSI: 32 kHz low-speed internal RC that drives the independent watchdog and optionally the RTC used for auto-wakeup from Stop and Standby modes
- LSE: 32.768 kHz low-speed external crystal or clock that optionally drives the real-time clock (rtc_ck)
- HSI48: internal 48 MHz RC that potentially drives the USB and the RNG
- PLL2 and PLL3 clocks (PLL3 clock is available only on STM32H562/H563/H573 devices)

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

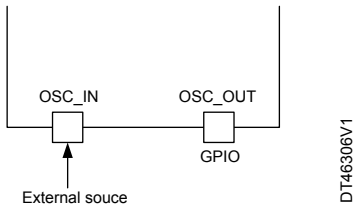
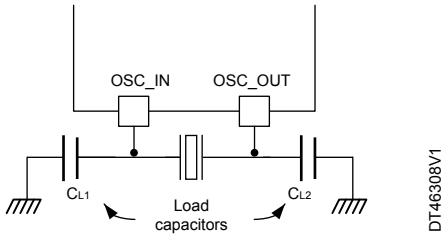
3.1 HSE clock

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Table 1. HSE/LSE clock sources

Clock source	Hardware configuration
External clock	
Crystal/ceramic resonators	 CL1 and CL2 values depend on the quartz. Refer to the application note *Oscillator design guide for STM8AF/AL/S and STM32 microcontrollers* (AN2867) for more details.

3.1.1 External crystal/ceramic resonator (HSE crystal)

The 4 MHz to 50 MHz external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in Table 1. Refer to the electrical characteristics section of the datasheet for more details.

3.1.2 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 50 MHz. The external clock signal (square, sinus or triangle) with ~40-60 % duty cycle depending on the frequency (refer to the datasheet) must drive the OSC_IN pin while the OSC_OUT pin can be used a GPIO (see Table 1).

3.2 HSI clock

The HSI clock signal is generated from an internal 64 MHz RC oscillator. The HSI block provides the default system clock (32MHz) after a reset. The HSI RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator. However, even with calibration, the frequency is less accurate than an external crystal oscillator or ceramic resonator. The HSI clock can be selected as system clock after wakeup from Stop mode.

For more details, refer to section 'Clock security system (CSS)' in the reference manual.

3.3 CSI oscillator

The CSI is a low-power RC oscillator that can be used directly as system clock, peripheral clock, or PLL input.

The CSI advantages are the following:

- low-cost clock source since no external crystal is required
- faster startup time than HSE (a few microseconds)
- very low-power consumption,

The CSI provides a clock frequency of about 4 MHz, while the HSI is able to provide a clock up to 64 MHz. CSI frequency, even with frequency calibration, is less accurate than an external crystal oscillator or ceramic resonator. The CSI can be switched ON and OFF through the CSION bit. The CSIRDY flag indicates whether the CSI is stable or not. At startup, the CSI output clock is not released until this bit is set by hardware.

The CSI cannot be switched OFF if one of the two conditions is met:

- The CSI is used directly (via software mux) as system clock.
- The CSI is selected as reference clock for PLL1, with PLL1 enabled and selected to provide the system clock (via software mux).
  In that case the hardware does not allow programming the CSION bit to 0. The CSI can be disabled or not when the system enters Stop mode. In addition, the CSI clock can be driven to the MCO2 output and used as clock source for other application components.
  Even if the CSI settling time is faster than the HSI, care must be taken when the CSI is used as kernel clock for communication peripherals: the application must take into account the following parameters:
  - the time interval between the moment where the peripheral generates a kernel clock request and the moment where the clock is really available
  - the frequency precision

3.4 LSE clock

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator (see Table 1). It provides a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The crystal oscillator driving strength is configured using the LSEDRV[1:0] bits in the RCC_BDCR, according to crystal specification, to obtain the best compromise between robustness and short start-up time on one side and low-power-consumption on the other side.

External source (LSE bypass)

In this mode, an external clock source must be provided, with a frequency up to 1 MHz. The external clock signal (square, sinus or triangle) with ~50 % duty cycle, must drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO (see Table 1).

3.5 LSI clock

The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby modes for the independent watchdog (IWDG) and RTC.

The clock frequency is 32 kHz. When the IWDG is enabled or when the RTC or TAMP is clocked by the LSI.

4 Packages

4.1 Package summary

The package selection must consider the constraints that are strongly dependent upon the application. The list below summarizes the most frequent ones:

- Number of interfaces required: some interfaces may not be available on some packages. Some interfaces combination may not be possible on some packages.
- PCB technology constrains: small pitch and high-ball density may require more PCB layers and higher-class PCB
- Package height.
- PCB available area.
- Noise emission or signal integrity of high-speed interfaces.
- Smaller packages usually provide better signal integrity. This is further enhanced as small-pitch and high-ball density requires multilayer PCBs that allow better supply/ground distribution.
- Compatibility with other devices.

Table 2. Package summary for STM32H562/H563/H573 devices

Package	Size (mm)	Height (mm)(1)	Pitch (mm)	LDO option	SMPS option
LQFP176	24 x 24	1.6	0.5	X	X
LQFP144	20 x 20	1.6	0.5	X	X
LQFP100	14 x 14	1.6	0.5	X	X
LQFP64	10 x 10	1.6	0.5	X	NA
UFBGA176	10 x 10	0.6	0.65	X	X
UFBGA169	7 x 7	0.6	0.50	X	X
VFQFPN68	8 x 8	1	0.4	X	NA
WLCSP80	3.50 x 3.27	0.58	0.35	NA	X

1. *Maximum value.*

Table 3. Package summary for STM32H523/H533 devices

Package	Size (mm)	Pitch (mm)	Height (mm)(1)
LQFP144	20 x 20	0.5	1.6
UFBGA144	10 x 10	0.8	0.6
LQFP100	14 x 14	0.5	1.6
UFBGA100	7 x 7	0.5	0.6
LQFP64	10 x 10	0.65	0.6
LQFP48	7 x 7	1.6	0.5
UFQFPN48	7 x 7	0.6	0.5
WLCSP39	2.76 x 2.78	0.4	0.58

1. *Maximum value.*

Table 4. Package summary for STM32H503 devices

Package	Size (mm)	Pitch (mm)	Height (mm)(1)
LQFP64	10 x 10	0.5	1.6
LQFP48	7 x 7	0.5	1.6

Package	Size (mm)	Pitch (mm)	Height (mm)(1)
UFQFPN48	7 x 7	0.5	0.6
UFQFPN32	5 x 5	0.5	0.6
WLCSP25	2.33 x 2.24	0.4	0.58

1. *Maximum value.*

4.2 Pinout summary

Table 5. Pinout summary for STM32H562/H563/H573 devices

Pin name(1)	STM32H562/H563/H573 packages (LDO option)							STM32H563/H573 packages (SMPS option)					
	LQFP64	LQFP100	LQFP144	LQFP176	UFBGA169	UFBGA176	VFQFPN68	LQFP100	LQFP144	LQFP176	UFBGA169	UFBGA176	WLCSP80
Specific I/Os													
PC14-OSC32_IN	X	X	X	X	X	X	X	X	X	X	X	X	X
PC15-OSC32_OUT	X	X	X	X	X	X	X	X	X	X	X	X	X
PH0-OSC_IN	X	X	X	X	X	X	X	X	X	X	X	X	X
PH1-OSC_OUT	X	X	X	X	X	X	X	X	X	X	X	X	X
System pins													
NRST	X	X	X	X	X	X	X	X	X	X	X	X	X
BOOT0	X	X	X	X	X	X	X	X	X	X	X	X	X
Power pins													
VDDA	X	X	X	X	X	X	X	X	X	X	X	X	X
VSSA	X	X	X	X	X	X	X	X	X	X	X	X	X
VDDIO2	-	-	X	X	X	X	-	-	X	X	X	X	-
VDDUSB	-	X	X	X	X	X	-	X	X	X	X	X	X
VCAP	X	X	X	X	X	X	X	X	X	X	X	X	X
VBAT	X	X	X	X	X	X	X	X	X	X	X	X	X
VDDSMPS	-	-	-	-	-	-	-	X	X	X	X	X	X
VSSSMPS	-	-	-	-	-	-	-	X	X	X	X	X	X
VLXSMPS	-	-	-	-	-	-	-	X	X	X	X	X	X
VREF+	-	X	X	X	X	X	-	X	X	X	X	X	-
VREF-	-	X	-	-	X	X	-	-	-	-	X	X	-
Number of VDD	4	5	10	14	10	13	4	5	10	14	10	11	6
Number of VSS	4	5	11	12	11	37	4	5	11	13	11	37	6

1. *'X' = pin is present; '-' = pin is absent*

Table 6. Pinout summary for STM32H523/H533 devices

Pin name(1)	WLCSP39	UFQFPN48	LQFP48	LQFP64	UFBGA100	LQFP100	UFBGA144	LQFP144
Specific I/Os								
PC14-OSC32_IN	x	x	x	x	x	x	x	x
PC15-OSC32_OUT	x	x	x	x	x	x	x	x
PH0-OSC_IN	x	x	x	x	x	x	x	x
PH1-OSC_OUT	x	x	x	x	x	x	x	x
System pins								
NRST	x	x	x	x	x	x	x	x
BOOT0	x	x	x	x	x	x	x	x
Power pins								
VDDA	x	x	x	x	x	x	x	x
VSSA	x	x	x	x	x	x	x	x
VDDIO2	-	-	-	-	x	-	x	x
VDDUSB	-	-	-	-	x	x	x	x
VCAP	2	2	2	2	2	2	2	2
VBAT	x	x	x	x	x	x	x	x
VREF+	-	-	-	-	x	x	x	x
VREF-	-	-	-	-	-	-	x	-
Number of VDD	3	3	3	4	5	5	7	11
Number of VSS	3	3	3	4	5	5	12	11

1. *'X' = pin is present; '-' = pin is absent*

Table 7. Pinout summary for STM32H503 devices

Pin name(1)	LQFP64	LQFP48	UFQFPN48	UFQFPN32	WLCSP25
Specific I/Os					
PC14-OSC32_IN	X	X	X	X	X
PC15-OSC32_OUT	X	X	X	X	X
PH0-OSC_IN	X	X	X	-	-
PH1-OSC_OUT	X	X	X	-	-
System pins					
NRST	X	X	X	X	X
BOOT0	X	X	X	X	X
Power pins					
VDDA	X	X	X	X	X(2)
VSSA	X	X	X	X(3)	X(4)
VDDIO2	-	-	-	-	X
VCAP	X	X	X	X	X
VBAT	X	X	X	-	-
Number of VDD	4	3	3	2	1
Number of VSS	4	3	3	1(5)	1

1. *'X' = pin is present; '-' = pin is absent.*
2. *VDDA is connected with VDD on same ball.*
3. *VSSA and VSS are connected and available on exposed pad.*
4. *VSSA is connected with VSS on same ball.*
5. *VSS connected to exposed pad.*

5 Boot configuration

5.1 Boot mode selection

The STM32H562/H563/H573 devices embed the SBS peripheral that controls key boot and security features.

The main boot control actions are listed below:

- Run the product with or without TrustZone® enabled.
- Select between ST-iROT or OEM-iROT.
- Boot when launching a debug authentication sequence.
- Select boot between the Bootloader or the user flash memory boot/
- Initialize the HDPL boot value.

For STM32H503 devices, at startup, a BOOT0 pin and NSBOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
  - Bootloader
  - Debug authentication library (ST-DA)

When boot from user flash memory is selected, the boot address is defined by NSBOOTADD. This address can be locked thanks to NSBOOT_LOCK.

5.1.1 Boot configuration for STM32H523/H533/H562/H563/H573 devices

For STM32H562/H563/H573 devices, the boot configurations are selected considering the product settings:

- BOOT0: to select booting on user flash memory or RSS (root secure services)
- BOOT_UBE option byte to select the iROT between ST-iROT and OEM-iROT
- TZEN option byte to activate/deactivate the Trust Zone
- sbs_boot_addresses: list of addresses defined by the flash memory:
  - NSBOOTADD: non-secure boot address
  - SECBOOTADD: secure boot address
- PRODUCT_STATE: option byte to activate the different security mechanisms depending on the product use.
- sbs_dbg_req: used to launch the debug authentication protocol when booting

For STM32H562/H563/H573 devices, the boot control logic sets the following data:

- sbs_init_vtor_s: vector address for Cortex-M33 secure entry point
- sbs_init_vtor_ns: vector address for Cortex-M33 non-secure entry point
- sbs_tz_state (secure/non-secure): Informs the Cortex-M33 on the secure state of the core
- HDPL: a monotonic counter incremented during the boot stages

Table 8. STM32H533/H573 Boot mode when TrustZone is disabled (TZEN=0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NA(1)	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning	X	NA	NA	RSS	RSS
Provisioned, Closed, Locked	X	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

1. *NA = Not available.*

Table 9. STM32H533/H573 Boot mode when TrustZone is enabled (TZEN=0xB4)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPT SR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	X	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	0xB4	NA(1)	Bootloader	Bootloader
	1	0xC3	NA	ST-iROT	ST-iROT
Provisioning	X	NA	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	X	0xC3	ST-iROT	ST-iROT	ST-iROT
	X	0xB4	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

1. *NA = Not available.*

Table 10. STM32H523/H563 Boot mode when TrustZone is disabled (TZEN=0xC3)

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA(1)	Bootloader	Bootloader
Provisioning	X	NA	RSS	RSS
Provisioned, Closed, Locked	X	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

1. *NA = Not available.*

Table 11. STM32H523/H563 Boot mode when TrustZone is enabled (TZEN=0xB4)

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	NA(1)	Bootloader	Bootloader
Provisioning	X	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	X	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

1. *NA = Not available.*

5.1.2 Boot configuration for STM32H503 devices

For STM32H503 devices, the boot configurations are selected considering the product settings.

At startup, a BOOT0 pin and NSBOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
  - Bootloader
  - Debug authentication library (ST-DA)

Table 12. Boot modes for STM32H503 devices

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	Bootloader	Bootloader
Provisioned, closed, locked	x	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

5.2 System bootloader

The system bootloader is located in the system memory, programmed by ST during the production. It is used to reprogram the flash memory using one of the following serial interfaces.

Table 13. STM32H523/H533/H562/H563/H573 and STM32H503 devices bootloader communication peripherals

System bootloader peripherals	STM32H523/H533 devices I/O pin	STM32H562/H563/H573 series I/O pin	STM32H503 series I/O pin
DFU	PA11/PA12		
USART1	PA10/PA9		
USART2	PA3/PA2		PA15/PA5
USART3	PD9/PD8(1)	PD9/PD8(1)	PA3/PA4
FDCAN(2)	PB5/PB13		PB5/PB15
I2C1	PB8/PB9(3)	NA	NA
I2C2	NA	NA	PB3/PB4
I2C3	PA8/PC9(4)	PA8/PC9	NA
I2C4	NA	PD12/PD13	NA
I3C1	PB6(5)/PB7	PB6/PB7	PB6/PB7
SPI1	PA7/PA6/PA5/PA4		PA7/PA0/PA8/PB8
SPI2	PC1(6)/PB14/PB10/ PB12	PC1/PB14/PB10/ PB12	PB1/PB14/PB10/PB12
SPI3	PC12/PC11/PC10/PA15(3)		PC12/PC11/PC10/PD2

1. *Only for LQFP100, LQFP144, UFBGA144 and UFBGA100*
2. *On STM32H5xx devices, FDCAN bootloader does not use an external quartz, and uses instead HSI and PLL*
3. *Not available for LQFP48, UFQFN48, WLCSP39*
4. *PC9 is replaced by PB4 on LQFP48, UFQFN48 and WLCSP39*
5. *PB6 is replaced by PB8 on LQFP48, UFQFN48 and WLCSP39*
6. *PC1 is replaced by PB15 on LQFP48, UFQFN48 and WLCSP39*

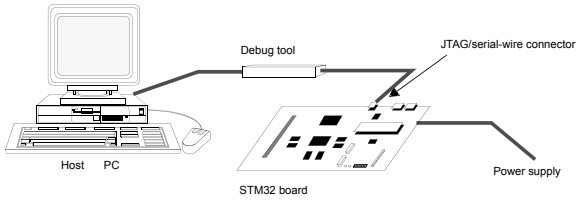
For more details refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

6 Debug management

The Host/Target interface is the hardware equipment that connects the host to the application board. This interface is made of three components, a hardware debug tool, a JTAG or a serial-wire connector and a cable connecting the host to the debug tool.

The figure below shows the connection of the host to a development board.

Figure 10. Host-to-board connection



6.1 SWJ-DP (serial-wire and JTAG debug port)

The core of the STM32H5 microcontrollers integrates the serial wire / JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port that combines a 5-pin JTAG-DP interface and a 2-pin SW-DP interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

Note: All SWJ port IOs can be reconfigured to other functions by software, but debugging is no longer possible. All SWJ port IOs can be reconfigured to other functions by software, but debugging is no longer possible.

For more details on the SWJ debug port, refer to the reference manual of the product.

The NRST pin is needed to run debug authentication.

6.2 Pinout and debug port pins

The devices are available in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

6.2.1 SWJ-DP pins

Five pins are used as outputs for the SWJ-DP, as alternate functions of the GPIOs (general-purpose I/Os). These pins are available on all packages and detailed in the table below.

Table 14. JTAG/Serial-wire debug port pins

Pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Description	
JTMS/SWDIO	Input	JTAG test mode select	Input/Output	Serial-wire data in/out	PA13
JTCK/SWCLK	Input	JTAG test clock	Input	Serial-wire clock	PA14
JTDI (1)	Input	JTAG test data input	-	-	PA15
JTDO	Ouput	JTAG test data output	-	-	PB3
nJTRST	Input	JTAG test reset	-	-	PB4

1. *TDI is hosted on the same IO as a USBPD-CC line. To avoid pull-up/down conflict, a user option can help to decide whether the pad is used as TDI or as CC.*

6.2.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins that are immediately usable by the debugger host.

Note: The trace outputs are not assigned except if explicitly programmed by the debugger host.

The table below shows the different possibilities for releasing some pins

Table 15. SWJ-DP I/O pin availability

Available debug ports	SWJ-DP I/O pin assigned				
	PA13 /JTMS/ SWDIO	PA14 /JTCK/ SWCLK	PA15 /JTDI	PB3 /JTDO	PB4/nJTRST
Full SWJ-DP (JTAG-DP + SW-DP) Reset state	x	x	x	x	x
Full SWJ-DP (JTAG-DP + SW-DP) but without JNTRST	x	x	x	x	-
JTAG-DP disabled and SW-DP enabled	x	x	-		
JTAG-DP disabled and SW-DP disabled	Released				

6.2.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must not be floating since they are directly connected to flip-flops that control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the devices embed the following internal resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes the control again, and the software can then use these I/Os as standard GPIOs. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

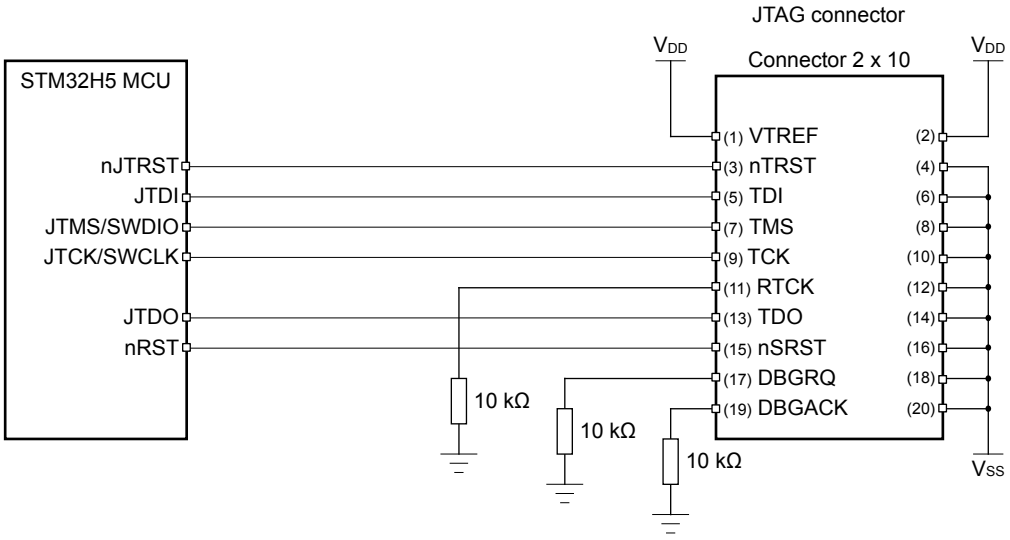
- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

Note: The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST, but there is no special recommendation for TCK. However, for the devices, an integrated pull-down resistor is used for JTCK. Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.2.4 SWJ-DP connection with standard JTAG connector

The figure below shows the connection between the device and a standard JTAG connector.

Figure 11. JTAG connector implementation



6.3 Serial wire debug (SWD) pin assignment

The same SWD pin assignment, detailed in the table below, is available on all packages.

Table 16. SWD port pins

SWD pin	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	Input/Output	Serial-wire data input/output	PA13
SWCLK	Input	Serial-wire clock	PA14

6.3.1 SWD pin assignment

After reset, the pins used for the SWD are assigned as dedicated pins that can be immediately used by the debugger host. However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for GPIO use.

For more details on how to disable SWD port, refer to the section 'I/O pin alternate function multiplexer and mapping section of the reference manual.

6.3.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of it. The reset states of the GPIO control registers put the I/Os in the equivalent states:

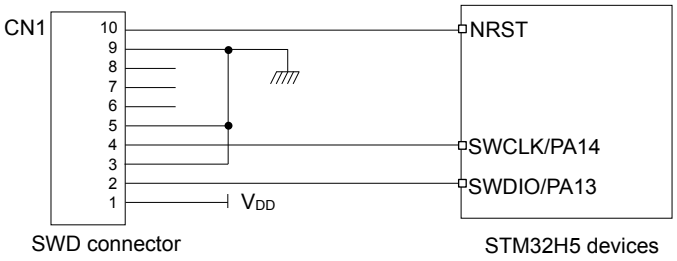
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

The embedded pull-up and pull-down resistors remove the need to add external resistors.

6.3.3 SWD port connection with standard SWD connector

The figure below shows the connection between the device and a standard SWD connector.

Figure 12. SWD connector implementation



7 Recommendations

7.1 PCB (printed circuit board)

For technical reasons, it is best to use a multilayer printed circuit board PCB, with a separate layer dedicated to the ground (V_{SS}) and another dedicated to the V_{DD} supply.

This provides both good decoupling and good shielding effect. For many applications, cost reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for the ground and the power supply.

7.2 Component position

A preliminary layout of the PCB must separate circuits into different blocks:

- high-current circuits
- low-voltage circuits
- digital component circuits
- circuits separated according to their EMI contribution, in order to reduce noise due to cross-coupling on the PBC.

7.3 Ground and power supply

The following rules related to grounding must be respected:

- Ground every block (noisy, low-level sensitive, digital or others) individually.
- Return all grounds to a single point.
- Avoid loops or ensure they have a minimum area.

In order to improve analog performance, the user must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device.

The power supplies must be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

7.4 Decoupling

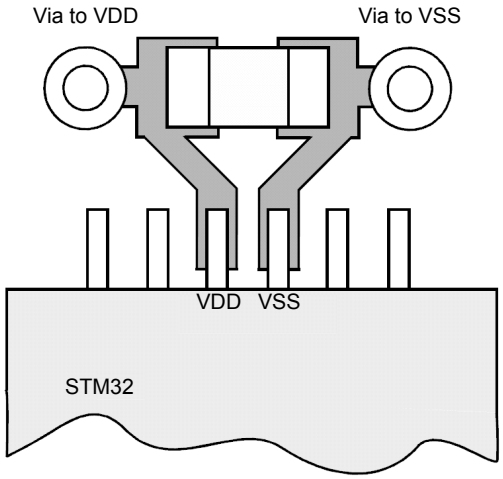
All power-supply and ground pins must be properly connected to the power supplies. These connections (including pads, tracks and vias) must have the lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power-supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and one single ceramic capacitor (minimum 4.7 µF) connected in parallel.

Some package use a common VSS for several VDD instead of a pair of power pins (one VSS for each VDD), in that case the capacitors must be between each VDD and the common VSS. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application requirements.

The figure below shows the typical layout of such a VDD/VSS pair.

Figure 13. Typical layout for VDD/VSS pin pair



7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands).
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example, clock)
- Sensitive signals (example: high impedance)

7.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase the EMC performance and avoid extra power consumption, the unused features of the device must be disabled and disconnected from the clock tree, as follows:

- The unused clock source must be disabled.
- The unused I/Os must not be left floating.
- The unused I/O pins must be configured as analog input by software, and must be connected to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down, or configured as output mode using software.

8 Reference design

8.1 Description

The reference design shown in the following figures is based on The STM32H573I-DK Discovery board, the NUCLEO-H563ZI and the NUCLEO-H503 in UFBGA176+25 SMPS, LQFP144 and LQFP64 packages, respectively .

This reference design can be tailored to any STM32H503, STM32H523/33 and STM32H562/63/73 device with a different package, using the pin correspondence given in Section 8.2.

Clock

Two clock sources are used for the MCU:

- LSE: X1– 32.768 kHz crystal for the embedded RTC
- HSE: X2– crystal for the MCU

See Section 3 for more details.

Reset

The reset signal is active low in the reference design figures shown in Section 8.2.

The reset sources include:

- the reset button (B1)
- debugging tools via the connector CN1

See Section 2.4 for more details.

Boot mode

The user can add a switch on the board to change the boot option.

See Section 5 for more details.

Note: When waking up from Standby mode, the BOOT pin is sampled, and the user must pay attention to its value.

SWD interface

The reference design shows the connection between the devices and a standard SWD connector.

See Section 6 for more details.

Note: It is recommended to connect the RESET pins, so as to be able to reset the application from the tools and also to run debug authentication for debug opening.

Power supply

See Section 2 for more details.

8.2 Component references

The following tables listThe following table lists the components in the STM32H5 Nucleo-64 boards (reference design MB1814). The STM32H5 Nucleo-144 boards (reference design MB1404) and the STM32H5 Discovery boards (reference design MB1677).

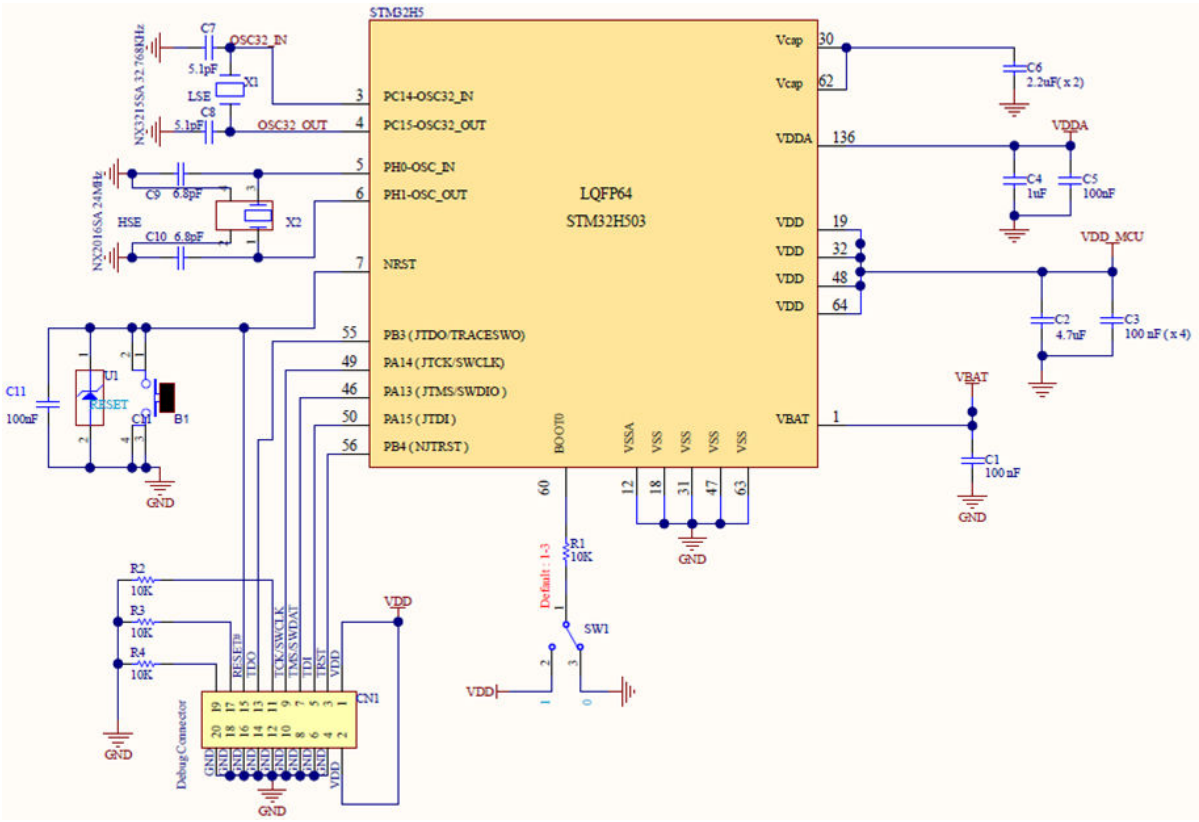
The components list is based on:

- STM32H503 device (see Figure 14)
- STM32H563 device, without SMPS (see Figure 15)
- STM32H573 device, with SMPS (see Figure 16)

Table 17. Components of STM32H5 Nucleo-64 boards

Reference	Type	Value	Quantity	Comments
B1	Push-button	-	1	-
C4	Tantalum or ceramic capacitor	1 µF	1	Decoupling capacitor
C2	Tantalum or ceramic capacitor	4.7 µF	1	Decoupling capacitor required for the package
C1	Ceramic capacitor	100 nF	7	For each external power pin
C3(x4), C5, C11				
C6(x2)	Tantalum or ceramic capacitor	2.2 µF	2	Required by the internal LDO regulator
C7, C8		5.1 pF	2	Used for LSE, HSE: values depend on crystal characteristics
C9, C10		6.8 pF	2	
X1	Quartz	32.768 kHz	1	Used for LSE
X2		24 MHz	1	Used for HSE
R1	Resistor	10 kΩ	1	Maintains BOOT0 pin at a logic low or high level
R2, R3, R4			3	Used for the ST-LINK interface
SW1	Switch	-	1	Used to select the right boot mode

Figure 14. STM32H503 reference design

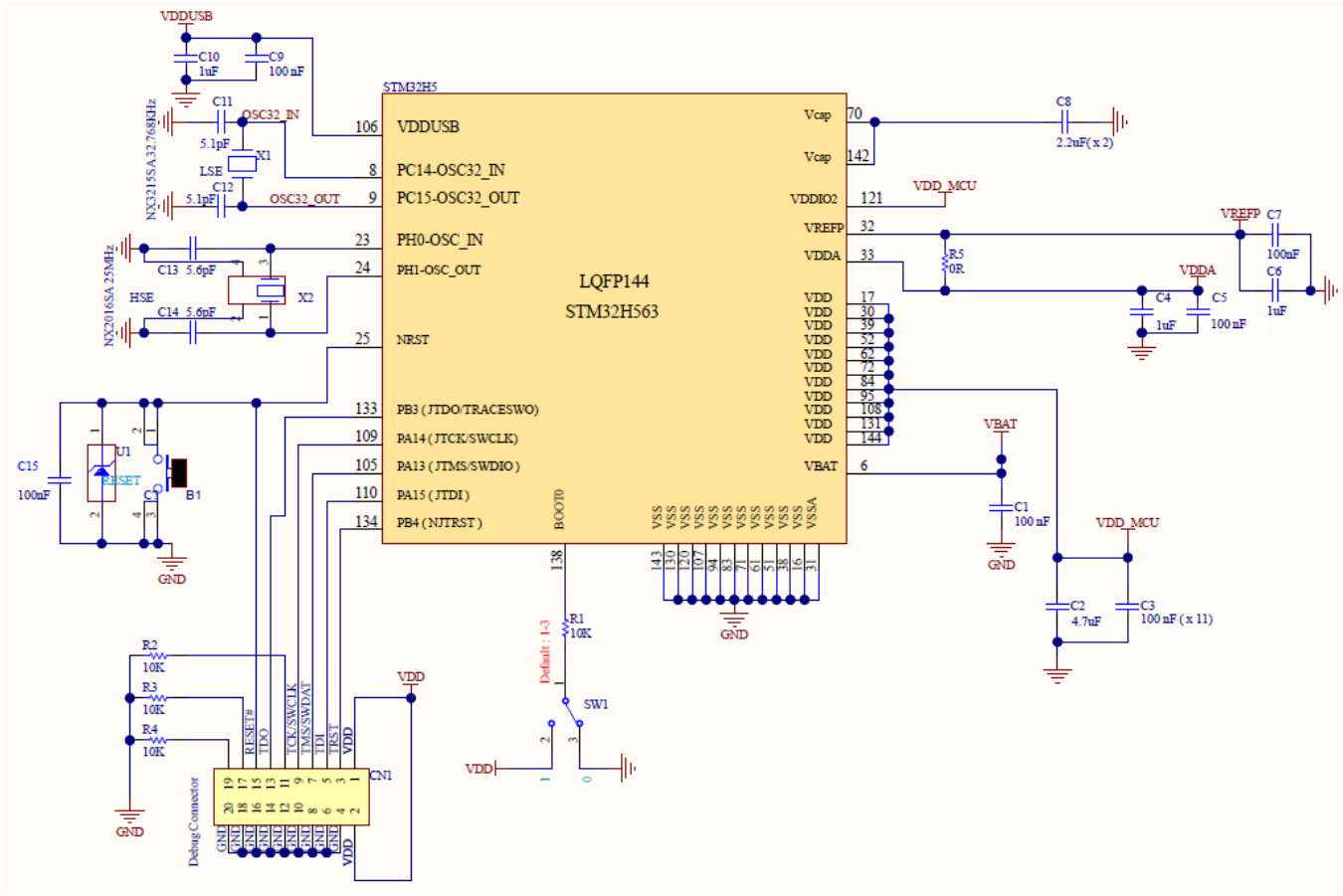


Note: It is recommended to connect the two VCAP pins together.
If there are two VCAP pins (such as for the LQFP64 package), each pin must be connected to a 2.2µF (typical) capacitor (for a total approximately 4.4 µF).
If only one VCAP pin is available, it must be connected to a 4.7 µF capacitor.

Table 18. Components of STM32H5 Nucleo-144 boards

Reference	Type	Value	Quantity	Comments
B1	Push-button	-	1	-
C4, C6	Tantalum or ceramic capacitor	1 µF	2	Decoupling capacitor
C2	Tantalum or ceramic capacitor	4.7 µF	1	Decoupling capacitor required for the package
C1	Ceramic capacitor	100 nF	15	For each external power pin
C3(x11), C5, C7, C15				
C9				
C10	Tantalum or ceramic capacitor	1 µF		
C8(x2)	Tantalum or ceramic capacitor	2.2 µF	2	Required by the internal LDO regulator
C11, C12		5.1 pF	2	Used for LSE, HSE: values depend on crystal characteristics
C13, C14		5.6 pF	2	
X1	Quartz	32.768 kHz	1	Used for LSE
X2		25 MHz	1	Used for HSE
R1	Resistor	10 kΩ	1	Maintains BOOT0 pin at a logic low or high level
R2, R3, R4			3	Used for the ST-LINK interface
R5		0 Ω	1	Optionality mounted if VDDA is connected to VREFP
SW1	Switch	-	1	Used to select the right boot mode

Figure 15. STM32H523/H56x reference design (LDO example)

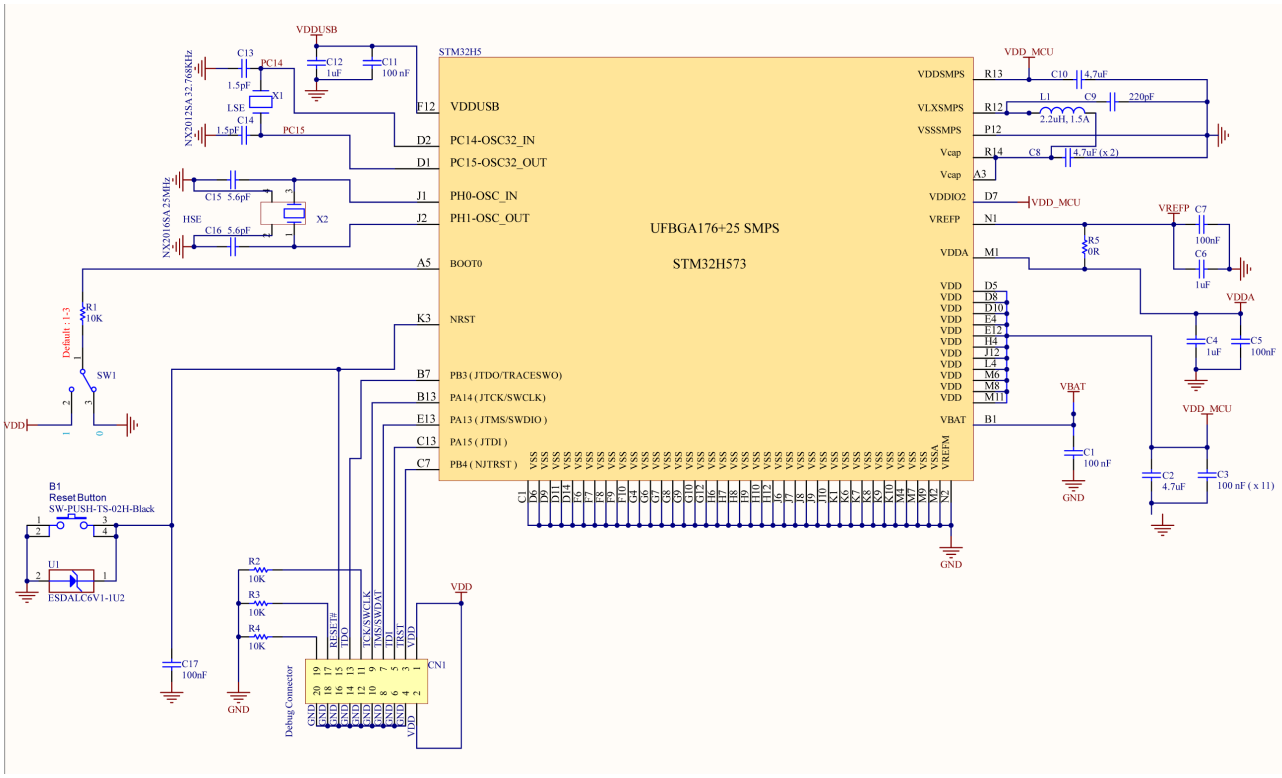


Note: It is recommended to connect the two VCAP pins together.

Table 19. Components of STM32H5 Discovery boards

Reference	Type	Value	Quantity	Comments
B1	Push-button	-	1	-
C4, C6	Tantalum or ceramic capacitor	1 µF	2	Decoupling capacitor
C2	Tantalum or ceramic capacitor	4.7 µF	1	Decoupling capacitor required for the package
C1	Ceramic capacitor	100 nF	17	For each external power pin
C3(x11), C5, C7, C17				
C11				
C12	Tantalum or ceramic capacitor	1 µF		
C8(x2)	Tantalum or ceramic capacitor	4.7 µF	2	Required on each VCAP pin of packages with SMPS
C9		220 pF	1	Required on VLXSMPS pin of packages with SMPS
C10		4.7 µF	1	Required by the internal SMPS regulator
C13, C14		1.5 pF	2	Used for LSE, HSE: values depend on crystal characteristics
C15, C16		5.6 pF	2	
X1	Quartz	32.768 kHz	1	Used for LSE
X2		25 MHz	1	Used for HSE
L1	Coil	2.2 µH	1	Required for SMPS packages on VLXSMPS pin
R1	Resistor	10 kΩ	1	Maintains BOOT0 pin at a logic low or high level
R2, R3, R4			3	Used for the ST-LINK interface
R5		0Ω	1	Optionally mounted if VDDA is connected to VREFP
SW1	Switch	-	1	Used to select the right boot mode

Figure 16. STM32H573 reference design (SMPS example)



Note: It is recommended to connect the two VCAP pins together.

It is recommended to use a large plane VCAP and connect the SMPS pin to the VCAP plane with a large wire (as the total power is flowing through this wire). Then, put the 100nF ceramic capacitor on each VCAP (as close as possible to the VCAP ball) and add the 4.7uF on each VCAP ball.

9 PCB routing guidelines for STM32H5xx devices

9.1 PCB stack-up

In order to reduce the reflections on high-speed signals, it is necessary to match the impedance between the source, sink, and transmission lines. The impedance of a signal trace depends on its geometry and its position with respect to any reference planes. The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized. The minimum configuration that can be used is 4 or 6 layers stack-up. An 8 layers boards may be required for a very dense PCBs that have multiple SDRAM/ SRAM/NOR/LCD components.

The following stack-ups are intended as examples as a starting point for helping in a stack-up evaluation and selection. These stack-up configurations are using a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. Therefore, high speed signals on top layer have a solid GND reference plane which helps to reduce the EMC emissions, as going up in number of layers and having a GND reference for each PCB signal layer further improves the radiated EMC performance.

Figure 17. Four layer PCB stack-up example

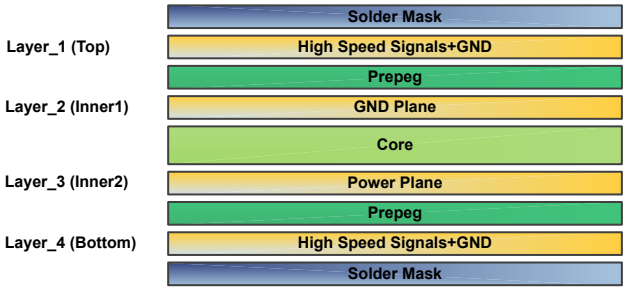
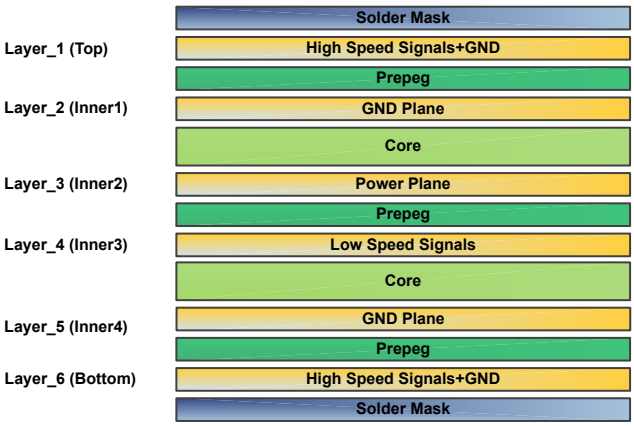


Figure 18. Six layer PCB stack-up example



9.2 Crystal oscillator

Use the application note: Oscillator design guide for STM8S, STM8A and STM32 microcontrollers (AN2867), for further guidance on how to layout and route crystal oscillator circuits.

9.3 Power supply decoupling

An adequate power decoupling for STM32H5xx devices is necessary to prevent an excessive power noise and ground bounce noise. Refer to Section 2.2: Power supply schemes.

The follow the recommendations:

- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU. For BGA packages, it is recommended to place the decoupling capacitors on the other side of the PCB (see Figure 19).
- Add the recommended decoupling capacitors for as many VDD/GND pairs as possible.
- Connect the decoupling capacitor pad to the power and ground plane with a wider, short trace/via. This allows reducing the series inductance, maximizing the current flow and minimizing the transient voltage drops from the power plane which also reduces the possibility of ground bounce.

Figure 20 shows an example of decoupling capacitor placement underneath STM32 devices, closer to the pins and with fewer vias.

Figure 19. Decoupling capacitor placement depending on package type

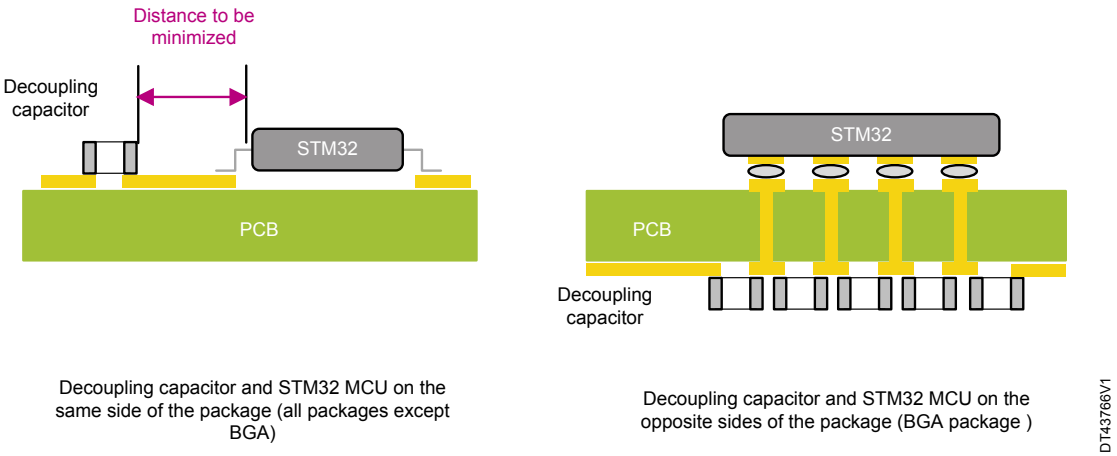
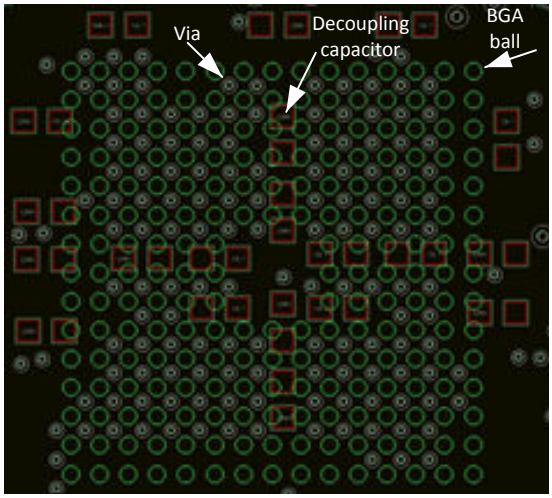


Figure 20. Example of decoupling capacitor placed underneath the STM32 device



9.4 High speed signal layout

9.4.1 SDMMC bus interface

Interface connectivity

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the AHB peripheral bus and Multi Media cards (MMCs), SD memory cards and SDIO cards. The SDMMC interface is a serial data bus interface, that consists of a clock (CK), command signal (CMD) and 8 data lines (D[0:7]).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf switching cap between PWR and GND).
- Trace the impedance: 50 Ω ± 10%
- The skew being introduced into the clock system by unequal trace lengths and loads, minimize the board skew, keep the trace lengths equal between the data and clock.
- The maximum skew between data and clock should be below 250 ps @ 10mm.
- The maximum trace length should be below 120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used.
- The trace capacitance should not exceed 20 pF at 3.3 V and 15 pF at 1.8 V.
- The maximum signal trace inductance should be less than 16 nH.
- Use the recommended pull-up resistance for CMD and data signals to prevent bus floating.
- The mismatch within data bus, data, and CK or CK and CMD should be below 10mm.
- Keep the same number of vias between the data signals.

Note: The total capacitance of the SD memory card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line. The total bus capacitance is $C_L = C_{Host} + C_{Bus} + N*C_{Card}$ where the host is an STM32H5xx device, bus is all the signals and Card is SD card.

9.4.2 Flexible memory controller (FMC) interface

Interface connectivity

The FMC controller and in particular SDRAM memory controller which has many signals, most of them have a similar functionality and work together. The controller I/O signals could be split in four groups as follows:

- An address group which consists of row/column address and bank address
- A command group which includes the row address strobe (NRAS), the column address strobe (NCAS), and the write enable (SDWE)
- A control group which includes a chip select bank1 and bank2 (SDNE0/1), a clock enable bank1 and bank2 (SDCKE0/1), and an output byte mask for the write access (DQM)
- A data group/lane which contains 8 signals: the eight D (D7–D0) and the data mask (DQM)

Note: It depends on the used memory: SDRAM with x8 bus widths have only one data group, while x16 bus-width SDRAM has two lanes

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50 Ω ± 10%
- The maximum trace length should be below 120mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Reduce the crosstalk, place data tracks on the different layers from the address and control lanes, if possible. However, when the data and address/control tracks coexist on the same layer they must be isolated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to diminish the skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least 3x of the trace away from others signals. Use as less vias as possible to avoid impedance change and reflection. Avoid using serpentine routing.
- Match the clock traces to the data/address group traces within ±10mm.
- Match the clock traces to each signal trace in the address and command groups to within ±10mm (with maximum of <= 20 mm).
- Trace the capacitances:
  - At 3.3 V keep the trace within 20 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 30 pF.
  - At 1.8 V keep the trace within 15 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 20 pF.

9.4.3 Octo-SPI interface (OCTOSPI)

Interface connectivity

The OCTOSPI is a specialized communication interface targeting the regular-command frame format with the command, address, alternate byte, dummy cycles, and data phase and the HyperBus™ protocol with its frame format. OCTOSPI interface consists of a clock (CLK), Inverted clock to support 1.8 V HyperBus protocol (NCLK), a chip select signal (nCS), up to 8 data lines (IO[0:7]) and Data strobe/write mask signal from/to the memory (DQS).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50 Ω ± 10%
- The maximum trace length should be below 120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least 3x of the trace away from other signals. Use as less vias as possible to avoid the impedance change and reflection. Avoid using a serpentine routing.
- Match the trace lengths for the data group within ± 10 mm of each other to diminish skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match the lengths.

9.4.4 Embedded trace macrocell (ETM)

Interface connectivity

The ETM enables the reconstruction of the program execution. The data are traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the data bus of 4 lines D[0:3] and the clock signal CLK.

Interface signals layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND.
- Trace the impedance: 50 Ω ± 10%

- All the data trace should be as short as possible (<=25 mm).
- Trace the lines which should run on the same layer with a solid ground plane underneath it without a via.
- Trace the clock which should have only point-to-point connection. Any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible. If longer are required, there should be a possibility to optionally disconnect them (for example, by jumpers).

Revision history

Table 20. **Document revision history**

Date	Version	Changes
27-Mar-2023	1	Initial release.
12-Jul-2023	2	In Section 2.2: Power supply schemes: • Corrected Figure 5. STM32H563/H573 power-supply scheme with SMPS and Figure 6. STM32H523/H533/H562/H563/H573 power-supply scheme with LDO • Added note below the figures.
11-Mar-2024	3	Added: • STM32H523/H533 to devices • Section 9: PCB routing guidelines for STM32H5xx devices Updated: • Section 2.2: Power supply schemes • Section 2.4.5: Bypass mode • Section 4.1: Package summary • Section 4.2: Pinout summary • Section 5.2: System bootloader • Section 8.1: Description • Section 8.2: Component references

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