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Application note

VIPower M0-9 SPI considerations

Introduction

VIPower M0-9 SPI drivers require higher value SPI bus resistors to limit the bus current during negative voltages. The higher bus resistance can limit the bus frequency. The minimum resistor values are dependent on the bus configuration. The slowest path in the bus defines the maximum safe bus frequency.

This application note explains why there is a need for the larger value bus resistors, outlines how to calculate the bus resistor values and estimates the resulting maximum bus frequency.

1 Functionality

ST-SPI is a standard serial communications protocol used to provide communications between a microcontroller and a peripheral IC within a module. The standard SPI bus consists of 4 lines:

- CSN (chip select not)
- SDI (serial data in) to the satellite device
- SDO (serial data out) of the satellite device
- SCK (serial clock)

A standard SPI bus protocol uses the clock edges to synchronize the serial data that is communicated to and from the host - satellite system. The standard SPI bus protocol is very flexible and allows many variations. ST has defined an overall standard that is intended for use in all body function IC's. This specific SPI protocol is called ST-SPI. The M0-9 SPI bus protocol is a subset of ST-SPI.

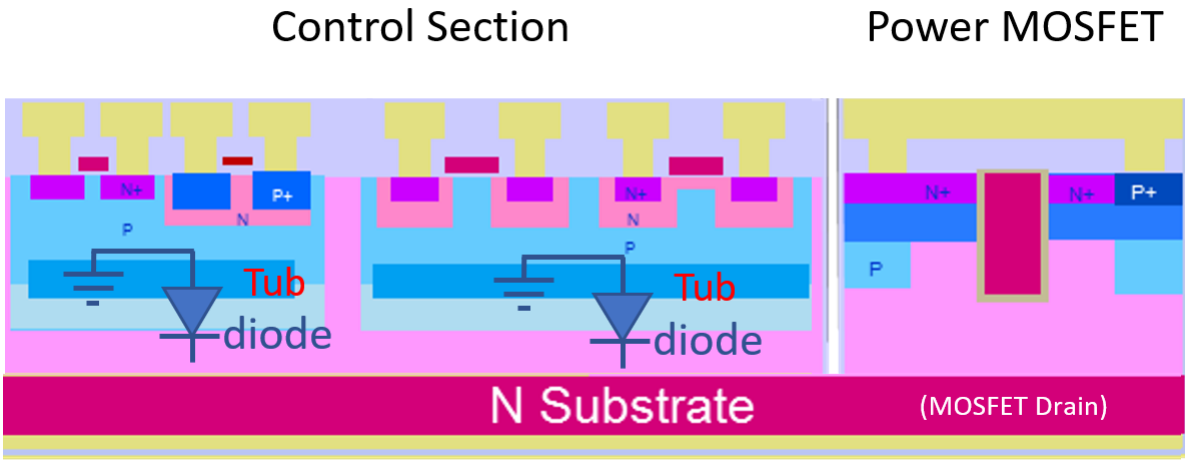
A more detailed description of the ST-SPI protocol can be found in the technical note TN0897.

2 M0-9 protections

2.1 Technology

The M0-9 process is based on a vertical MOSFET process where the drain of the MOSFET is the substrate, or the back of the IC. The back of the IC is connected to the exposed pad on the underside of the package. A VIPower high side driver is essentially a power MOSFET with a control circuit inserted.

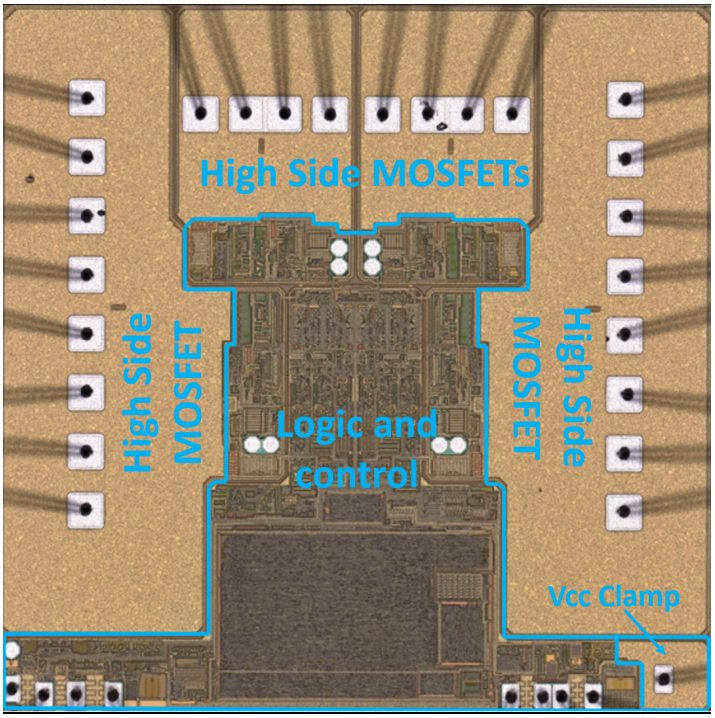
Figure 1. M0-9 simplified cross section



Semiconductor integrated circuits (the control portion) typically have a grounded substrate. This is done to keep all of the parasitic P-N junctions inherent in the integrated process from being forward biased. This means that the control circuit of the VIPower high side drivers resides in a grounded “tub” on the MOSFET drain (see Figure 1).

Because this is a semiconductor, the interface between the grounded tub and the drain is a diode. This diode is reverse biased as long as the drain (the supply) is higher than the grounded tub. When the voltage inverts (supply goes below ground), the drain-tub diode forward biases and current flows. This can be a damaging event unless there is something limiting that current.

Figure 2. **M07 control and power**

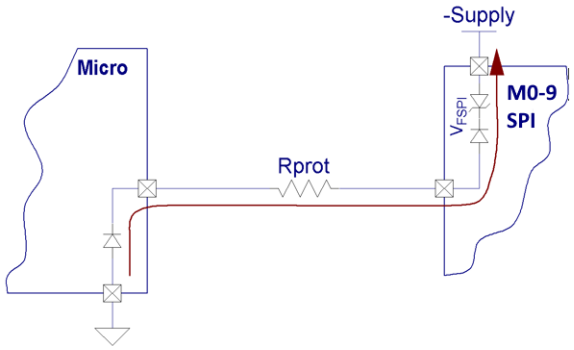


There is also a clamping component between V_{CC} and device ground that clamps low energy spikes that can appear on the supply. This clamping component also has a reverse biased body diode associated with it.

2.2 Current path

The current path during a negative voltage event starts at the ground of the microcontroller through the supply pin of the M0-9 drivers (see Figure 3. Simplified current path during a negative supply voltage). This current must be limited by the SPI bus protection resistors between the Host microcontroller and the M0-9 SPI driver.

Figure 3. Simplified current path during a negative supply voltage



R_{prot} in Figure 3 represents any of the SPI bus protection resistors, RSDO, RSDI, RSCK, or RCSN. There are three considerations:

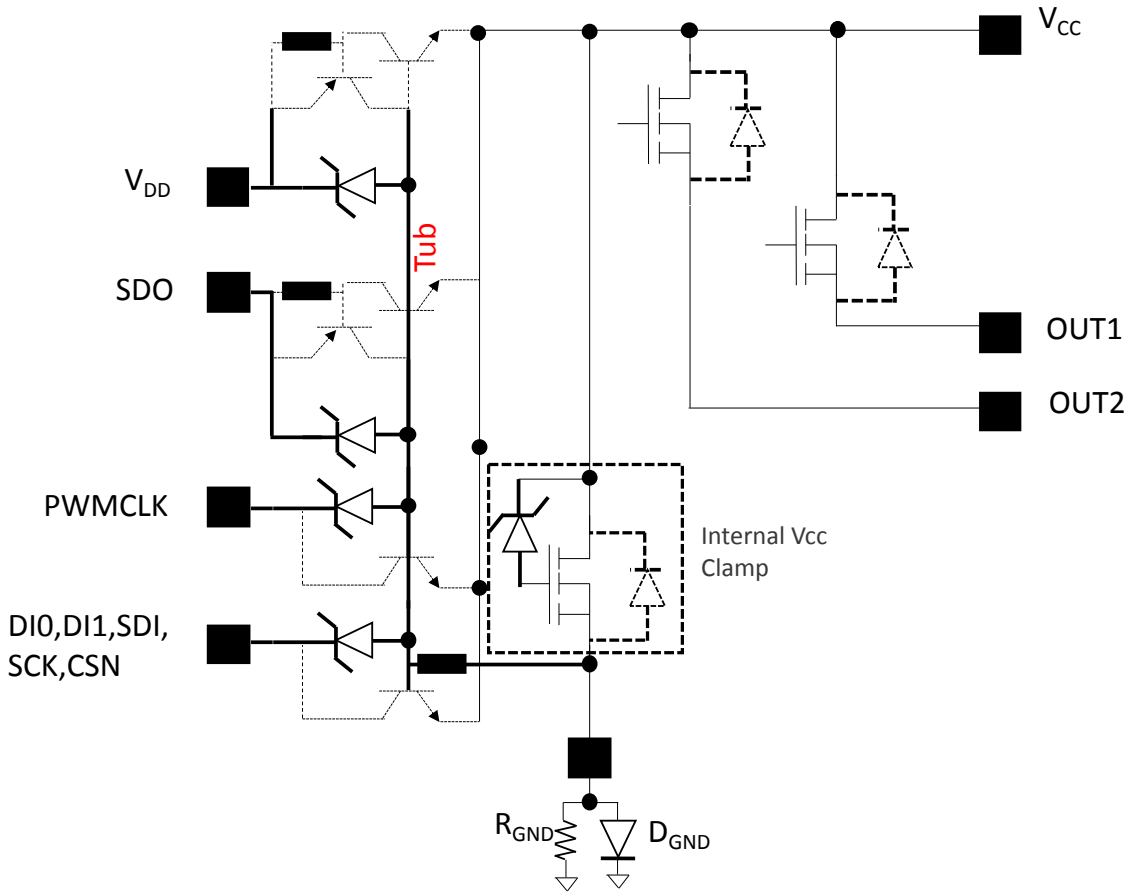
1. RSDI and RSCK are considered together
2. RCSN is separated in that it will always only have one device associated with it and does not greatly affect SPI timing
3. RSDO is considered separately as this node is the most complex to analyze and by far the slowest of the four

2.3 Protection

The effect of having these parasitic components is that the control section cannot handle reverse voltages without some sort of protection. As a result, a ground protection circuit is needed for the control section only.

This comes in the form of a diode-resistor pair from device ground to the circuit board ground (R_{GND} and D_{GND} as shown in the figure below).

Figure 4. M0-9 SPI internal and parasitic components



All of this was discussed to illustrate the need to protect the I/O from negative transients on V_{CC}. With the blocking diode and resistor on the ground pin, any negative transients on the supply is essentially shown up in various degrees on the I/O pins, including V_{DD}. To limit the resulting uncontrolled current through the I/O, limiting or protection resistors are needed for all the I/O pins including V_{DD}. This changes the standard low ohmic SPI resistor to something that more effectively limits damaging transient currents during negative transients. The SPI maximum frequency may be affected as this resistance increases.

3 Calculations for protection resistor values

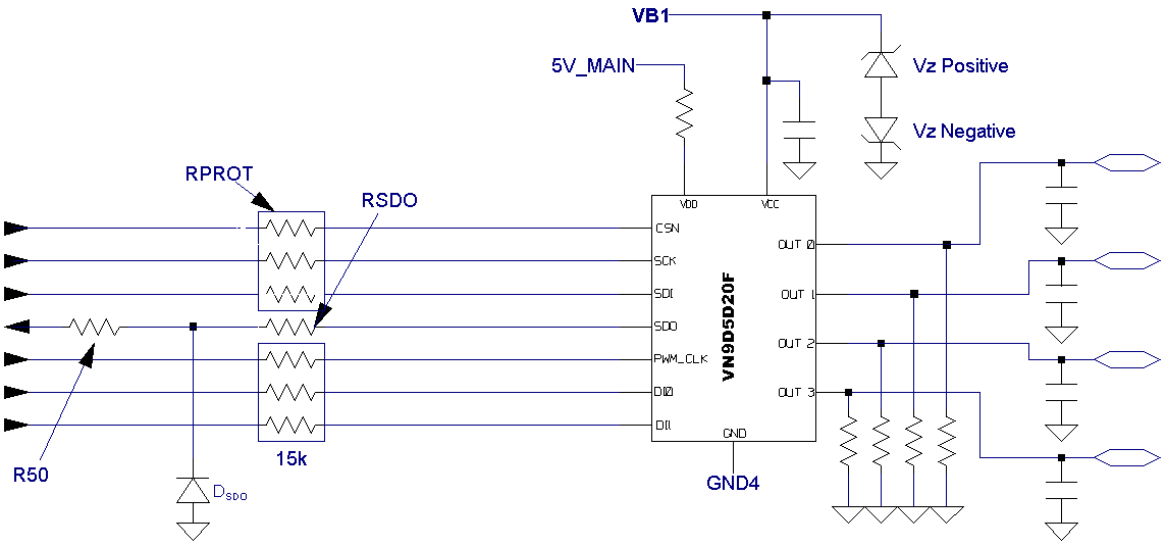
The two bounding parameters that define the limits of the protection resistor values are injection current during the transient, and bus speed. Injection current limitations define the minimum value resistance allowed. This limit can come from the driver or the micro. Bus speed requirements define the upper limit to the resistance value. In some configurations, the minimum resistance can reduce bus speed considerably. As a result, the maximum allowable bus speed may be defined giving the minimum allowable protection resistor.

3.1 Minimum SPI BUS resistor calculations

The first line of defense for negative transients is a clamp on the supply to limit the negative transient. This negative clamp (Vz negative in the figure below) limits the peak negative transient voltages.

The lowest value the SPI bus resistor can be is limited by the maximum current the host micro or the driver can experience when the I/O pin is pulled below ground. The Rprot resistors limit the peak current out of the micro and into the driver when there is a negative transient on V_{CC}.

Figure 5. Single device with protections



The peak of that clamped voltage is then used to determine the minimum protection resistor size.

Equation - Defining the minimum protection resistance

$$R_{prot} = \frac{V_{rev} - V_{FSPI} - V_{Dmicro}}{I_{lim\_SPI}} \quad (1)$$

Where:

- R_{prot} = SPI bus protection resistors referenced in the datasheet as either RCSN, RSCK or RSDI
- V_{rev} = peak negative voltage as defined by the negative voltage clamping in the supply clamping structure (Vz negative + forward voltage of Vz positive)
- V_{FSPI} = the voltage difference from V_S to the I/O pin (V_S - $V_{I/O}$) during reverse voltage (see Table 1)
- I_{lim_SPI} = peak current allowable by the bus. For a single device on the bus that can be either the micro or the driver. The M0-9 driver is limited to the currents referenced in the Table 1. This may be limited by the host micro maximum allowable current
- V_{Dmicro} = the voltage drop across the host micro substrate diode. Typically, this is 0.6 V

Once R_{Prot} is calculated, the next level up 1% resistor is selected such that any tolerance variation does not fall below the above calculated value.

Table 1. SPI pin capability during reverse polarity

PIN	V_{FSPI} (V_S - $V_{I/O}$) during reverse voltage	I_{rev} reverse current capability
SDI	5 V	10 mA
SDO	1 V	100 mA
CSN	5 V	10 mA
SCK	5 V	10 mA

V_{FSPI} and I_{rev} values are different for SDO than the other pins as this is a driver and it is designed to handle more current. As a result the protection resistor for SDO is calculated differently.

The negative transient clamp on the supply (Vz negative, see Figure 5) should be greater in amplitude than the reverse battery requirements for the vehicle. Considering Zener tolerances and resistances, -18 V is about the least the negative clamp can safely be.

Power dissipation during reverse battery conditions should be considered to ensure that the resistor wattage is respected. This is especially true if a lower resistor value is used for the SDO protection resistor. Transients themselves are not typically long enough in duration to be a thermal issue for a resistor. Only reverse battery conditions are then considered. The simple equation for the SPI protection resistors is:

Equation - Protection resistor power calculation

$$R_{prot} = \frac{(V_{rev} - V_{FSPI} - V_{Dmicro})^2}{P_{Rprot}} \quad (2)$$

Where:

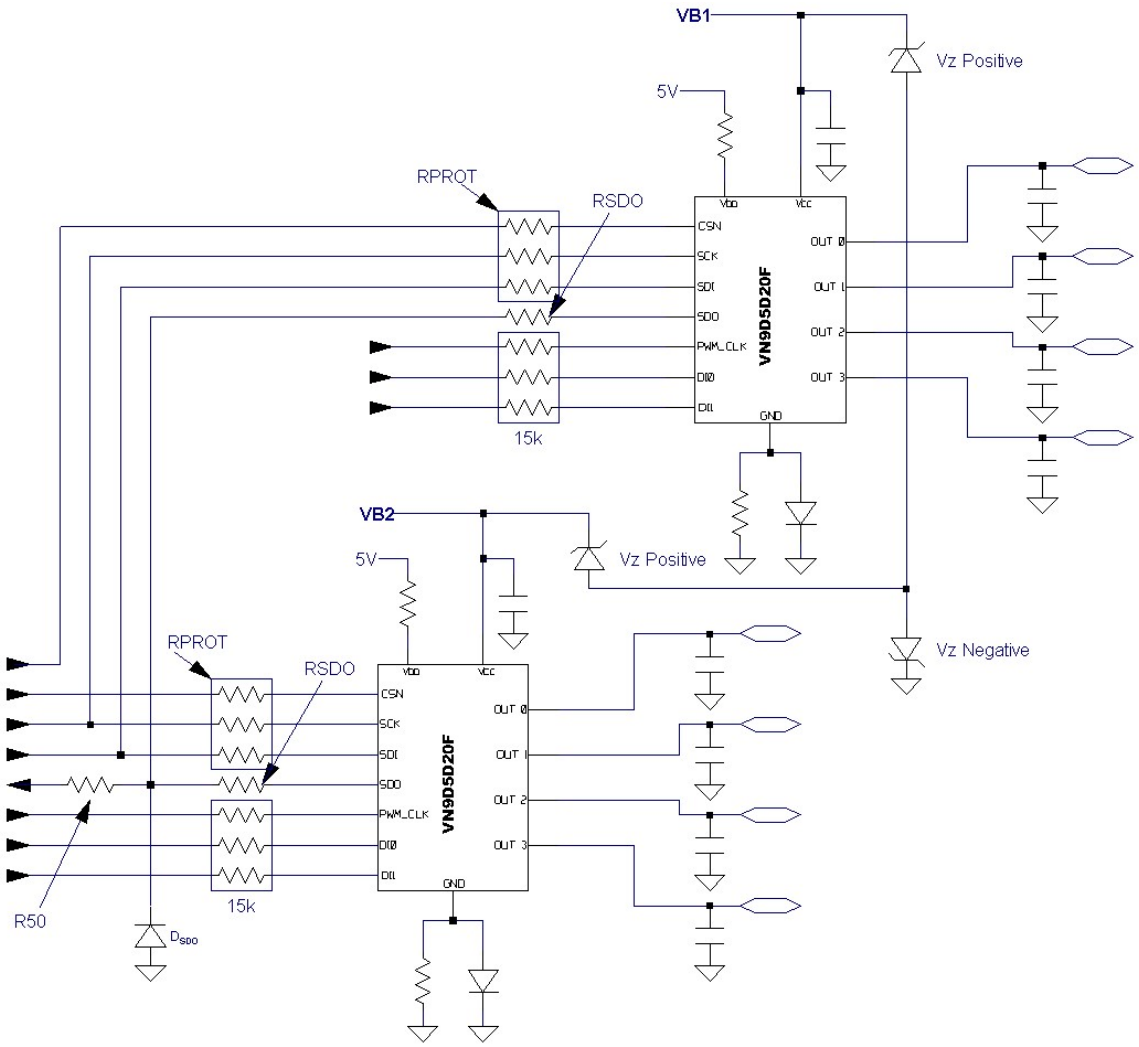
- R_{prot} = SPI bus protection resistors referenced in the datasheet as either RCSN, RSCK, RSDI or RSDO
- V_{rev} = the reverse battery voltage
- V_{FSPI} = (V_S - $V_{I/O}$) during reverse voltage (see Table 1)
- V_{Dmicro} = the voltage drop on the substrate diode in the host micro I/O (typically 0.6 V)

If there are multiple devices on the same SPI bus, this resistor value does not change if they are all on one supply. The current out of the micro is effectively limited by the single resistor regardless of the number of devices on the bus. However, if different M0-9 drivers do not share the same supply or the same ground protection resistor-diode, then the SPI signals need to be separated from each other by some resistance to limit the current. There may be transients on one supply and not on the other.

This is done by adding set of parallel protection resistors for each driver or set of drivers on a supply. Each set of resistors adds a parallel path for current draw out of the host micro during a reverse voltage event. In effect a single SPI bus with devices not sharing the same supply multiplies the protection resistor size by the number of supplies in the system.

The figure below illustrates two devices sharing a single SPI bus where these two devices do not share their supplies (one is VB1 the other is VB2). Because transients do not necessarily couple to both supplies, the I/Os of these devices require separation to limit any currents between them. Therefore, they each have their own set of protection resistors. As a result, each then provides an additional current path from the micro during a reverse voltage condition.

Figure 6. Multiple devices on different supplies

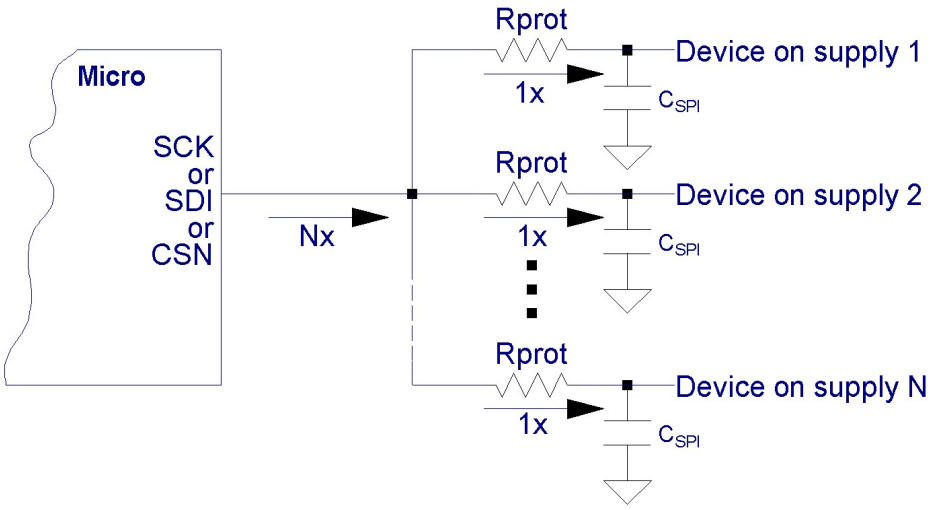


3.1.1 CSN, SCK, SDI protection resistors

The parallel protection resistor values need to increase to limit the peak current out of the host micro during a negative transient. For each additional device on a separate supply, the protection resistor increases by the minimum value as defined by Equation 1. For Figure 6, the protection resistor value would be twice the value calculated as there are two devices not sharing the same power supply.

For N supplies the equivalent circuit looks like the figure below.

Figure 7. SDI, SCK, and CSN configuration



To keep the current in the micro within its limits the equation for the protection resistor size is then proportional to the number of supplies used. This is accounted as in the equation below.

Equation - Protection resistor multiplier

$$R_{prot}(N_S) = N_S \frac{V_{rev} - V_{FSPI} - V_{Dmicro}}{I_{lim\_SPI}} \quad (3)$$

Where:

- N_S = the number of different power supplies used in the array of devices sharing the same SPI bus

The next level up to 1% resistor can be selected to ensure that the resistance does not fall below the calculated value.

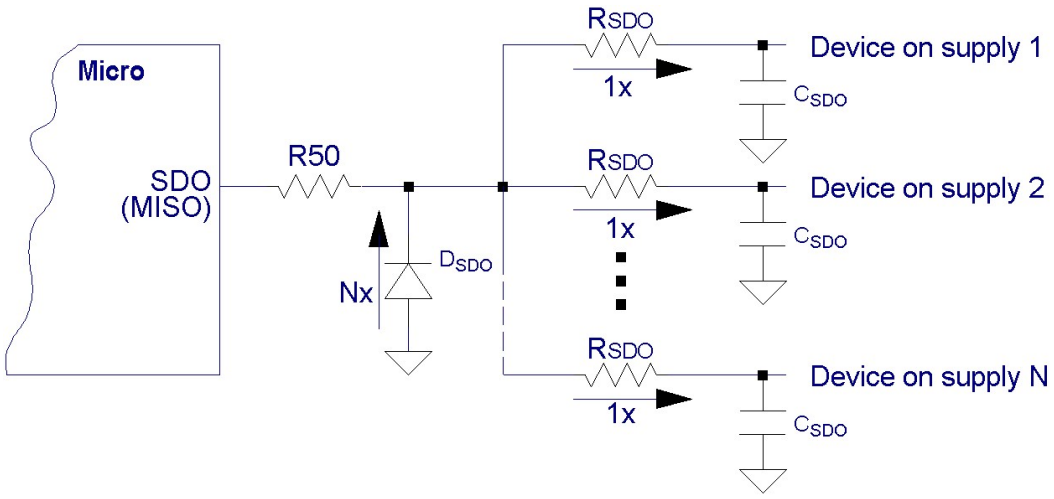
The optimum solution would be to separate the drivers using different supplies so that there is only one supply per SPI bus.

3.1.2 SDO protection resistors

The SDO signal path has a different set of difficulties to overcome. SDI, SCK, and CSN signals are all driven by the micro. As a result, all of the devices receiving these signals are only affected by the capacitances located directly within their nodes (see Figure 7). Each “node” contains the devices that share a common supply.

With the SDO signal, what the micro sees is affected by all of the system capacitances. As a result, the impact of the high resistance SPI bus resistors is much greater. This then requires a different method to keep this effect to a minimum.

Figure 8. SDO configuration



When a device on Supply 1 drives the SDO, the SDO capacitances in all of the other supply “nodes” affect the signal seen at the micro.

Fortunately, we can take advantage of the higher current capability of the SDO pin (see Table 1). Here, because of the addition of the diode D_{SDO} (see Figure 8) we only need to consider the SDO pin current capability of a single M0-9 driver protection resistor formula. The Diode D_{SDO} will shunt any current that the micro would have seen. The addition of R50 (RSDO1 in the datasheet, 50 Ω) limits any microcontroller current due to differences in the diode forward voltages between the micro and D_{SDO}.

Equation - SDO protection resistor calculation

$$R_{SDO} = \frac{V_{rev} - V_{FSDO} - V_{D\_SDO}}{I_{lim\_SDO}} \quad (4)$$

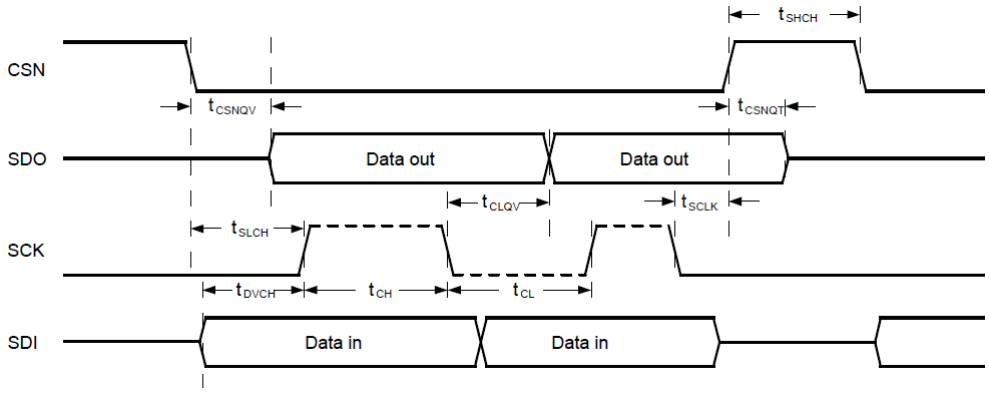
The SDO resistor does not need to be “multiplied” based on the number of supplies as the current is coming from a common point that can handle the higher current, the D_{SDO} diode. Equation 4 above does not take into account the power dissipation this resistor will experience during a reverse battery event, which could be close to 1 W. A compromise can be considered at the cost of SPI bus speed. Use Equation 2 to recalculate the SDO protection resistors based on power dissipation.

A note, some improvement in SPI bus speed can be made by incorporating the SDO diode configuration shown in Figure 8 for SCK and SDI. Using the diode eliminates the resistance multiplier (N_S) shown in Equation 3. For example, a three-supply system has one third the SPI bus resistance and as a result, a considerably faster bus.

3.2 Calculating the maximum SPI bus frequency

Once the minimum protection resistor values are calculated, a calculation can be done to determine the maximum bus frequency. Each SPI pin has different limitations. For instance, any serial clock (SCK) signal delay will allow for more relative delay on the SDI as they are both affected by the similar delays. However, any SCK delay into the driver will add delay to the SDO timing coming from the driver as SDO is predicated on SCK timing at the driver. Adding to that, the clock from the host micro is not aware of any delay on SCK seen at the driver. The limiting factor to bus speed is then a combination of SCK and SDO delay (including internal SCK to SDO valid delays t_{CQLV}).

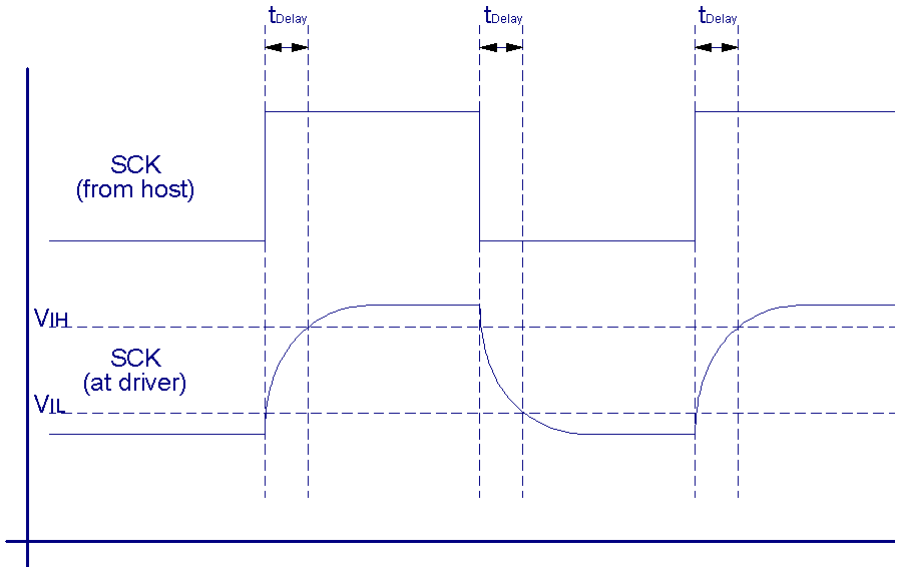
Figure 9. SPI timing diagram



3.2.1 Serial clock delay

Bus capacitance and protection resistance generates an R-C time constant delay that slews the transitions on signals between the host and the driver. We can assume that this slew rate is symmetrical. We can expect the slew rate to be similar for falling edges as it is for rising edges. As a result, to simplify the equations we only consider one side.

Figure 10. SCK slew from R-C time constant



The Equation 5 below defines the falling edge of the SCK signal (the simpler of the two equations). This is for a single device on the SPI bus. Multiple devices contribute to the delay depending on how the bus is configured:

Equation - Defining the SCK falling edge

$$V_{SCK}(t) = V_{DD}e^{\frac{-t}{(R_{prot1\%} + R_{micro})C_{SPI}}} \quad (5)$$

Where:

- $R_{prot1\%}$ is the minimum SPI bus protection resistor as defined by Equation 3 above and then selected from the available 1% resistor values
- R_{micro} is the host micro I/O sink/source resistance. This value may be asymmetrical (the sink resistance does not necessarily equal the source resistance)
- C_{SPI} is the input capacitance at the SCK pin. Any other bus capacitance can be added here as well
- V_{DD} is the SPI bus voltage

Setting $V_{SCK}(t)$ to equal the driver input low threshold (V_{IL}) and solving for $t_{SCKDelay}$ we obtain:

Equation - SCK delay due to bus capacitance

$$t_{SCKdly} = C_{SPI}(R_{prot1\%} + R_{micro})\ln\left(\frac{V_{DD}}{V_{IL}}\right) \quad (6)$$

For multiple drivers on the same supply, the bus input capacitance adds. C_{SPI} then is multiplied by the number of devices (N_D) on the same SPI bus. For every device added (N_D) the delay is increased proportionately. So, the total bus capacitance is the SPI pin input capacitance multiplied by the number of drivers sharing the same protection resistor (N_D x C_{SPI}).

We can also incorporate the effect of using drivers that have different supplies as well.

Equation - Simplified SCK delay

$$t_{SCKdly} = N_D C_{SPI}(R_{prot1\%} + R_{micro})\ln\left(\frac{V_{DD}}{V_{IL}}\right) \quad (7)$$

Where:

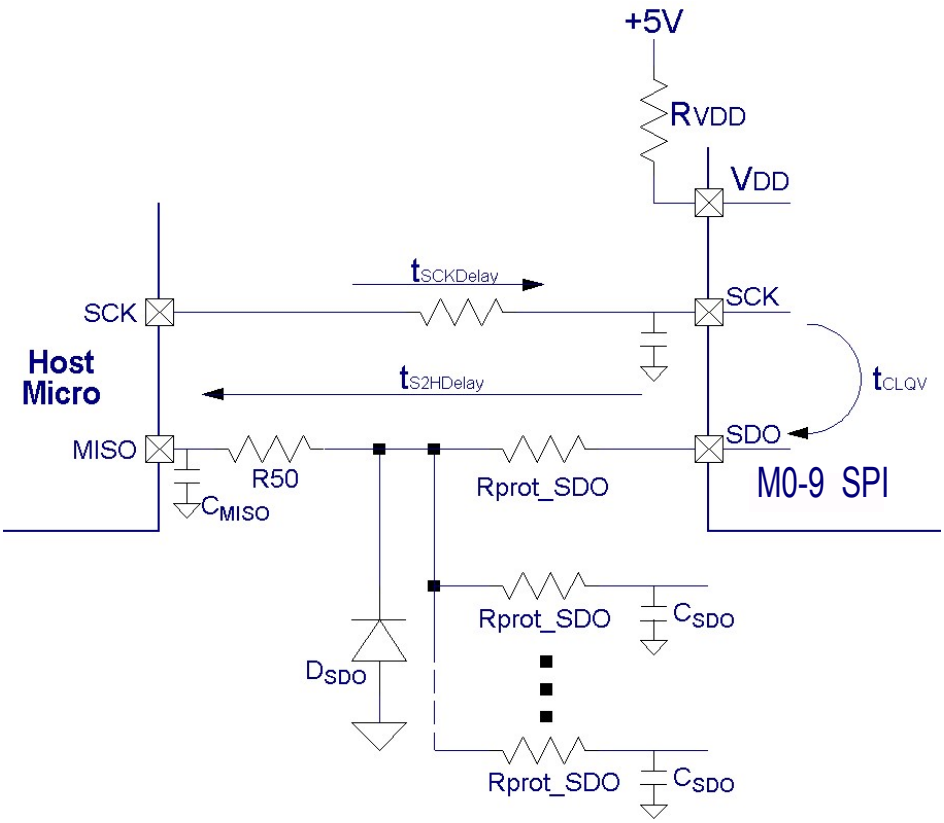
- N_D is the largest number of devices sharing the same supply
- $R_{prot1\%}$ is the minimum SPI bus protection resistor as defined by Equation 3 above and then selected from the available 1% resistor values
- R_{micro} is the host micro I/O sink/source resistance. This value can be asymmetrical (the sink resistance does not necessarily equal the source resistance)
- C_{SPI} is the input capacitance for the SCK pin. Any other bus capacitance can be added here as well
- V_{DD} is the SPI bus voltage
- V_{IL} is the input low threshold at SCK (0.3xV_{DD} for the M0-9 SPI drivers)

3.2.2 SDO delay

The SDO is read by the host micro on the rising edge of SCK. The host micro has only the SCK signal that it produces to synchronize the returning SDO information. As a result, any SDO delay in the system, whether it be created by the R-C time constants of the bus going to or coming from the driver, or internal delays of the driver itself, will affect the timing on SDO that the Host micro sees. The total SDO delay then incudes:

- $t_{SCKDelay}$, SCK to driver delay described in EQ 6 above
- t_{CLQV}, Clock low to SDO output valid delay (see Figure 9)
- $t_{S2HDelay}$, SDO to host delay due to the R-C time constant created by the protection resistor and the bus capacitance between the protection resistor and the host micro

Figure 11. Cumulative SDO to Host delays



The next rising edge of the SCK at the micro will clock-in the SDO data. If the delay to SDO is too long, then the data may be corrupted. This is why it is the slowest path in the system.

Equation - Total SDO delay with respect to the Host micro

$$t_{SDOdly} = t_{SCKdly} + t_{CQLV} + t_{S2Hdly} \quad (8)$$

The SDO protection resistor calculations can be extremely complex depending on the total bus configuration. A few simplifications (assumptions) can be made to reduce its complexity with very little influence on the end result. They are:

- The capacitive loading at the drivers is much higher than what the micro MISO pin provides
- R_{SDO} is much higher than R50
- The voltage at the SDO diode is virtually identical to the voltage seen at the micro MISO pin

The worst-case timing is rise time. During the SDO rise time, the current is coming from V_{DD}. The V_{DD} pin has a protection resistor, R_{VDD}, that adds to the output resistance of the SDO driver (SDO $R_{DS(on)}$ ~200 Ω). ST recommends R_{VDD} to be a 330 Ω, 1/2 W resistor. This makes the total output resistance of the SDO driver, R_{OUT} = 530 Ω.

It is important to note that Equation 9 below ONLY applies to the systems with 2 or more supplies.

Equation - SDO delay from SDO to MISO for multiple supplies

(9)

$$t_{SDOdly} = \frac{N_T C_{SDO}}{N_S - 1}[R_{OUT} - N_S(R_{OUT} + R_{SDO})]\ln\frac{(V_{DD} - V_{IH})[R_{OUT} - N_S(R_{OUT} + R_{SDO})]}{V_{DD}(N_S - 1)(R_{OUT} + R_{SDO})}$$

Where:

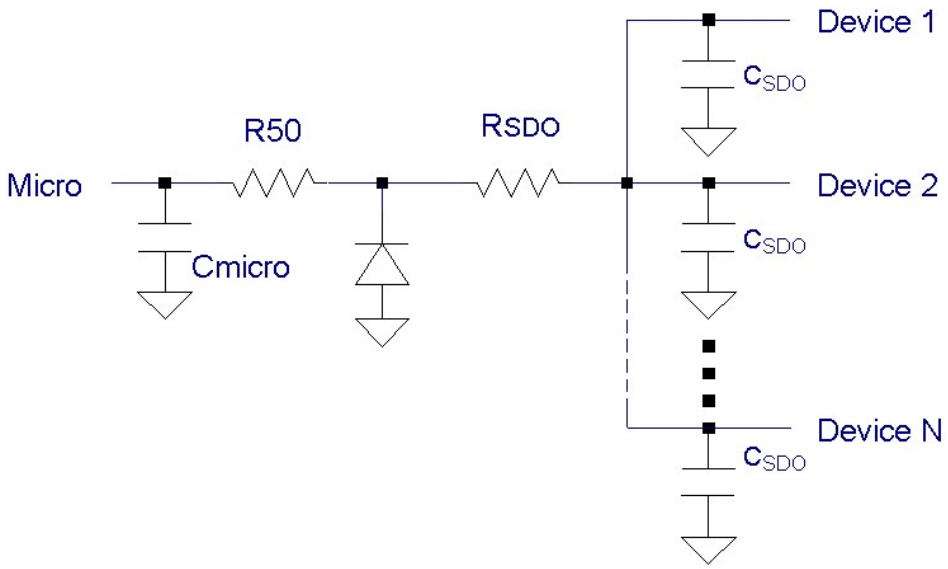
- N_T = the total number of drivers sharing the same SPI bus
- C_{SDO} = SDO driver input capacitance
- R_{SDO} = the calculated 1% tolerance SDO protection resistor
- R_{OUT} = the driver SDO total output resistance (SDO $R_{DS(on)}$ + R_{VDD} = 530 Ω)
- V_{DD} = voltage above R_{VDD}
- V_{IH} = host micro input low voltage threshold

The worst case timing is communicating from the node with the least number of devices. For instance, if there are three supplies with 5 devices where the split was two devices on one supply, two devices on a second supply, and a single device on the third. The slowest SDO signal would be from the single device on the third supply.

To improve the margin, the voltage used for V_{IH} may be increased.

For systems with only one supply, the SDO resistor can be calculated by Equation 1 where the diode D_{SDO} may not be necessary to attain the desired bus speed. If D_{SDO} is not used then the max current, I_{lim_SPI},is governed by what the micro can handle. If D_{SDO} is used, then the max current is governed by the SDO pin at the driver (see Table 1).

Figure 12. Single supply timing configuration



If D_{SDO} is not used, then R_{50} in Equation 10 is 0 Ω. The limit to the current without D_{SDO} the max current is governed by the micro capability.

Equation - SDO delay from SDO to MISO for a single supply

$$t_{SDOdly} = R_{OUT}\left(C_{SDO}N_T + \frac{C_{MISO}(R_{OUT} + R_{SDO} + R_{50})}{R_{SDO} + R_{50}}\right)\ln\left(\frac{V_{DD}}{V_{DD} - V_{IH}}\right) \quad (10)$$

Again, the above equation is an estimation. To obtain the most accurate estimation, the best method would be to run a Spice simulation taking into account all of the nodes. The resulting delay can be inserted into Equation 11 to estimate the maximum SPI bus frequency.

3.2.3 Max frequency

The maximum SPI frequency is the sum of the above delays added to the internal SCK to a valid SDO delay, t_{CQLV}.

Equation - Max SPI bus frequency

$$f_{SPI} = \frac{1}{2\left(t_{SCKdly} + t_{CQLV} + t_{SDOdly}\right)} \quad (11)$$

Where:

- t_{SCKdly} = the delay that appears at the M0-9 driver SCK pin, Equation 6
- t_{CQLV} = the driver internal delay from falling edge of clock to a valid SDO
- t_{SDOdly} = the slowest delay that appears between the M0-9 driver and the microcontroller MISO pin. This can be Equation 9 or Equation 10 depending on the configuration

Using V_{IH} as the upper threshold for the t_{SDOdly} should be sufficient to ensure that the system will communicate. V_{IH} in itself has some reasonable margin. However, the SDO waveform at the micro at this frequency will not be very square. SDO is by far, the slowest waveform in the system.

4 Summary

There are two steps in determining SPI bus capability. The first is calculating the minimum allowable protection resistors. From those calculations, a maximum frequency estimation can be established.

The protection resistor values for CSN, SDI, and SCK depend on the number of drivers that sit on different power supplies (N_S). These resistors are provided to limit the current out of the micro (and into the driver) when the power supply voltage is negative. The SDO signal timing is affected by all of the drivers on the bus. Secondly, the SDO pins on the drivers can handle a much higher current. This both requires and allows the SDO signal path to use a much lower protection resistor value.

The optimum operating frequency is obtained by limiting the M09-SPI drivers on a single SPI bus to one supply. Adding drivers on different supplies increases the protection resistor value and thus slows the bus down. With a single supply, there is only one set of protection resistors between the micro and the drivers. All of the above equations (except for Equation 10) are useful for the systems with one or more supplies. Equation 10 being limited to systems using only one supply.

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
02-Dec-2021	1	Initial release.
22-Mar-2022	2	Updated Figure 4. M0-9 SPI internal and parasitic components.

Contents