DDR memory routing guidelines for STM32MP13x product lines

Introduction

This application note applies to the STM32MP13x product lines (STM32MP131, STM32MP133, and STM32MP135).

This application note provides guidance on how to implement a DDR3, DDR3L, LPDDR2, and LPDDR3 memory interface on the application boards of the STM32MP13x product lines.

This document provides interface schematics, layout implementation rules, and best practices.

Table 1. Device summary

Reference	Product lines
STM32MP13x	STM32MP131, STM32MP133, STM32MP135

1 General information

The devices of the STM32MP13x product lines are STM32 32-bit devices based on Arm® Cortex® processors with a 16-bit DDR interface [1].

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The following table presents a non-exhaustive list of terms and acronyms used in this document.

Table 2. Terms and acronyms

Acronym	Definition
A/C	Addresses and commands
DDR3 SDRAM	Double data rate of third generation SDRAM
DDR3L SDRAM	Double data rate of third generation low-voltage SDRAM
DQ	Data
DQMx	Data mask
DQSx_N/DQSx_P	Data strobe N/Data strobe P
GND	Ground
HF	High frequency
LPDDR2 SDRAM	Low-power double data rate 2 SDRAM
LPDDR3 SDRAM	Low-power double data rate 3 SDRAM
MT/s	Mega transfers per second
PCB	Printed circuit board
SDRAM	Synchronous dynamic random access memory
STPMIC	Highly integrated power-management device for microprocessors
VTT	Termination voltage

Table 3. Reference documents

Document number	Title
[1]	Reference manual *STM32MP13xx advanced Arm®-based 32-bit MPUs* (RM0475)
[2]	STPMIC1 datasheet (DS12792)

2 Design interface constraints

The external DDR interface of STM32MP13x devices can address different types of memory:

- DDR3 and DDR3L with a data rate of 1066 MT/s, voltage at 1.5 V for DDR3 and 1.35 V for DDR3L. More information on DDR3 SDRAM can be found on JEDEC DDR3 SDRAM Standard JESD79-3F.
- LPDDR2 and LPDDR3 with a data rate of 1066 MT/s, voltage at 1.2 V. More information on LPDDR2 and LPDDR3 can be found on JEDEC LPDDR2 Standard JESD209-2F, and JEDEC LPDDR3 Standard JESD209-3C.

Low-voltage and high data-rate speed narrow the tolerances in terms of read eye opening, and contribute to a higher risk of system instability. As a result, there are many constraints and design sensitivities to consider when working with memory interfaces. For example:

- Most signals are single-ended: only the clocks are differential signals.
- Signals can be connected either point-to-point or in fly-by topology.

Continuous board size reductions usually impose performance limitations on the interfaces, and increase challenges when designing a DDR interface.

Given that DDR connections on both the STM32MP13x device and the memory device interface are fixed, the physical layout has very limited flexibility:

- There is a minimum amount of signal routing required, which cannot be reduced further.
- There are impedance constraints to be managed.

To ensure correct signal and power integrity, basic design rules regarding trace isolation, length equalization, power distribution and decoupling, and impedance matching must be respected.

This document lists the rules that must be applied in order to implement a state-of-the-art memory interface in 4- or 6-layer boards.

STMicroelectronics highly recommends reusing the layout of the STM32 device reference designs. These layouts have been tested and have been proven stable.

3 Memory architecture options

The three packages of STM32MP13x devices offer a 16-bit interface. They can be connected to one LPDDR2/3, one or two DDR3/3L with different ways of connection:

Table 4. Package summary of STM32MP13 product lines

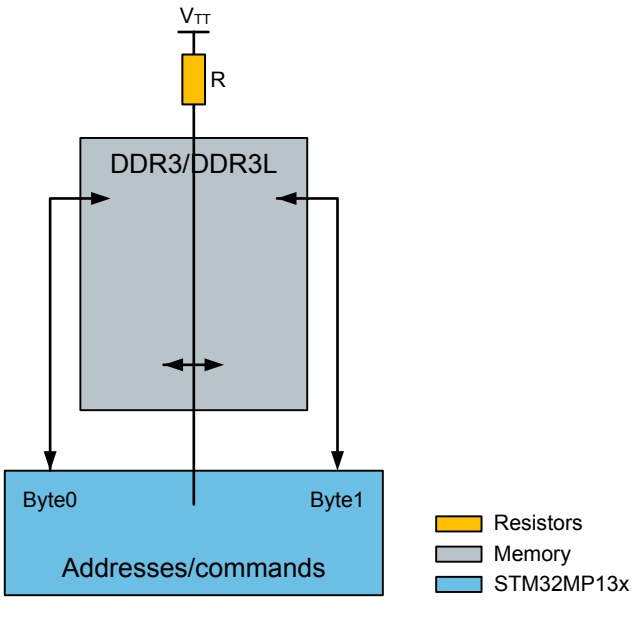
Package type	LFBGA289 (14 × 14 mm)	TFBGA289 (9 × 9 mm)	TFBGA320 (11 × 11 mm)
16-bit interface	X	X	X

3.1 16-bit DDR3/DDR3L interface with one memory

For 16-bit DDR3 or DDR3L interfaces, one 16-bit DDR3/3L is used. With this configuration, STM32MP13x devices can drive up to a 1-Gbyte memory (1 x 8 Gbits).

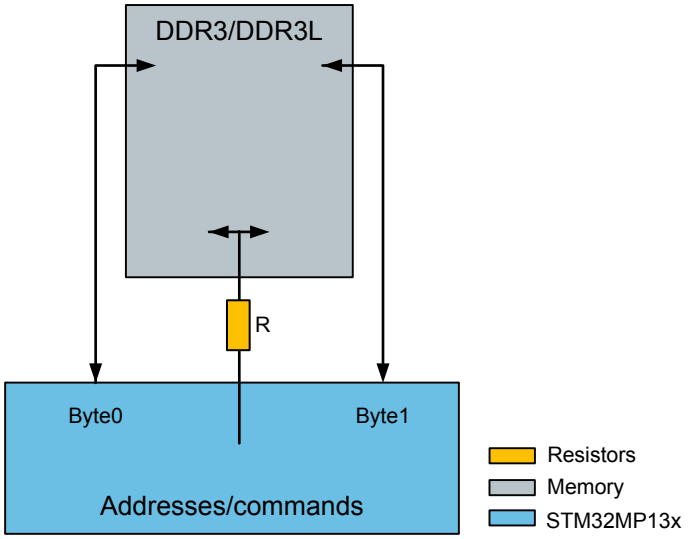
Data lines use a point-to-point connection. Addresses and command lines use termination resistors.

Figure 1. 16-bit DDR3/3L connection with termination resistors on address/command lines



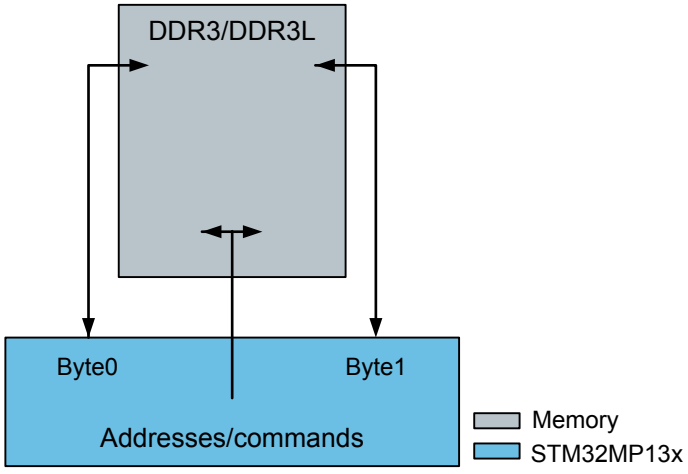
Another possibility to connect one DDR3/3L if termination resistors are not used, is to connect a serial resistor on each address/command line, close to the device.

Figure 2. 16-bit DDR3/3L connection with serial resistors on address/command lines



The last possibility is to connect directly each line to one DDR3/3L, if termination resistors or serial resistors are not used on address/command lines. This type of connection requires that the device and the DDR3/3L are very close.

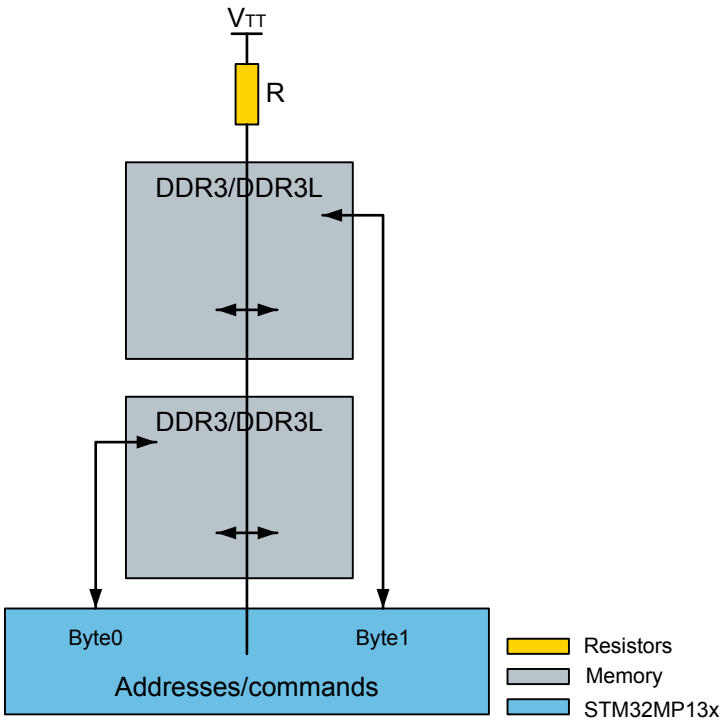
Figure 3. 16-bit DDR3/3L connection without resistors



3.2 16-bit DDR3/DDR3L interface with two memories

For 16-bit DDR3 or DDR3L interfaces, two 8-bit DDR3/3L can be used in fly-by topology. The STM32MP13x device can drive up to a 1-Gbyte memory (2 x 4 Gbits).

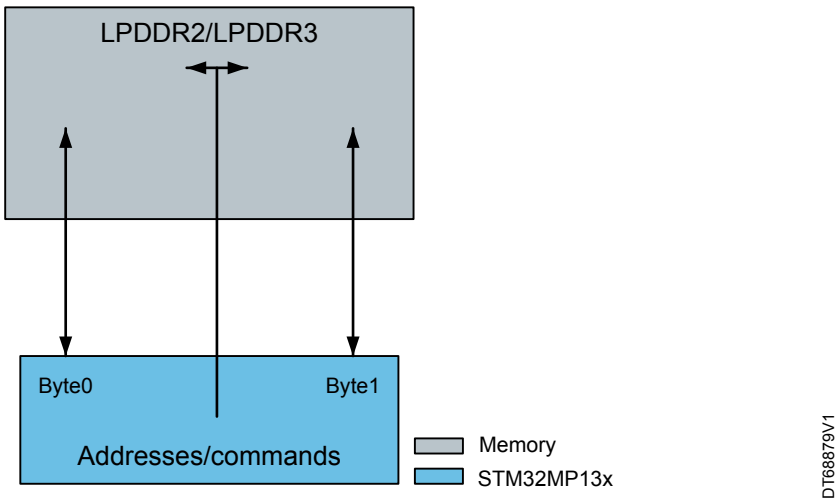
Figure 4. Two 8-bit DDR3/3L connection in fly-by topology



3.3 16-bit LPDDR2/LPDDR3 interface

For 16-bit LPDDR interfaces, one 16-bit LPDDR2/3 is used in point-to-point connection.

Figure 5. 16-bit LPDDR2/3 point to point connection



4 DDR3/DDR3L schematic implementation

A DDR3/3L implementation must include the following elements:

- a single DDR3/3L connection or a standard fly-by topology with two DDR3/3L,
- a cost-optimized point-to-point topology,
- miscellaneous signals,
- power supplies and reference voltage.

These elements are detailed below.

4.1 Single DDR3/3L connection

A connection with one DDR3/DDR3L comprises:

- a distributed A/C bus with 56 Ω on-board termination to V_{TT} (= V_{DD_DDR} / 2),
- a differential clock with differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor,
- a mandatory point-to-point connection of the data bus (two swappable bytes, and swappable bits in the same byte), including:
  - 16 data signal bits (DQ)
  - two data mask signals (DQMx)
  - two differential clocks (DQSx_N/DQSx_P).

4.2 Cost-optimized point-to-point topology

This topology can be used with one DDR3/3L and without V_{TT}. It comprises:

- a point-to-point connection of every A/C bus, with no termination on-board,
- 33 Ω serial resistors, recommended for every A/C of the DDR, in order to reduce reflection. If DDR3/3L is very close to the STM32MP13x device, these resistors can be removed. Refer to the *ST reference design* or the examples in the *DDR memory routing examples for STM32MP13x product lines*, available on www.st.com.
- CLK_N/CLK_P signals, which are terminated differentially by one 100 Ω resistor,
- a point-to-point connection of the data bus (two swappable bytes, and swappable bits in the same byte), including:
  - 16 data signal bits (DQ)
  - two data mask signals (DQMx)
  - two differential clocks (DQSx_N/DQSx_P).

4.3 Standard fly-by topology with two DDR3/3L

A standard fly-by topology includes:

- a distributed A/C bus with 56 Ω on-board termination to V_{TT} (= V_{DD_DDR} / 2)
- a differential clock, distributed to all DDR devices, with a differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor
- a point-to-point connection of the data bus (two swappable bytes, and swappable bits in the same byte on two 8-bit DDR3/3L), including:
  - 16 data signal bits (DQ)
  - two data mask signals (DQMx)
  - two differential clocks (DQSx_N/DQSx_P)

4.4 Miscellaneous signals

The following signals must be included in the schematic:

- DDR_RESETN: asynchronous low-speed reset signal from the DDR controller to DDR devices
  A 10 kΩ pull-down resistor is required. This signal is driven low during the power-on, or when a reset is required. Otherwise, the signal must be driven high by default.
- DDR_ZQ: requires, for DDR impedance calibration, that resistors are placed between the signal balls and ground as follows:
  - a 240 Ω (±1%) resistor must be placed between the ZQ ball on each DDR and ground plane.
  - a 240 Ω (±1%) resistor must also be placed between the ZQ ball of the device and ground plane.
- DDR_CKE (clock enable): activates (registered *high*) and deactivates (registered *low*) the internal circuitry and clocks on the DRAMs. A 10 kΩ pull-down resistor is required.

4.5 Power supplies and reference voltage

The following power supplies and reference voltage components must be provided to the DDR:

- V_{REF} reference voltage (= V_{DD_DDR} / 2)
- V_{TT} power supply (= V_{DD_DDR} / 2)
- V_{DD_DDR} power plane

V_{REF} reference voltage (= V_{DD_DDR} / 2)

This reference voltage is required by the STM32MP13x and DDR3/3L devices in order to properly sample A/C and data signals. Its noise level must remain very low, as described in the JEDEC standard.

There are two possibilities:

- independent V_{REF} generators (VREFCA, VREFDQ) for STM32MP13x and DDR3/3L
  Each VREF generator is based on a resistance bridge with two 1 kΩ (±1%) resistors from V_{DD_DDR}, plus a local 100 nF decoupling capacitor. V_{REF} must be generated as close as possible to its corresponding ball.
- a common V_{REF} for STM32MP13x and DDR3/3L
  The V_{REF} generator from an external device is delivered to STM32MP13x and DDR3/3L with a local 100 nF decoupling capacitor. The STPMIC1x [2] can deliver V_{REF}.

V_{TT} power supply (= V_{DD_DDR} / 2)

This power supply is used exclusively in DDR3/3L interfaces. This is the termination voltage for address and control (A/C) signals.

An external V_{TT} voltage generator is recommended. The STPMIC1x [2] can deliver V_{TT}. A strong V_{TT} decoupling is required. It must be as close as possible to the termination resistors.

V_{DD_DDR} power plane

This is the DDR interface power supply. It is equal to 1.5 V (1.425-1.575 V) for DDR3, or equal to 1.35 V (1.283-1.45 V) for DDR3L.

This plane requires mandatory decoupling capacitors relative to ground plane, with bulk and HF capacitors. These capacitors must be close to the power supply pins for STM32MP13x and DDR devices.

5 LPDDR2/LPDDR3 schematic implementation

An LPDDR2/3 implementation must comprise the following elements (detailed later in this section):

- a point-to-point topology
- miscellaneous signals
- power supplies and reference voltage

5.1 Point-to-point topology

A standard point-to-point topology includes:

- 12 A/C signals,
- a differential clock with differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor,
- a point-to-point connection of the data bus (two bytes with 16-bit LPDDR2/3), including:
  - 16 data signal bits (DQ): Byte 0 of LPDDR2/3 must be connected to byte 0 of the STM32MP13x device. There is no possibility to swap bits in this byte.
  - two data mask signals (DQMx)
  - two differential clocks (DQSx_N/DQSx_P)

5.2 Miscellaneous signals

The following signals must be included in the schematic:

- DDR_ZQ: requires, for LPDDR2/3 impedance calibration, that resistors are placed between the signal balls and ground as follows:
  - a 240 Ω (±1%) resistor must be placed between the ZQ ball on the LPDDR2/3 chip and ground plane.
  - a 240 Ω (±1%) resistor must be placed between the ZQ ball of the STM32MP13x device and ground plane.
- DDR_CKE (clock enable): activates (registered *high*) and deactivates (registered *low*) the internal circuitry and clocks on DRAMs. A 10 kΩ pull-down resistor is required.

5.3 Power supplies and reference voltage

The following power supplies and reference voltage must be provided to the DDR:

- V_{REF} reference voltage (= V_{DD2_DDR} / 2)
- V_{DD2_DDR} power plane
- V_{DD1_DDR} power supply

V_{REF} reference voltage (= V_{DD2_DDR} / 2)

V_{REF} is required by STM32MP13x and LPDDR2/3 to properly sample A/C and data signals. Its noise level must remain very low, as described in the JEDEC standard.

Two options are possible:

- Independent V_{REF} generators (VREFCA, VREFDQ) for STM32MP13x and LPDDR2/3.
  Each V_{REF} generator is based on a resistance bridge with two 1 kΩ (±1%) resistors from V_{DD_DDR}, plus a local 100 nF decoupling capacitor.
  V_{REF} must be generated as close as possible to its corresponding ball.
- A common V_{REF} for STM32MP13x and LPDDR2/3.
  The V_{REF} generator from an external device is delivered to STM32MP13x and LPDDR2/3 with a local 100 nF decoupling capacitor.
  The STPMIC1x [2] can deliver V_{REF}.

V_{DD2_DDR} power plane

This is the LPDDR2/3 interface power supply. It is equal to 1.2 V (1.14-1.30 V).

This plane requires mandatory decoupling capacitors relative to ground plane, with bulk capacitors.

The HF capacitors must be close to the power supply pins for both STM32MP13x and LPDDR2/3.

V_{DD1_DDR} power supply

This is the core power supply of LPDDR2/3. It is equal to 1.8 V (1.7-1.95 V).

6 PCB design considerations

The basic PCB design considerations to take into account are detailed in the following sections.

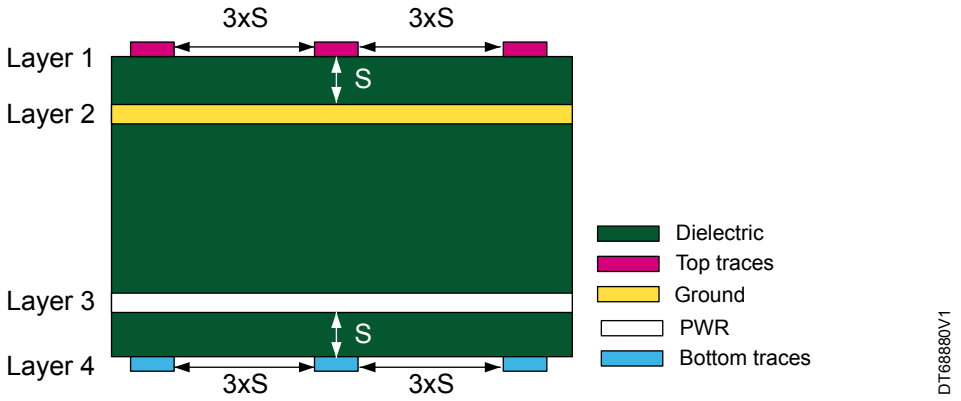
6.1 Trace isolation distance

In order to reduce crosstalk, glitches, and jitter caused by neighboring traces (sometimes referred to as *aggressors*), a minimum isolation distance must be provided around every trace.

S-3S isolation rule

If "S" is the distance between a trace and its reference plane (ground plane for top-layer traces, and PWR plane for bottom-layer traces), a trace is said to be isolated if the distance between it and its direct neighbor is greater than or equal to 3xS. The figure below shows this rule in practice.

Figure 6. S-3S isolation rule illustration



In other words, S-3S is the minimum isolation spacing rule. If more space between traces is available, it must be used to separate signals as much as possible (such as S-4S or S-10S).The more space there is between traces, the better the signal isolation and noise immunity is.

The S-3S rule is not applicable below BGA devices (memory and STM32MP13x devices) because of fan-out constraints. When the S-3S rule is not applicable, the length of the segments that are in conflict with the rule must be minimized.

Layouts using an S-1S spacing must be avoided as often as possible. If the S-3S rule is not applicable, maximizing the distance between traces as much as possible (S-2S rule) is preferable, instead of using an S-1S layout.

6.2 Length equalization

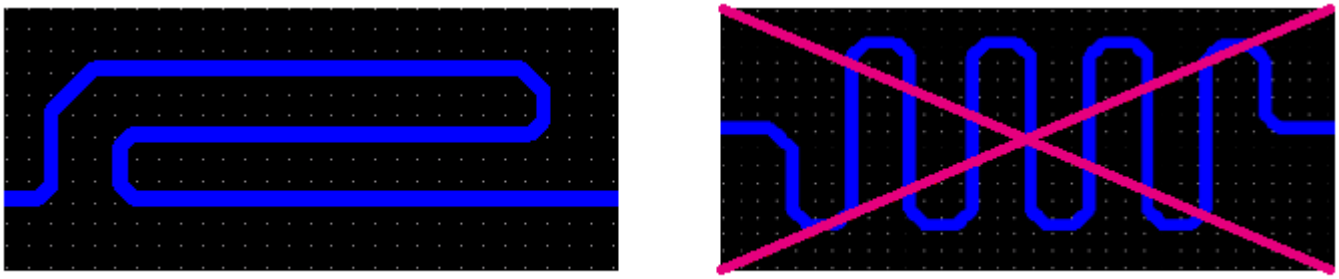
Signals of the same group must have matching setup and hold timings when they arrive at their destination. To meet these timing constraints, trace length equalization may be required.

The whole signal path from STM32MP13x device to the memory must be taken into account, including the package and board trace lengths.

Length equalization patterns

When routing traces to equalize lengths, some patterns are recommended. For example, switchback patterns are preferred over serpentine shaped patterns, as the latter can provoke orthogonal propagation, which compromises the integrity of the signal.

Figure 7. Length equalization patterns



The S-3S isolation rule must also be applied within the equalization pattern, meaning that the minimum distance between sections of the same trace should be greater or equal to S-3S.

In the case of differential signals:

- Intra-pair length equalization is not allowed.
- The spacing between N and P must be constant.
- The mean value length of N and P signals that must be considered for a differential pair, is given by: Lsig = (LsigN + LsigP) / 2.

The STMicroelectronics templates and the length equalization tables can be used to simplify the task of equalizing signal trace lengths. These tables include the trace lengths of the packages and can be obtained from the *DDR memory routing examples for STM32MP13x product lines*, available on www.st.com.

6.3 Impedance

The driver impedance (ZDRV) is usually 34 Ω or 40 Ω, while the on-die termination impedance (ZODT) is usually 60 Ω.

The board impedance must be controlled in order to guarantee proper transmission line setup, in accordance with the trace geometry (width and spacing), and the stack-up of the board.

For DDR3/3L and LPDDR2/3 interfaces, STMicroelectronics recommends the following impedances:

- for single-ended signals: 55 Ω ±10%.
- for differential signals: 100 Ω differential ±10%.

6.4 Layer allocation for 4-layer boards

Layers must be allocated and implemented as detailed below, without exception:

- Top layer:
  - This layer is dedicated to traces with the highest sensitivity.
  - The traces are referenced to the unified, internal ground plane.
  - There are no impedance breaks.
  - There is no coupling allowed to noisy power supplies.
- Layer 2 (GND) internal layer:
  - This is the unified internal ground plane.
  - It must be connected by a matrix of vias to the top and bottom ground areas.
- Layer 3 (V_{DD_DDR} for DDR3/3L or V_{DD2_DDR} for LPDDR2/3) internal layer:
  - This is the dedicated power supply plane, which supplies on board power distribution.
- Bottom layer:
  - This is a second signal layer used for traces. It is possible to have impedance breaks in this layer, due to the discontinuity of the reference power supply plane.

6.5 Layer allocation for 6-layer boards with TFBGA289

Layers must be allocated and implemented as detailed below, without exception.

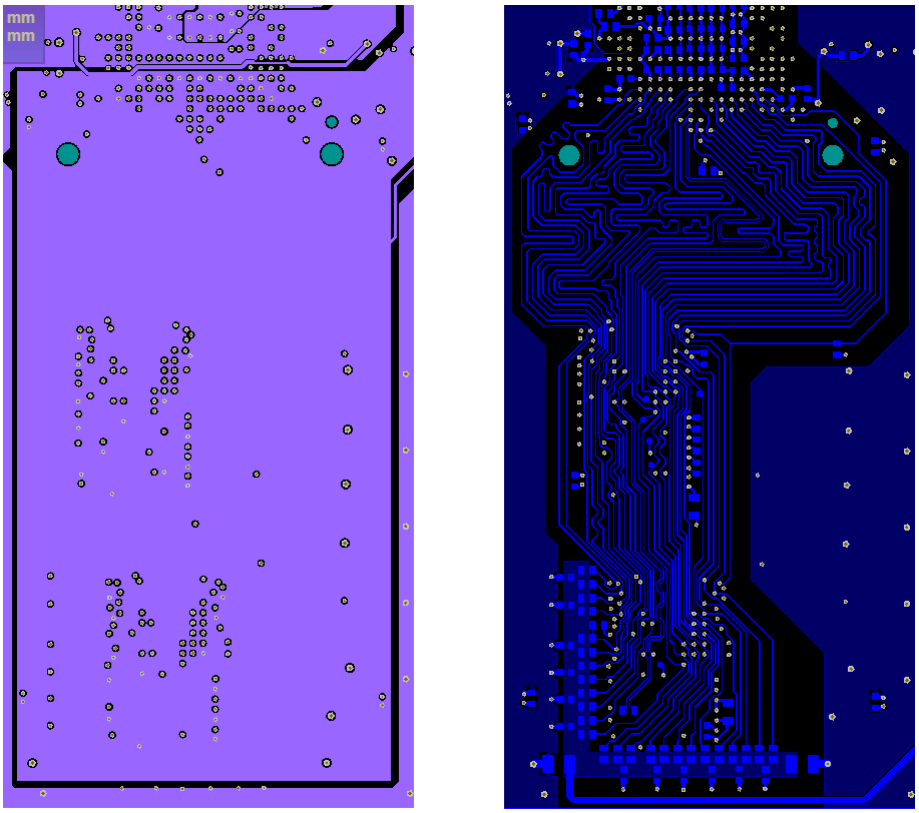
- Top layer:
  - This layer is dedicated to data traces.
  - The traces are referenced to the unified, internal ground (GND) plane.
  - There are no impedance breaks.
  - There is no coupling allowed to noisy power supplies.
- Layer 2 (GND) internal layer:
  - This is the unified internal ground plane.
  - It must be connected by a matrix of vias to the top and bottom ground areas.
- Layer 3 internal layer:
  - This layer is dedicated to A/C traces.
- Layer 4 internal layer:
  - This layer has a ground plane above the V_{DD_DDR} or V_{DD2_DDR} power plane.
- Layer 5 (V_{DD_DDR} for DD3/3L or V_{DD2_DDR} for LPDDR2/3) internal layer:
  - This is the dedicated power supply plane, which supplies on board power distribution.
- Bottom layer:
  - Decoupling capacitors use this layer.

6.6 V_{DD_DDR} power plane specification

A/C signals are laid out on the bottom layer of the 4-layer PCB.

The internal layer 3 must be a unified V_{DD_DDR} (V_{DD2_DDR} for LPDDR2/3) power plane, which fully overlaps the memory bottom-layer signals, in order to avoid any impedance breaks due to traces referenced to multiple power planes.

Figure 8. Example of DDR3L A/C signal layout and corresponding power plane



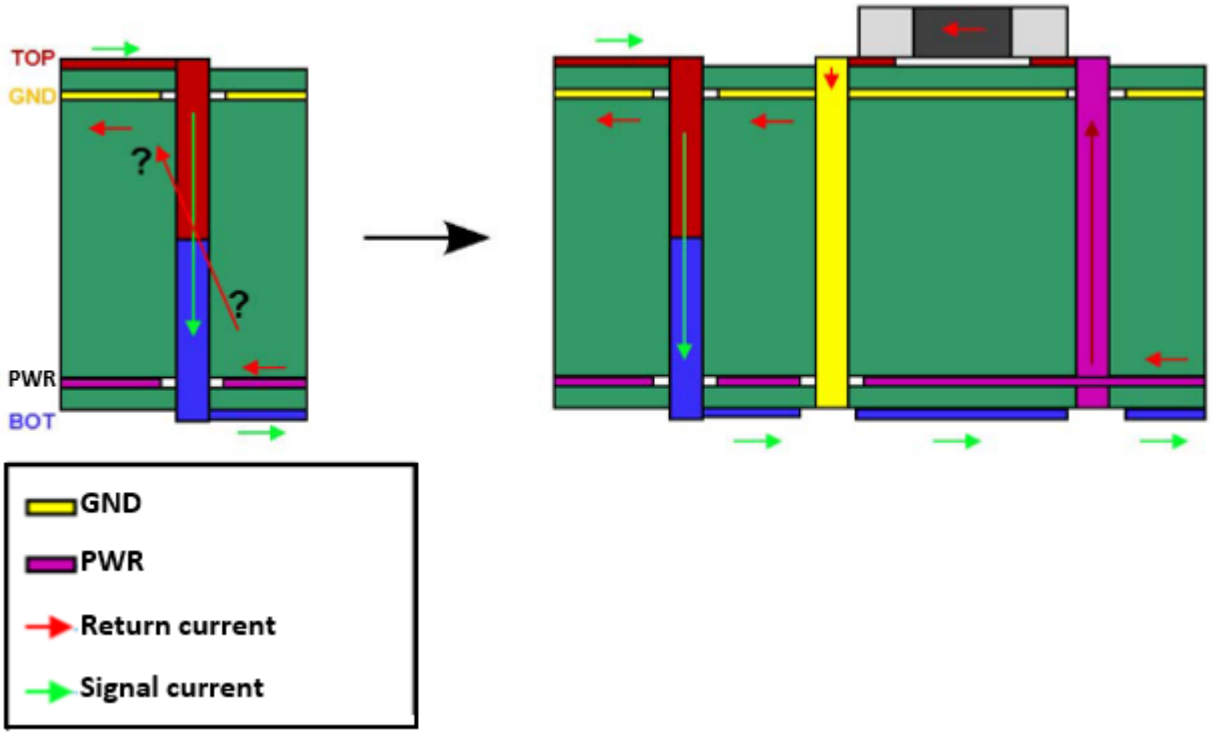
Internal layer 3 Bottom layer

6.7 Layer change capacitors

When a sensitive signal moves from the top layer of the board to the bottom layer (or vice versa), a 100 nF capacitor must be placed as close as possible to the signal via. It must be connected from one side to the layer 2 (GND), and from the other side to the layer 3 (V_{DD_DDR} for DDR3/3L, V_{DD2_DDR} for LPDDR2/3).

This design requirement is absolutely necessary in order to provide an HF return current reference path to the signal. The capacitor can be placed on either the bottom or top layer (as shown in the figure below).

Figure 9. Use of layer change capacitors



When multiple signals are changing layers in the same area of the board (such as in the case of A/C bus distribution), it may become impossible to place a single capacitor close to each via. The solution in this case is to add a single capacitor for a group of vias. The number of capacitors must be as high as needed for the specific board design, and they must be placed as close as possible to the via area.

6.8 Types of decoupling capacitors

Power integrity is essential for avoiding voltage drops and, by consequence, eye closure, and erroneous data transmission.

Core and sensitive power supplies (like V_{DD_DDR}) must be laid out by using internal power planes, and by using maximum width, in order to minimize the distribution impedance. In addition, decoupling capacitors are required.

There are two types of capacitors:

- bulk capacitors
  These capacitors provide an on-board energy tank for low-frequency, high-current needs. Capacitance values can range from 10 µF to 100 µF. Refer to the *ST reference design* or to the *DDR memory routing examples for STM32MP13x product lines*, available on www.st.com, to choose a capacitor value appropriate for the specific power supply used. Bulk capacitors do not need to be placed very close to their destination.
- high-frequency (HF) capacitors
  These capacitors provide a local energy tank for high-frequency current bursts. They must be placed as close as possible to the destination (power pins or balls). A better practice is to implement fewer capacitors, but placed in optimum positions, in order to reduce the connection inductance.

6.9 Minimizing connection inductance with HF capacitors as decoupling capacitors

The decoupling capacitors placement must ensure minimum connection inductance.

The closer the capacitor is to its destination, the more efficient it is. This is particularly true for HF capacitors.

Putting capacitors on the top layer can provide far better decoupling efficiency than placement on the bottom layer.

However, the location of these capacitors can be constrained by BGA fan-out. This section provides best practices for capacitor placement in order to minimize connection inductance, and to improve decoupling efficiency, for both top and bottom layers.

6.9.1 Placing capacitors on the top layer

Capacitors placed on the PCB top layer cannot be very close to BGA balls due to package constraints.

However, if a capacitor is connected by a direct top-layer power trace to the BGA ball, its connection inductance remains smaller than if the capacitor is located much closer, but on the bottom layer, owing to the GND layer position in the stack-up (GND is the return current layer). The amount of connection inductance that results is directly linked to the area of the current loop.

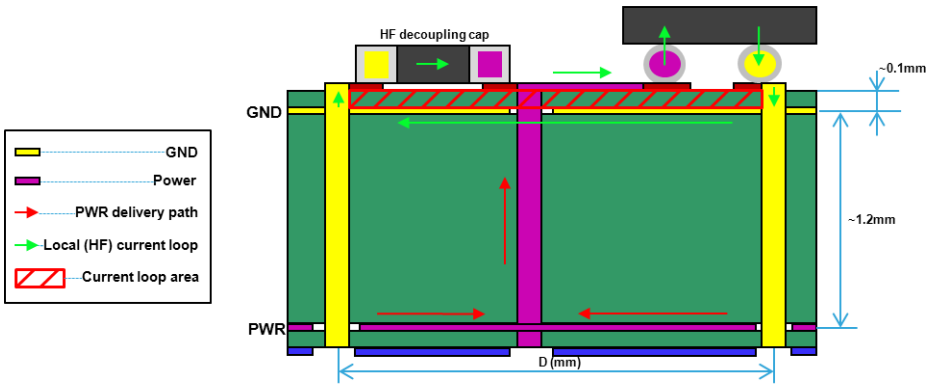
Therefore top layer placement offers:

- Pros
  - Small current loop area, resulting in low connection inductance, and good decoupling capability.
  - Free space on the bottom layer for other signal layouts. As memory A/C trace layouts are usually on the bottom layer, this allows more flexibility for A/C length equalization/spacing requirements.
- Cons
  - Placement of capacitors on the top layer is very often not possible for main BGA decoupling because of fan-out constraints.

When possible, HF capacitor must be placed on the top layer, with a top-layer direct power connection. The layer 2 (GND) provides a close return path, which results in a small current loop area and optimal decoupling efficiency.

For example, in the layout shown in the figure below, the resulting current loop area is: Current loop area = 0.1 × D. If D = 5 mm, the current loop area is in the region of 0.5 mm^2.

Figure 10. Placement of an HF capacitor on the top layer



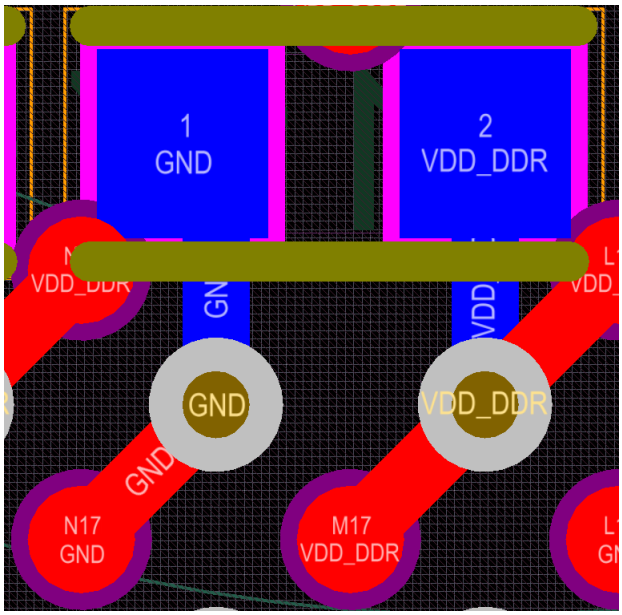
6.9.2 Placing capacitors on the bottom layer

When top-layer decoupling is not possible, placement of capacitors must be on the bottom layer.

While the connection inductance is higher than for top-layer capacitor placement, due to the bigger current loop area, bottom layer placement remains most of the time the only decoupling option for main BGA. Following some basic implementation rules allow for an optimization of this placement. For best results, the capacitor must be placed right below the BGA balls.

When placing HF capacitors on the bottom layer, aim to have the shortest possible connections, and a good via placement directly below the BGA, as shown in the figure below.

Figure 11. HF capacitor on bottom layer

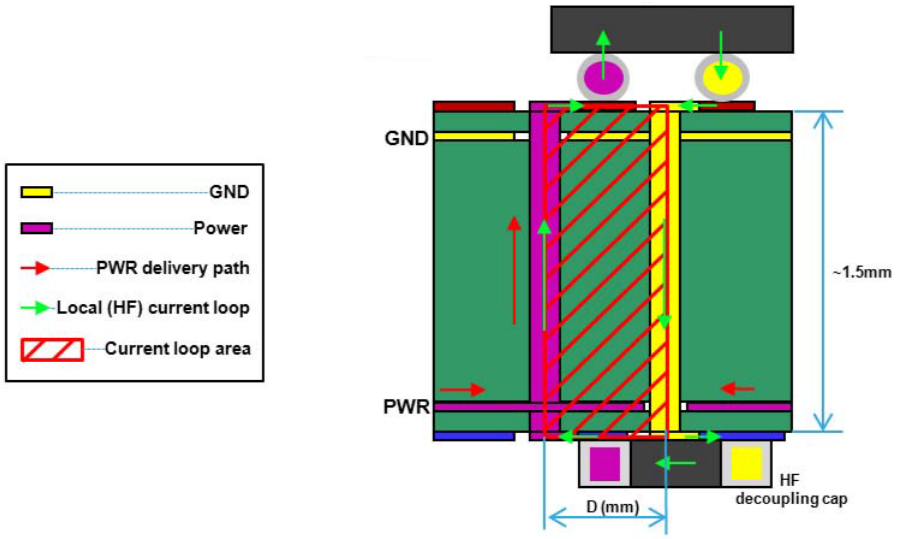


In the following example, the resulting current loop area is:

Current loop area = 1.5× D

If D equals 1.0 mm, the resulting current loop area is 1.5 mm^2, as compared to 0.5 mm^2 for a top-layer placement at a 5 mm distance. In other words, a capacitor situated on the top layer, 15 mm from the power ball, would have the same efficiency as a capacitor situated on the bottom layer, directly below the power ball. This illustrates the higher efficiency of top-layer capacitor placement relative to bottom-layer placement.

Figure 12. Placement of an HF capacitor on the bottom layer



7 Memory layout rules

This section presents a code of best practices rules to be applied by signal type on memory interfaces. These recommendations are based on the basic PCB design rules.

7.1 Data signal rules for 16-bit memory interfaces

There are two different (independent) signal groups over 2 bytes:

- Byte0 = DQ[7:0], DQM0, DQS0_N and DQS0_P
- Byte1 = DQ[15:8], DQM1, DQS1_N and DQS1_P

For these data signals, the following rules must be applied:

- These data signals must only be routed on the top layer of the PCB.
- Whenever possible, the S-3S isolation rule (as a minimum) must be applied.
  Due to the constraints of high via density and BGA pitch, exceptions can only be made when signals are very close to the memory or to the STM32MP13x device.
  When the S-3S rule is not applicable, the layout must be designed to optimize the isolation rule (such as S-2S or S-1.5S). Segments where S-1S is the only option must be as short as possible.
- For DDR3 and DDR3L, as fly-by topology is used with two 8-bit DDR3/3L, do not apply the same length equalization on-board for both bytes. Apply the rule below to the byte of first DDR3/3L and to the byte of second DDR3/3L:
  - DQ or DQM to DQS_N/DQS_P ±40 mils (1.016 mm)
  - DQS_N/DQS_P length must be from 0 to 590 mils (14.986 mm) shorter than CLK_N/ CLK_P length (CLK_N/CLK_P must be the longest traces).
  - Length of the byte of second DDR3/3L compared to length of the byte of first DDR3/3L 1300 mils (33.02 mm) max
- • For one 16-bit DDR3/3L or LPDDR2/3, the rule below must be applied to each byte:
  - DQ or DQM to DQS_N/DQS_P ±40 mils (1.016 mm)
  - DQS_N/DQS_P length must be from 0 to 590 mils (14.986 mm) shorter than CLK_N/ CLK_P length (CLK_N/CLK_P must be the longest traces).

Trace length = substrate length + via length + board track length

Differential trace length (DSQS_N/DQS_P) = (Trace length N + Trace length P) / 2

Note: Always refer to the ST reference design or to the examples in the DDR memory routing examples for STM32MP13x product lines on www.st.com for signal ordering, BGA fan-out and layout examples.

7.2 Address and control (A/C) signal rules

The following signals are included in A/C groups:

- for DDR3/3L A[15:0]: BA[2:0], RASN, CASN, WEN, CSN, CKE, ODT, CLK_N, CLK_P
- for LPDDR2/3 A[9:0]: CSN, CKE, CLK_N, CLK_P

The following design rules must be applied for A/C signals:

- Except with TFBGA289, the PCB bottom layer must be used for A/C distribution to memory devices. The top layer is reserved for connections to the memory (stubs) and A/C bus crossing.
- The S-3S isolation rule as a minimum must be applied wherever possible.
  When the S-3S rule is not applicable, the layout must be designed to optimize the isolation rule (such as S-2S, S-1.5S). Segments where S-1S is the only option must be as short as possible.
  Due to constraints of high via density and BGA pitch, exceptions can only be made when signals are very close to the memory or the STM32MP13x device.
- Length equalization rules:
  - A/C length must be from 0 to 40 mils (1.016 mm) shorter than CLK_N / CLK_P length.
  - CLK_N/ CLK_P maximum length 4.72 inch (12 cm)

  Trace length = substrate length + via length + board track length
  Differential trace length (CLK_N/CLK_P) = (Trace length N + Trace length P) / 2
- In case of fly-by topology used for DDR3/3L:
  Length of A/C, CLK_N/CLK_P of second DDR3/3L compared to length of A/C, CLK_N/CLK_P of first DDR3/3L 1300 mils (33.02 mm) max.

Note: Always refer to the ST reference design or to the examples in the DDR memory routing examples for STM32MP13x product lines on www.st.com for signal ordering, BGA fan-out and layout examples.

7.3 DDR_ZQ signal

This signal must be laid out, so that the trace from the ball to the reference resistor is as short as possible. Good isolation from any noisy aggressor signals must be ensured.

7.4 Power plane rules

This section describes the rules to follow to design the power planes.

7.4.1 V_{DD_DDR} (V_{DD2_DDR} for LPDDR2/3) power plane

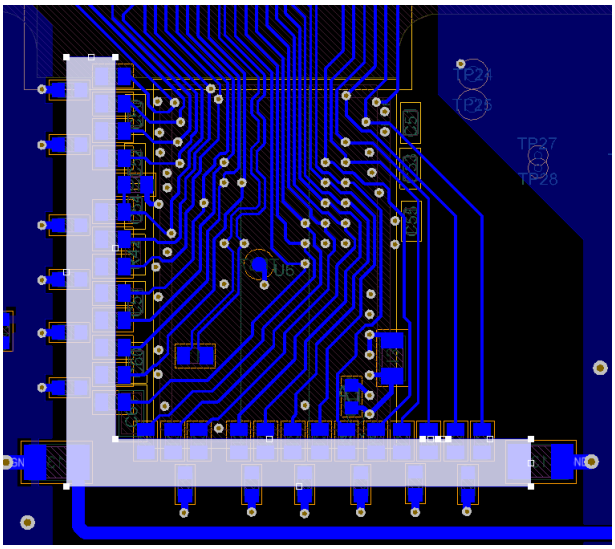
- Power plane must be unified at layer 3 for 4-layer boards and layer 5 for 6-layer boards.
- This power plane must overlap every DDR3/3L (LPDDR2/3) trace on the bottom layer for 4-layer boards, in order to avoid impedance discontinuities.
- The V_{DD_DDR} power plane connection to the V_{DD_DDR} power supply, to STM32MP13x, and to each memory, must be done by multiple vias.
- Standard decoupling rules must be applied:
  - Bulk capacitors must be placed between the voltage regulator, the STM32MP13x device, and the memories.
  - HF decoupling capacitors must be placed as close as possible to each of the power pins, following the low-inductance connection recommendations outlined in Section 6.9 Minimizing connection inductance with HF capacitors as decoupling capacitors.

7.4.2 V_{TT} power plane rule

The V_{TT} power supply is used in DDR3/3L interfaces.

- The V_{TT} termination voltage must be considered as a power supply.
- Due to V_{DD_DDR} constraints (an unified plane in layer 3 for 4-layer boards, overlapping the DDR area), the V_{TT} layout must be managed as an island on the bottom layer. Refer to the figure at the end of this section.
- The V_{TT} regulator must be located close to the RTT terminations.
- One HF capacitor must be reserved for two RTT termination resistors, and must be placed as close as possible to them.
- Bulk capacitors can be placed anywhere between the V_{TT} regulator and terminations.
- Leave sufficient spacing around the V_{TT} island, to reduce crosstalk.

Figure 13. Layout of V_{TT} power plane island



Revision history

Table 5. **Document revision history**

Date	Version	Changes
18-Jan-2023	1	Initial release

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