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AN5672

Application note

Solenoid driver channels parallel mode functionality: guidelines and limits

Introduction

This document is intended to integrate the information provided in the L9305 product datasheet, in order to facilitate the correct usage of parallel mode functionality featured for solenoid driver channels. Guidelines are suggested for the device correct operation in parallel mode. Configuration and diagnostic items involved are highlighted.

1 Solenoid driver channels parallel mode operation

The 4 channels can be configured to work in parallel mode to allow regulation of higher current set-points: suitable for example in applications where HILOAD = 1 accuracy and resolution are not matching the desired target.

Channel parallelization can be enabled only for fixed channel pairs:

- ch0 can parallel with ch1 only
- ch2 can parallel with ch3 only

In parallel mode one channel acts as a master (ch0, ch2) and the other as a slave (ch1, ch3); both channel current sense measurements are kept active to measure load current split between channel pairs and the two measurements are combined and used to close control loop on master logic only.

Configuration of parallel mode is done through master channel registers. The following master parameters are valid for both channels, overwriting slave channel configuration (if any):

- current set-point
- dither parameters
- control loop parameters (KI, KP, fix/var frequency mode selector, KFI, etc…)

As a consequence of described implementation, resulting resolution of current and dither set-point registers is doubled, since target value is applied on both channels in parallel: it means that in parallel mode 1LSB = 0.5 mA instead of default 0.25 mA for HILOAD = 0, while 1LSB = 0.66 mA instead of default 0.33 mA for HILOAD = 1. Resulting accuracy for current measurement is kept at 1% for high current range while is doubled from 5 mA to 10 mA for low current range for HILOAD = 0. For HILOAD = 1, accuracy for current measurement is kept at 4% for high current range while is doubled from 20 mA to 40 mA for low current range.

Feedback of measured average current is kept distinguished like in normal operation and available for each channel on its own register with nominal LSB of 0.25 mA or 0.33 mA according to HILOAD setting. The same applies for HS-LS compare check and applied offset compensation.

The following parameters are kept independent between master and slave channels and particular attention must be paid for proper configuration settings:

- HW/SW mode selection
- HS/LS configuration
- INx/NDISx functionality
- diagnostic
- calibration data
- offset compensation

To enable parallel mode the following conditions must be verified, in case any of the following is missing the channels will be kept independent following their own settings:

- Bit 14 and/or Bit 15 in SERVENA register must be set to 1 (Bit 14 enables parallel mode for ch0-ch1 pair, Bit 15 for ch2-ch3 pair)
- SOLENDRV configuration must be equal for the selected parallel channel pair

Even if diagnostic is kept independent, faults causing tri-state condition will affect both channels in parallel mode.

Global registers for enabling parallel mode operation are the following:

Service Enable - SERVENA

Address Global Base Address + 0x00
Type Read/Write
Description General SERVICE Enable bits

Table 1. SERVENA register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15]	Parallel mode selection for ch2-ch3	0	1	Read/Write
[14]	Parallel mode selection for ch0-ch1	0	1	Read/Write
[13:10]	Unused	00 0000	00 0000	Read
[9]	RAM retrigger 1: Download calibration data from EEPROM. 0: Download complete or inactive	0	0	Read/Write
[8]	Spread Spectrum Disable: 0: Main Clock Spread Spectrum Enabled 1: Main Clock Spread Spectrum Disabled	0	0	Read/Write
[7:1]	Unused	000 0000	000 0000	Read
[0]	Stagger Enable: 1: Stagger Enabled. 0: Stagger Disabled. Valid only when channel is in Fixed Frequency mode	0	0	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

Solenoid Drivers Enable - SOLENDR

Address Global Base Address + 0x01
Type Read/Write
Description Solenoid Driver Configuration

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15:8]	Unused	All "0"	All "0"	Read
[7:6]	Solenoid Driver State, Channel 3 00: Driver Off, OFF State Diagnostics disabled and masked 01 : Driver tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	01	Read/Write
[5:4]	Solenoid Driver State, Channel 2 00: Driver Off, OFF State Diagnostics disabled and masked 01 : Drives tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	01	Read/Write

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[3:2]	Solenoid Driver State, Channel 1 00: Driver Off, OFF State Diagnostics disabled and masked 01 : Drives tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	01	Read/Write
[1:0]	Solenoid Driver State, Channel 0 00: Driver Off, OFF State Diagnostics disabled and masked 01: Drives tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	01	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

1.1 Channel registers configuration details

For channel pair configuration, the following registers can be written just for master channel, because the corresponding slave channel registers will be overwritten with the same settings.

Current Setpoint - SETPOINT

Address Channel_X_BaseAddress + 0x06

Type Read/Write

Description Register stores current setpoint code (HW mode current control). Current Control SETPOINT is coded into 13 bits. Current value depends on HILOAD bit

Table 2. SETPOINT register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15]	Auto Limit: Activates the transient mode on setpoint change: 0: Inactive 1: Active	0	0	Read/Write
[14:13]	Unused	0	0	Read
[12:0]	Current Setpoint Code	All "0"	User's setup	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

Control Configuration - CTRLCFG

Address Channel_X_BaseAddress + 0x07

Type Read/Write

Description -

Table 3. CTRLCFG register detail

Register bit	Field name/description	Default values	Typical conf. (1)	Type
[15:14]	Transition Time: Too long period detection (if the current PWM time exceeds this threshold, the controller enters the transient state): 00: 2.5 * Tpwm 01 : 4.5 * Tpwm 10: 8.5 * Tpwm 11 : 16.5 * Tpwm	0	0	Read/Write
[13:12]	Unused	0	0	Read
[11]	HW feedback Frequency Mode: 0: Fixed Frequency(2) 1: Variable Frequency	0	0	Read/Write
[10:0]	Target PWM Period Code	All "0"	User's setup	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*
2. *For Fixed frequency Mode D[11] = 0 (default).*

Gains Configuration - KGAINS

Address Channel_X_BaseAddress + 0x09

Type Read/Write

Description Register stores KI (Integral error gain: HW mode current control) and KP (Proportional error gain: HW mode current control)

Table 4. KGAINS register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15:6]	Unused	All "0"	All "0"	Read
[5:3]	KI: Integral Gain of HW current control loop (fixed & variable freq.)	100	110(2)	Read/Write
[2:0]	KP: Proportional Gain of HW current control loop (fixed freq. only)	100	100(2)	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*
2. *KI and KP parameters are strongly dependant on specific load and need to be fine tuned on actual application.*

Frequency Control - KFREQCTRL

Address Channel_X_BaseAddress + 0x08

Type Read/Write

Description Register stores KF, FCIL (Variable frequency forward gain: HW mode current control)

Table 5. KFREQCTRL register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15:6]	unused	All "0"	All "0"	Read
[5:3]	KFI: Integral Gain of Frequency Control Loop	101	101(2)	Read/Write
[2:0]	FINT_START: Start value for frequency integrator upon exiting transient mode	111	111(2)	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*
2. *KFI and and FINT_START parameters are strongly dependant on specific load and need to be fine tuned on actual application.*

Dither Programming 1 - DITHPGM1

Address Channel_X_BaseAddress + 0x04

Type Read/Write

Description Dither Generator Configuration

Table 6. DITHPGM1 register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15]	Dither Enable: 0: Disabled 1: Enabled	0	User's setup	Read/Write
[14]	DITHER_SYNC_EN: 0: Disabled 1: Enabled	0	User's setup	Read/Write
[13]	SYNC TYPE: 0: Dither Synchronization at each Dither Step 1: Dither Synchronization at each dither Period	0	User's setup	Read/Write
[12:8]	Unused	All "0"	All "0"	Read
[7:0]	Istep: Current step Value	0101 0000	User's setup	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

Dither Programming 2 - DITHPGM2

Address Channel_X_BaseAddress + 0x05
Type Read/Write
Description Dither Generator Configuration

Table 7. DITHPGM2 register detail

Register bits	Field name/description	Default values	Typical conf.(1)	Type
[15:13]	Unused	0	0	Read
[12:8]	Nstep: Number of steps in a quarter of dither period	0 0101	User's setup	Read/Write
[7:6]	Unused	0	0	Read
[5:0]	Tstep: Number of PWM cycles for each dither step	00 1010	User's setup	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

All remaining channel specific registers are kept independent between master and slave channels and particular attention must be paid for proper configuration settings both for master and slave channel. In particular, the following registers must be set identical between master and slave.

Configuration 1 - CONFIGURATION1

Address Channel_X_BaseAddress + 0x02
Type Read/Write
Description Configuration register provides information related to channel configuration

Table 8. CONFIGURATION1 register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15]	Unused	0	0	Read
[14]	OFS_CMP_DIS: 0: Current Sense Offset Compensation Active 1: Current Sense Offset Compensation disabled	0	0	Read/Write
[13]	CALIBRATION_DIS: 0: Digital Current Sense Calibration Active 1: Digital Current Sense Calibration Disabled	0	0	Read/Write
[12:11]	Unused	0	0	Read
[10]	Solenoid Logic BIST: 0: Logic BIST Reset 1: Logic BIST Enabled	0	0	Read/Write
[9]	Td_Blank: 0: Long Blanking Time 1: Short Blanking Time	0	0	Read/Write
[8]	HILOAD: Current Sense Scale: 0: 1.5 A Max Current Range 1: 2.0 A Max Current Range	0	0	Read/Write

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[7]	Unused	0	0	Read
[6]	Overcurrent threshold selection: 0: 4 A Theshold 1: 5 A Threshold	0	User's setup	Read/Write
[5]	Enable OFF Diagnosis: 0: Disabled (OFF) 1: Enabled	0	0	Read/Write
[4]	Unused	0	0	Read
[3]	Solenoid Load Configuration: 0: Low Side 1: High Side	0	User's setup	Read/Write
[2]	Current Feedback Control Mode: 0: HW Feedback 1: SW Feedback	0	User's setup	Read/Write
[1:0]	Output Slew Rate: 00: 0.4 V/µs 01: 1.0 V/µs 10: 4.0 V/µs 11: 8.0 V/µs	0	11	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

Configuration 2 - CONFIGURATION2

Address Channel_X_BaseAddress + 0x03

Type Read/Write

Description Configuration Register for channel configuration self-tests. Before restarting any tests, wait for the register to return to "0"

Table 9. CONFIGURATION2 register detail

Register bit	Field name/description	Default values	Typical conf.(1)	Type
[15:2]	Unused	All "0"	All "0"	Read
[1]	Solenoid Diag Self Test: Short, Open Load and PWM Check 0: Self Test Disabled 1: Self Test Enabled	0	0	Read/Write
[0]	GND_SOL loss self test 0: Self TestDisabled 1: Self Test Enabled	0	0	Read/Write

1. *Typical configuration for parallel mode (different configuration might be needed, depending on specific customer's application).*

1.2 Setup recommendations

It is mandatory to use only maximum Output Slew Rate setting: CONFIGURATION1[1:0] = 11.

In parallel mode, to avoid cross-conduction issues, a minimum ON time is recommended, depending on VBATP level; in particular, limitations suggested are the following:

- 15 µs @ VBATP = 19 V
- 20 µs @ VBATP = 35 V

This requires user's knowledge of VBAT maximum rating and load characteristics, in order to determine minimum allowable Current Setpoint, according to the procedure described in the next section.

1.2.1 Minimum Current Setpoint calculation

Given a load, with known resistance value R, and knowing VBATP value, full-on (unregulated) current can be calculated as:

$$Full\ On\ Current = \frac{VBATP}{R} \quad (1)$$

Regulated current on the load, can be expressed as function of PWM signal duty cycle:

$$I\_LOAD = Full\ On\ Current \times PWM\_DC \quad (2)$$

Minimum allowed I_LOAD is the current L9305 will regulate with minimum allowed TON (15 µs) and maximum VBATP and can be calculated joining previous expressions as follows:

$$minimum\ I\_LOAD = \left(\frac{maximum\ VBATP}{R}\right) \times \left(\frac{15\ \mu s}{T\_PWM}\right) \quad (3)$$

From this value, Current Setpoint to be written in CHX_SETPOINT register can be calculated as follows:

- HILOAD = 0 → normal current mode - single bit resolution = 0.25 mA

$$ch\ X\ setpoint = \frac{minimum\ I\_LOAD}{0.25} \quad (4)$$

- HILOAD = 1 → normal current mode - single bit resolution = 0.33 mA

$$ch\ X\ setpoint = \frac{minimum\ I\_LOAD}{0.33} \quad (5)$$

1.3 Operative hints

1.3.1 Channel enabling

For parallel mode operativity, the following settings must be written:

- **SERVENA[15:14] = 11b**
- **SOLENDR[7:0] = 10101010b**

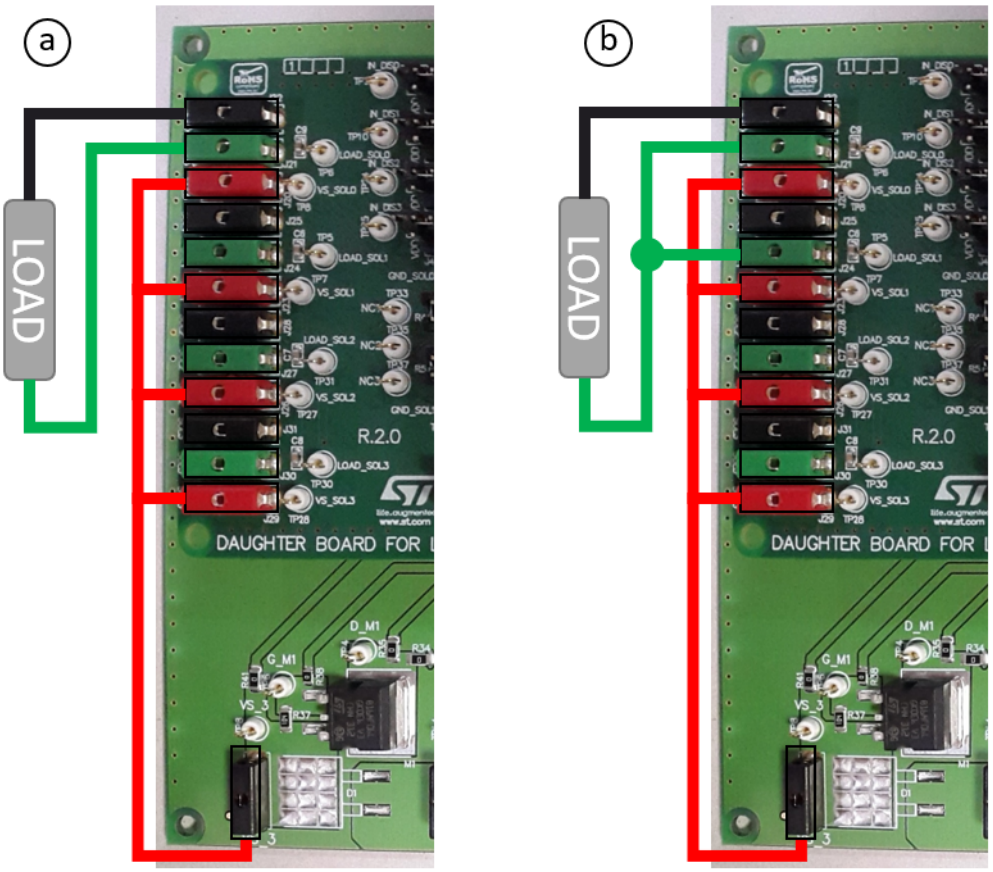
With these settings, ch2-3 and ch0-1 will be configured to operate in parallel and all channels will be enabled in pwm-mode. For each pair, current setup, pwm period and other settings will be the ones user configured, namely, for ch2 and ch0 (also known as “master” channels, while ch3 and ch1 are known as “slave” channels); see Section 1.1 Channel registers configuration details for detailed list of overridden settings.

Note that for parallel mode to operate with master’s parameters, both channels have to be enabled by their respective SOLENDR bits. If master channel of a pair is disabled, slave keeps working with its specific settings.

1.3.2 Load connection

Although working in parallel mode, a load can be phisically connected to either one of the two LOADx pins of the master/slave pair, as shown in Figure 1 (a), where load is connected to LOAD0 pin of the ch0-ch1 parallel configuration.

Figure 1. Load connection in parallel mode



Note: Be aware that, when parallel mode is used, reliable current reading will be available only on AVGCUR register of the channel to which load is phisically connected.

To avoid such problem, the simplest solution is to connect the load to both LOADx pins of the parallel channel, as shown in Figure 1 (b).

Parallel channels enabling bits can be modified while the solenoid is energized and the current regulation loop is working; should this happen, each channel will immediately start operating in stand-alone mode, according to its specific current setpoint, pwm period, KP and KI settings etc. General recommendation is to avoid runtime change of SERVENA[15:14] bits, however, according to the specific application, and being the user aware of the system behaviour during the parallel/stand-alone transition, it could be in principle perfomed.

2 Parallel mode operation - faults and diagnostic management details

2.1 Overcurrent Protection

In the following analysis of overcurrent protection during parallel mode operation, two possible scenarios will be considered:

- the situation of Load_solX pin short to battery;
- the situation of Load_solX pin short to ground.

When overcurrent protection is triggered, the following SPI register is involved:

Exceptions 1 - EXCEPTIONS1

Address	Channel_X_BaseAddress + 0x00
Type	Read Only
Description	Solenoid Driver Fault Status

Table 10. EXCEPTIONS1 register detail

Register bit	Field name/description	Default values	Type
[15]	Thermal Warning (T_WARN): 0: No Fault 1: Thermal Warning Present	0	Clear on Read
[14]	EEPROM CRC Error on CSA Calibration Data: 0: No Fault 1: CRC Error	0	Read
[13]	EEPROM CRC error on A2D trimming bits: 0: No Fault 1: CRC Error	0	Read
[12]	PWM Check Fault (ON State): 0: No Fault 1: Fault	0	Clear on Read
[11]	PWM Check Comp Mismatch (ON State): 0: No Fault 1: Fault	0	Clear on Read
[10:9]	Solenoid Logic BIST Status: (ADC mismatch, out of regulation, Solenoid driver control loop) 00: Idle 01: BIST running 10: BIST passed 11: BIST failed	0	Read
[8:7]	Solenoid Diag Self Test (OFF State): 00: Self Test pass 01: DIAG_LV comparator fail 10: DIAG OL comparator fail	0	Clear on Read

Register bit	Field name/description	Default values	Type
	11: Self Test fail		
[6]	Open Load (OFF State): 0: No Fault 1: Open load	0	Clear on Read
[5]	Short Detection (OFF State): 0: No Fault 1: Short Detected	0	Clear on Read
[4]	Solenoid ADC Mismatch monitor: 0: No Fault 1: Mismatch Fault Detected	0	Clear on Read
[3]	LS Clamp Active (ON state): 0: No Fault 1: LS Clamp Activated	0	Clear on Read
[2]	HS Over Current (ON State) 0: No Fault 1: HS Over Current	0	Clear on Read
[1]	LS Over Current (ON State) 0: No Fault 1: LS Over Current	0	Clear on Read
[0]	T_SD: (Thermal Shutdown) 0: No Fault 1: Thermal Shutdown Fault	0	Clear on Read

2.1.1 Load_solX pin short to VBATP

General test case settings:

SR for Vload_solX voltage: CONFIGURATION1, D[1:0] = 11 → 8V/µs

Current set point for each channel 0.4 A, SETPOINT, D[12:0] = 640h: total current in the load 0.8 A

PWM control frequency = 8 KHz (7.692 KHz), CTRLCFG, D[10:0] = 0Dh

Case A: Short to VBATP executed on Load_solX of master channel CHX.

No power-on reset occurs.

As soon as Vload_solX is shorted to VBATP, DUT master (CHX) and slave (CHX+1) channels go into Low Side Over Current protection.

The parallel couple of channels other than the faulty one (i.e. ‘X’) keep working according to their configurations.

Master channel X registers:

- LS_OC is set
- DriveState_CHX [1:0] is set ‘01’ → CHX tristate

Registers CHX_CONFIGURATION1, CHX_SETPOINT and CHX_CFG are kept with their value (not reset).

Slave channel X+1 registers:

- LS_OC is set
- DriveState_CHX+1 [1:0] is set ‘01’ → CHX+1 tristate

Registers CHX+1_CONFIGURATION1, CHX+1_SETPOINT and CHX+1_CFG are kept with their value (not reset).

If both channels are attempted to be re-enabled before removing short to VBATP fault, LS_OC bit is set only for master channel and both channels are tri-stated.

When both master and slave channels LS_OC bit is set, there can be 2 scenarios:

- After short to VBATP fault is removed, if master Channel X EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, both master and slave channel are kept tri-stated, until master channel EXCEPTIONS1 register is read and LS_OC cleared. After Master channel LS_OC bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.
- After short to VBATP fault is removed, If slave Channel X+1 EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, slave Channel X+1 remains tri-stated, while master channel CHX is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**). Slave channel remains tri-stated and provides no current until its EXCEPTIONS1 register is read and LS_OC cleared. After Slave channel LS_OC bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.

After short fault is removed, both Channel X and Channel X+1 EXCEPTIONS1 register must be read and then DUT channel X and channel X+1 needs to be re-enabled by microcontroller, before they can operate again.

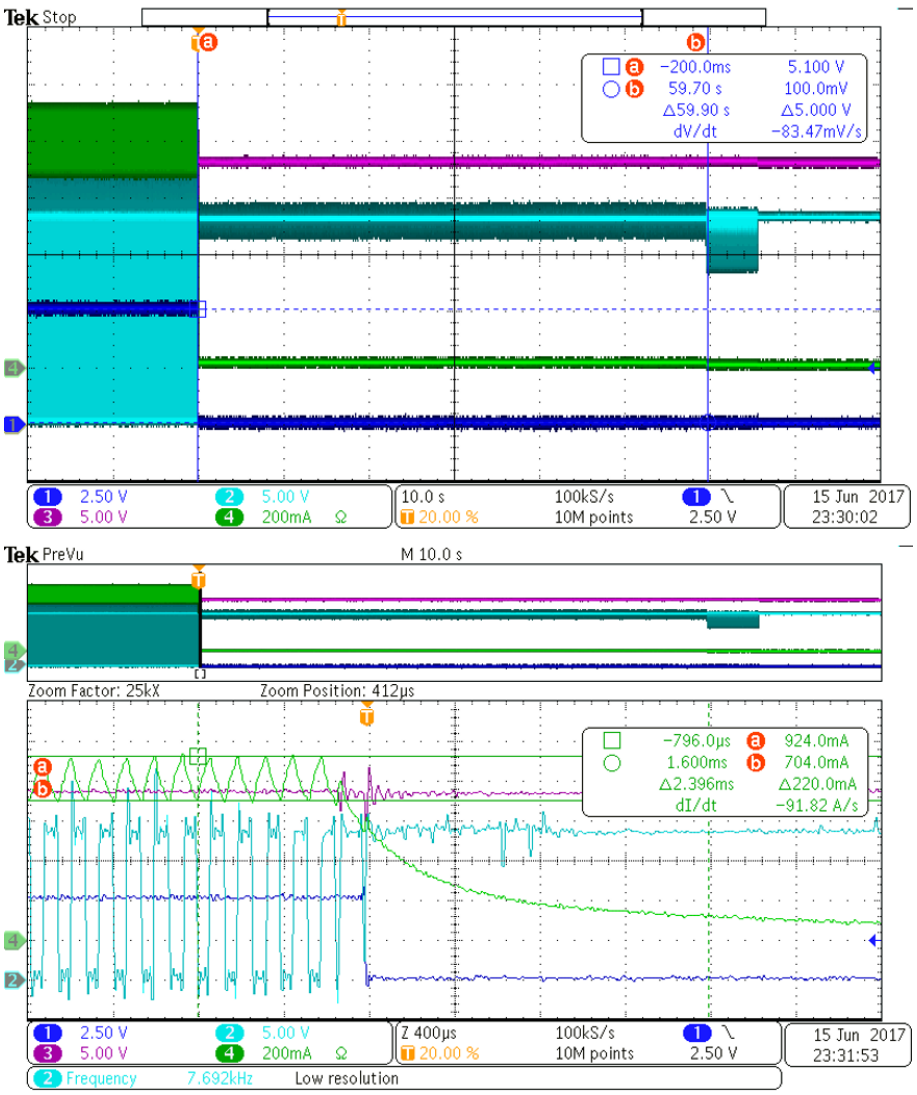
DUT is class C provided that it is managed by microcontroller, otherwise it is functional class D.

No damages on DUT, so after test DUT is still working as before.

Table 11. OVC test A, monitored variables

Measurement	Result	Expected by set-up	Product ISO 16750 class
PWM frequency	0-7.696 kHz	7.692kHz	Class C with micro/ Class D without micro
nPOR_flag	Not set	Not set	Class A
Charge_Pump_UV	Not set	Not set	Class A
FAULTn	set	set	Class C with micro/ Class D without micro
LS_OC	set	set	Class C with micro/ Class D without micro
DriveState_CHX [1:0]	‘01’	‘01’	Class C with micro/ Class D without micro

Figure 2. **Vload_sol0 short to VBATP - Load current**



Legenda: Ch1: FAULTn, Ch2: Vload_sol0, Ch3: VBATP, Ch4: Iload

Case B: Short to VBATP executed on Load_solX+1 of master channel CHX+1.

No power-on reset occurs.

As soon as Vload_solX is shorted to VBATP, DUT master (CHX) and slave (CHX+1) channels go into Low Side Over Current protection.

The parallel couple of channels other than the faulty one (i.e. ‘X’) keep working according to their configurations.

Master channel X registers:

- LS_OC is not set
- DriveState_CHX [1:0] is set ‘01’ → CHX tristate

Registers CHX_CONFIGURATION1, CHX_SETPOINT and CHX_CFG are kept with their value (not reset).

Slave channel X+1 registers:

- LS_OC is set
- DriveState_CHX+1 [1:0] is set ‘01’ → CHX+1 tristate

Registers CHX+1_CONFIGURATION1, CHX+1_SETPOINT and CHX+1_CFG are kept with their value (not reset).

If both channels are attempted to be re-enabled before removing short to VBATP fault, LS_OC bit is set for both master and slave channels and they are tri-stated.

When both master and slave channels LS_OC bit is set, there can be 2 scenarios:

- After short to VBATP fault is removed, if master Channel X EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, both master and slave channel are kept tri-stated, until master channel EXCEPTIONS1 register is read and LS_OC cleared. After Master channel LS_OC bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.
- After short to VBATP fault is removed, If slave Channel X+1 EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, slave Channel X+1 remains tri-stated, while master channel CHX is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**). Slave channel remains tri-stated and provides no current until its EXCEPTIONS1 register is read and LS_OC cleared. After Slave channel LS_OC bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.

After short fault is removed, both Channel X and Channel X+1 EXCEPTIONS1 register must be read and then DUT channel X and channel X+1need to be re-enabled by microcontroller, before they can operate again properly.

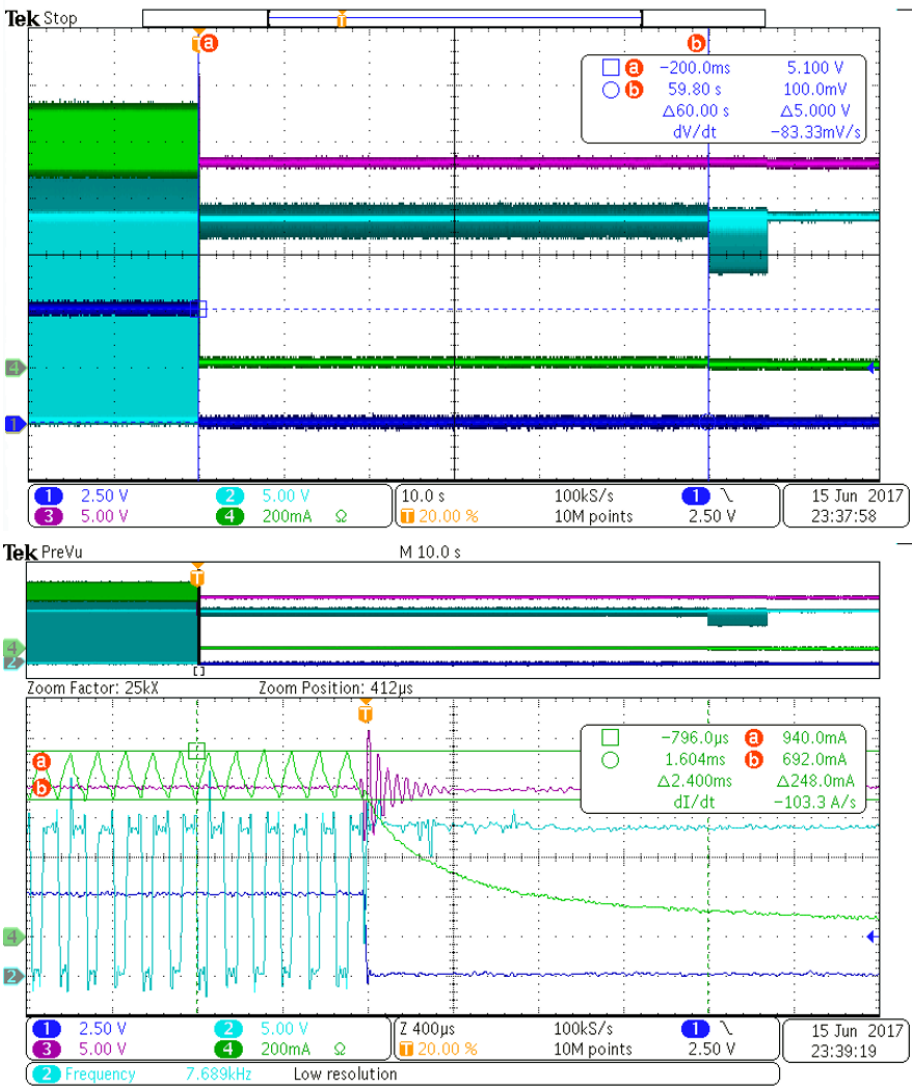
DUT is class C provided that it is managed by microcontroller, otherwise it is functional class D.

No damages on DUT, so after test DUT is still working as before.

Table 12. OVC test B, monitored variables

Measurement	Result	Expected by set-up	Product ISO 16750 class
PWM frequency	0-7.696 kHz	7.692kHz	Class C with micro/ Class D without micro
nPOR_flag	Not set	Not set	Class A
Charge_Pump_UV	Not set	Not set	Class A
FAULTn	set	set	Class C with micro/ Class D without micro
LS_OC	set	set	Class C with micro/ Class D without micro
DriveState_CHX [1:0]	‘01’	‘01’	Class C with micro/ Class D without micro

Figure 3. **Vload_sol1 short to VBATP - Load current**



Legenda: Ch1: FAULTn, Ch2: Vload_sol1, Ch3: VBATP, Ch4: Iload

2.1.2 Load_solX pin short to ground

General test case settings:

- SR for Vload_solX voltage: CONFIGURATION1, D[1:0] = 11 → 8V/µs
- Current set point for each channel 0.4 A, SETPOINT, D[12:0] = 640h: total current in the load 0.8 A
- PWM control frequency = 8 KHz (7.692 KHz) , CTRLCFG, D[10:0] = 0Dh

Case A: Short to GND executed on Load_solX of master channel CHX.

No power-on reset occurs.

As soon as Vload_solX is shorted to GND, DUT master (CHX) and slave (CHX+1) channels go into High Side Over Current protection.

The parallel couple of channels other than the faulty one (i.e. ‘X’) keep working according to their configurations.

Master channel X registers:

- HS_OC is set
- DriveState_CHX [1:0] is set ‘01’ → CHX tristate

Registers CHX_CONFIGURATION1, CHX_SETPOINT and CHX_CFG are kept with their value (not reset).

Slave channel X+1 registers:

- HS_OC is not set
- DriveState_CHX+1 [1:0] is set ‘01’ → CHX+1 tristate

Registers CHX+1_CONFIGURATION1, CHX+1_SETPOINT and CHX+1_CFG are kept with their value (not reset).

If both channels are attempted to be re-enabled before removing short to GND fault, HS_OC bit is set for both master and slave channels and they are tri-stated.

When both master and slave channels HS_OC bit is set, there can be 2 scenarios:

- After short to GND fault is removed, if master Channel X EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, both master and slave channel are kept tri-stated, until master channel EXCEPTIONS1 register is read and HS_OC cleared. After Master channel HS_OC bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.
- After short to GND fault is removed, If slave Channel X+1 EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, slave Channel X+1 remains tri-stated, while master channel CHX is re-enabled and it provides load with global couple setpoint+100mA current (**NOK**). Slave channel remains tri-stated and provides no current until its EXCEPTIONS1 register is read and HS_OC cleared. After Slave channel HS_OC bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.

After short fault is removed, both Channel X and Channel X+1 EXCEPTIONS1 register must be read and then DUT channel X and channel X+1need to be re-enabled by microcontroller, before they can operate again properly.

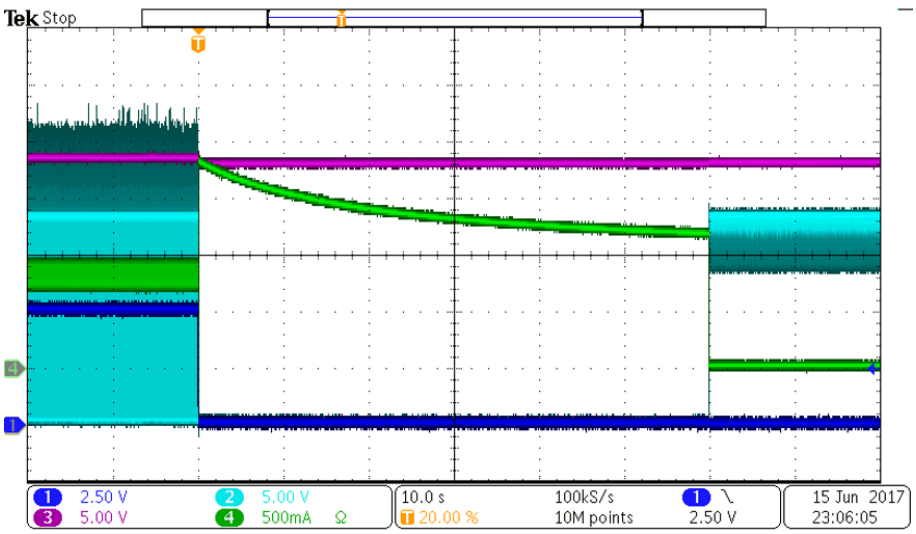
DUT is class C provided that it is managed by microcontroller, otherwise it is functional class D.

No damages on DUT, so after test DUT is still working as before.

Table 13. STG test A, monitored variables

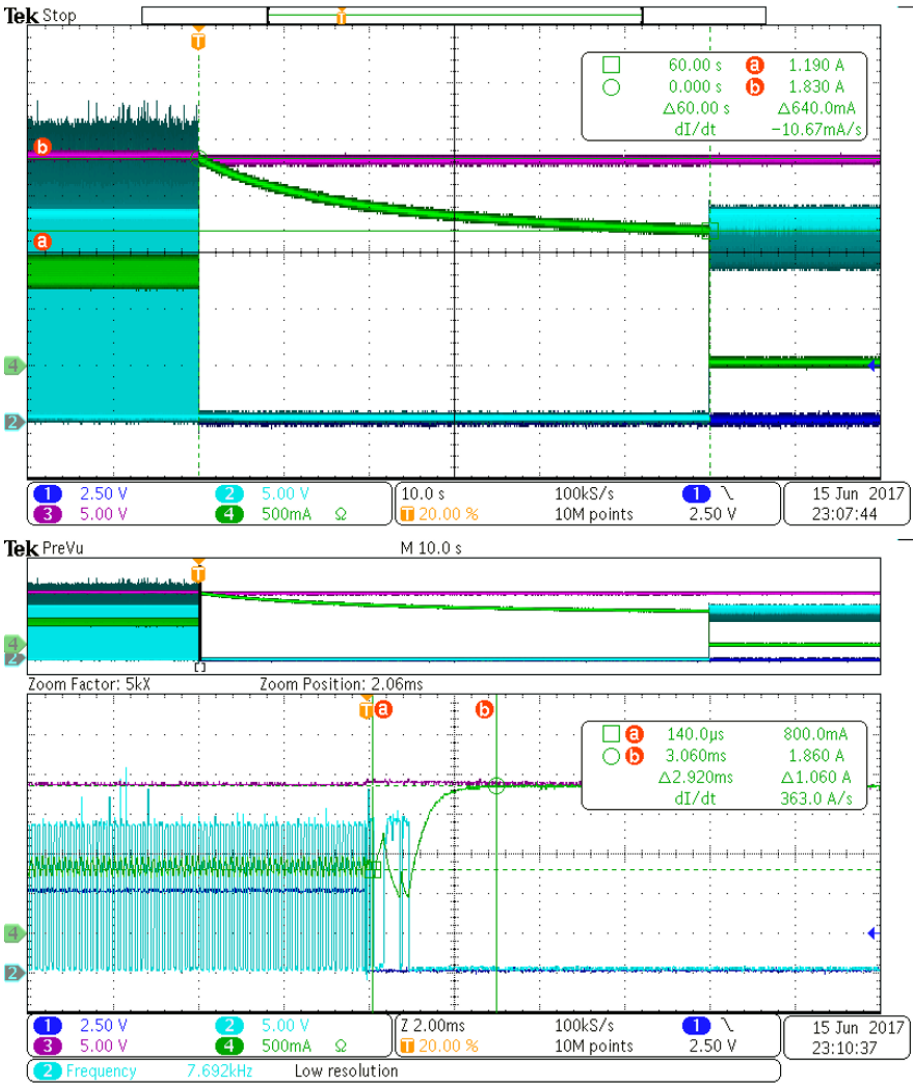
Measurement	Result	Expected by set-up	Product ISO 16750 class
PWM frequency	0-7.696 kHz	7.692kHz	Class C with micro/ Class D without micro
nPOR_flag	Not set	Not set	Class A
Charge_Pump_UV	Not set	Not set	Class A
FAULTn	set	set	Class C with micro/ Class D without micro
HS_OC	set	set	Class C with micro/ Class D without micro
DriveState_CHX [1:0]	‘01’	‘01’	Class C with micro/ Class D without micro

Figure 4. Vload_sol0 short to GND



Legenda: Ch1: FAULTn, Ch2: Vload_sol0, Ch3: VBATP, Ch4: Iload

Figure 5. Vload_sol0 short to GND - Load current details



Legenda: Ch1: FAULTn, Ch2: Vload_sol0, Ch3: VBATP, Ch4: Iload

Case B: Short to GND executed on Load_solX+1 of slave channel CHX+1.

No power-on reset occurs.

As soon as Vload_solX is shorted to GND, DUT master (CHX) and slave (CHX+1) channels go into High Side Over Current protection.

The parallel couple of channels other than the faulty one (i.e. ‘X’) keep working according to their configurations.

Master channel X registers:

- HS_OC is not set
- DriveState_CHX [1:0] is set ‘01’ à CHX tristate

Registers CHX_CONFIGURATION1, CHX_SETPOINT and CHX_CFG are kept with their value (not reset).

Slave channel X+1 registers:

- HS_OC is set
- DriveState_CHX+1 [1:0] is set ‘01’ à CHX+1 tristate

Registers CHX+1_CONFIGURATION1, CHX+1_SETPOINT and CHX+1_CFG are kept with their value (not reset).

If both channels are attempted to be re-enabled before removing short to GND fault, HS_OC bit is set for both master and slave channels and they are tri-stated.

When both master and slave channels HS_OC bit is set, there can be 2 scenarios:

- After short to GND fault is removed, if master Channel X EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, both master and slave channel are kept tri-stated, until master channel EXCEPTIONS1 register is read and HS_OC cleared. After Master channel HS_OC bit is cleared on read, the couple CHX(master) and CHX+1(slave) operate properly.
- After short to GND fault is removed, If slave Channel X+1 EXCEPTIONS1 register is not read and both Channel X and Channel X+1 are attempted to be re-enabled, slave Channel X+1 remains tri-stated, while master channel CHX is re-enabled and it provides load with global couple setpoint+100mA current (**NOK**). Slave channel remains tri-stated and provides no current until its EXCEPTIONS1 register is read and HS_OC cleared. After Slave channel HS_OC bit is cleared on read, the couple CHX(master) and CHX+1(slave) operate properly.

After short fault is removed, both Channel X and Channel X+1 EXCEPTIONS1 register must be read and then DUT channel X and channel X+1need to be re-enabled by microcontroller, before they can operate again properly.

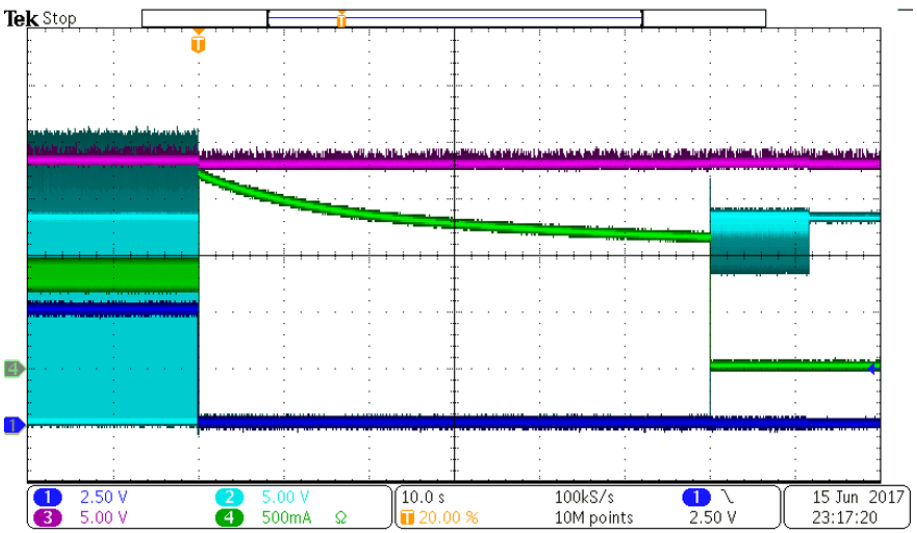
DUT is class C provided that it is managed by microcontroller, otherwise it is functional class D.

No damages on DUT, so after test DUT is still working as before.

Table 14. STG test B, monitored variables

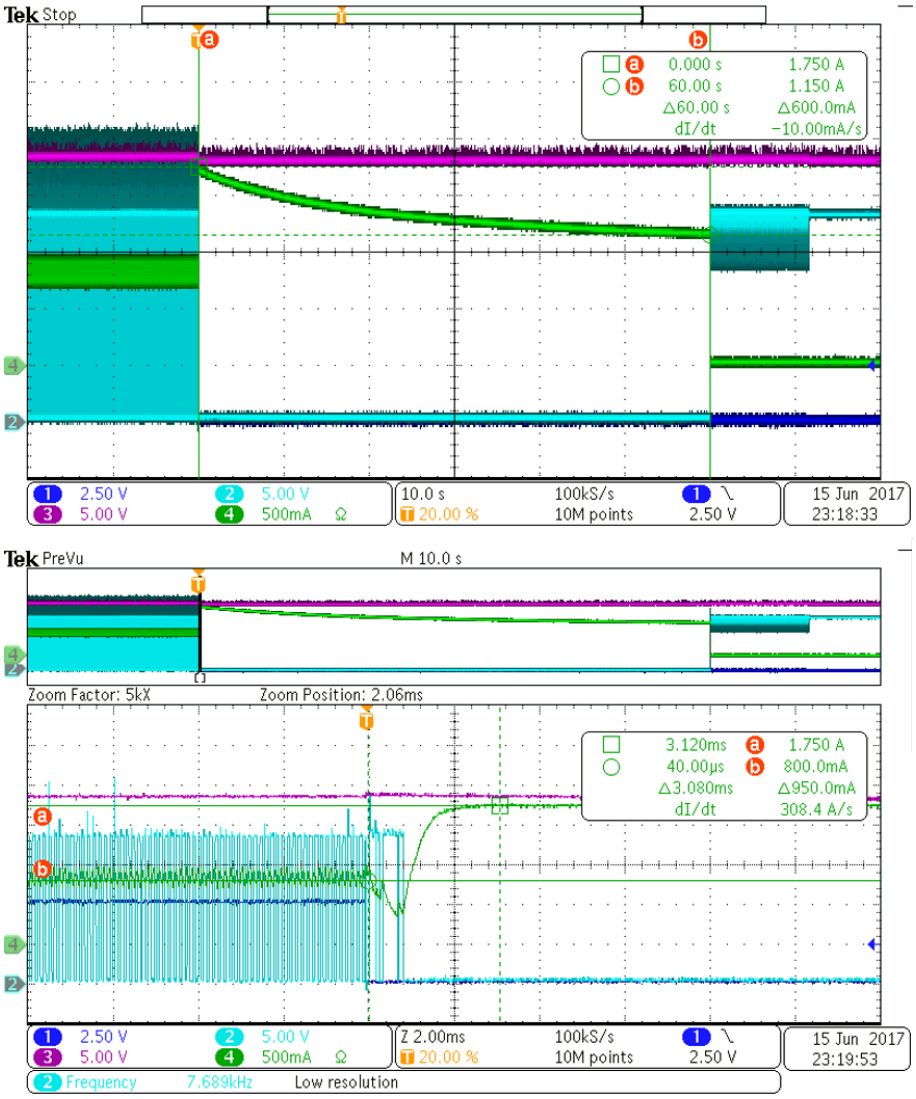
Measurement	Result	Expected by set-up	Product ISO 16750 class
PWM frequency	0-7.696 kHz	7.692kHz	Class C with micro/ Class D without micro
nPOR_flag	Not set	Not set	Class A
Charge_Pump_UV	Not set	Not set	Class A
FAULTn	set	set	Class C with micro/ Class D without micro
HS_OC	set	set	Class C with micro/ Class D without micro
DriveState_CHX [1:0]	‘01’	‘01’	Class C with micro/ Class D without micro

Figure 6. Vload_sol1 short to GND



Legenda: Ch1: FAULTn, Ch2: Vload_sol1, Ch3: VBATP, Ch4: Iload

Figure 7. **Vload_sol1 short to GND - Load current details**



Legenda: Ch1: FAULTn, Ch2: Vload_sol1, Ch3: VBATP, Ch4: Iload

2.2 Low Side Clamping protection

When a solenoid channel is configured for low side operation, current recirculation occurs through the internal high side transistor. If the supply Vs_solX of the high side driver is lost, the voltage at LOAD_SOLx pin can become unpredictable and possibly exceed the absolute rating of the device. To prevent this condition from damaging the device, the low side driver has an integrated clamping circuit to limit the peak voltage.

Should the low side clamping structure be activated during normal operation (i.e. solenoid supply line within normal operating range), the channel is put in tri-state (setting the Solenoid Driver Status bits to 01) and the Low Side Clamp Active fault flag D[3] is set in the EXCEPTIONS1 register. To restart the channel, the MCU must clear the fault by reading the EXCEPTIONS1 register and re-enable the channel.

The involved SPI register for LS Clamping protection is still EXCEPTIONS1 (refer to description in Section 2.1 Overcurrent Protection).

In order to analyze LS Clamping protection the scenario of Vs_solX loss during parallel mode operation has been considered.

2.2.1 Loss of Vs_solX connection - parallel solenoid driver channels configuration

General test case settings:

- SR for Vload_solX voltage: CONFIGURATION1, D[1:0] = 11 → 8V/µs
- Current set point for each channel 0.4 A, SETPOINT, D[12:0] = 640h: total current in the load 0.8 A
- PWM control frequency = 8 KHz (7.692 KHz) , CTRLCFG, D[10:0] = 0Dh

Case A: Open fault executed on Vs_solX connection of the master channel (CHX) of the solenoid driver couple.

Solenoid load is provided with a total current around 850 mA.

In master channel CHX:

- In CHX_EXCEPTIONS1 Solenoid_ADC_Mismatch bit is set ‘1’
- In CHX_EXCEPTIONS2 HS-LS_Compare_fault bit is set ‘1’
- AVGCUR register returns a current around 300 mA
- PWM_SENSE register returns a 130 µs as a PWM period

In slave channel CHX+1:

- In CHX+1_EXCEPTIONS1 Solenoid_ADC_Mismatch bit is set ‘1’
- In CHX+1_EXCEPTIONS2 HS-LS_Compare_fault bit is set ‘1’
- In CHX+1_EXCEPTIONS2 Out_of_Regulation fault bit is set ’1’
- AVGCUR register returns a current around 550 mA
- PWM_SENSE register returns a 130 µs as a PWM period

Once the connection on Vs_solX of the master channel (CHX) is restored, the solenoid driver couple get back working automatically as before the fault was injected.

Case B: Open fault executed on Vs_solX connection of the slave channel (CHX+1) of the solenoid driver couple.

Solenoid load is provided with a total current around 850 mA.

In master channel CHX:

- In CHX_EXCEPTIONS2 HS-LS_Compare_fault bit is set ‘1’
- AVGCUR register returns a current around 550 mA
- PWM_SENSE register returns a 130 µs as a PWM period

In slave channel CHX+1:

- In CHX+1_EXCEPTIONS1 Solenoid_ADC_Mismatch bit is set ‘1’
- In CHX+1_EXCEPTIONS2 HS-LS_Compare_fault bit is set ‘1’
- AVGCUR register returns a current around 300 mA
- PWM_SENSE register returns a 130 µs as a PWM period

Once the connection on Vs_solX of the master channel (CHX+1) is restored, the solenoid driver couple get back working automatically as before the fault was injected.

Case C: Open fault executed on Vs_solX connection of both master (CHX) and slave channel (CHX+1) of the solenoid driver couple. Both master and slave driver channels of the couple under test are tri-stated (SOLENDR DriverState_CHx[1:0] = ’01’. Solenoid load driven by the couple under test is provided with a total current around 0 mA.

Solenoid driver couple other than the tested one keep on operating correctly.

In master channel CHX:

- In CHX_EXCEPTIONS1 Solenoid_ADC_Mismatch bit is set ‘1’
- In CHX_EXCEPTIONS1 LS_Clamp_Active is set ‘1’
- In CHX_EXCEPTIONS2 HS-LS_Compare_fault bit is set ‘1’
- AVGCUR register returns a current around 0 mA
- PWM_SENSE register returns a PWM period around 130 µs depending on the time frame when open fault has been executed
- TMOUT bit is set ‘1’ sometimes

In slave channel CHX+1:

- In CHX+1_EXCEPTIONS1 Solenoid_ADC_Mismatch bit is set
- In CHX+1_EXCEPTIONS1 LS_Clamp_Active is set ‘1’

- In CHX+1_EXCEPTIONS2 HS-LS_Compare_fault bit is set
- AVGCUR register returns a current around 300 mA
- PWM_SENSE register returns a PWM period around 130 µs depending on the time frame when open fault has been executed
- TMOUT bit is set ‘1’ sometimes

Once the connection on Vs_solX of both master (CHX) and slave channel (CHX+1) is restored, user should read LS_Clamp_Active bit in EXCEPTIONS1 register of both master (CHX) and slave channel (CHX+1) and then set DriveState_CHX[1:0] and DriveState_CHX+1[1:0] to ‘10’, in order to the solenoid driver couple get back working as before the fault was injected.

- If only master channel CHX LS_Clamp_Active bit in EXCEPTIONS1 register is read and both channels are attempted to be re-enabled → master channel is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**).

  Slave channel remains tri-stated and provides no current until its LS_Clamp_Active bit is read and cleared.

  After slave channel LS_Clamp_Active bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.
- If only slave channel CHX+1 LS_Clamp_Active bit in EXCEPTIONS1 register is read and both channels are attempted to be re-enabled → both channels of the couple cannot be re-enabled and are kept tri-stated, until master channel CHX LS_Clamp_Active bit in EXCEPTIONS1 register is read and cleared.

  After master channel LS_Clamp_Active bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.

When only Vs_solX connection of master (CHX) channel is restored:

- If only master channel CHX LS_Clamp_Active bit in EXCEPTIONS1 register is read and both channels are attempted to be re-enabled → master channel is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**).

  Slave channel remains tri-stated and provides no current until its LS_Clamp_Active bit is read and cleared.

  After slave channel LS_Clamp_Active bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate as in **Case B**.
- If only slave channel CHX+1 LS_Clamp_Active bit in EXCEPTIONS1 register is read and both channels are attempted to be re-enabled → both channels of the couple cannot be re-enabled and are kept tri-stated, until master channel CHX LS_Clamp_Active bit in EXCEPTIONS1 register is read and cleared. After master channel LS_Clamp_Active bit is cleared on read, the couple CHX(master) and CHX+1(slave) operate the same as in **Case B**.

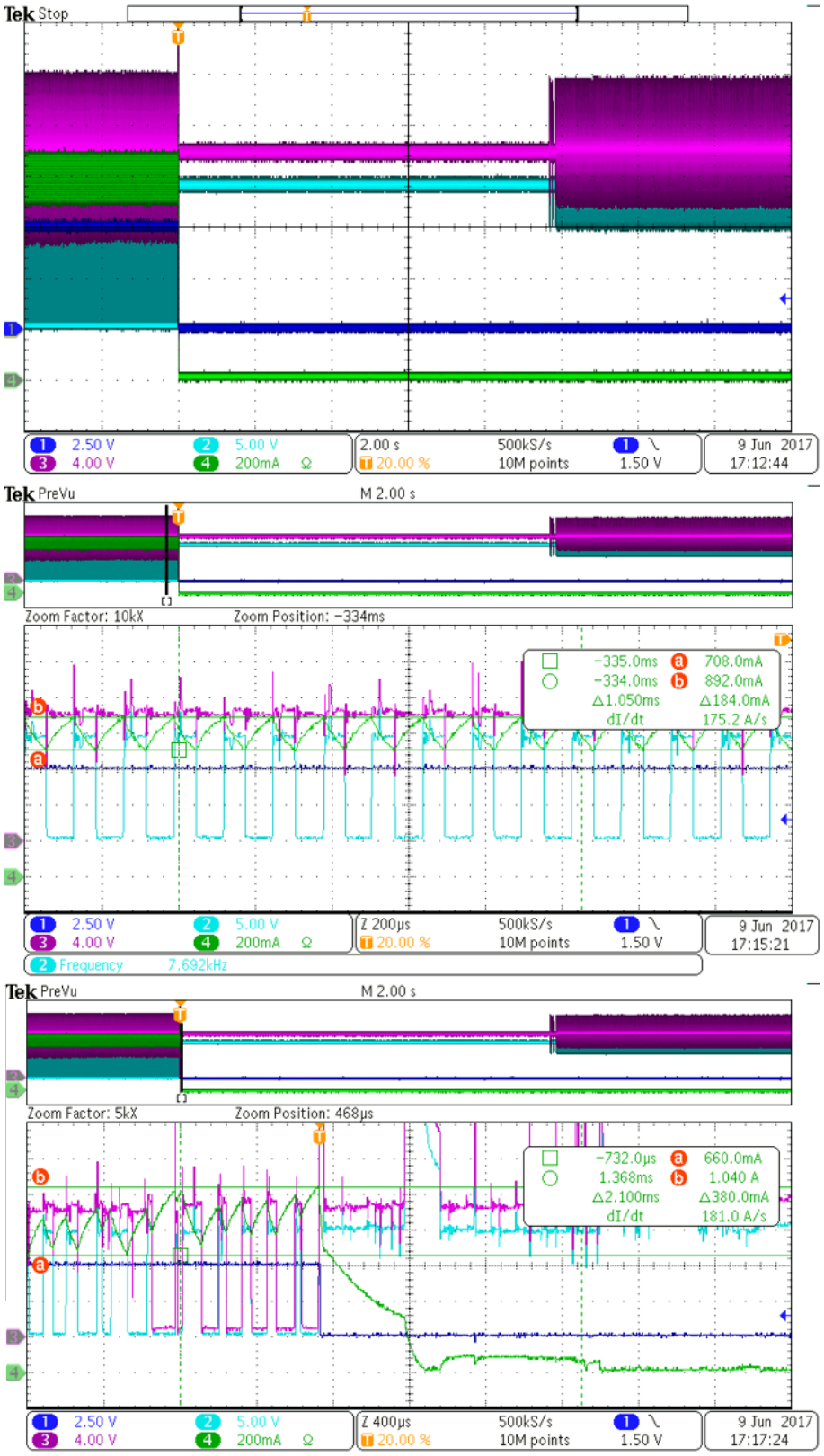
When only Vs_solX connection of slave (CHX+1) channel is restored:

- If only master channel CHX LS_Clamp_Active bit in EXCEPTIONS1 register is read and both channels are attempted to be re-enabled → master channel is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**).

  Slave channel remains tri-stated and provides no current until its LS_Clamp_Active bit is read and cleared.

  After slave channel LS_Clamp_Active bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate as in **Case A**.
- If only slave channel CHX+1 LS_Clamp_Active bit in EXCEPTIONS1 register is read and both channels are attempted to be re-enabled → both channels of the couple cannot be re-enabled and are kept tri-stated, until master channel CHX LS_Clamp_Active bit in EXCEPTIONS1 register is read and cleared. After master channel LS_Clamp_Active bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate the same as in **Case A**.

Figure 8. **Vs_solX connection open on both master and slave channels - LS_Clamp_Active bit unmasked**



Legenda: Ch1: FAULTn, Ch2: Vload_sol0, Ch3: Vs_sol0, Ch4: Iload

2.3 Loss of load ground connection diagnostic

In the following analysis the loss of GND_solX pin will be considered while L9305 is operating parallel mode.
The following SPI register is involved for such a diagnostic.

Exceptions 2 - EXCEPTIONS2

Address Channel_X_BaseAddress + 0x01
Type Read Only
Description Solenoid Driver Fault Status

Table 15. EXCEPTIONS2 register detail

Register bit	Field name/description	Default values	Type
[15:6]	Unused	All "0"	Read
[5]	GND_SOL Loss Self Test Status 0: Test Complete 1: Test Running	0	Clear on Read
[4]	Out of regulation 0: No Fault 1: Out of Regulation After 8 PWM Cycles	0	Clear on Read
[3]	GND_SOL loss fault 0: No Fault 1: Solenoid Ground Loss Detected	0	Clear on Read
[2]	RAM CRC error 0: No Fault 1: CRC Fault Detected on RAM Read	0	Clear on Read
[1]	HS/LS compare Fault: 0: No Fault 1: Fault Detected	0	Clear on Read
[0]	Configuration Register Monitor: 0: No Fault 1: Fault Detected	0	Clear on Read

2.3.1 Loss of GND_solX Connection - parallel solenoid driver channels configuration

General test case settings:

- SR for Vload_solX voltage: CONFIGURATION1, D[1:0] = 11 → 8 V/µs
- Current set point for each channel 0.4 A, SETPOINT, D[12:0] = 640h: total current in the load 0.8 A
- PWM control frequency = 8 KHz (7.692 KHz) , CTRLCFG, D[10:0] = 0Dh

When solenoid load ground loss is induced on either master (CHX) or slave (CHX+1) channel of the couple, the following scenario occurs in both cases.

- Channel X and Channel X+1 (couple of channels under test) currents go to 0 A, as soon as GND_solX connection is broken; other couple of channels go on operating normally.

- During GND_solX interruption:
  - For the couple of channels under test SOLENDR register DriverState_CHX and DriverState_CHX+1 are set ‘01’ → CHX and CHX+1 of the same couple are put tristate
  - For the couple of channels under test, CHX_AVGCUR = 0 DEC (0 HEX) fix and CHX+1_AVGCUR = 0 DEC (0 HEX) fix → a current of 0 mA is internally sensed
  - CHX_PWMSENSE and CHX+1_PWMSENSE return a PWM period, which is randomly different every time the test is repeated, but it is fix if PWM period readings are repeated more times during the same test (**NOK**). This is due to the fact that by construction asynchronous open GND_solX or GND_solX+1 event occurs during PWM and affects PWM period calculation.
  - TMOUT bit is set for both channels of the couple under test.
  - By monitor circuit architecture, GND_SOL_loss_fault bit is set, but it is cleared on read even if GND_solX connection is still broken (**NOK**).

Nevertheless there is the following difference when the load ground loss fault is injected on either the master channel or the slave channel of the couple.

When load GND loss test is executed on master solenoid driver channel of the couple (CHX):

- If GND_solX connection is still broken and only slave solenoid driver channel is attempted to be re-enabled before or after reading GND_SOL_loss_fault bit of master channel, slave channel CHX+1 is re-enabled and it provides load with only its set-point current (**NOK**).
- If GND_solX connection is still broken, both channels of the couple cannot be re-enabled even if the GND_SOL_loss_fault bit has been read: when re-enable of both channel of the couple is attempted, none of the channels of the couple is enabled and master channel GND_SOL_loss_fault bit is set again even if it has been cleared on read.
  - Master channel CHX GND_SOL_loss_fault bit is set again even if it has been cleared on read and both channels are kept tristate.
- After the connection is restored, Channel X needs GND_SOL_loss_fault bit to be read and DriverState_CHX/CHX+1 to be set ’10’, in order to the couple CHX and CHX+1 operate parallel mode properly.

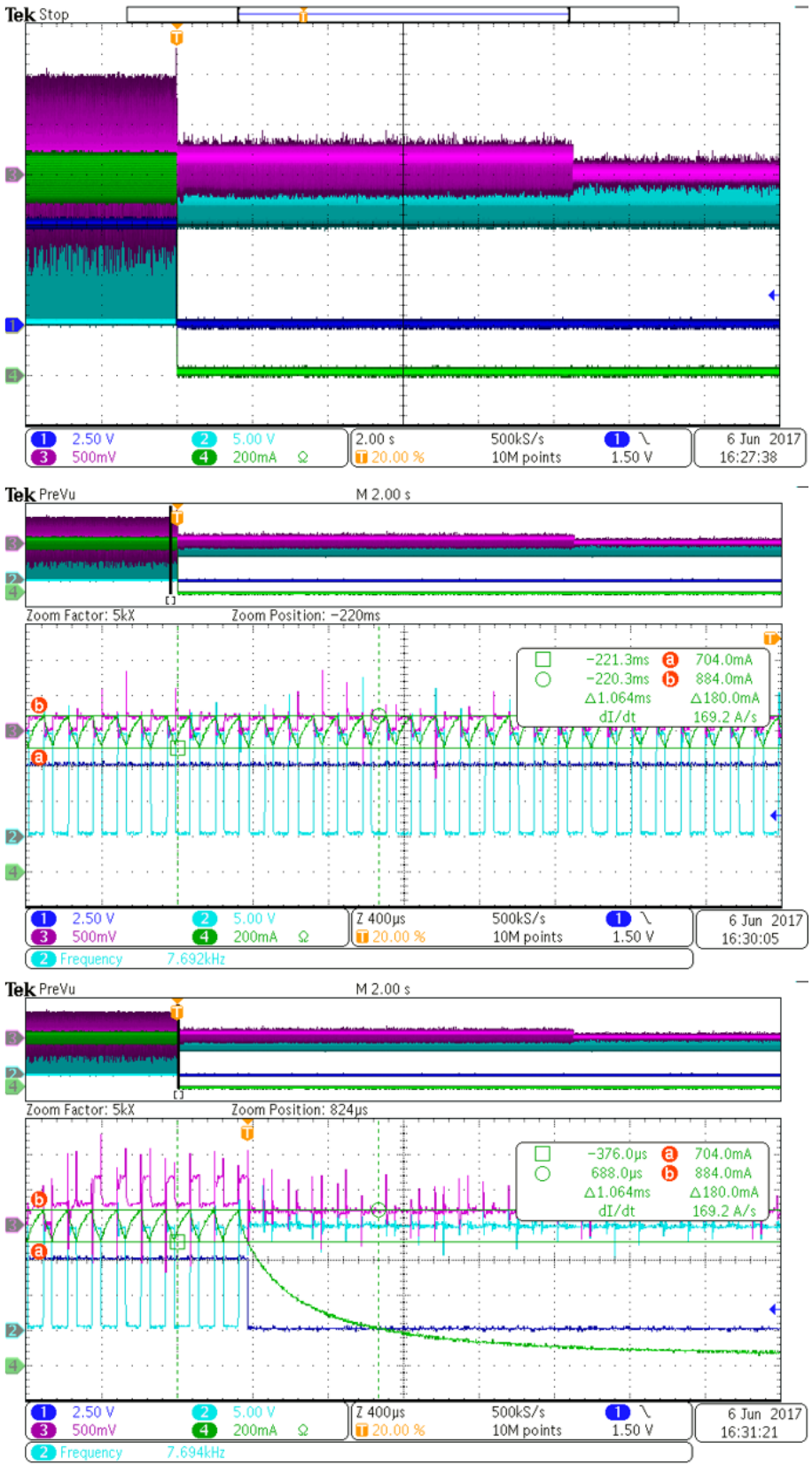
When GND loss test is executed on slave solenoid driver channel of the couple (CHX+1):

- If GND_solX+1 connection is still broken and only master solenoid driver channel is attempted to be re-enabled before or after reading GND_SOL_loss_fault bit of slave channel, master channel is re-enabled and it provides load with only its setpoint current (**NOK**).
- If GND_solX+1 connection is still broken and both channels of the couple are attempted to be re-enabled before or after the GND_SOL_loss_fault bit has been cleared on read: master channel is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**).
  - Slave channel GND_SOL_loss_fault bit is set again even if it has been cleared on read and if it is read, master channel is put tristate again.
- If GND_solX+1 connection is restored and both channels of the couple are attempted to be re-enabled before the GND_SOL_loss_fault bit has been cleared on read: master channel is re-enabled and it provides load with global couple setpoint + 100 mA current (**NOK**). Slave channel remains tri-stated and provides no current until its GND_SOL_loss_fault bit is read and cleared.
  - After Slave channel GND_SOL_loss_fault bit is cleared on read, the couple CHX (master) and CHX+1 (slave) operate properly.
- After the connection is restored, Channel X+1 needs GND_SOL_loss_fault bit to be read and DriverState_CHX/CHX+1 to be set ’10’, in order to the couple CHX and CHX+1 operate properly.

In order to guarantee proper operation of the parallel solenoid driver channels couple, external MCU must always read GND_SOL_loss_fault bit before and after each couple re-enable attempt.

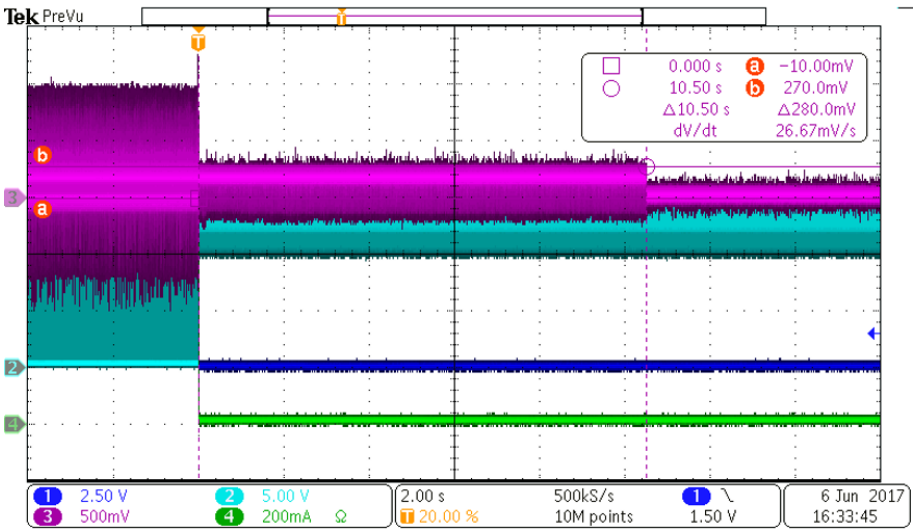
If GND_SOL_loss_fault bit is unmasked, then FAULTn goes low when GND_solX is unconnected: it needs GND_SOL_loss_fault bit to be read for FAULTn getting back high.

Figure 9. **GND_solX connection open - GND_SOL_loss_fault bit unmasked**



Legenda: Ch1: FAULTn, Ch2: GND_sol0, Ch3: Vload_sol0, Ch4: Iload_sol0

Figure 10. **GND_solX connection open - GND_solX voltage details**



Legenda: Ch1: FAULTn, Ch2: GND_sol0, Ch3: Vload_sol0, Ch4: Iload_sol0

2.4 Loss of load connection

Loss of load connection during parallel mode operation is analyzed, when driver channels are on.

There is no ON Diagnostic managing open load connection.

2.4.1 Loss of load connection - parallel solenoid driver channels

General test case settings:

- SR for Vload_solX voltage: CONFIGURATION1, D[1:0] = 11 → 8 V/µs
- Current set point for each channel 0.4A, SETPOINT, D[12:0] = 640h: total current in the load 0.8 A
- PWM control frequency = 8KHz (7.692KHz) , CTRLCFG, D[10:0] = 0Dh

Case A: Open fault executed on Load_solX connection of the master channel (CHX) of the solenoid driver couple.

Master Channel X current goes to 0 A, as soon as load connection is broken and the whole load driver couple current is sustained by the slave channel (CHX+1); other couple channels go on operating normally.

During load connection interruption, for master CHX:

- CHX_AVGCUR = 4÷16380 DEC (3FFC HEX) fix → a current of -1÷1 mA is internally sensed
- PWM period of 130 is sensed by CHX_PWMSENSE
- TMOUT bit is not set

During load connection interruption, for slave CHX+1:

- CHX+1_AVGCUR≈3200 DEC (C80 HEX) → a current around 800 mA is internally sensed
- PWM period of 130 is sensed by CHX+1_PWMSENSE
- TMOUT bit is not set
- Out_of_regulation bit is set

After the connection is restored, Channel X automatically re-starts operating the same way as before interruption without any re-enabling step.

Case B: Open fault executed on Load_solX+1 connection of the slave channel (CHX+1) of the solenoid driver couple.

Slave Channel X+1 current goes to 0 A, as soon as load connection is broken and the whole load driver couple current is sustained by the master channel CHX; other couple channels go on operating normally.

During load connection interruption, for master CHX:

- CHX_AVGCUR≈3200 DEC (C80 HEX) --> a current around 800 mA is internally sensed
- PWM period of 130 is sensed by CHX_PWMSENSE

- TMOUT bit is not set

During load connection interruption, for slave CHX+1:

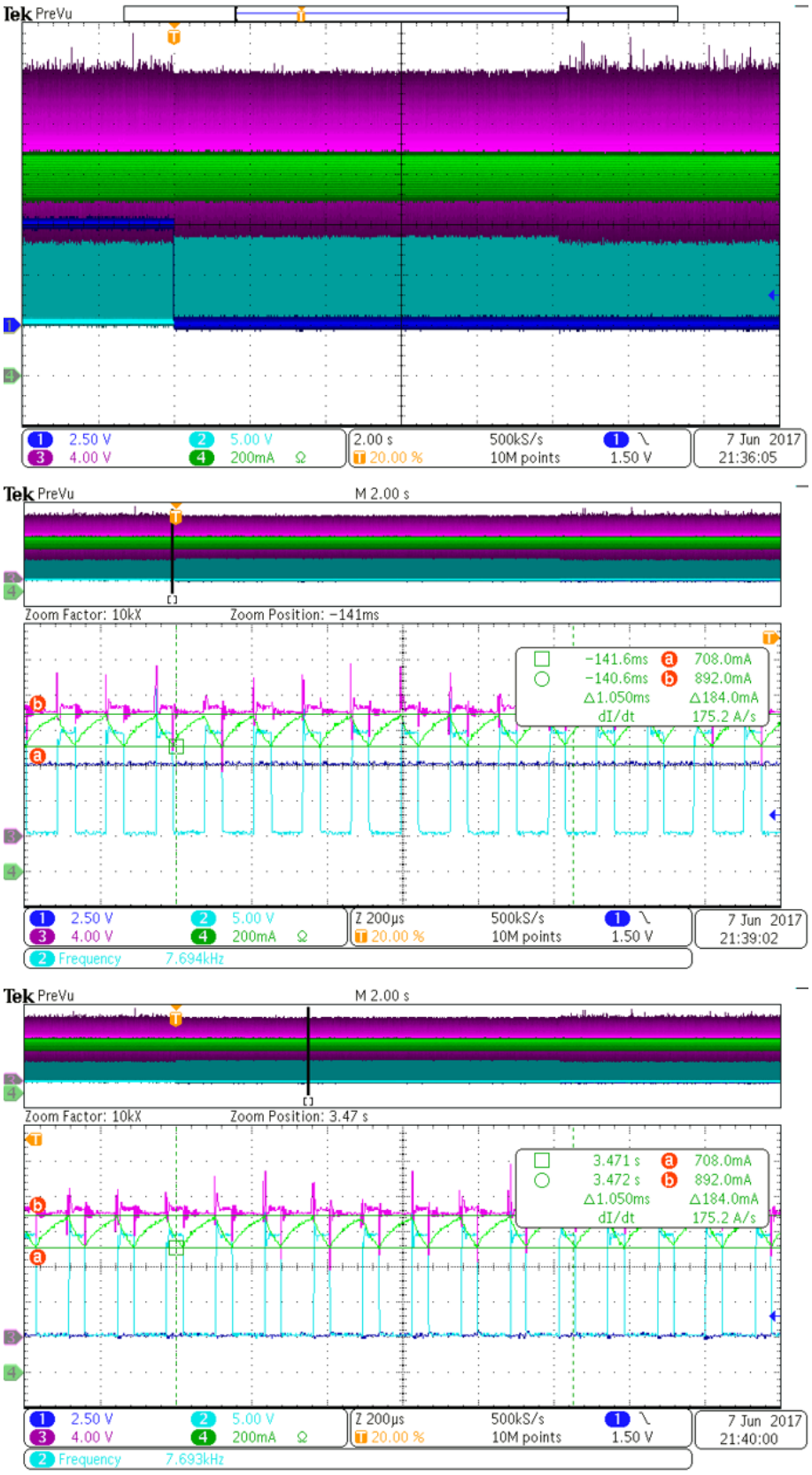
- CHX+1_AVGCUR = 4÷16380 DEC (3FFC HEX) fix → a current of -1÷1 mA is internally sensed
- PWM period of 130 is sensed by CHX+1_PWMSENSE
- TMOUT bit is not set
- Out_of_regulation bit is set

After the connection is restored, Channel X+1 automatically re-starts operating the same way as before interruption without any re-enabling step.

In both cases Out of regulation bit is set on slave CH_X+1 EXCEPTIONS2 register.

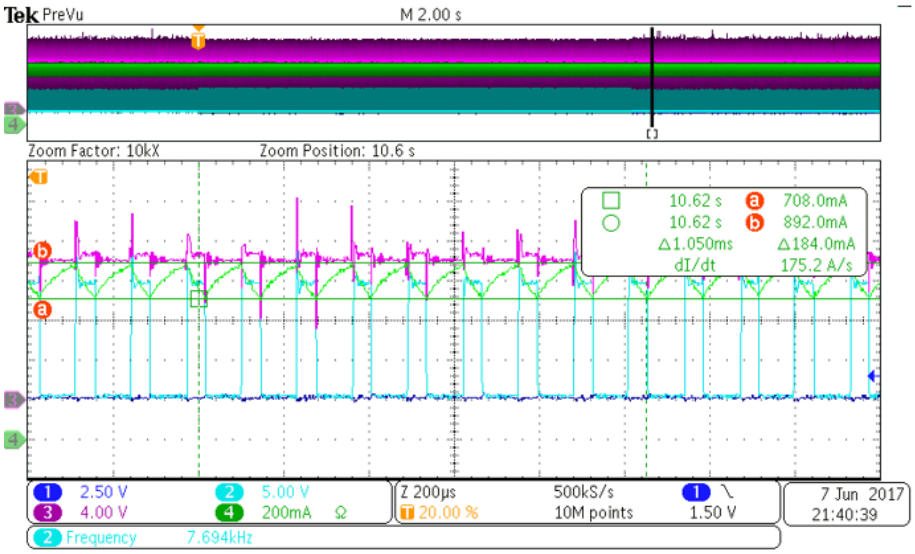
If Out_of_regulation bit is unmasked, then FAULTn goes low when Fail Safe switch is unconnected: it needs Out_of_regulation bit to be read for FAULTn getting back high.

Figure 11. **Load connection open - Out_of_regulation bit unmasked**



Legenda: Ch1: FAULTn, Ch2: Vs_sol0, Ch3: Vload_sol0, Ch4: Iload_sol0

Figure 12. Load connection open restored - Out_of_regulation bit unmasked



Legenda: Ch1: FAULTn, Ch2: Vs_sol0, Ch3: Vload_sol0, Ch4: Iload_sol0

Revision history

Table 16. **Document revision history**

Date	Version	Changes
28-Apr-2021	1	Initial release.

Contents

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