
Hardware current control loop - Parameters choice for load driving optimization

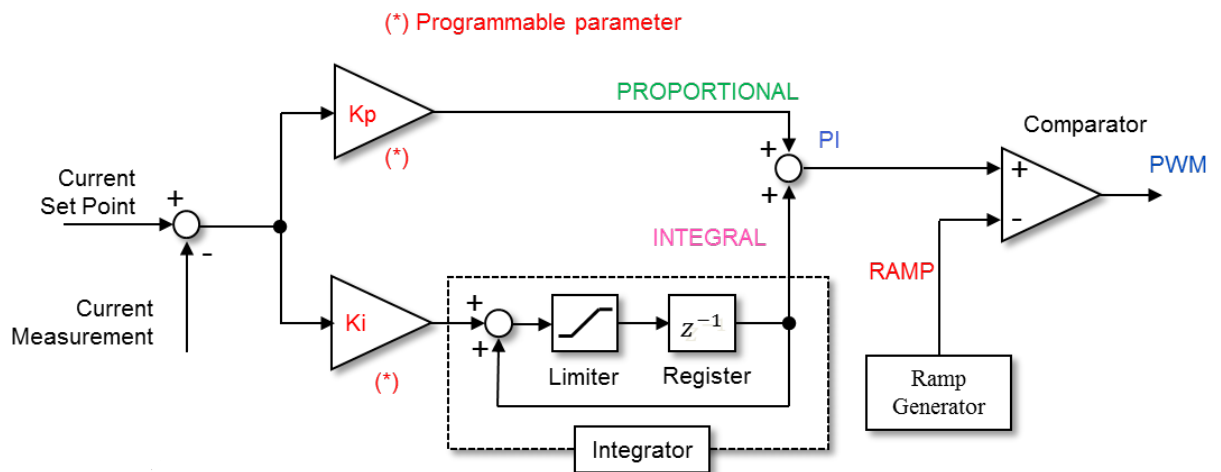
Introduction

This document is intended to integrate the information provided in the L9305 product datasheet, so as to facilitate the choice of the best configuration parameters, in order to drive an external load, when the device operates either in Fixed Frequency Hardware Current Control loop or in Variable Frequency Hardware Current Control loop.

1 Current hardware control mode with fixed frequency

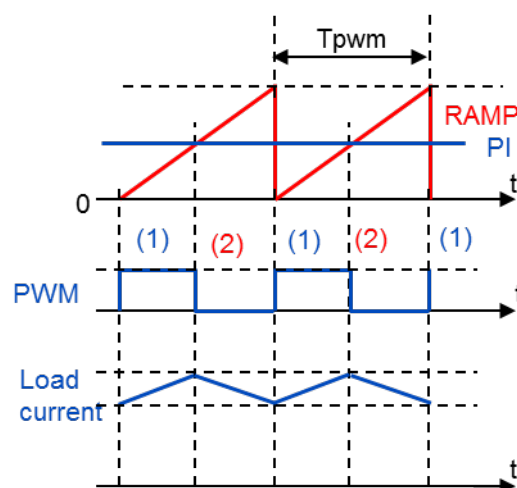
In this section, the user will be provided with an empirical procedure and some examples, in order to choose the optimum KI and KP parameters for driving loads in Current Hardware Control mode with Fixed Frequency. The fixed frequency control subtracts the current measurement signal from the programmed set point to create the error signal. The proportional and integral amplifiers process the error signal and generate the PROPORTIONAL and INTEGRAL signals. The processing of PROPORTIONAL and INTEGRAL signals depends on the user programmed values of KP and KI in the Channel_x.KGAINS register. The control loop then adds PROPORTIONAL and INTEGRAL signals and compares the result with the ramp generator.

Figure 1. Fixed frequency algorithm



The LIMITER in the integral path, limits the integral signal automatically to the RAMP signal to ensure the fastest PWM changes to reduce current over and under shoot. An example of the current control block diagram is shown in the Figure 1.

Figure 2. Fixed frequency signals



In fixed frequency current control, the basic operation is dependent on the ramp generator and the PI signal as follows:

- Switch OFF point (1): the PI signal crosses the RAMP signal from high to low, the output driver is switched off and the load CURRENT reaches its maximum peak value.
- Switch ON point (2): every clock based T_{PWM} periods, the RAMP signal resets and the output driver is switched on and the load current reaches its minimum peak value.

To optimize current control capability, the user must properly select KP and KI amplitude settings (Channel_x.KGAINS) for each application.

- **KP**: parameter controls the amplitude of the Proportional signal and is calculated as:

$$KP = 2^{KP_sel} \quad (1)$$

- **KI**: parameter controls the amplitude of the Integral signal and is calculated as:

$$KI = 2^{KI_sel} \quad (2)$$

1.1

KP and KI parameters optimization for static current setpoint

Given a load, a driver HS/LS configuration, a static current setpoint and a PWM frequency, in order to optimize load driving, the user can try to use all KI and KP values empirically and build up a table like in the Figure 3.

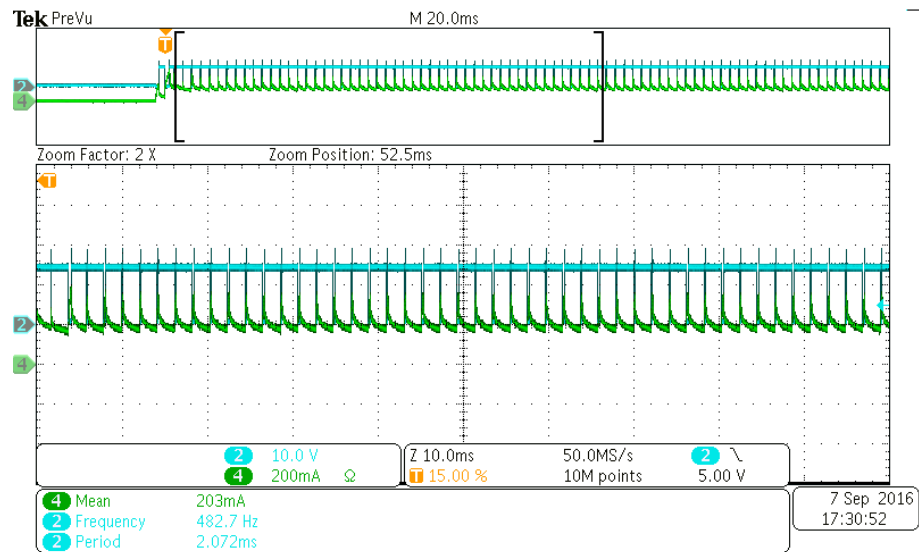
Operatively, once connected the load to the solenoid channel, the user should program the related SPI registers CONFIGURATION1, SETPOINT, CFG and KGAINS (see Section 1.1.1 SPI registers for fixed frequency mode).

Figure 3. KI-KP choice table

		KI							
		0	1	2	3	4	5	6	7
KP	0								
	1								
	2								
	3								
	4								
	5								
	6								
	7								

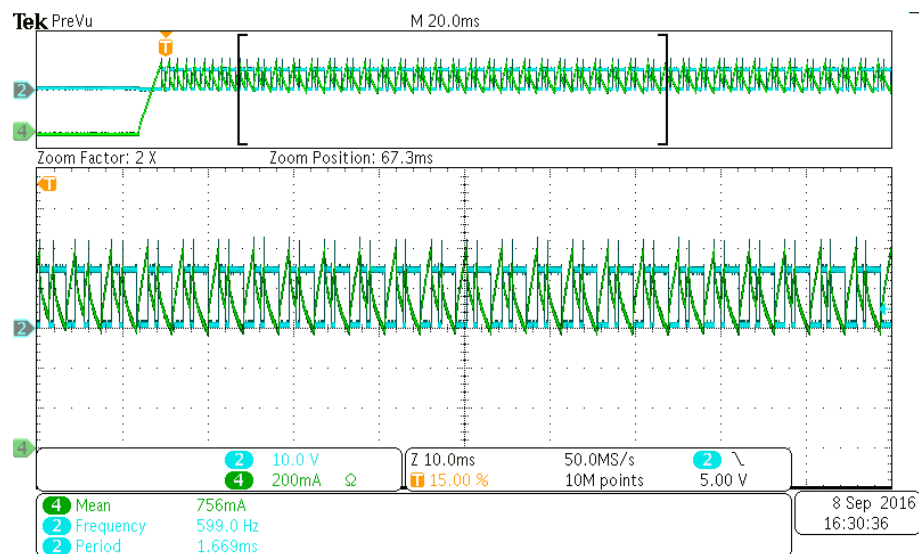
Green cells represent KP/KI combinations for which load average current is in line with product specification accuracy and current waveform is correct from PWM switching ripple and PWM frequency point of view. Red cells are those for which load average current is not in line with product specification accuracy and current waveform shows unwanted spikes and is not correct from PWM switching ripple and PWM frequency point of view.

Figure 4. Fixed frequency mode: correct regulation



Note: Setpoint $I = 200 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
No unwanted peaks.

Figure 5. Fixed frequency mode: incorrect regulation



Note: Setpoint $I = 800 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
Wrong average current, wrong PWM frequency and unwanted peaks.

1.1.1 SPI registers for fixed frequency mode

To operate in Hardware Control, Fixed Frequency mode, the involved SPI registers are the following ones:

Configuration 1 - CONFIGURATION1

Address Channel_X_BaseAddress + 0x02

Type Read/Write

Description Configuration register provides information related to channel configuration

Table 1. CONFIGURATION1 register detail

Register bit	Field name/description	Default values	Type
[15]	Unused	0	Read
[14]	OFS_CMP_DIS: 0: Current Sense Offset Compensation Active 1: Current Sense Offset Compensation disabled	0	Read/Write
[13]	CALIBRATION_DIS: 0: Digital Current Sense Calibration Active 1: Digital Current Sense Calibration Disabled	0	Read/Write
[12:11]	Unused	0	Read
[10]	Solenoid Logic BIST: 0: Logic BIST Reset 1: Logic BIST Enabled	0	Read/Write
[9]	Td_Blank: 0: Long Blanking Time 1: Short Blanking Time	0	Read/Write
[8]	HILOAD: Current Sense Scale: 0: 1.5 A Max Current Range 1: 2.0 A Max Current Range	0	Read/Write
[7]	Unused	0	Read
[6]	Overcurrent threshold selection: 0: 4 A Theshold 1: 5 A Threshold	0	Read/Write
[5]	Enable OFF Diagnosis: 0: Disabled (OFF) 1: Enabled	0	Read/Write
[4]	Unused	0	Read
[3]	Solenoid Load Configuration: 0: Low Side 1: High Side	0	Read/Write
[2]	Current Feedback Control Mode: 0: HW Feedback 1: SW Feedback	0	Read/Write
[1:0]	Output Slew Rate: 00: 0.4 V/ μ s	0	Read/Write

Register bit	Field name/description	Default values	Type
	01: 1.0 V/μs 10: 4.0 V/μs 11: 8.0 V/μs		

In order to avoid thermal power dissipation and device heating, it is better to choose Output Slew Rate “10: 4.0 V/μs” or “11: 8.0 V/μs”.

Output Slew Rate must be chosen properly also in relation to the operating PWM switching frequency, in particular when high PWM switching frequencies are required by the driven load:

- At high operating PWM switching frequencies, current accuracy could be affected and degraded by a too slow Output Slew Rate, because high flat duty cycle phase of Load_solX voltage waveform is too short with respect to the PWM period, so the load ON phase is not effective in driving the load properly.
- At high operating PWM switching frequencies and higher setpoint currents (~1 A, 1.5 A), channel overheating could occur due to a too slow Output Slew Rate, thus causing channel thermal shutdown.

HILOAD = 0/1 sets the regulated current full scale.

Current Setpoint - SETPOINT

Address Channel_X_BaseAddress + 0x06

Type Read/Write

Description Register stores current setpoint code (HW mode current control). Current Control SETPOINT is coded into 13 bits. Current value depends on HILOAD bit

Table 2. SETPOINT register detail

Register bit	Field name/description	Default values	Type
[15]	Auto Limit: Activates the transient mode on setpoint change: 0: Inactive 1: Active	0	Read/Write
[14:13]	Unused	0	Read
[12:0]	Current Setpoint Code	All "0"	Read/Write

Current setpoint formulas:

- HILOAD = 0 → Normal current mode - Single bit resolution = 0.25 mA - Max Avg. Current 1.5 A.

$$Target\ Average\ Current = Setpoint[12:0] \times 0.25 \quad (3)$$

- HILOAD = 1 → High current mode - Single bit resolution = 0.33 mA - Max Avg. Current 2.0 A.

$$Target\ Average\ Current = Setpoint[12:0] \times 0.33 \quad (4)$$

The maximum guaranteed ripple current for the device's specified accuracy is 0.5 A peak to peak for HILOAD = 0 and 0.66 A peak to peak for HILOAD = 1. If the channel is enabled and programmed with 0x0000h current setpoint, the power output is forced with duty cycle 0 (recirculation path fully on) and the current measurement is disabled; Setpoint codes higher than 0x1770h are reserved for calibration and offset compensation purposes: in case such codes are selected, the accuracy is not guaranteed.

When CHx.SETPOINT = 0000 and channel x is controlled Hardware mode (CONFIGURATION1.D[2] = 0), then current measurement is disabled and AVGCUR always returns all '0', even if channel x is driven full-on.

Control configuration - CTRLCFG

Address Channel_X_BaseAddress + 0x07

Type Read/Write

Description -

Table 3. CTRLCFG register detail

Register Bit	Field name/description	Default Values	Type
[15:14]	Transition Time: Too long period detection (if the current PWM time exceeds this threshold, the controller enters the transient state): 00: $2.5 * T_{pwm}$ 01 : $4.5 * T_{pwm}$ 10: $8.5 * T_{pwm}$ 11 : $16.5 * T_{pwm}$	0	Read/Write
[13:12]	Unused	0	Read
[11]	HW feedback Frequency Mode: 0: Fixed Frequency ⁽¹⁾ 1: Variable Frequency	0	Read/Write
[10:0]	Target PWM Period Code	All "0"	Read/Write

1. For Fixed frequency Mode $D[11] = 0$ (default).

Table 4. Target PWM period formulas

PWM code [10:0]		Period [μ s]	Frequency [Hz]	Status
hex	dec			
0x000	0	50	20000	Short period/High frequency range PWM Period = $50 \mu\text{s} + \text{PWM Code } D[10:0] * 5 \mu\text{s}$
0x001	1	55	18180	
...	
0x009	9	95	10520	
0x00A	10	100	10000	PWM Period = $\text{PWM Code } D[10:0] * 10 \mu\text{s}$ Normal Period/Frequency range.
0x00B	11	110	9090	
...	
0x681	1665	16650	60.06	
0x682	1666	16660	60.02	Values clamped to Maximum period of 16.67 ms
0x683	1667	16670	60.02	
...	...	16670	60.02	
0x7FF	2047	16670	60.02	

Gains configuration - KGAINS

Address	Channel_X_BaseAddress + 0x09
Type	Read/Write
Description	Register stores KI (Integral error gain: HW mode current control) and KP (Proportional error gain: HW mode current control)

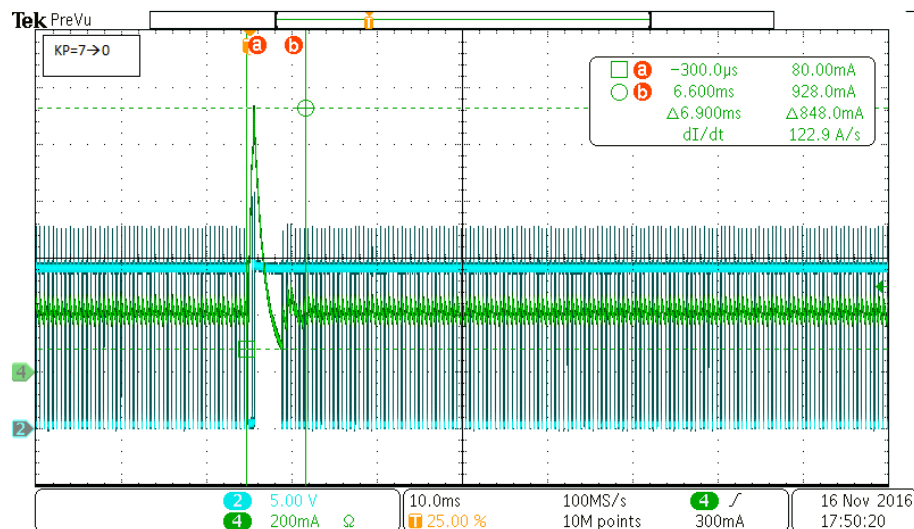
Table 5. KGAINS register detail

Register bit	Field name/description	Default values	Type
[15:6]	Unused	All "0"	Read
[5:3]	KI: Integral Gain of HW current control loop (fixed & variable freq.) ⁽¹⁾	100	Read/Write
[2:0]	KP: Proportional Gain of HW current control loop (fixed freq. only) ⁽¹⁾	100	Read/Write

1. KI and KP can be changed while solenoid driver channel is operating.

Note: When device is regulating a certain average current in fixed frequency mode, if KI and KP parameters are changed, sometimes big spikes are generated and current is no more correctly regulated: KP changing from higher values to lower values is responsible for this issue. In fact, spikes are generated on regulated load current when KP is changed from higher values to lower values: the worst case is $KP = 7 \rightarrow 0$.
When regulating a certain current with static setpoint in fixed frequency mode with optimized KP and KI, there is no need to change KI and KP as described above: avoid such a kind of changes.

Figure 6. Effect of KP big reduction during regulation



Solenoid drivers enable - SOLENDR

Address Global Base Address + 0x01
Type Read/Write
Description Solenoid driver configuration

Table 6. SOLENDR register detail

Register bit	Field name/description	Default values	Type
[15:8]	Unused	All "0"	Read
[7:6]	Solenoid Driver State, Channel 3 00: Driver Off, OFF State Diagnostics disabled and masked 01 : Driver tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	Read/Write
[5:4]	Solenoid Driver State, Channel 2 00: Driver Off, OFF State Diagnostics disabled and masked 01 : Drives tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	Read/Write
[3:2]	Solenoid Driver State, Channel 1 00: Driver Off, OFF State Diagnostics disabled and masked 01 : Drives tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	Read/Write
[1:0]	Solenoid Driver State, Channel 0 00: Driver Off, OFF State Diagnostics disabled and masked 01: Drives tristate. OFF DIAG depending on bit on config reg 10: Drives on in PWM. OFF DIAG off and masked 11: Drives on in full-on. OFF DIAG off and masked	01	Read/Write

Note: Channel X should be enabled PWM mode and with OFF Diagnostic masked ("10").

1.2 KP and KI parameters optimization for dynamic current setpoint

When a current setpoint has to be changed dynamically between two or more values some additional steps are needed for KI and KP optimization with respect to the previous case of static setpoint. In the following procedure description, current setpoint will be varied between 2 values.

It has been assumed that a load, a driver HS/LS configuration, a PWM frequency and two current setpoints are given.

First of all, each current setpoint can be considered separately as a static one and the procedure for KI and KP optimization can be executed separately for each one, as described in [Section 1.1 KP and KI parameters optimization for static current setpoint](#).

Once a table similar to the KI-KP table (see [Figure 3](#)) has been built up for each current setpoint, transitions should be considered between the lower setpoint and the upper one and vice versa. The purpose of KI and KP optimization should be smooth and regular current transitions: both in raising and in falling transitions current should make continuous straight transitions and current waveform should have its steady state triangular shape, by one cycle after the transition is complete.

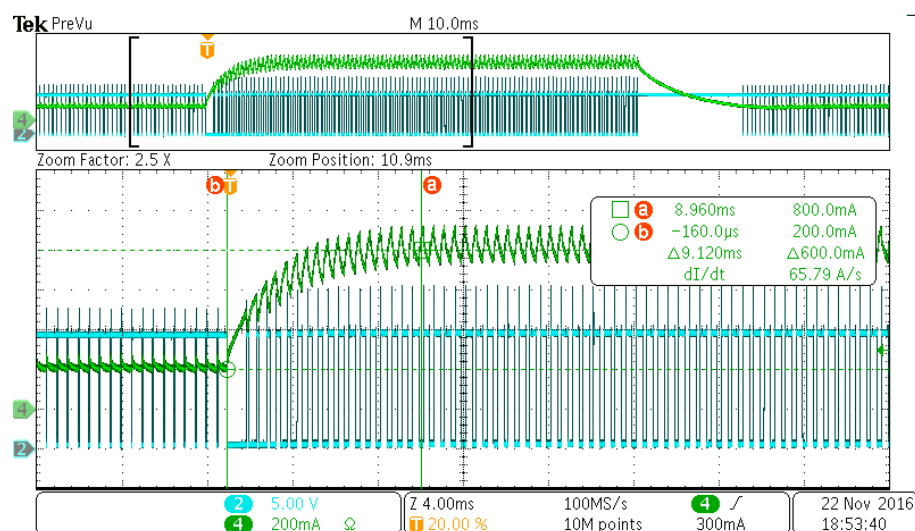
In order to achieve current transitions optimization, the user should try each couple of KI and KP good for lower setpoint and each couple of KI and KP good for upper setpoint, by changing them right after the related setpoint has been set by SPI.

Note: Both raising and falling transitions could be affected by current spikes, if KP is changed from higher values to lower values: obviously, the worst case is $KP = 7 \rightarrow 0$.

In the previous procedure the user finds optimized KP and KI set for both lower current setpoint and higher current setpoint: if KP is the same in both cases, no overshoots will occur in setpoint transitions.

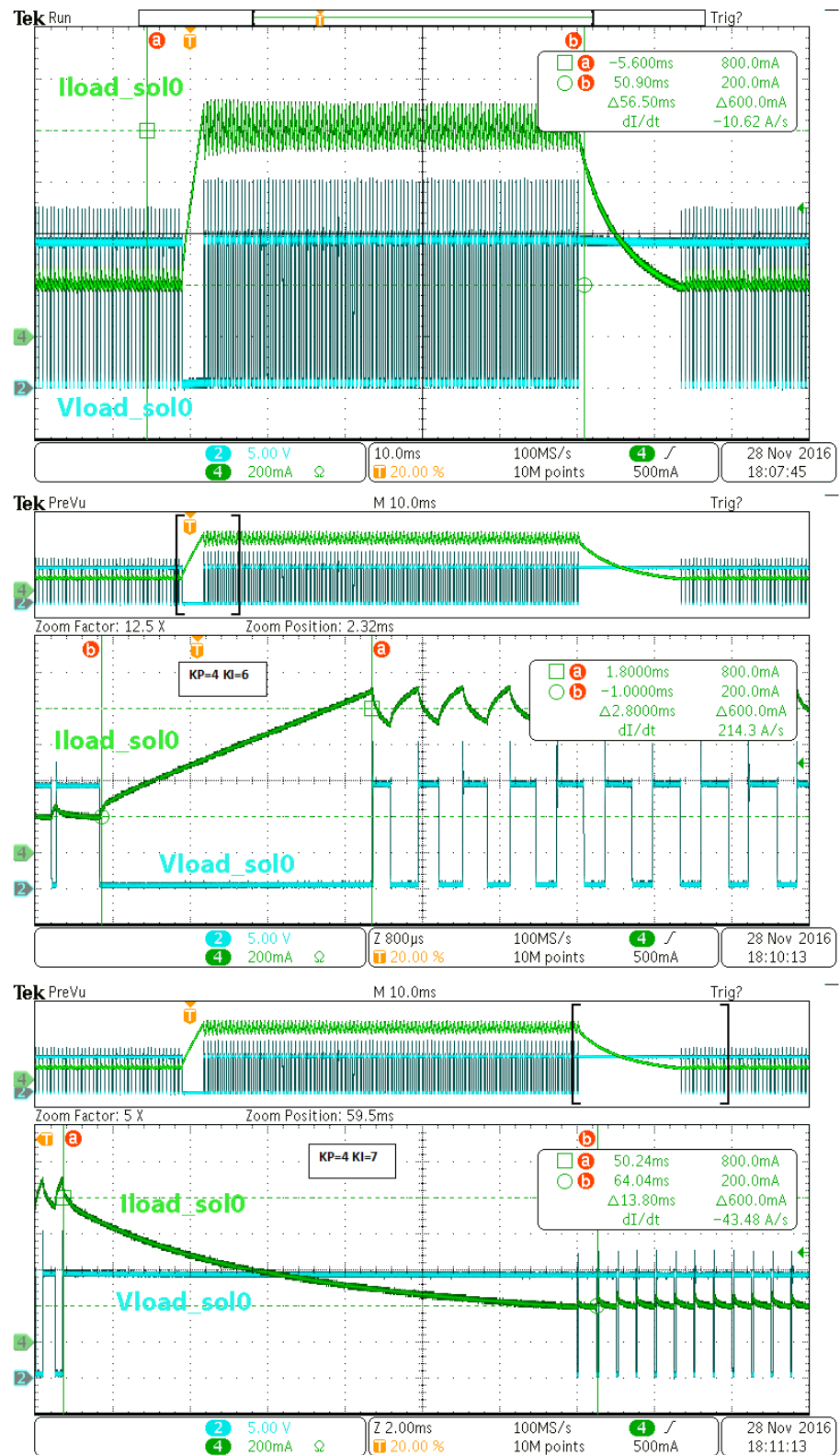
If KP is not the same in both low \rightarrow high and high \rightarrow low transitions, then overshoots could occur when setting KP from higher values to lower values. In this case, the user should consider controlling the current through variable frequency HW feedback mode by optimizing the variable frequency parameters, KI and KFI, in order to avoid current overshoots during setpoint transitions.

Figure 7. Fixed frequency mode: inaccurate current setpoint transition



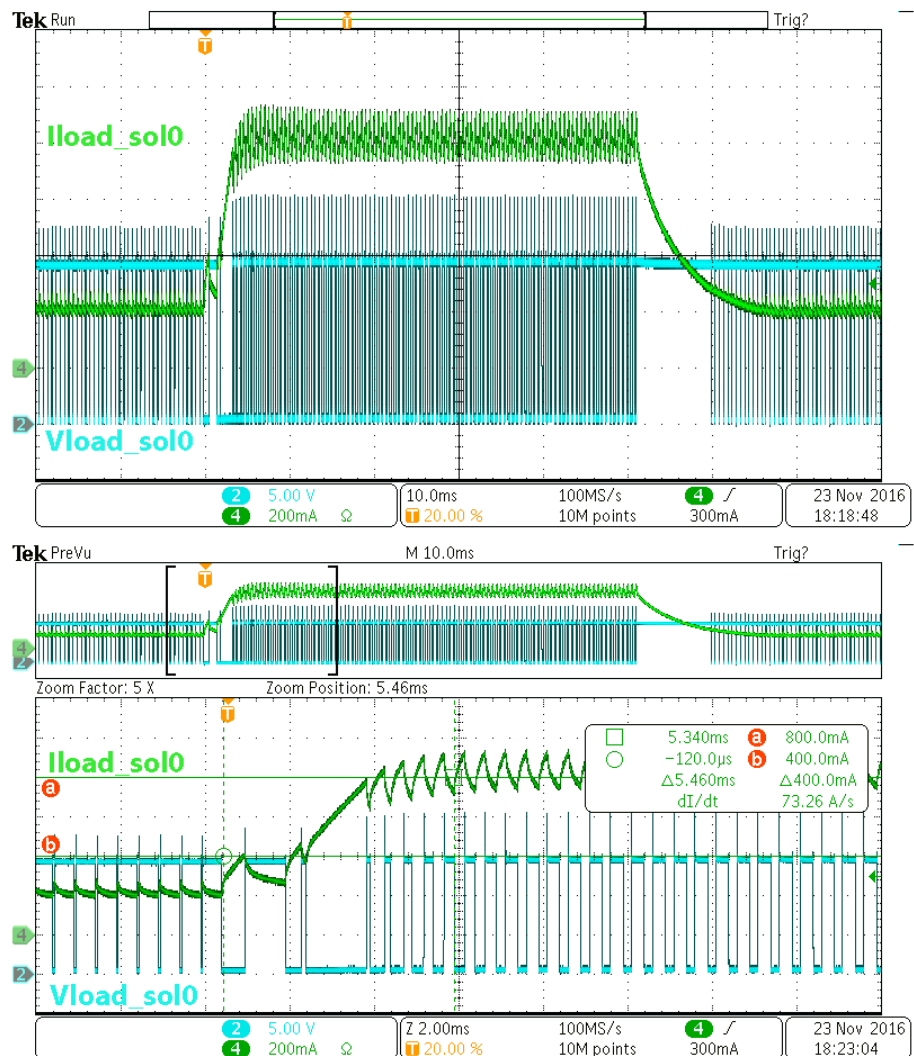
Note: Setpoint $I = 200 \text{ mA} \rightarrow 800 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
Current waveform is not straight and smooth changing from the lower to the higher setpoint.

Figure 8. Fixed frequency mode: accurate current setpoint transition



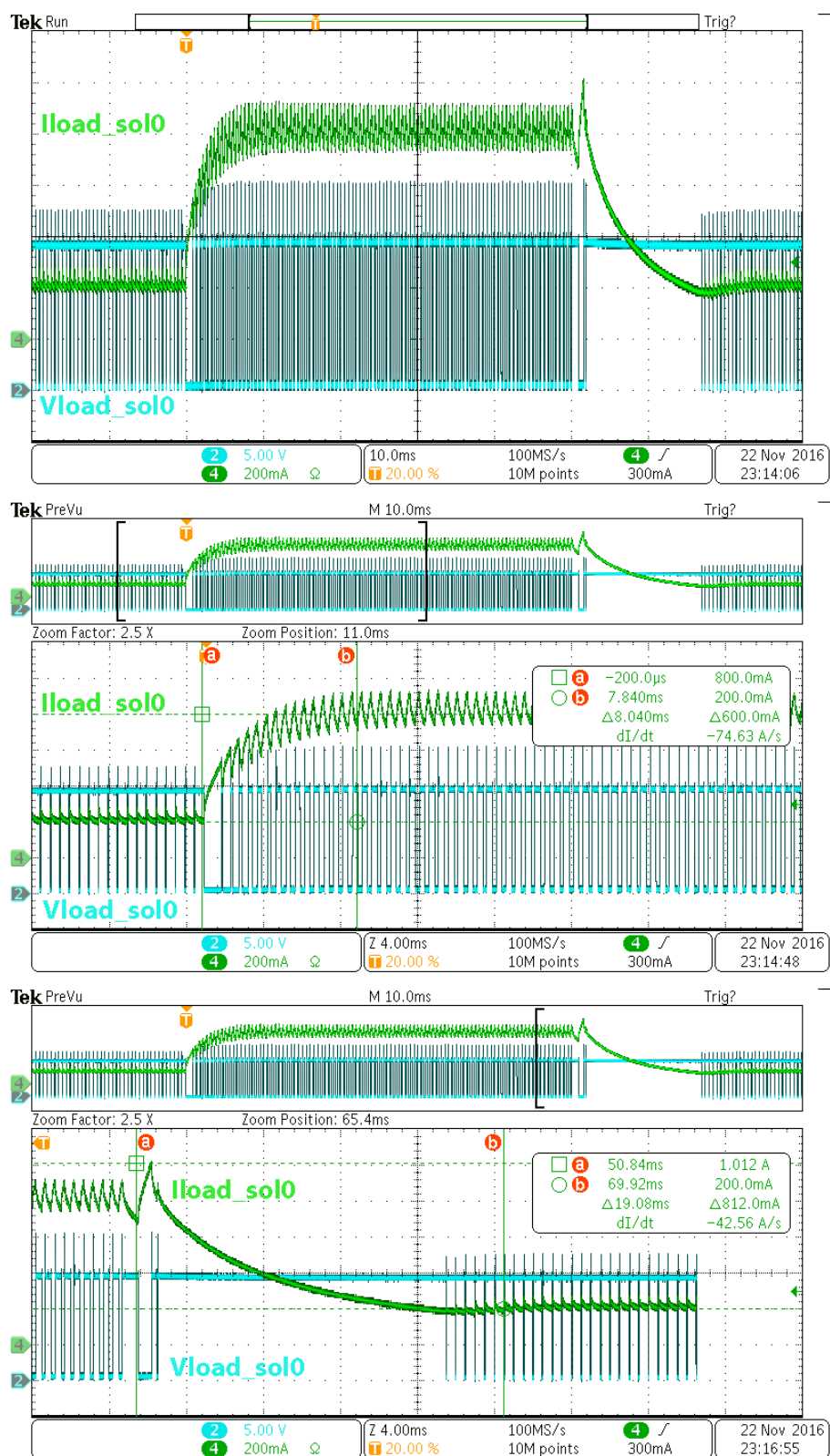
Note: Setpoint $I = 200\text{ mA} \rightarrow 800\text{ mA}$, PWM frequency $f = 2\text{ kHz}$
 $KI = 6$ and $KP = 4$ set after the $0.2\text{ A} \rightarrow 0.8\text{ A}$ transition
 $KI = 7$ and $KP = 4$ set after the $0.8\text{ A} \rightarrow 0.2\text{ A}$ transition
Current waveform is straight and smooth changing from the lower to the higher setpoint.
Current waveform has its steady state triangular shape once cycle after the transition is complete.

Figure 9. Spikes on the raising transition



Note: Setpoint $I = 200\text{ mA} \rightarrow 800\text{ mA}$, PWM frequency $f = 2\text{ kHz}$
 $KI = 4$ and $KP = 4$ set after the $0.2\text{ A} \rightarrow 0.8\text{ A}$ transition
 $KI = 5$ and $KP = 7$ set after the $0.8\text{ A} \rightarrow 0.2\text{ A}$ transition

Figure 10. Incorrect raising and falling transitions



Note: Setpoint $I = 200 \text{ mA} \rightarrow 800 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
 $KI = 5$ and $KP = 6$ initial values.
 KI and KP default values after the $0.8 \text{ A} \rightarrow 0.2 \text{ A}$ transition
 Wrong raising transition and spikes on the falling transition.

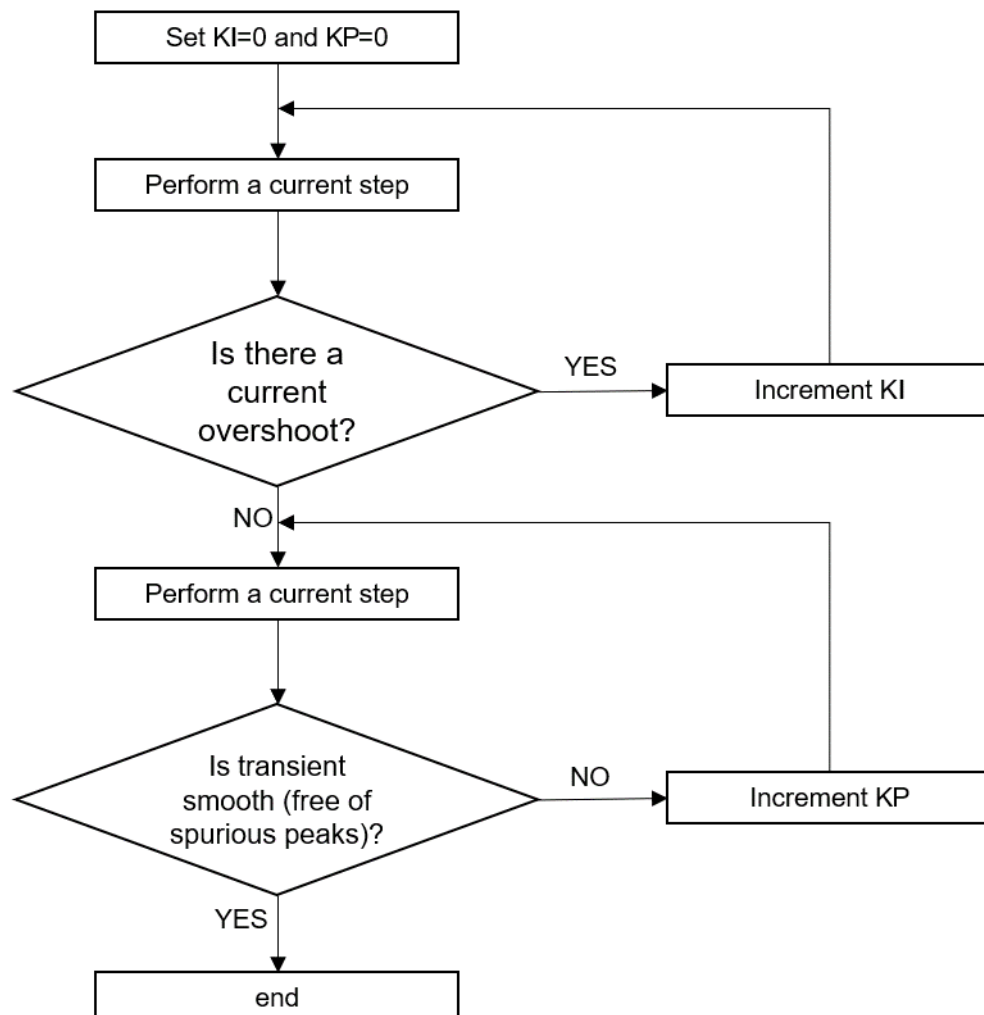
1.2.1 Algorithm for KP/KI search

P-I current control best coefficients research could be performed either in an exhaustive way, as described in Section 1.1 KP and KI parameters optimization for static current setpoint, by blindly trying all possible KP/KI combinations and choosing the best one, or in an algorithmic way, which provides a faster and reliable way to determine the most performing coefficients settings for a given transition between two current setpoints.

The proposed procedure is valid for both HS and LS configuration, on any given channel and any current setpoint transition.

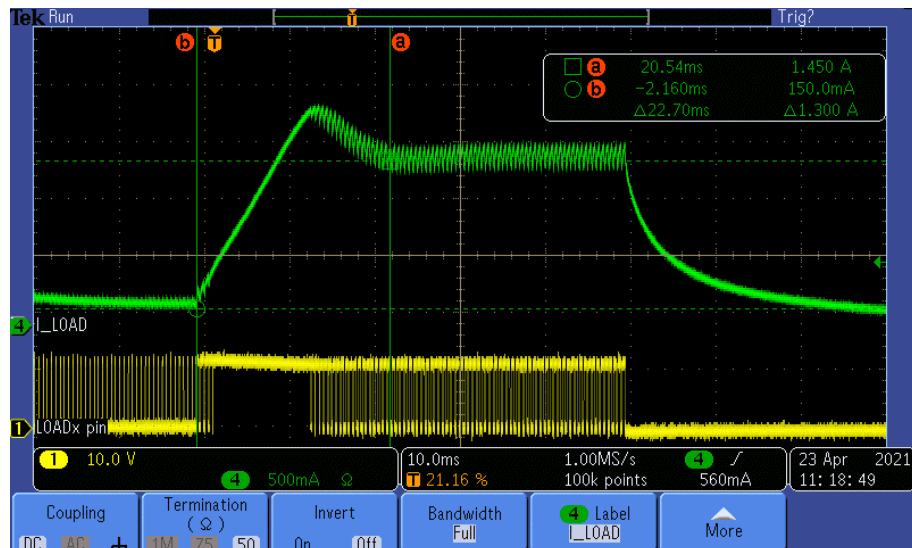
Following figure shows the suggested algorithm.

Figure 11. KI/KP selection algorithm



Next pictures shows an example of a 200 mA to 1.5 A transition optimization process on a solenoid, done according to the proposed algorithm. Channel is configured in HS mode and pwm frequency is 2 kHz.

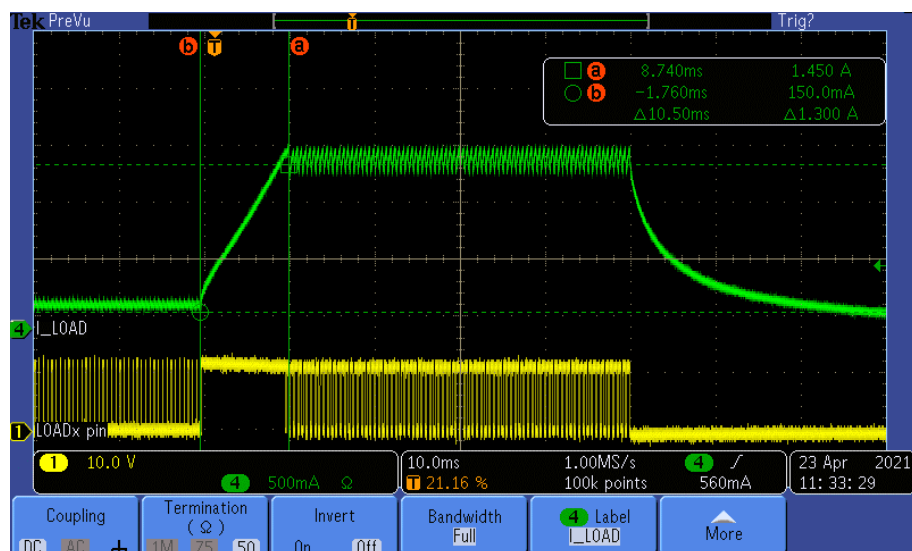
Figure 12. 200 mA - 1.5 A not optimized transition



Regulation shows some spurious peaks during the transition and a large overshoot.

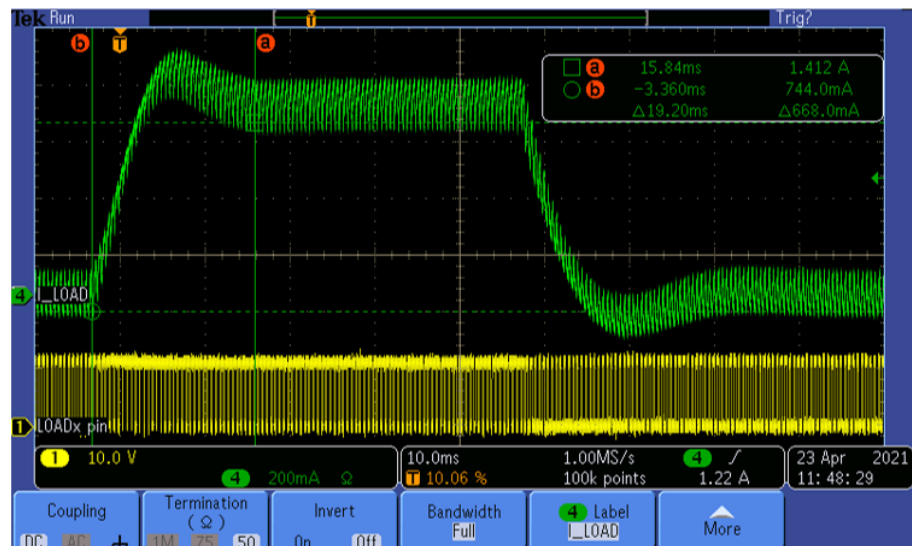
Following the algorithm, the best coefficients have been found ($KI = 6$, $KP = 1$), allowing a fast and smooth transition, without any overshoot.

Figure 13. 200 mA - 1.5 A optimized transition

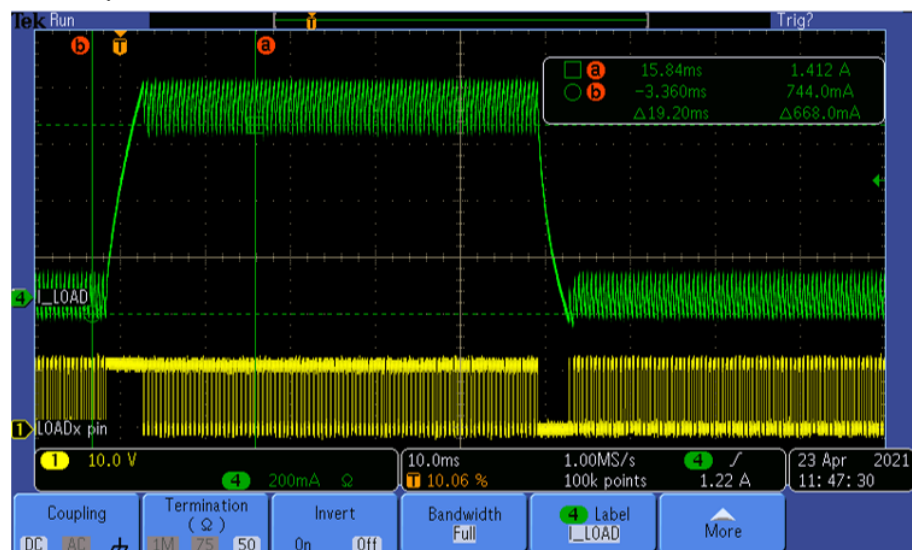


In the following example, the same solenoid in the same driver configuration, is driven with a current step from 800 mA to 1.5 A; the example allows to see the effect of optimization on both rising and falling transitions.

Figure 14. 800 mA - 1.5A transition



a. not optimized



b. optimized

Next picture shows the response with the same configuration to a VBAT variation from 12 V to 6 V (and v.v.) of a channel driving 800 mA.

Figure 15. Response to VBAT variation - not optimized

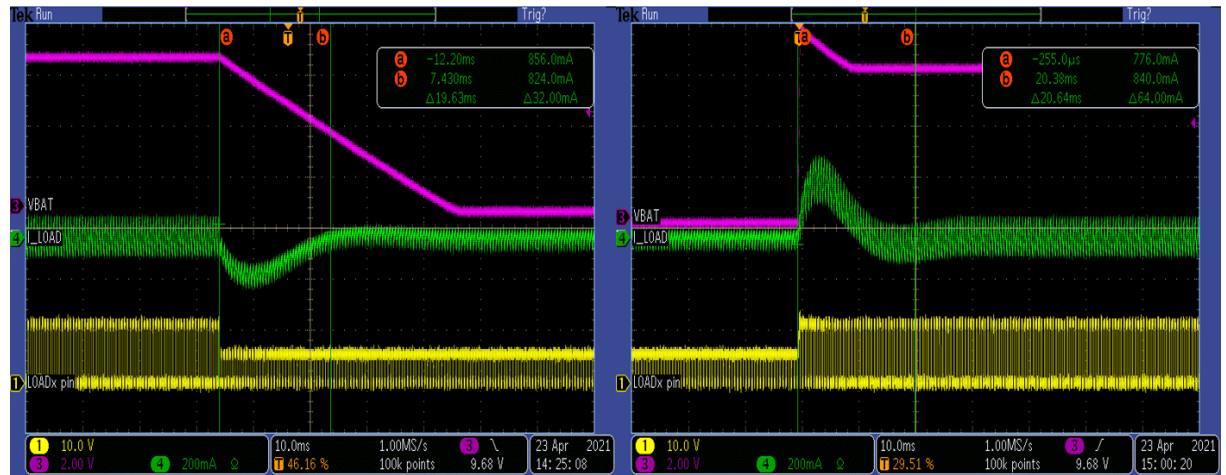


Figure 16. Response to VBAT variation - optimized



Again, applying KP/KI values found using the algorithm allows the regulator to respond to VBAT variations without any impact on load current average value, also in case of a rapid VBAT variation (see Figure 16 - scope screen on the right).

2 Current hardware control mode with variable frequency

In this section, the user will be provided with an empirical procedure and some examples, in order to choose the optimum parameters for driving loads in Current Hardware Control mode with Variable Frequency.

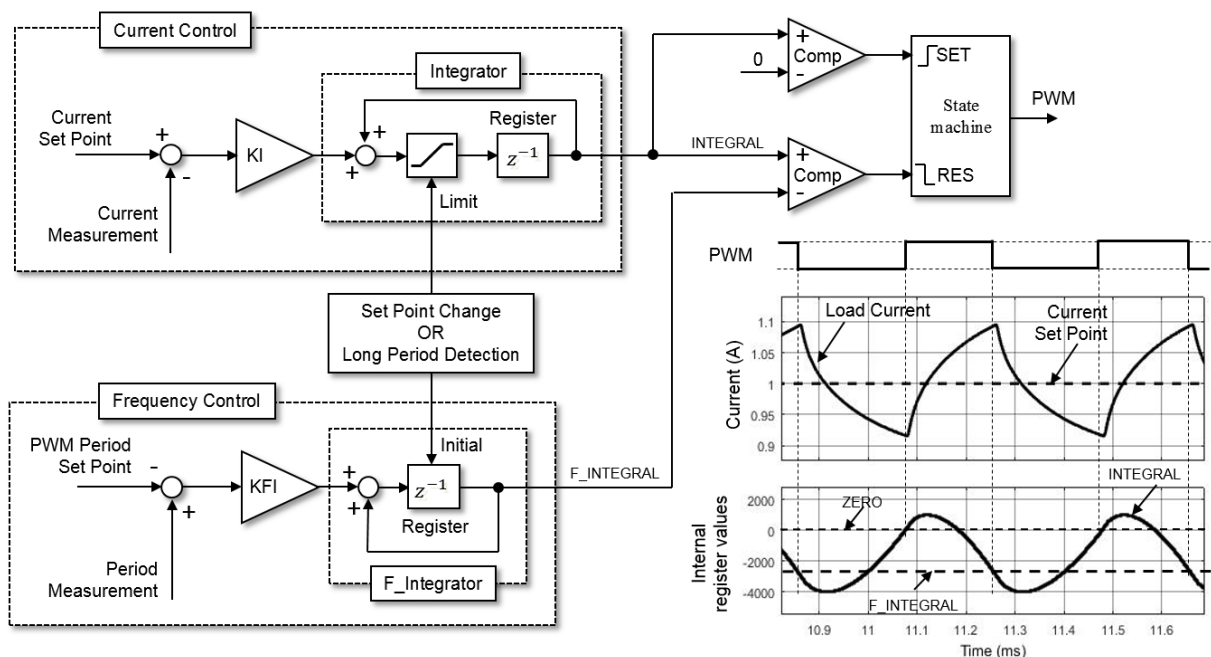
In Figure 17, the current control loop subtracts the measured current from the programmed setpoint to derive an error signal. The integral amplifier with gain KI processes the error signal creating the INTEGRAL signal. The frequency control loop subtracts the PWM period set point T_{PWM} from the measured PWM period creating a period error signal. The integral amplifier with gain KFI, processes the period error and generates the resulting frequency integral (F_I) output signal.

Variable frequency control operation is dependent on the INTEGRAL signal, F_I signal and zero level signal as follows:

- Switch OFF point: the INTEGRAL signal crosses the F_I signal from high to low, the output driver is switched off and the load CURRENT reaches its maximum peak value.
- Switch ON point: the INTEGRAL signal crosses the zero level signal from low to high, the output driver is switched ON, and the load CURRENT reaches its minimum peak value.

The variable frequency control provides a transient mode for optimization of the transient condition behavior. In this way, it eliminates the current overshoot and allows the fastest reaching of the final frequency. The transient mode is entered in case of a change of the current setpoint (Set Point Change) while the Auto Limit control bit is set. The transient mode is also entered in case the PWM period is longer than a threshold (Long Period Detection). The 2-bit control input Transition Time (D[15:14] in CTRLCFG register) selects the Long Period Detection threshold.

Figure 17. Variable frequency algorithm



In transient mode the integrator limits the INTEGRAL signal within the user programmable limits, this guarantees the fastest current transitions between different set points without showing over/undershoot. The integrator limits of the variable frequency control are not automatically calculated; the user-programmed parameters POSINTLIM and NEGINTLIM are available for optimized positive and negative integrator limits.

In transient mode the F_INTEGERAL signal at the frequency integrator output is set to a programmable value with the 3 control bits FINT_START (D[2:0] in KFREQCTRL register), in this way the F_INTEGERAL signal starts close to its final value when exiting from the transient mode.

To optimize the controller response for different applications, the following parameters must be programmed by the user:

- *KI* (Channel_x.KGAINS)
- *KFI* (Channel_x.KFREQCTRL)
- *POSINTLIM* & *NEGINTLIM* (Channel_x.INTGLIM)
- *Auto Limit* (Channel_x.SETPOINT)
- *Transition Time* (Channel_x.CTRLCFG)
- *Fint_Start* (Channel_x.KFREQCTRL)

Programming values can be selected considering the following:

- **KI**: Integral portion of the loopgain. It can be calculated as

$$KI = 2^{KI_{sel}} \quad (5)$$

- **KFI**: Integral portion of the frequency control loop gain. It can be calculated as

$$KFI = 2^{KFI_{sel}} \quad (6)$$

- **POSINTLIM**: Positive Integrator Saturation Limit. It can be calculated as

$$POSINTLIM = 2^{(POSINTLIM_{sel} - 1)} \quad (7)$$

- **NEGINTLIM**: Negative Integrator Saturation Limit. It can be calculated as

$$NEGINTLIM = -2^{(NEGINTLIM_{sel} - 1)} \quad (8)$$

- **AUTO_LIMIT**:

- If AUTOL_LIMIT_SEL = 0 → Transient mode is insensitive to changes of Current Set Point
- If AUTOL_LIMIT_SEL = 1 → Any change in the current set point activates the transient mode

- **FINIT_START**:

- If FINIT_START_SEL = 0

$$FINIT_{START} = 0 \quad (9)$$

- If FINIT_START_SEL > 0

$$FINIT_{START} = NEGINTLIM \times 2^{(FINIT_{START}_{sel} - 7)} \quad (10)$$

- **TRANSITION TIME**: Too long PWM period detection: if the current PWM time exceeds this threshold, the controller enters the transient state. It can be programmed as follows:

- If TRANSITION TIME = 0

$$TRANSTIME = 2,5 \times T_{PWM} \quad (11)$$

- If TRANSITION TIME = 1

$$TRANSTIME = 4,5 \times T_{PWM} \quad (12)$$

- If TRANSITION TIME = 2

$$TRANSTIME = 8,5 \times T_{PWM} \quad (13)$$

- If TRANSITION TIME = 3

$$TRANSTIME = 16,5 \times T_{PWM} \quad (14)$$

2.1 Variable frequency parameters optimization for static current setpoint

Given a load, a driver HS/LS configuration, a static current setpoint and a PWM frequency, in order to optimize load driving, the user should choose the optimum variable frequency parameters.

Operatively, once connected the load to the solenoid channel, the user should program the related SPI registers CONFIGURATION1, SETPOINT, CFG, KFREQCTRL, KGAINS (only KI) and INTGLIM.

Procedure sequence is as follows:

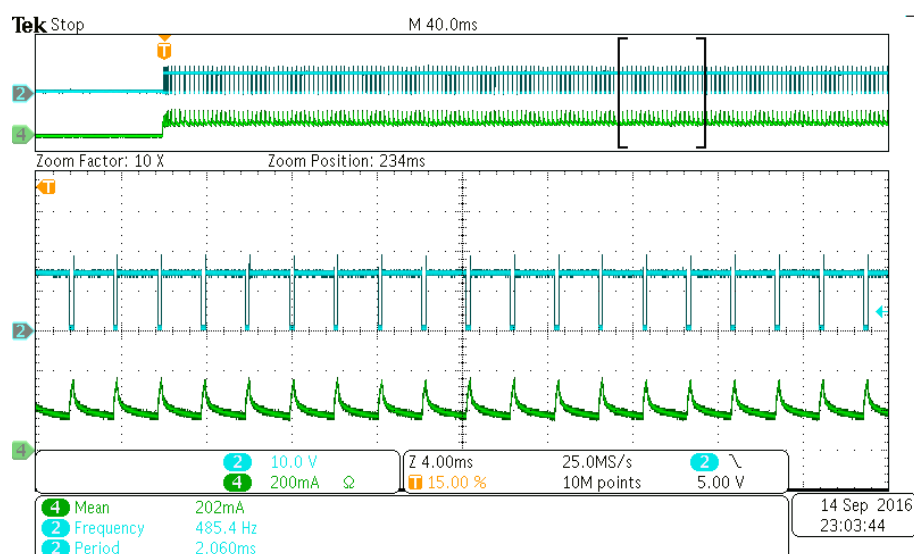
1. Set CONFIGURATION1
2. Set SETPOINT
3. Set CFG
4. Set INT_OUT_SEL[15:14] in INTGLIM register and read INTOUT register, in order to have:
 - a. 00: Integrator Low Threshold
 - b. 10: Integrator Min Level
 - c. 11: Integrator Max Level
5. In INTGLIM register set NEGINTLIM[7:4]= NEGINTLIM_sel according to the formula , in which NEGINTLIM=Integrator Min Level read in step 4)
6. In INTGLIM register set POSINTLIM[3:0]= POSINTLIM_sel according to the formula , in which POSINTLIM=Integrator Max Level read in step 4)
7. In KFREQCTRL register set FINT_START[2:0]= FINITSTART_sel according to the formula , in which FINIT_START= Integrator Low Threshold read in step 4)
8. Try all KI and KFI values empirically and build up a table as follows:

Figure 18. KI-KFI choice table

KFI	KI							
	0	1	2	3	4	5	6	7
0	current 502.5mA period 5.495ms	current 502.9mA period 3.773ms	current 502.6mA period 2.089ms avgcur=7CF 499.75 pwmsense 7D6=2006 7E5=2021	current 502.6mA period 2.073ms avgcur=7CF 499.75 pwmsense 7C2=1986 7D6=2004	current 502.6mA period 2.070ms avgcur=7CF 499.75 pwmsense 7C8=1992 7D2=2002	current 502.6mA period 2.070ms avgcur=7CF 499.75 pwmsense 7CD=1997 7D6=2004	current 502.6mA period 2.075ms avgcur=7CF 499.75 pwmsense 7C5=1989 7D2=2002	current 502.6mA period 2.072ms avgcur=7CF 499.75 pwmsense 7CD=1997 7D8=2000
1	current 582.7mA period 5.358ms	current 502.7mA period 5.187ms	current 502.9mA period 3.799ms	current 502.6mA period 2.105ms avgcur=7CF 499.75 pwmsense 7FE=2046 802=2054	current 502.6mA period 2.085ms avgcur=7CF 499.75 pwmsense 7CA=1994 7DB=2011	current 502.6mA period 2.063ms avgcur=7CF 499.75 pwmsense 7CC=1996 7D7=2007	current 502.6mA period 2.078ms avgcur=7CF 499.75 pwmsense 7CC=1996 7D5=2009	current 502.8mA period 2.072ms avgcur=7CF 499.75 pwmsense 7C8=1992 7D5=2000
2	current 655.3mA period 5.291ms	current 580.9mA period 5.349ms	current 504.7mA period 5.501ms	current 503.2mA period 3.808ms	current 502.5mA period 2.124ms avgcur=7CF 499.75 pwmsense 810=2064 81C=2076	current 502.7mA period 2.070ms avgcur=7CF 499.75 pwmsense 7C8=1992 7D5=2005	current 502.7mA period 2.074ms avgcur=7CF 499.75 pwmsense 7CD=1997 7D8=2008	current 502.6mA period 2.062ms avgcur=7CF 499.75 pwmsense 7C7=1991 7D4=2000
3	current 711.6mA period 6.178ms	current 656.7mA period 5.261ms	current 581.3mA period 5.348ms	current 504.8mA period 5.494ms	current 502.9mA period 3.811ms	current 502.5mA period 2.102ms avgcur=7CF 499.75 pwmsense 7FA=2042 807=2055	current 502.7mA period 2.072ms avgcur=7CF 499.75 pwmsense 7C6=1990 7D4=2004	current 502.7mA period 2.080ms avgcur=7CF 499.75 pwmsense 7C5=1989 7D6=2000
4	current 723.4mA period 6.471ms	current 712.5mA period 5.919ms	current 659.2mA period 5.245ms	current 582.5mA period 5.342ms	current 504.4mA period 5.500ms	current 502.9mA period 3.824ms	current 502.5mA period 2.144ms avgcur=7CF 499.75 pwmsense 811=2065 81D=2077	current 502.5mA period 2.075ms avgcur=7CF 499.75 pwmsense 7CA=1994 7D9=2000
5	current 725.5mA period 6.459ms	current 721.3mA period 6.049ms	current 710.7mA period 5.623ms	current 653.5mA period 5.245ms	current 580.4mA period 5.348ms	current 504.7mA period 5.460ms	current 503.2mA period 3.809ms	current 502.6mA period 2.123ms avgcur=7CF 499.75 pwmsense 811=2065 81B=2075
6	current 729.2mA period 6.507ms	current 725.9mA period 6.242ms	current 721.2mA period 5.936ms	current 710.7mA period 5.517ms	current 652.1mA period 5.242ms	current 579.5mA period 5.350ms	current 504.7mA period 5.473ms	current 503.2mA period 3.833ms
7	current 732.8mA period 6.685ms	current 731.1mA period 6.374ms	current 727.7mA period 6.136ms	current 721.5mA period 5.859ms	current 710.7mA period 5.490ms	current 653.6mA period 5.238ms	current 579.5mA period 5.347ms	current 504.7mA period 5.477ms

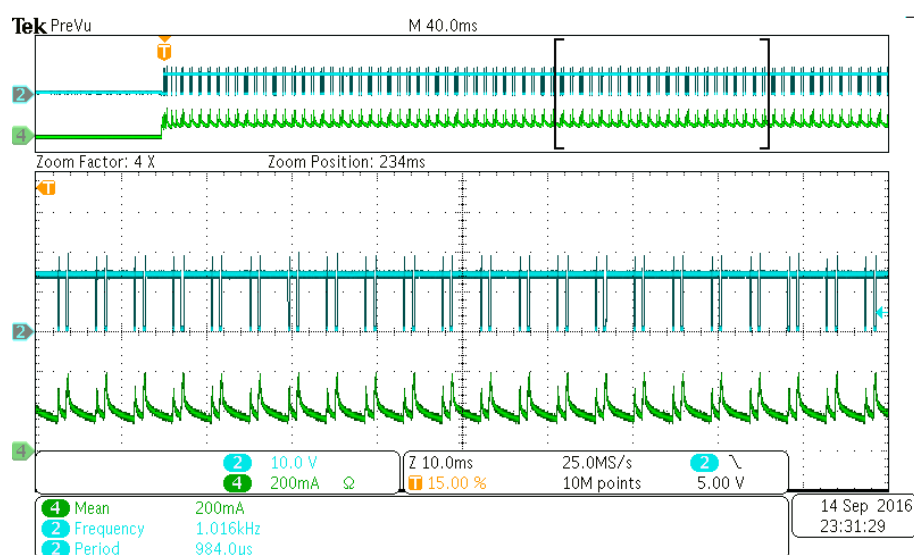
Green cells represent KFI/KI combinations for which load average current is in line with product specification accuracy and current waveform is correct from PWM switching ripple and PWM frequency point of view. Red cells are those for which load average current is not in line with product specification accuracy and current waveform shows unwanted spikes and is not correct from PWM switching ripple and PWM frequency point of view.

Figure 19. Variable frequency mode: correct regulation



Note: Setpoint $I = 200 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
No unwanted peaks.

Figure 20. Variable frequency mode: incorrect regulation



Note: Setpoint $I = 200 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
Wrong average current, wrong PWM frequency and unwanted peaks.

2.1.1 SPI registers for variable frequency mode

To operate in Hardware control, Variable Frequency mode, the registers involved are those listed in [Section 1.1.1 SPI registers for fixed frequency mode](#), plus the following ones:

Note: *In variable frequency HW feedback mode only KI should be considered. KP is not effective and not significant. Channel X should be enabled PWM mode and with OFF Diagnostic masked ("10").*

Frequency control - KFREQCTRL

Address	Channel_X_BaseAddress + 0x08
Type	Read/Write
Description	Register stores KF, FCIL (Variable frequency forward gain: HW mode current control)

Table 7. KFREQCTRL register detail

Register bit	Field name/description	Default values	Type
[15:6]	unused	All "0"	Read
[5:3]	KFI: Integral Gain of Frequency Control Loop	101	Read/Write
[2:0]	FINT_START: Start value for frequency integrator upon exiting transient mode	111	Read/Write

Integrator limit - INTGLIM

Address	Channel_X_BaseAddress + 0x0A
Type	Read/Write
Description	-

Table 8. INTGLIM register detail

Register bit	Field name/description	Default values	Type
[15:14]	INT_OUT_SEL: 00: Integrator Low Threshold 01: Integrator High Threshold 10: Integrator Min Level 11: Integrator Max Level	All "0"	Read/Write
[13:8]	Unused	00 0000	Read
[7:4]	NEGINTLIM	10001	Read/Write
[3:0]	POSINTLIM	1	Read/Write

Note: *According to INT_OUT_SEL configuration, on INTOUT register user can read:*

- 00: Integrator Low Threshold
- 01: Integrator High Threshold
- 10: Integrator Min Level
- 11: Integrator Max Level

Integrator output - INTOUT

Address Channel_X_BaseAddress + 0x14
Type Read only
Description Integrator output monitor

Table 9. INTOUT register detail

Register bit	Field name/description	Default values	Type
[15:0]	Integrator Output Monitor: Unsigned	All "0"	Read

2.2 Variable frequency parameters optimization for dynamic current setpoint

When a current setpoint has to be changed dynamically between two or more values some additional steps are needed for variable frequency parameters optimization with respect to the previous case of static setpoint. In the following procedure description, the current setpoint will be varied between 2 values.

It has been assumed that a load, a driver HS/LS configuration, a PWM frequency and two current setpoints are given.

First of all, each current setpoint can be considered separately as a static one and the procedure for variable frequency parameters optimization can be executed separately for each one, as described in [Section 2.1 Variable frequency parameters optimization for static current setpoint](#).

Once a table similar to KI-KFI table (see [Figure 18](#)) has been built-up for each current setpoint, transitions should be considered between the lower setpoint and the upper one and vice versa. The purpose of variable frequency parameters optimization should be smooth and regular current transitions: both in raising and in falling transitions current should make continuous straight transitions and current waveform should have its steady state triangular shape, by few cycles after the transition is complete.

In order to achieve current transitions optimization, the user should try each couple of KI and KFI optimized for lower setpoint and each couple of KI and KFI optimized for upper setpoint, by changing them right after the related setpoint has been set by SPI.

Transient mode PWM period behavior both in raising and in falling current transition is influenced by the overall variable frequency parameters optimization.

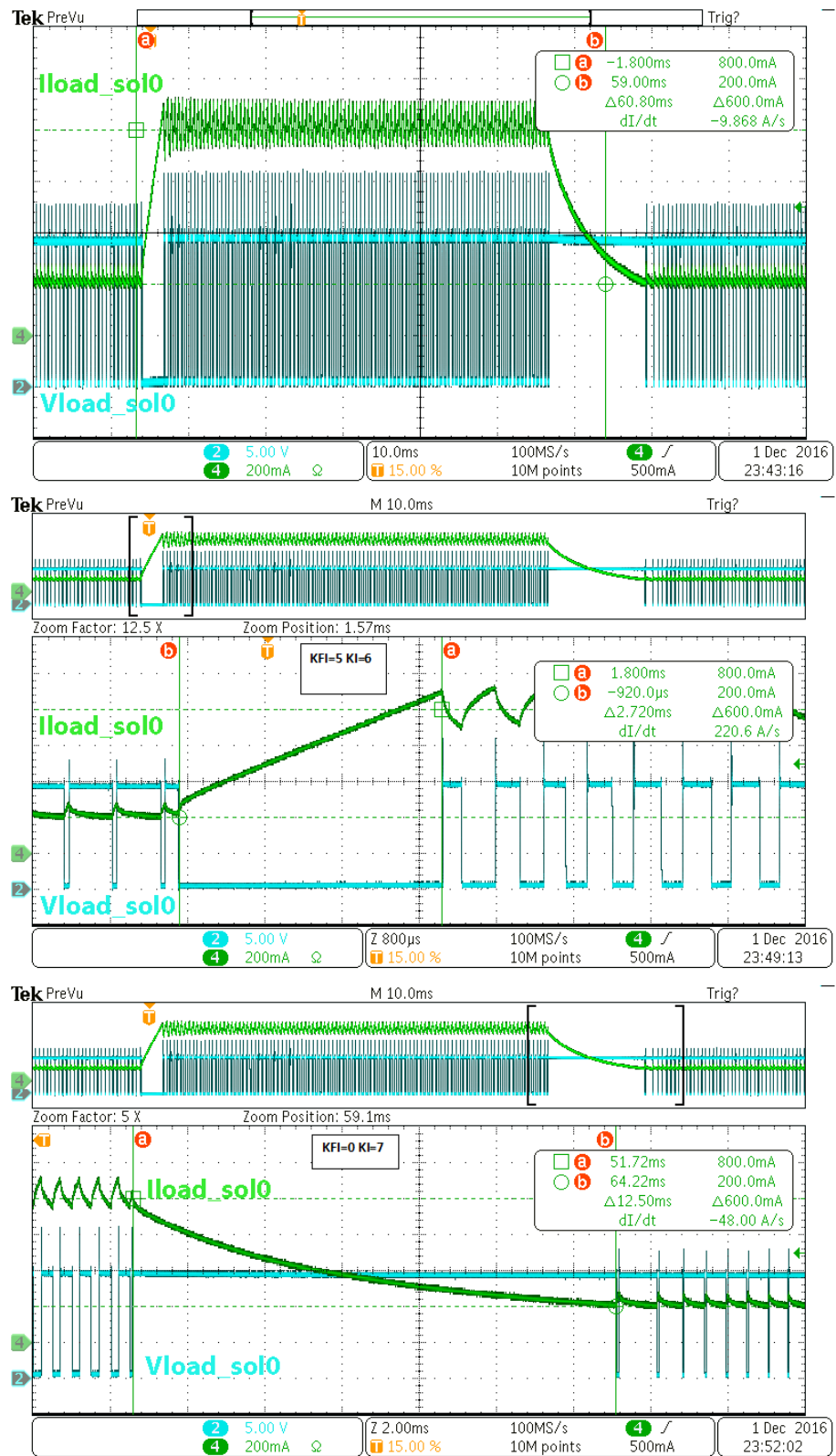
Note: *When driving a load in variable frequency mode, since the overall control is integral, current unwanted overshoot never occur during raising and falling transitions for all optimized couples of KI and KFI, even if such parameters are changed from higher values to lower values in current setpoint transitions.*

When driving a load in fixed frequency mode, both raising and falling transitions could be affected by current spikes, if KP is changed from higher values to lower values: obviously, the worst case is $KP = 7 \rightarrow 0$.

In fixed frequency mode, if KP is not the same in both low \rightarrow high and high \rightarrow low transitions, then overshoots could occur when setting KP from higher values to lower values.

In this case, the user should prefer controlling the current through variable frequency HW feedback mode by optimizing the variable frequency parameters, KI and KFI, in order to avoid current overshoots during setpoint transitions.

Figure 21. Variable frequency mode: accurate current setpoint transition



Note: Setpoint $I = 200 \text{ mA} \rightarrow 800 \text{ mA}$, PWM frequency $f = 2 \text{ kHz}$
 $KFI = 5/FINT_START = 7$, $POSINTLIM = 5/NEGINTLIM = 8$
 $KI = 6$ set after the $0.2 \text{ A} \rightarrow 0.8 \text{ A}$ transition
 $KFI = 0/FINT_START = 6$, $POSINTLIM = 4/NEGINTLIM = 8$ and $KI = 7$ set after the $0.8 \text{ A} \rightarrow 0.2 \text{ A}$ transition
 Current waveform is straight and smooth changing from the lower to the higher setpoint.
 Current waveform has its steady state triangular shape, few cycles after the transition is complete.

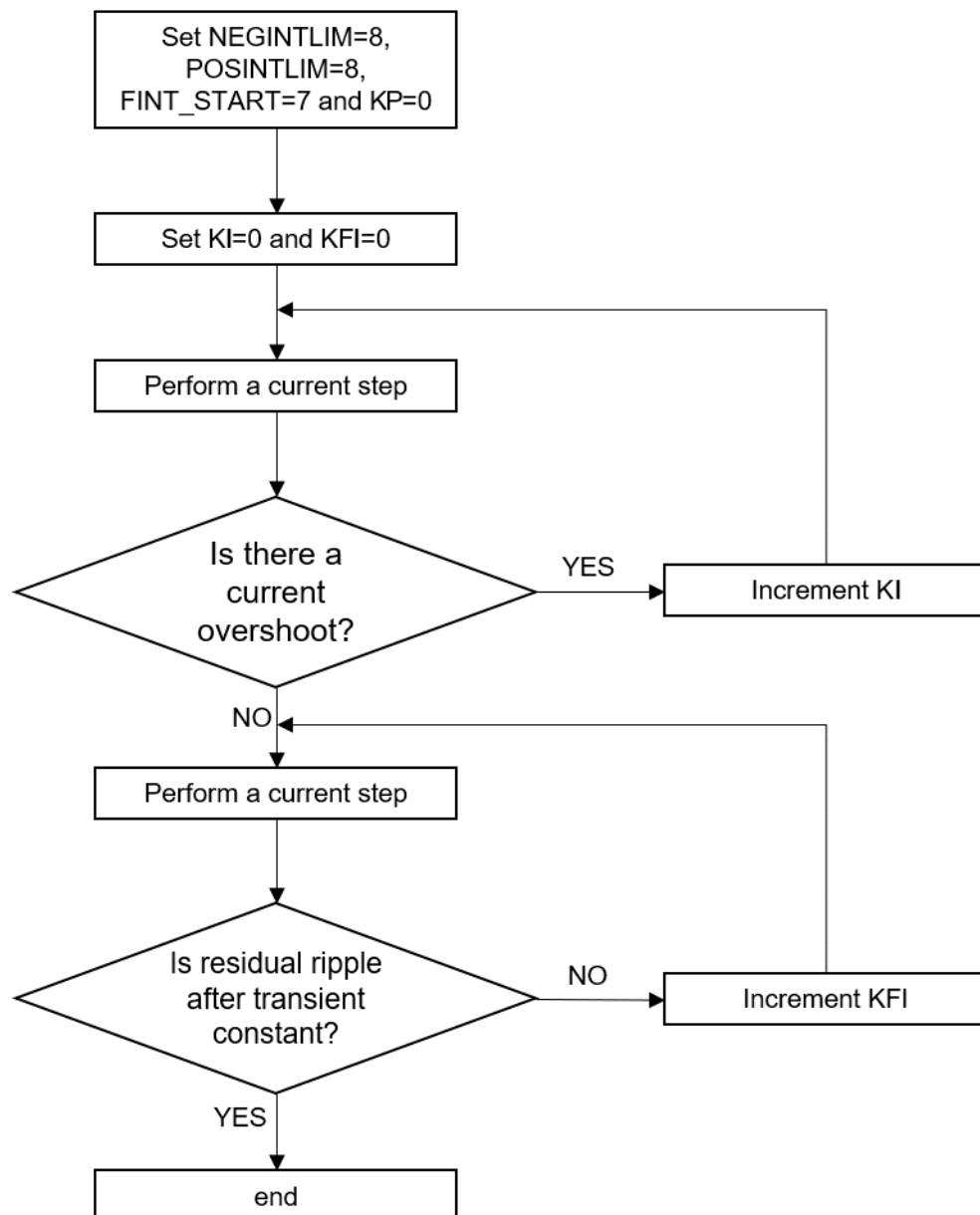
2.2.1 Algorithm for KI/KFI search

This section provides an alternative method to determine KI/KFI coefficients needed for Variable Frequency control mode. The proposed algorithm uses fixed POSINTLIM, NEGINTLIM and FINT_START values and, should the user change them, Ki and KFI previously found through the algorithm might need additional trimming, which, however, can be performed using the very same method.

The proposed procedure is valid for both HS and LS configuration, on any given channel and any current setpoint transition.

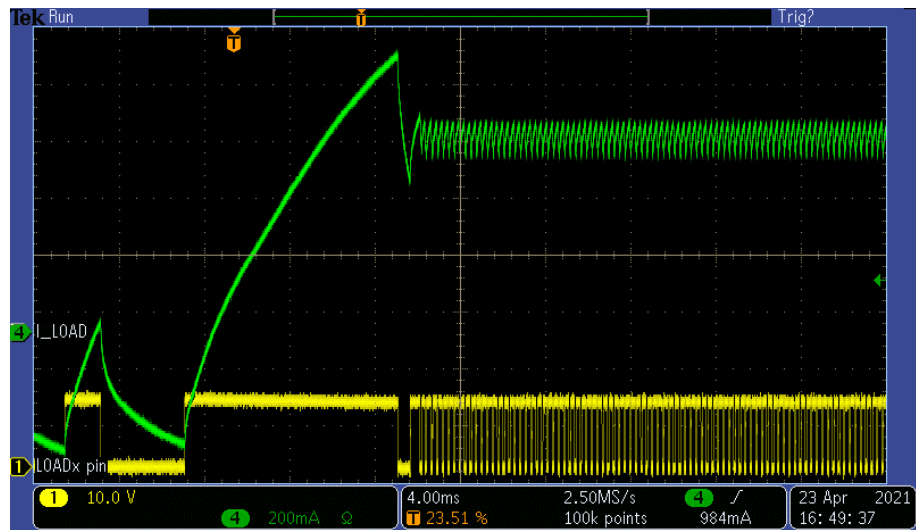
Following figure shows the suggested algorithm.

Figure 22. KI/KFI selection algorithm



Next pictures shows an example of a 500 mA to 1.5 A transition optimization process on a solenoid, done according to the proposed algorithm. Channel is configured in HS mode and pwm frequency is 2 kHz.

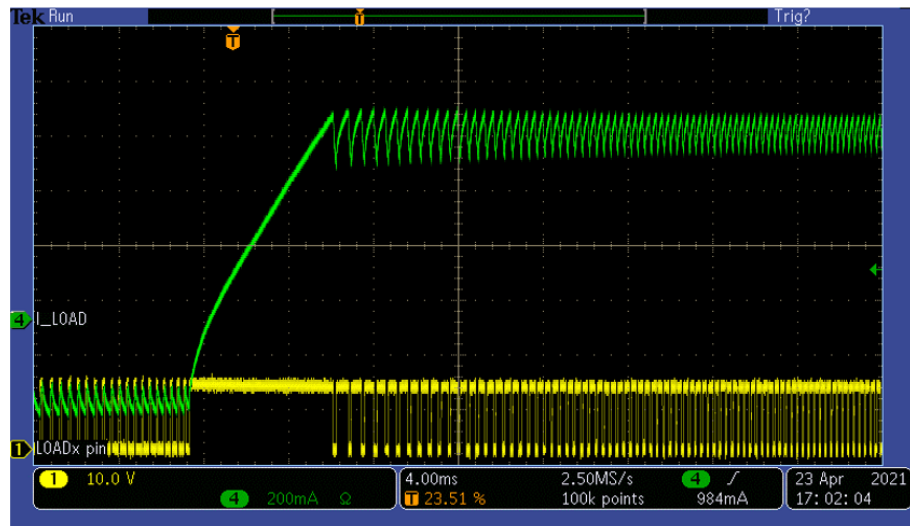
Figure 23. 500 mA - 1.5 A, variable frequency mode, not optimized



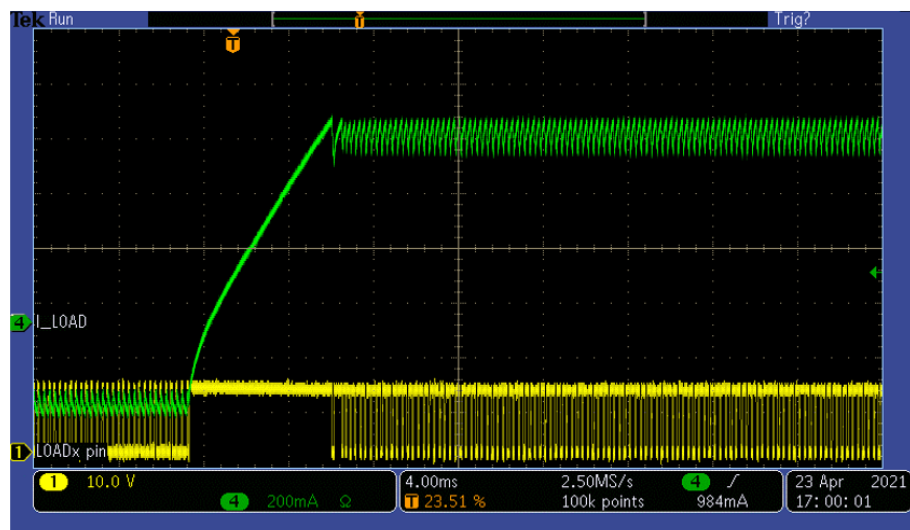
Load current transition has a large overshoot and 500 mA current is affected by a large ripple.

Next picture shows the results of the optimization performed following the algorithm: in Figure 24 (a), optimal KI has been found, obtaining the reduction of the initial overshoot; however, the regulated current still shows a quite big residual ripple, with higher amplitude just after the current setpoint step. This can be corrected by adding the effect of KFI coefficient, leading to the result shown in Figure 24 (b) after the optimization of the parameter.

Figure 24. Variable frequency parameters optimization



a. KI effect



b. KFI effect

Revision history

Table 10. Document revision history

Date	Version	Changes
28-Apr-2021	1	Initial release.

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