Application note

STWLC68JRH - Tuning guide

Introduction

This document is describing how to change the configuration of STWLC68JRH to achieve target performance.

The configuration of the STWLC68JRH is stored in non-volatile OTP memory. After power up of the device the configuration is retrieved from the OTP and used by FW. In parallel corresponding I^2C registers are updated based on the configuration from OTP. These I^2C registers, which are described in detail below, allow on-the-fly change of the configuration. A new value which is written into the I2C registers is immediately effective and retained until the device is powered down. Modification of the STWLC68JRH configuration through I^2C registers rather than via OTP is recommended because OTP configuration can be programmed only once unlike the I^2C registers located in RAM without any limits of rewritting attempts. When the tuning of the application is completed, the final configuration.h file is generated by Graphical User Interface (GUI) and used for OTP programming of blank devices. Since the configuration file is based on current content of the I^2C registers, the stored values should be verified prior proceeding with the generation of the .h file.

Note: Blank samples without any configuration in OTP will not respond to the Digital ping of the Tx. They are supposed to be used in DC Mode only (DC power connected to Vrect) to allow OTP programming or Configuration setting & generation using the GUI.

1 Interrupts

The core of the STWLC68JRH is designed to support different kinds of events through interrupt management. Table 1 reports the interrupts that can be enabled and configured.

1.1 Interrupts

Table 1. Interrupts

Name	Description
OTP_Int	Triggered when Over Temperature Protection happened (one of the OTP source exeeds the defined threshold)
OCP_Int	Triggered when Over Current Protection happened (one of the OCP source exeeds the defined threshold)
OVP_Int	Triggered when Over Voltage Protection happened (one of the OVP source exeeds the defined threshold)
Out_On_Int	Output of chip is enabled
Out_Off_Int	Output of chip is disabled
Sig_Str_Int	Signal Strength packet has been sent
Vrect_Rdy_Int	Vout is enabled if it is not blocked by other conditions - i.e. blocked by GPIO

1.2 Interrupt Enable (INT_EN)

Each bit of register enables the corrensponding interrupt bit. If the interrupt occurrs, the corresponding bit is set high in Interrupt Latch (INT_LATCH) register.

Table 2. Interrupt Enable (INT_EN)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0010	INT_EN	Out_Off_Int_En	Out_On_Int_En				OVP_Int_En	OCP_Int_En	OTP_Int_En
0x0011						Vrect_Rdy_Int_En	Sig_Str_Int_En		

1.3 Interrupt Clear (INT_CLR)

Each bit of register is cleared by writing "1" to the corresponding interrupt bit.

Table 3. Interrupt Clear (INT_CLR)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0012	INT_CLR	Out_Off_Int_Clr	Out_On_Int_Clr				OVP_Int_Clr	OCP_Int_Clr	OTP_Int_Clr
0x0013						Vrect_Rdy_Int_Clr	Sig_Str_Int_Clr		

1.4 Interrupt Latch (INT_LATCH)

Each corresponding bit is permanently set high until the bit is cleared by Interrupt Clear (INT_CLR) register. If the bit has to be cleared, write "1" to corresponding interrupt bit.

Table 4. Interrupt Latch (INT_LATCH)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0014	INT_LATCH†	Out_Off_Int_Latch	Out_On_Int_Latch				OVP_Int_Latch	OCP_Int_Latch	OTP_Int_Latch
0x0015						Vrect_Rdy_Int_Latch	Sig_Str_Int_Latch		

1.5 Interrupt Status (INT_STA)

The bits of INT_STA register are updated runtime and they are temporary set when the corresponding interrupt source is active.

Table 5. Interrupt Status (INT_STA)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0016	INT_STA†	Out_Off_Int_Flag	Out_On_Int_Flag				OVP_Int_Flag	OCP_Int_Flag	OTP_Int_Flag
0x0017						Vrect_Rdy_Int_Flag	Sig_Str_Int_Flag		

2 Protections

The STWLC68JRH is designed to protect itself and the application by means of dedicated internal circuits. Over-voltage, over-current and over-temperature are the typical events that can potentially trigger these protections. The bits of the PROT_EN register, summarized in Section 1 , are used to enable the desired protections.

2.1 Protection Enable (PROT_EN)

Table 6. Protection Enable (PROT_EN)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00C0	PROT_EN					Tshdn_OTP_En	Vntc_OTP_En	Tlr_OTP_En	Trect_OTP_En
0x00C1								Fxd_OVPS_En	Adj_OVPS_En
0x00C2									Irect_OCP_en

2.2 EPT on Event (PROT_EPT)

Since the transmitter stops its activity when End-of-Power Transfer (EPT) is received, the STWLC68JRH can be programmed to issue such a request on specific events. The PROT_EPT register allows the user select the events that should generate an EPT packet.

Table 7. EPT on Event (PROT_EPT)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00C4	PROT_EPT						Vntc_OTP_EPT_Req	Tlr_OTP_EPT_Req	Trect_OTP_EPT_Req
0x00C5								Fxd_OVPS_EPT_Req	Adj_OVPS_EPT_Req
0x00C6									Irect_OCP_EPT_Req

2.3 Output disable on Event

Similarly to PROT_EPT register, the PROT_OD allows associating specific events to the disconnection of the VOUT output.

Table 8. Output disable on Event

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00C8	PROT_OD						Vntc_OTP_Out_Disc	Tlr_OTP_ Out_Disc	Trect_OTP_ Out_Disc
0x00C9									Vrect_OVP_ Out_Disc
0x00CA									Irect_OCP_ Out_Disc

2.4 Source of OTP (Over Temperature Protection)

The STWLC68JRH has two internal temperature sensors, conveniently placed close to the rectifier and to the main linear regulator. An external temperature sensor (usually an NTC resistor) could be managed through the NTC pin (see STWLC68JRH data-sheet for details). The bits of the OTP_LATCH registers are set when the corresponding over-temperature thresholds are crossed.

Table 9. Source of OTP (Over Temperature Protection)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0018	OTP_LATCH†						NTC_OTP_Latch	Rect_OTP_Latch	Lin_Reg_OTP_Latch

Lin_Reg_OTP_Latch – Source of over-temperature protection which is controlled by temperature sensor of main linear regulator (Output)

Rect_OTP_Latch – Source of Over-Temperature protection which is controlled by temperature sensor of rectifier

NTC_OTP_Latch - Source of Over-Temperature protection which is controlled by external NTC sensor

2.5 Source of OVP (Over Voltage Protection)

The over-voltage condition, eventually detected at VRECT pin, actually consists of two independent circuits triggered by two different voltage thresholds (see STWLC68JRH data-sheet for details). The OVP_LATCH register reports a latched information, indicating that an OVP condition occurred or is in progress.

Table 10. Source of OVP (Over Voltage Protection)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0019	OVP_LATCH†							Fxd_OVPS_Latch	Adj_OVPS_Latch

Adj_OVPS_Latch – Source of Over-Voltage protection which is controlled by FW

Fxd_OVPS_Latch - Source of Over-Voltage protection which is controlled by HW

2.6 Source of OCP (Over Current Protection)

The maximum current flowing from rectifier is measured and compared to a programmable threshold: if such a threshold is crossed, the least significant bit of OCP_LATCH register is set. A corresponding action can be triggered by such an event.

Table 11. Source of OCP (Over Current Protection)

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x001A	OCP_LATCH†								OCP_Latch

2.7 OTP threshold of rectifier temperature sensor

Threshold for Over-Temperature protection based on rectifier sensor in °C which is related to Rect_OTP_Latch in Source of OTP (Over Temperature Protection) register.

Table 12. OTP threshold of rectifier temperature sensor

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00A6	TRECT_OTP	Over-Temperature detection Threshold related to Rectifier Temperature sensor							
0x00A7									

2.8 OTP threshold of main linear regulator temperature sensor

Threshold for Over-Temperature protection based on main linear regulator sensor in °C which is related to Lin_Reg_OTP_Latch in Source of OTP (Over Temperature Protection) register.

Table 13. OTP threshold of main linear regulator temperature sensor

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00A8	TLR_OTP	Over-Temperature detection Threshold related to main Linear Regulator Temperature sensor							
0x00A9									

2.9 OTP threshold of external NTC temperature sensor

Threshold for Over-Temperature protection based on NTC in mV which is related to NTC_OTP_Latch in Source of OTP (Over Temperature Protection) register.

Table 14. OTP threshold of external NTC temperature sensor

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00AA	VNTC_OTP	Over-Temperature detection Threshold related to external NTC pin							
0x00AB									

2.10 OVP threshold at VRECT pin of rectifier voltage sensor

Threshold for Over-Voltage protection in mV which is related to Adj_OVPS_Latch in Source of OVP (Over Voltage Protection) register and is also using as threshold of IEXT protection (see STWLC68JRH datasheet).

Table 15. OVP threshold at VRECT pin of rectifier voltage sensor

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00AC	VRECT_OVP	VRECT Over-Voltage detection Threshold (Adjustable OVP-Clamper)							
0x00AD									

2.11 OCP threshold of current sensor

Threshold for Over-Current protection based on current sensor in mA which is related to OCP_Latch in Source of OCP (Over Current Protection) register.

Table 16. OCP threshold of current sensor

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00AE	IRECT_OCP	IRECT Over-Current detection Threshold							
0x00AF									

3 ASK modulation

The ASK modulation index can be changed according to the operating condition (rectifier current). Two ranges for the output current are defined and the modulation pins (both COMMx and CLAMPx pairs) are managed accordingly.

The current threshold indicates the switching between normal current range of ASK modulator and low current range of ASK modulator (see ASK Modulation configuration register)

3.1 Threshold of ASK settings

The lower threshold (NCR to LCR transition) is the value set in the LCR_THR register, while the upper threshold (LCR to NCR transition) is given by:

Threshold = LCR_THR + LCR_HYST

Table 17. Threshold of ASK settings

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0041	LCR_THR	Normal-Current Range (NCR) to Low-Current Range (LCR) threshold (4 mA/step)							

3.2 Hysteresis of ASK settings

Table 18. Hysteresis of ASK settings

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0042	LCR_HYST	Low-Current Range (LCR) to Normal-Current Range (NCR) hysteresis (4 mA/step)							

3.3 ASK Modulation configuration

Once the low-current and normal-current ranges are defined, the operation of the modulation pairs (COMMx and CLAMPx pins) is set thruogh the MOD_CFG register.

Table 19. ASK Modulation configuration

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0043	MOD_CFG			LCR_Clamp_Mod_En	LCR_Comm_Mod_En			NCR_Clamp_Mod_En	NCR_Comm_Mod_En

NCR_Comm_Mod – COMM1 and COMM2 capacitors are used in normal current mode

NCR_Clamp_Mod – CLAMP1 and CLAMP2 capacitors are used in normal current mode

LCR_Comm_Mod – COMM1 and COMM2 capacitors are used in low current mode

LCR_Clamp_Mod – CLAMP1 and CLAMP2 capacitors are used in low current mode

3.4 Adaptive dummy load

The dummy load is adaptive current load ensuring the minimal total current.

Table 20. Adaptive dummy load

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0044	IDMYL_SET				Dummy load current: 0 mA to 310 mA (10 mA/step)				

Example:
Idle current is 20 mA
Output current is 100 mA
Adaptive dummy load is set to 200 mA
Dummy current which balances the load is 80mA to ensure total load is 200 mA

4 Foreign Object Detection (FOD)

FOD parameters used for FOD calibration, for more details see the STWLC68JRH FOD application note which is available on st.com

Table 21. FOD_CTC

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0080	FOD_CTC	FOD Current Threshold Calibration							

Table 22. FOD_GSC

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0083	FOD_GSC	FOD Gain Scaler Calibration							

Table 23. FOD_OLC

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0087	FOD_OLC	FOD Offset Level Calibration							

Table 24. FOD_DCR

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x008B	FOD_DCR	Coil DC-Resistance for FOD calculation							

5 Monitoring registers

5.1 Operating frequency

Table 25. Operating frequency

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0038	AC_FREQ†	Rectifier Operating Frequency (in kHz)							
0x0039									

5.2 Signal strength

Signal strength value which is sent to transmitter during the first phase of communication.

Table 26. Signal strength

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x003A	S_STR_TX†	Signal Strength Level sent to transmitter							

5.3 Output voltage

Table 27. Output voltage

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x003C	VOUT_SET	Output Voltage setting: 25 mV to 22 V (25 mV/step)							
0x003D									

5.4 Main linear regulator voltage drop

The device is maintaning the voltage drop on the main linear regulator (Vrect - Vout) based on the measured current from rectifier. Relationship between current from rectifier and target voltage drop is defined in Figure 1.

The effect of this settings has direct impact on heating of chip. The settings has to be the compromise between avoiding impact of negative Vrect modulation on output and also heating of the chip.

Figure 1. Target drop-out of main linear regulator

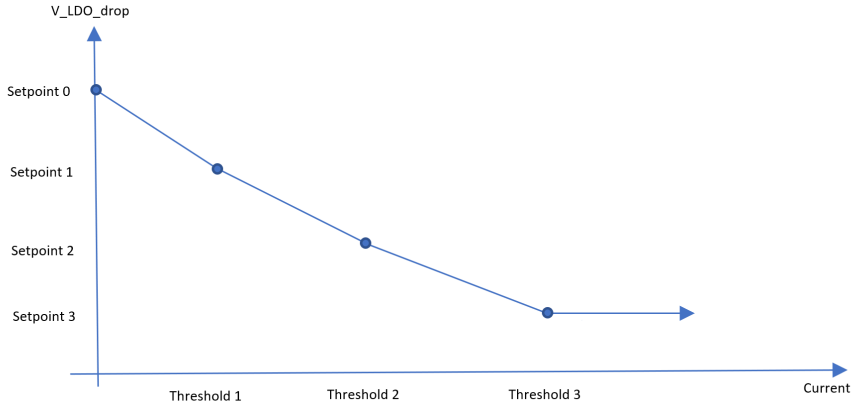

Table 28. Main linear regulator voltage setting

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0049	VDROP_V0	Linear regulator target drop-out voltage, setpoint 0							
0x004A	VDROP_V1	Linear regulator target drop-out voltage, setpoint 1							
0x004B	VDROP_V2	Linear regulator target drop-out voltage, setpoint 2							
0x004C	VDROP_V3	Linear regulator target drop-out voltage, setpoint 3							
0x004D	VDROP_C1	Linear regulator target drop-out voltage, current threshold 1							
0x004E	VDROP_C2	Linear regulator target drop-out voltage, current threshold 2							
0x004F	VDROP_C3	Linear regulator target drop-out voltage, current threshold 3							

Note: ADC reading of Vrect voltage can show offset error in range of tens of mV based on the soldering profile & PCB layout. This offset shall be constant for all devices on the same PCB and soldered using same soldering profile. It is good practice to measure this offset i.e. in DC mode and adjust the LDO drop curve setting.

I.e. for target real Vdrop = 100mV and having Vrect offset error = +40mV the Vdrop in Configuration shall be set to 60mV

6 General settings and command registers

6.1 Idle power consumption

Idle current consumption of the application when is in DC mode (supplied from Vrect) and the IDMYL register has to be set to 0mA.

This value is used for self-calibration of the current sensor. If the internal LDOs 1V8 and 5V0 are used to supply any external peripherals in the final application these peripherals shall be connected and supplied during this measurement so their power consumption shall be included in this value.

Table 29. Idle power consumption

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0098	IDLE_CC	Chip idle current consumption (in mA)							

6.2 Automatic output enable

Threshold of Vrect which is automatically enabled the main linear regulator after the exceeding of this threshold.

The formula is as following:

Threshold = VDROP_V0 - VTH_AOE

Table 30. Automatic output enable

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0040	VTH_AOE	Voltage threshold for automatic output enable: 240 mV to 1049 mV (16 mV/step)							

6.3 Vout UVLO

Table 31. Vout UVLO

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0045	VRECT_MIN	Vrect_Min_Ctrl_En			Minimum VRECT voltage (3.5V to 11V, 0.5 V/step) for constant VOUT				

6.4 Command register

Table 32. Command register

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0020	DIR_CMD						Send_EPT		Send_Msg
0x0021								Out_Off	Out_On

Send_EPT – Write "1" to this bit in case receiver should send EPT to transmitter (see EPT message register)

Out_On – Write "1" to this bit in case output should be enabled
Out_Off – Write "1" to this bit in case output should be disabled

6.5 TX message

Write data and write "1" to Command register, Send_Msg for sending of data to transmitter. The message packet content has to be compliant with Proprietary Packet definition in Qi specification.

Table 33. TX message

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0050	MSG_TX	Message packet content to be sent to transmitter via ASK modulation (see DIR_CMD register)							
0x0051									
0x0052									
0x0053									
0x0054									
0x0055									
0x0056									
0x0057									
0x0058									

6.6 EPT message

Set the Send_EPT bit in Command register for sending of EPT_MSG to transmitter.

Table 34. EPT message

Register Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0062	EPT_MSG	EPT Message (root cause event) added to EPT packet (see DIR_CMD register)							

Revision history

Table 35. **Document revision history**

Date	Version	Changes
10-Mar-2020	1	Initial release.

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