Application note

8-channel, 50 ksps to 1 Msps, 12-bit A/D converter

Introduction

The ADC120 is a low-power, 8-channel pure CMOS 12-bit analog-to-digital converter specified for conversion from 50 ksps to 1 Msps.

The architecture is based on a successive-approximation register with an internal track-and-hold cell. The ADC120 features 8 single-ended multiplexed inputs. The output serial data is straight binary and the communication interface is SPI standard compatible.

The analog and digital power supplies operate from 2.7 V to 3.6 V. The power consumption at 3.3 V nominal supply is as low as 6.6 mW.

The ADC120 comes in a plastic TSSOP-16 package, it can operate from -40 °C to +125 °C ambient temperature.

1 Overview

The ADC120 device is an 8-channel successive-approximation analog-to-digital converter running with 12-bit resolution at classical 3.3 V on analog and digital side. The communication level is compatible with almost all microcontrollers and it is performed through SPI interface.

2 SPI interface: communication signals

The Figure 1. Operational timing diagram, Figure 2. Serial timing diagram and Figure 3. SCLK and CSn timing parameters show the full duplex SPI interface communication signals used between the controller (master) and the device ADC120 (slave).

The ADC120 has a wording to make a correspondence with general SPI data lines. The following names are used:

- DIN is the signal generally named MOSI (master output slave input)
  - This signal is used to transfer to the slave the next channel number to be read
  - When the ADC120 state machine has decoded the channel sent on DIN, the internal multiplexer selects the channel and the ADC120 reads the voltage and provides the data.
- DOUT is the signal generally named MISO (master input slave output)
  - this signal is used to transfer to the master the data digitalized from the analog signal present on the channel that has been selected
- SCLK is the clock provided by the master to the ADC120
  - This clock is used internally to sample the signal
  - As the SPI interface runs on a 16-bit word, the internal sampling is clocked by the SCLK divided by 16 (a 1 Msps uses a 16 MHz clock)
- CSn (chip select) is directly linked to the slave selection line generally named SS (slave select)
  - CSn is a signal active on a low logic voltage
  - CSn selects the chip that communicates on the SPI physical interface
  - CSn is also used by the ADC120 as a power-ON signal to start internal state machine

Figure 1. Operational timing diagram

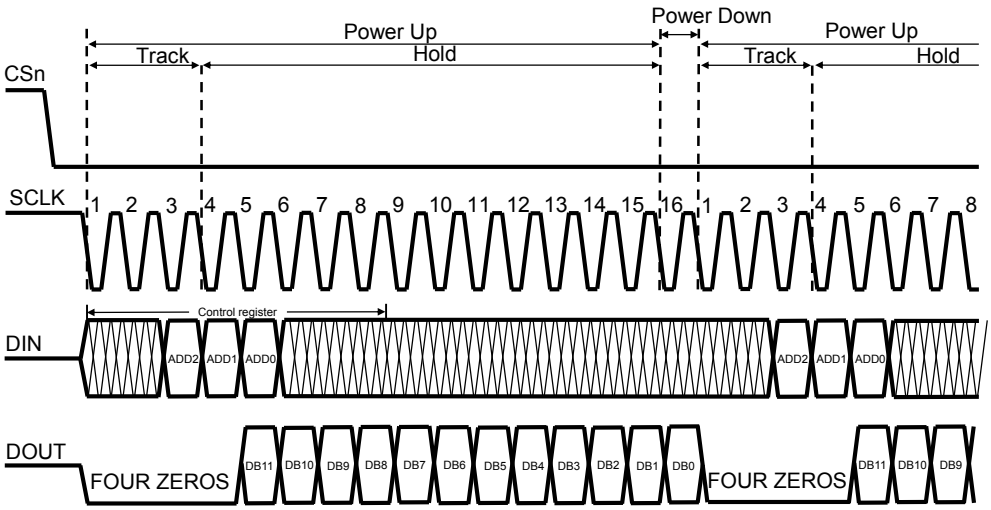


Figure 2. **Serial timing diagram**

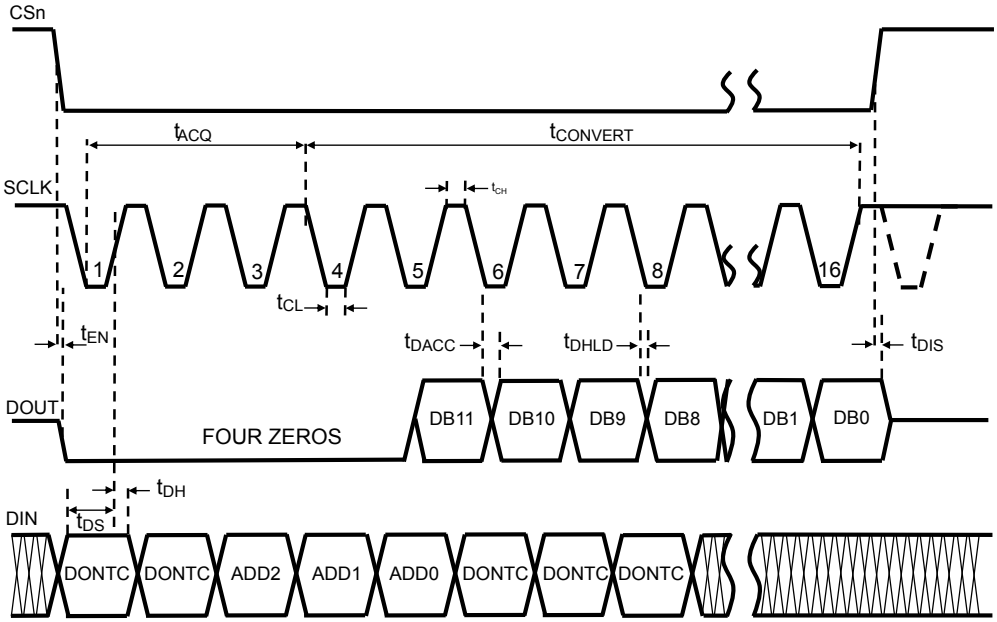
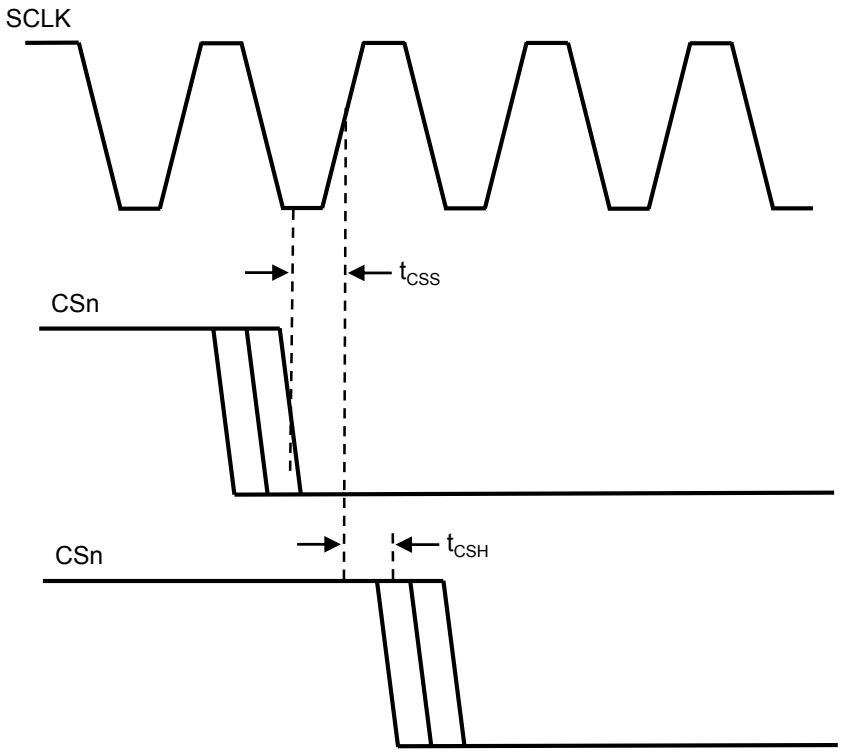


Figure 3. **SCLK and CSn timing parameters**



3 The ADC120 operating mode

The ADC120 can convert up to 8 different channels. It integrates a multiplexer that can route the signal input channel to the input capacitor used to digitalize the analog signal.

The ADC120 runs in two steps, the device starts and tracks the signal and then holds the input to make the digital code calculation. Thus, it transfers the data on the serial interface.

The ADC120 is active when the CSn is low. A correct clock frequency and cycle numbers on the SCLK pin must be used. As presented in Figure 1. Operational timing diagram, the first three clocks are used to track the input analog signal and the thirteen other clocks transfer the digitalized signal through the interface.

After the track and hold period, the data is present on the SPI bus output: on the DOUT line (MISO line). The data is transferred on 16 clock cycles: the first four bits are set to 0 and the converted data is transmitted on the 12 following bits, MSB first.

The user attention is drawn to the fact that the data sampled at T0 time is outputted at T0+16SCLK on the DOUT bus. Another important point is that the device measures the channel 0 just after the CSn has been set low. To get another channel measurement, a request must be sent and the results are obtained on the second bit frame.

During the tracking period, the device connects the sampling capacitor to the input; this capacitor is charged to the analog voltage. Particular attention should be taken to be sure that the ADC measures the right voltage, the settling time of the input should be in line with the ADC120 requirements. The ADC120 front-end is faced in Section 5 Analog inputs and analog front-end constraints.

4 ADC coding and maximum scaling value

The converted input voltage appears on the SPI interface in a 12-bit natural binary code format. The LSB (quantum) of the conversion is directly linked to the analog voltage that supplies the ADC.

$$LSB = \frac{AVCC}{2^{12}} = \frac{AVCC}{4096} \quad (1)$$

Typically, for 3.3 V analog supply, the LSB is rounded to 0.806 mV.

The transition between the code 0x00 and 0x01 has a different step of ½ LSB and then the difference between each code is 1 LSB.

Particular attention must be taken on the analog power supply, a proper decoupling by 1 uF in parallel with a 10 nF capacitor should be used.

To remove some low noise problems due to the variation of the voltage supply that is also the reference voltage, it is possible to use the analog power supply to also supply the sensor (temperature sensors, wheatstone bridges, current front-end amplifiers, etc.)

5 Analog inputs and analog front-end constraints

The ADC120 inputs run from 0 to AVCC voltage (rail-to-rail voltage), this input voltage should not be above the supply voltage because the ADC input is saturated, and the output code is 0x0FFF.

Depending on the voltage condition at the channel input, the protection diode of the device can conduct, and the conversion is then false.

During the track period, the capacitance seen has typically a value of 45 pF. The front-end of the application must take this value into account to be sure that the ADC120 measures the right input voltage. This is particularly true if the device runs dynamically to follow a voltage variation.

Generally, in front of each ADC channel a low-pass filter is present to filter the input signal and to perform an anti-aliasing filter. The simplest filter is composed of a resistor in series and a capacitor in parallel to the ground. This RC filter should present a particular characteristic and the components value can be calculated.

The cut-off frequency for a first order RC filter is as follows:

$$f_c = \frac{1}{2\pi RC} \quad (2)$$

where:

- f_c is the RC filter cut-off frequency

This filter frequency must be in line with the maximum sampling rate; the ADC120 has a maximum sampling rate at 1 Msps. The calculation is only done at that sample rate, for slower ADC sample rates, the filter should be different, but the calculation is still valid.

This maximum sampling rate is shared on the 8 channels. As this sampling rate is directly linked to the SPI clock frequency, and, the SPI runs on a 16-bit word; when all the 8-channel inputs are used, the sampling rate can be written as the following equation:

$$f_{SR} = \frac{F_{SCLK}}{16x8} \quad (3)$$

Where:

- f_{SR} is the sample rate frequency
- F_{SCLK} is the SPI clock frequency

Of course, the maximum sampling rate is obtained when a single channel is used. In that case, the sample rate frequency is the frequency calculated multiplied by eight, so we have:

$$f_{SR-1channel} = \frac{16MHz}{16} \quad (4)$$

where

- $f_{SR\_1channel}$ is the cut-off frequency for a unique channel

Given the Shannon sampling theorem:

$$f_{Sampling} > 2^{*} f_C \quad (5)$$

So, changing by the value both part of the anti-aliasing filter, the final equation, using Eq. (2), can be written as follows:

$$2^{*}\pi^{*} f_c = \frac{1}{RC} \quad (6)$$

and therefore

$$RC > \frac{1}{2^{*}\pi f} \quad (7)$$

Since the sampling rate is shared by the eight channels, the coefficient 8 must be applied and the result is:

$$RC > \frac{1}{2x8^{*}\pi f_C} \quad (8)$$

Concerning the ADC120, since it has the velocity of 1 Msps (1 MHz sampling), the clock frequency must be 16 MHz, the RC filter must be chosen with the following condition RC > 2.55e-6 s, in other words, the cut-off frequency must be f_C < 62.5 kHz.

In that case, the RC filter can be chosen with R= 300 Ω and C= 10 nF. It provides a RC = 3e-6 s, representing a cut-off frequency of 53 kHz.

6 Description of the device functional modes

The device runs only when the pin CSn is set to low otherwise the device is in standby mode with the lowest consumption on the power supplies.

So, when the CSn pin is at low level (grounded), respect to the SPI timing described in the SPI table of the datasheet, the device runs and can convert the voltage present on the selected input.

The clock of the device is used to perform the acquisition on a 16-clock cycle. The first 3 SCLK is the track period and the 13 following SCLK edge signal is the hold period.

The communication of the results of the conversion is present on DOUT on the following 16 clock cycle. Thus, the data read from T0 to T0+16 clock cycles are the data on DOUT sampled from T0-16 clock cycles to T0. Figure 1. Operational timing diagram shows the SPI communication.

Moreover the device can run in continuous mode or in burst mode.

- Continuous mode: the CSn is kept low and the clock is never stopped. The device takes the first 16 clocks to do the acquisition (track period) and the data transfer (hold period) and then the sequence is reproduced on the next 16 clocks till the CSn is set to low. Continuous mode provides the most important throughout.
- Burst mode: after 16 clocks the CSn signal goes high (when channel 0 is the channel to be read, otherwise, the CSn must be set high after 32 clock cycles to read one of the other 7 channels (channel selection is sent during the first 16 clock cycles on DIN), the device is stopped and ready to make another conversion when the chip is going to be selected. This burst mode allows a minimum consumption of the device to be performed into the system

The consumption is going to be averaged thanks to the shutdown after the conversion. Depending on the sampling time ($t_{converter}$) and the shutdown time ($t_{shutdown}$) the power consumption can be done by the equation below:

$$P_{device} = \frac{t_{convert}}{t_{convert} - t_{shutdown}} x\, P_{convert} + \frac{t_{shutdown}}{t_{convert} - t_{shutdown}} x\, P_{shutdown} \quad (9)$$

7 SPI interface and the device programming

7.1 Serial interface

The serial interface is 4-wire SPI compatible. The CSn selects the chip and acts as a power-on, when the CSn is high, the device DOUT is in high impedance and the clock is internally off. Otherwise, when CSn is low, the clock arrives on the SLCK pin of the device, and, the chip is ready to convert using the DIN to select the channel and DOUT to transfer the data to the processor with MSB first.

The clock controls the time for acquisition and for data transfer.

The clock must be sent after CSn is set low with a frame of 16 rising edges; this clock must be generated to program the device and read the data. In continuous mode, the clock must be an integer number multiple of 16 clocks to be able to make continuous measurements. In burst mode, a frame of 2 x16 clocks must be sent to read the predefined channel because by default, the first reading is done on the channel 0.

If the clock is always present, the clock and the CSn signals are dependent together. In Figure 3. SCLK and CSn timing parameters, the time T_{css} represents the time before the rising edge of the clock uses this edge as the first clock number. T_{csh} is the delay between the falling edge of the clock and the first rising edge of the DIN. In that case, the device can run properly on the next rising edge of the clock.

DIN selects the channel, the multiplexer is properly programmed and the signal at the input of the ADC must be settled to make a correct measurement without error.

7.2 Programming

The protocol is described into the operational timing diagram presented Figure 2. Serial timing diagram. The DIN and DOUT signal changes on the falling edge of the clock and the data is read on the rising edge of the clock.The device runs with a polarity CPOL = 0 and a phase CPHA = 0

When the product has CSn at low level and the clock in the good frequency range, the first 2-bits of the DIN are not interpreted (do not care) and the next 3-bit represents the next channel to be read then the rest of the 8-bit is also not interpreted (do not care).

The code sent to DIN selects one of the eight channels. The next table presents the code to position the multiplexer on the good channel.

Table 1. Input channel description

Channel	Hexadecimal code
Channel 0 (default)	0x00
Channel 1	0x08
Channel 2	0x10
Channel 3	0x18
Channel 4	0x20
Channel 5	0x28
Channel 6	0x30
Channel 7	0x38

DOUT is generated by the ADC, the data is set on the bus on the falling edge of the clock. The DOUT is set on a 16-bit frame for 12-bit information presented in natural binary format. The frame starts with 4-bit set to 0 and then the 12-bit conversion data is sent on the interface. When the frame does not start with 4 bits set to 0, the data is not correct. It is then important to restart the device, the master must set the CSn signal at high level, stop the clock and then make a new request to the ADC (send the CSn low, send the clock, send the DIN, receive the correct answer on the second reading of the bus if the address is not representing the channel 0).

In continuous mode, the reading of the data on DOUT starts on the rising edge of the 17th clock, the falling edge of the 16th clock is the startup to count the new number of clocks. Of course, the DIN is also read on this clock count (2 first bits are still “do not care and the 3 next bits select the channel according to Table 1. Input channel description”).

8 Application design and information

This section gives the main guidelines to the application designer to do an acceptable ADC acquisition design.

Figure 4. Typical ADC application

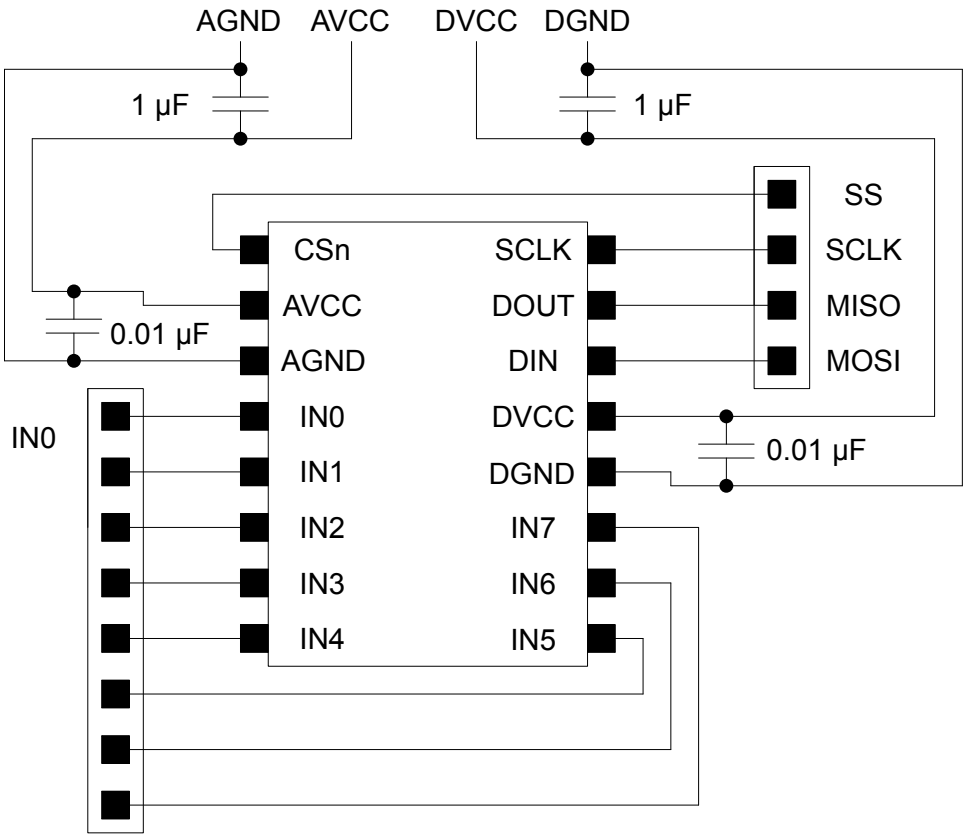


Figure 4. Typical ADC application presents the ADC120 schematic.

Some rules must be applied to get the best product performance. Thus the following recommendations must be applied when a board with the ADC120 is being designed.

Component placement: do not mix analog and digital components

A system is generally a complex association of different devices, some of them are purely analog (operational amplifier for example) and the others are mainly digital devices (microcontroller for instance), RF devices are also specific devices.

Whenever it is possible, a board split into 2 different parts is preferable; on one side, the analog devices and on the other, the digital products. The different PCB wires must be routed with attention, analog lines should be placed far from digital ones, specific layers can be used; or tracks separated by a real ground plane must be designed.

In this application note, the component is an analog-to-digital converter, thus both analogical and numerical signals are connected to the device input pins. It is suggested to have a differentiation on the board between the numerical and analogical signal paths and power supply paths. The general implementation through different layers or ground plane among wires must be used. Ground plane must be present under the component to ensure a proper shielding.

Ground plane and return path

Each PCB design is different and general rules must be applied. So, it is recommended to dedicate a layer to the ground plane. This ground plane, common-to-analog and digital devices, makes the shortest power return path. Via stitching is recommended to ensure the stability (the lowest impedance everywhere) of the ground plane. The ground plane must have an intact shape, it should not be cut by a wire, otherwise, the current can flow as close as the current signal. If it not possible, vias must be placed to minimize the return current path to the source. This return path must follow a very precise design, no large current loop must be done to minimize the radiation and the device perturbations. (This is mandatory for DCDC analog power source, digital or high frequency signal).

Power supply plane for analog and digital is not mandatory, but digital power supply path must not overlap the analog signal trace and the digital signal trace must not overlap analog power supply plane (on same or different layers).

Resistor and inductance paths

PCB route self-resistance and self-inductance should be considered, especially with fast transient signals or high frequency signals. Each resistance or inductance can cause a voltage error due to the current flowing through the route, even with a low current level. One of the best ways to route the board is to consider analog input as differential pair and the routing can be done without impedance control, minimizing the difference in trace length and using a ground plane shielding.

Decoupling capacitor (value, location)

Power supply lines must be decoupled by bypass capacitors connected to the ground; these capacitors perform a filtering of the power supply.

The best practice is to have several capacitors:

one of 100 nF (fast energy tank close to the power supply pin of the component). It is recommended to place the capacitor on the same layer of the devices to protect, this placement avoids any vias between the capacitor and the product and the capacitor effect is optimized.

Another capacitor of 10 µF (more consistent energy tank, longer to charge but more energy to power up component) is used and can be placed farther from the device; it is able to absorb the current peak at lower frequency. Tracks coming from the decoupling capacitor pads must be direct to the ground plane.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
22-Apr-2020	1	Initial release.

Contents