45W USB Type-C™ PD adapter board with controllers STCH03 QR flyback, SRK1001 adaptive synchronous rectifier and STUSB4761 USB Type-C™ PD

Introduction

This application note describes the operation and the performance of the EVLSTCH03-45WPD demo board.

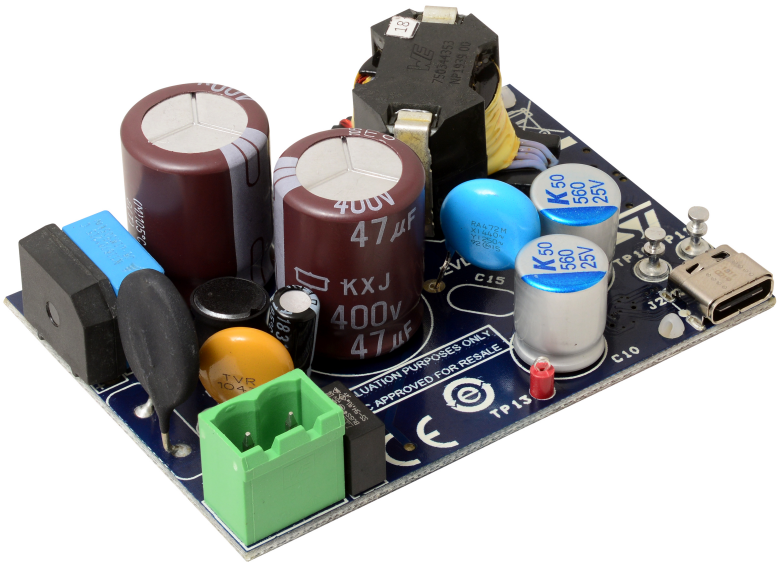
The EVLSTCH03-45WPD is designed to deliver a maximum output current of 3 A and a variable output voltage between 5 V and 20 V. The maximum power that the EVLSTCH03-45WPD demo board can deliver is 45 W.

The EVLSTCH03-45WPD is based on the quasi-resonant flyback controller STCH03, the synchronous rectifier controller SRK1001, and the USB-PD Type-C controller STUSB4761 .

The EVLSTCH03-45WPD 45W USB Type-C Power Delivery 3.0 adapter is a USB-IF certified solution and reference design, the respective Test ID reference are:

- Power Brick EVLSTCH03-45WPD TID: 2071
- PD Controller STUSB4761 TID: 2070

Figure 1. EVLSTCH03-45WPD evaluation board



Important:
This product is intended for evaluation purpose only. Although it is designed to satisfy safety isolation requirement it shall be operated in a designated test area by personnel qualified and all testing should be performed with an isolation transformer to provide the AC input to the demo board.

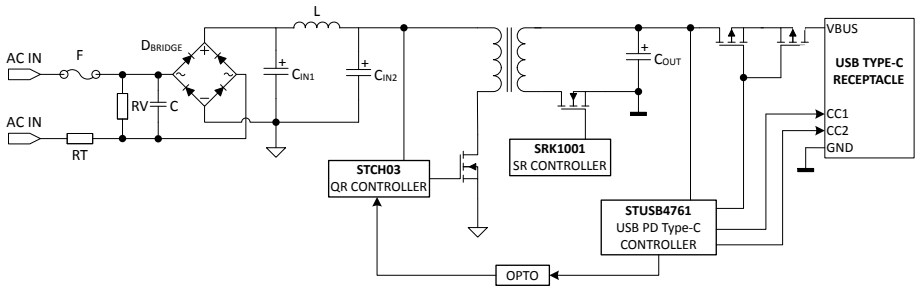
1 Introduction chapter 1

This application note describes how to design a 45 W Type-C Power Delivery adapter solution that supports the following PDOs: 5 V / 3 A, 9 V / 3 A, 12 V / 3 A, 15 V / 3 A, 20 V / 2.25 A and accepts a wide inputs main range (90 V_{AC} to 265 V_{AC}).

The EVLSTCH03-45WPD represents an effective solution where isolation from the AC mains is required, and where cost effectiveness, high efficiency and low standby power are essential.

The EVLSTCH03-45WPD is an isolated power supply developed for USB Type-C Power Delivery adapter applications. The primary side of the evaluation board implements a Quasi Resonant flyback converter based on an STCH03 controller with optocoupler feedback for the voltage regulation. The secondary side implements an Adaptive Synchronous Rectification based on the SRK1001 controller in order to increase the overall efficiency of the system. The management of the USB Type-C Power delivery is based on an STUSB4761 controller. Figure 2 below shows the block diagram of the demo board.

Figure 2. EVLSTCH03-45WPD evaluation board block diagram



The features of the three controllers used to realize this adapter allow a compact and lightweight design with high power density and with very low stand-by consumption, below 30 mW.

This evaluation board is compliant with CoC Tier 2 regulations thanks to the new MDmesh M6 technology primary Power MOSFET STF7N65M6 and new STripFET F7 technology and synchronous Power MOSFET STL110N10F7 that offer a very low on-state resistance.

The EVLSTCH03-45WPD is protected against destructive electrostatic discharge from the USB Type-C connector using a Dual Transil array for ESD protection, ESDA25L.

2 Specifications

Table 1 shows the specifications of the demonstration board. This design could be used to develop a charger/ adapter and the circuit board would need to be modified depending on shape and form factor of the housing. Performance should be evaluated with the new design and layout/components adjusted to meet the target specification.

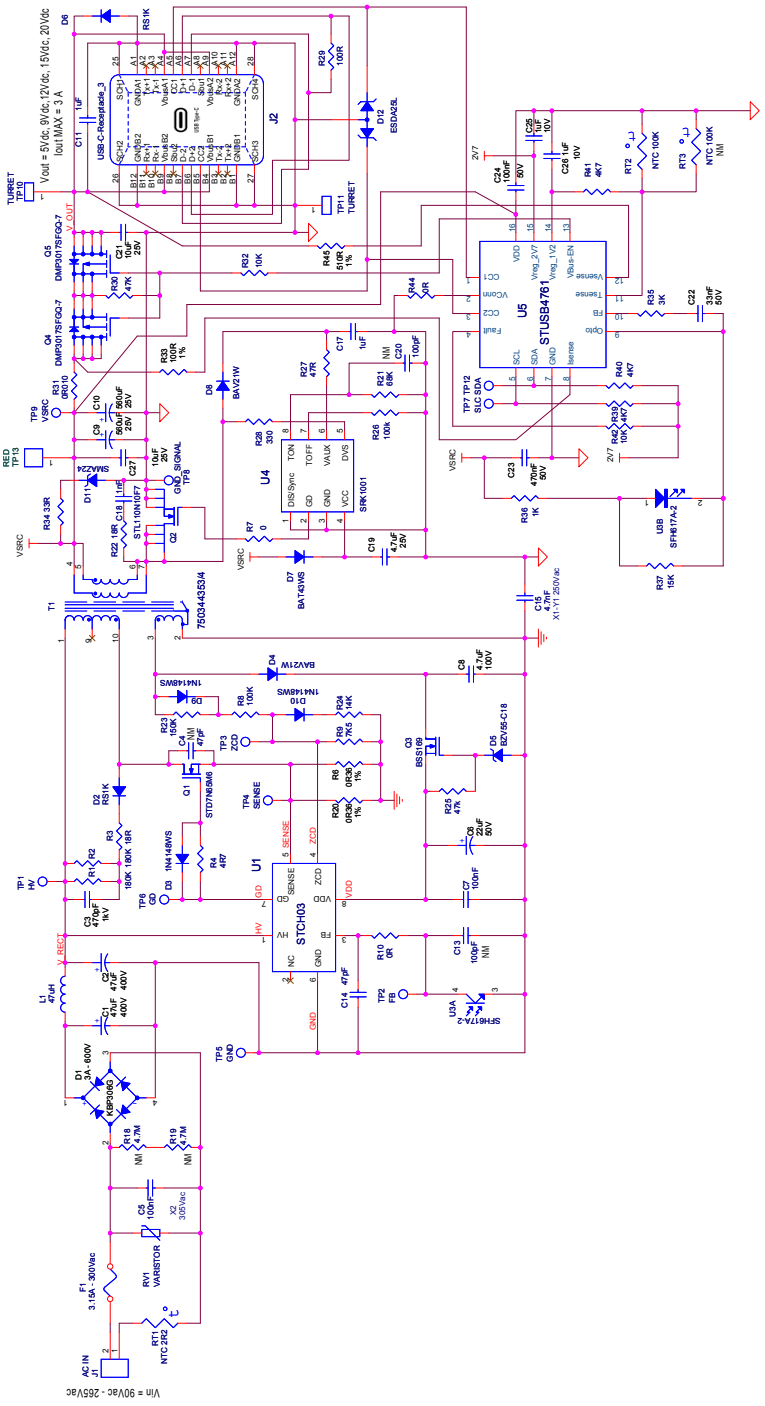
Table 1. EVLSTCH03-45WPD evaluation board specifications

Parameter	Symbol	Value
AC mains input voltage	V_{IN}	90 V_{AC} up to 265 V_{AC}
AC mains frequency	f_{IN}	47 Hz to 63 Hz
Nominal output current	$I_{OUT-NOM}$	3 A, at 5 V / 12 V / 15 V; 2.25 A, at 20 V
Maximum output current	$I_{OUT-MAX}$	$I_{OUT-NOM}$ + 12.5%
Maximum output power	$P_{OUT-MAX}$	45 W
Power Delivery Objects (PDOs)	V_{OUT}	5 V / 3 A, 9 V /3 A, 12 V / 3 A, 15 V / 3 A, 20 V / 2.25 A
Maximum efficiency	η	> 90%, at $P_{OUT-MAX}$
No-load input power	$P_{NO-LOAD}$	< 30 mW, at V_{OUT} = 5 V and no cable plug in
Power density	P/V	0.48 W/cm3
Ambient temperature	T_{AMB}	0°C up to 40 °C, free convection
Dimension	L x W x H	70 mm x 50 mm x 26.8 mm
Conducted EMI	EMI	EN55022 - Class B
Energy efficiency	-	Meeting all DOE and UE CoC requirements
Safety	-	EN60065
RoHS	-	Compliant

3 Schematic

The circuit diagram of the EVLSTCH03-45WPD evaluation board is shown in Figure 3.

Figure 3. EVLSTCH03-45WPD evaluation board schematic



4 Bill of materials

Table 2. **EVLSTCH03-45WPD evaluation board bill of materials**

Ref.	Part/Value	Description	Manufacturer
C1	47uF–400V	Aluminium Electrolytic	Niphon Chemicon
C2	47uF–400V	Aluminium Electrolytic	Niphon Chemicon
C3	470pF–1kV	Multilayer Ceramic X7R	Murata
C4	Not mounted	Capacitor	-
C5	0.1uF–305Vac	EMI Suppression MKP	TDK
C6	22uF–50V	Aluminium Electrolytic	Rubycon
C7	0.1uF–50V	Multilayer Ceramic X7R	Kemet
C8	4u7–100V	Multilayer Ceramic X7R	AVX
C9	560uF–25V	Aluminium Conductive Polymer	Kemet
C10	560uF–25V	Aluminium Conductive Polymer	Kemet
C11	1uF–50V	Multilayer Ceramic X7R	Samsung
C13	Not mounted	Capacitor	-
C14	Not mounted	Capacitor	-
C15	4.7nF–250Vrms	X1 Y1 Ceramic	Murata
C17	1uF–50V	Multilayer Ceramic X7R	Samsung
C18	1nF–2kV	Multilayer Ceramic X7R	Johansondielectrics
C19	4u7–25V	Multilayer Ceramic X7R	Kemet
C20	Not mounted	Capacitor	-
C21	10uF–25V	Multilayer Ceramic X7R	Kemet
C22	0.033uF–50V	Multilayer Ceramic X7R	Kemet
C23	0.47uF–50V	Multilayer Ceramic X7R	AVX
C24	0.1uF–50v	Multilayer Ceramic X7R	Kemet
C25	1uF–10V	Multilayer Ceramic X7R	Kemet
C26	1uF–10V	Multilayer Ceramic X7R	Kemet
C27	10uF–25V	Multilayer Ceramic X7R	Kemet
D1	3A–600V	Bridge Rectifier	Diodes
D2	RS1K / 1A–800V	Fast Switching Rectifier	Vishay
D3	1N4148WS / 150mA–100V	Small Signal Fast Switching Diode	Fairchild
D4	BAV21W / 250mA–250V	Small Signal Switching Diodes	Vishay
D5	BZV55 / C18–500mW	Zener Diode	Nexperia
D6	RS1K / 1A–800V	Fast Switching Rectifier	Vishay
D7	BAT43WS / 200mA–30V	Schottky Diode	Diodes
D8	BAV21W / 250mA–250V	Switching Diode	Diodes
D9	1N4148WS / 150mA–100V	Signal Diode	Fairchild
D10	1N4148WS / 150mA–100V	Signal Diode	Fairchild
D11	SMAZ24 / 1W	Zener Diode	Diodes
D12	ESDAL / 10mA–1.2V	Dual Transil	STMicroelectronics

Ref.	Part/Value	Description	Manufacturer
F1	3.15A–300Vac	Time-Delay Fuses	Copper Bussmann
J1	20A–300Vac	PCB Header Male/Female	WÜrth Electronics
J2	1054500101	Connector USB 3.1, type C, 90°	MOLEX
L1	47uH–1.8A	Fixed Inductor	WÜrth Electronics
Q1	STD7N65M6 / 0.91Ω–650V	Power Mosfet	STMicroelectronics
Q2	STL110N10F7 / 6mΩ–100V	Power Mosfet	STMicroelectronics
Q3	BSS169 / 12Ω–100V	Power Mosfet	Infineon
Q4	DMP3013SFV / 9.5mΩ–30V	Power Mosfet	Diodes
Q5	DMP3013SFV / 9.5mΩ–30V	Power Mosfet	Diodes
RT1	2.2R–7A	NTC	Epcos
RT2	100K–100mW	NTC	Vishay
RT3	Not mounted	NTC	-
RV1	275Vac–25A	SIOV metal oxide varistors	Epcos
R1	180k–0.5W	Anti-Surge Thick Film Chip	Panasonic
R2	180k–0.5W	Anti-Surge Thick Film Chip	Panasonic
R3	18R–0.5W	Anti-Surge Thick Film Chip	Panasonic
R4	4R7–0.125W	Thick Film Chip	Vishay
R6	0R36–0.5W	Flat Chip	TE
R7	0R–0.0625W	Thick Film Chip	Vishay
R8	100k–0.125W	Thick Film Chip	Yageo
R9	7k5–0.125W	Thick Film Chip	Vishay
R10	0R–0.0625W	Thick Film Chip	Vishay
R18	Not mounted	Resistor	-
R19	Not mounted	Resistor	-
R20	0R36–0.5W	Flat Chip	TE
R21	68k–0.0625W	Thick Film Chip	Vishay
R22	18R–0.250W	Thick Film Chip	Vishay
R23	150k–0.125W	Thick Film Chip	Vishay
R24	14k–0.125W	Thick Film Chip	Vishay
R25	47k–0.125W	Thick Film Chip	Yageo
R26	100k–0.0625W	Thick Film Chip	Yageo
R27	47R–0.0625W	Thick Film Chip	Vishay
R28	330R–0.0625W	Thick Film Chip	Yageo
R29	100R–0.0625W	Thick Film Chip	Yageo
R30	47k–0.125W	Thick Film Chip	Vishay
R31	0R010–0.750W	Power Thick Film Chip	SSM
R32	10k–0.0625W	Thick Film Chip	Vishay
R33	100R–0.250W	Thick Film Chip	Panasonic
R34	33R–0.250W	Thick Film Chip	Yageo
R35	3k–0.0625W	Thick Film Chip	Vishay

Ref.	Part/Value	Description	Manufacturer
R36	1k–0.0625W	Thick Film Chip	Yageo
R37	15k–0.0625W	Thick Film Chip	Vishay
R39	4k7–0.0625W	Thick Film Chip	Vishay
R40	4k7–0.0625W	Thick Film Chip	Vishay
R41	4.7k–0.0625W	Thick Film Chip	Vishay
R42	10k–0.0625W	Thick Film Chip	Vishay
R44	0R–0.125W	Thick Film Chip	Vishay
R45	510R–0.0625W	Thick Film Chip	Yageo
T1	750344353rev00	Transformer	WÜrth Electronics
U1	STCH03	Offline PWM controller	STMicroelectronics
U3	SFH617A-2	Optocoupler	Vishay
U4	SRK1001	Synchronous rectification controller	STMicroelectronics
U5	STUSB4761	USB PD Type-C controller	STMicroelectronics

5 PCB layout

The PCB layout top side and bottom side of the EVLSTCH03-45WPD evaluation board are shown in Figure 4 and Figure 5 respectively. The PCB uses a two-layer technology in FR4 material with copper thickness of 70 µm.

Figure 4. EVLSTCH03-45WPD PCB top layer layout

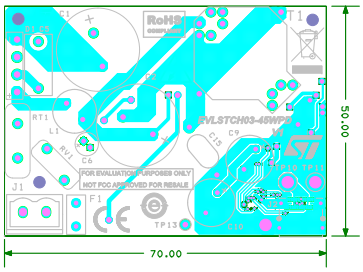
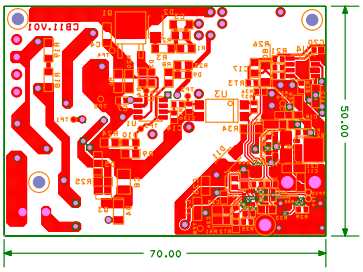


Figure 5. EVLSTCH03-45WPD PCB bottom layer layout

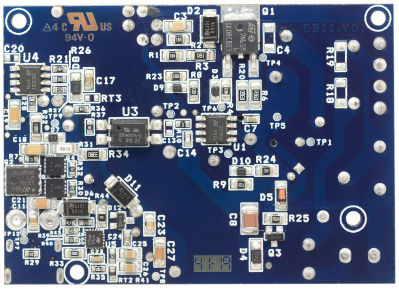


6 Board description

The EVLSTCH03-45WPD is an evaluation board based on the quasi-resonant flyback controller STCH03, the synchronous rectifier controller SRK1001, and the USB Power Delivery controller STUSB4761. Figure 6 and Figure 7 below show the top and bottom views of the demo board respectively.

Figure 6. EVLSTCH03-45WPD top view

Figure 7. EVLSTCH03-45WPD bottom view



6.1 Input stage and filtering

Fuse F1 provides protection from component failure and isolates the circuit from AC mains when a fault occurs. NTC thermistor RT1 is used to limit inrush current at start-up when the adapter is connected to AC mains. Varistor RV1 provides overvoltage protection due to voltage spikes and transient from AC mains. Capacitor C5 provides differential mode noise filtering for EMI attenuation. Bridge rectifier D1 rectifies the AC line voltage and provides a full wave rectified DC across C1 and C2. Inductor coil L1 placed between C1 and C2 allows to reduce the residual AC ripples present in the rectified DC. PI filter improves EMI performance.

6.2 Flyback controller and primary MOSFET

The STCH03 is a quasi-resonant flyback controller with HV start-up cell and a high performance low voltage PWM controller chip in the same package that minimizes power consumption.

This PWM controller turns on the primary MOSFET to allow energy to be stored inside the primary winding of the flyback transformer during the ON time. After the primary MOSFET turn-off, the energy is electromagnetically transferred to the secondary winding of the flyback transformer and hence to the secondary side capacitors and load.

CV regulation loop is achieved by secondary side feedback, the output voltage information is transfered via an optocoupler on the FB pin of the STCH03 to get the selected output voltage. The capacitor C14 on the FB pin and internal equivalent resistance of the pin R_{FB} provide a high frequency pole, while the loop compensation is done at secondary side by C22 and R35 connected to the CV regulator of the STUSB4761 controller.

CC regulation loop is fully integrated into the IC, R6 - R20 resistors set the primary side regulation current level and sense the current flowing on the primary MOSFET to implement the overcurrent protection (OCP).

To sense the transformer demagnetization, the ZCD pin is connected through a voltage divider (R23 // D9 + R8 – R9 // [R24 + D10]) to an auxiliary winding of the flyback transformer. The controller uses this pin to detect the zero-crossing signal for proper quasi-resonant operations and output voltage protection OVP and UVP.

For more detailed information on STCH03 operation and features, please refer to the datasheet (1).

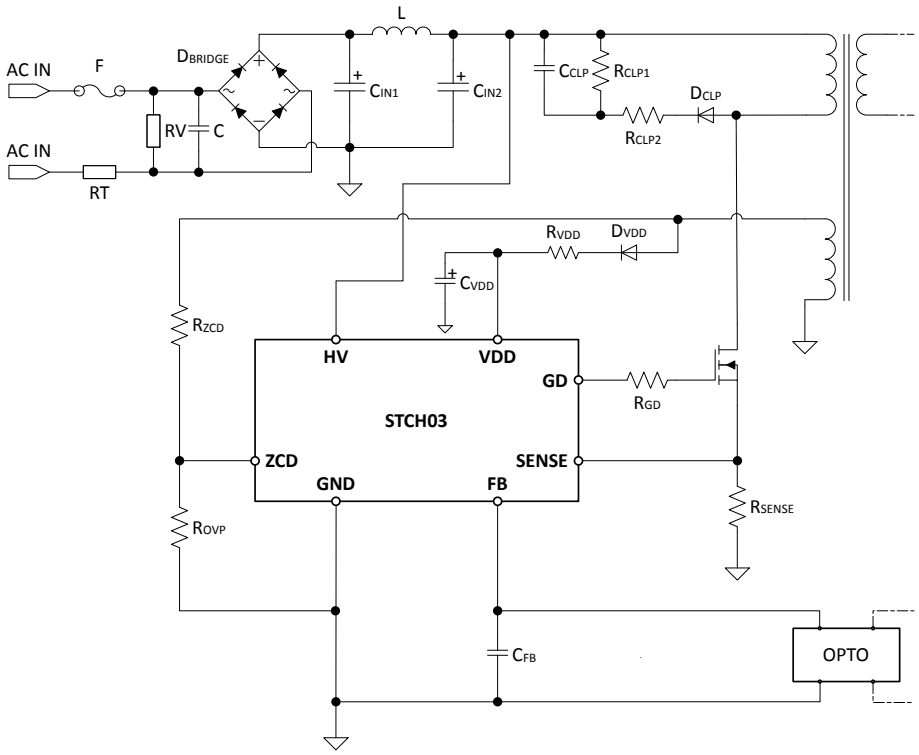
The Power MOSFET Q1 is a DPAK N-channel 650 V MDmesh M6 technology with $R_{DS(ON)}$ = 0.99 Ω. This new technology ensures a good compromise between low conduction losses and switching characteristics.

Described in the following paragraphs is a step-by-step design procedure of a quasi-resonant flyback converter for USB Type-C Power Delivery application based on STCH03 offline PWM controller for low stand-by adapters starting from the basic configuration shown in Figure 8 .

In this kind of application, the output voltage can vary from 5 V to 20 V so, it is very important to make pre-design choices in order to define the appropriate turn ratio of the power transformer.

Once the breakdown voltage of the Power MOSFET to be used has been defined, typically 650 V or 800 V, the maximum output voltage must be used to set the right turns ratio of the power transformer. At this point, using the maximum value of the current that can be delivered by the adapter and the turns ratio of the transformer, it is possible to define the other parameters as current sense resistor R_{SENSE}, zero current sense resistor R_{ZCD}, undervoltage sense resistor R_{UVP} and overvoltage sense resistor R_{OVP}.

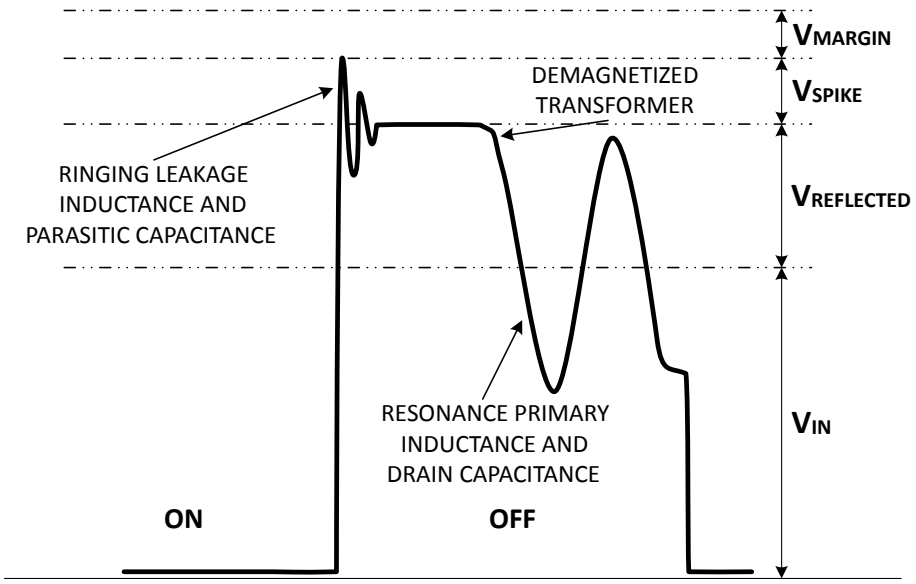
Figure 8. STCH03 configuration basic



6.2.1 Power MOSFET selection

The design of the transformer and in particular the value of the reflected voltage depends on the choice of the breakdown voltage of the Power MOSFET. In fact, the sum of the maximum input voltage, reflected voltage and overvoltage spike, due to the leakage inductance, must be lower than the breakdown of the internal Power MOSFET. It is mandatory to add some margin, typically 10% ÷ 30% more, to cover the possible overvoltage present in the main line. Figure 9 illustrates schematically how the drain voltage is composed.

Figure 9. **Voltage between drain and source of the Power MOSFET, V_{DS}**



The maximum voltage on the Power MOSFET drain is given by the following equation:

Equation 1

(1)

$$V_{DSMAX} = V_{INMAX} + V_{REFLECTED} + V_{SPIKE} + V_{MARGIN}$$

It is possible to derive the reflected voltage as

Equation 2

(2)

$$V_{REFLECTED} = V_{DSMAX} - V_{INMAX} - V_{SPIKE} - V_{MARGIN}$$

6.2.2 Turns ratio transformer selection

Once the reflected voltage is defined, it is possible to define the turns ratio of the transformer by the following equation:

Equation 3

(3)

$$n = \frac{N_{PRI}}{N_{SEC}} = \frac{V_{REFLECTED}}{V_{OUT}}$$

Where N_{PRI} is the number of the primary side windings, N_{SEC} is the number of secondary side windings, $V_{REFLECTED}$ is the reflected voltage given by Equation 3 and finally V_{OUT} is the maximum output voltage of the adapter.

6.2.3 Current sense resistor selection

The STCH03 primary side controller is equipped with the current primary side regulation and therefore it is very important to choose the right current regulation level that allows the management of the output current to the STUSB4761 secondary side controller. The output overcurrent protection is effective when measured current overcomes the maximum output current I_{OUT_MAX}. A good margin is to set the current primary side regulation level above 5% of the maximum output current I_{OUT_MAX} and this threshold depends only by the turns ratio of the transformer according to the following equation:

Equation 4

(4)

$$I_{PSR} = \frac{N_{PRI}}{N_{SEC}} \frac{K_I}{2R_{SENSE}}$$

It is possible to derive the current sense resistor as:

Equation 5

(5)

$$R_{SENSE} = \frac{N_{PRI}}{N_{SEC}} \frac{K_I}{2I_{PSR}} = \frac{N_{PRI}}{N_{SEC}} \frac{K_I}{2I_{OUT-MAX}(1 + 5/100)}$$

6.2.4 Zero current resistor selection

ZCD pin functions are transformer demagnetization sensing for quasi-resonant operation, input/output voltage monitor and feedforward compensation.

The R_{ZCD} resistor can be calculated as follows:

Equation 6

(6)

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRI}} \frac{L_{PR}R_{FF}}{T_D R_{SENSE}}$$

The value of the resistor depends on the turns ratio between auxiliary and primary windings, the value of the primary inductance and the value of the sense resistor R_{SENSE}. The other parameters are noted and available in the technical datasheet. It's recommended to split the value of R_{ZCD}, to improve the demagnetization sensing and the trigger for switching on of the Power MOSFET in Equation 7 and shown in Figure 10.

Equation 7

(7)

$$R_{ZCD} = R_{ZCD-1} + R_{ZCD-2}$$

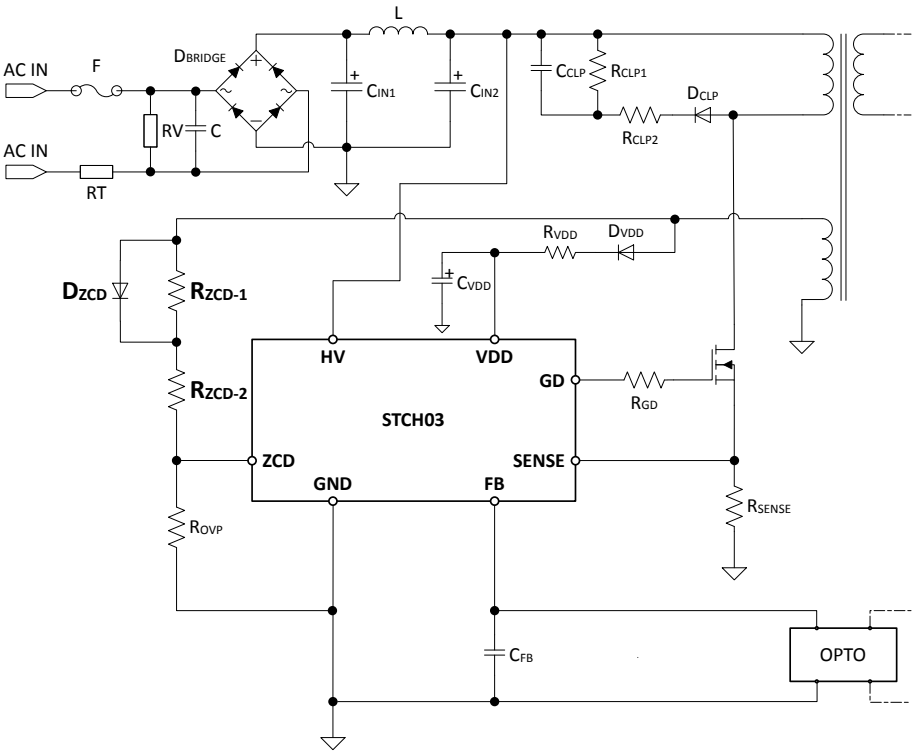
The constraint is to use a resistance value for R_{ZCD-2} lower than 120 kΩ.

Equation 8

(8)

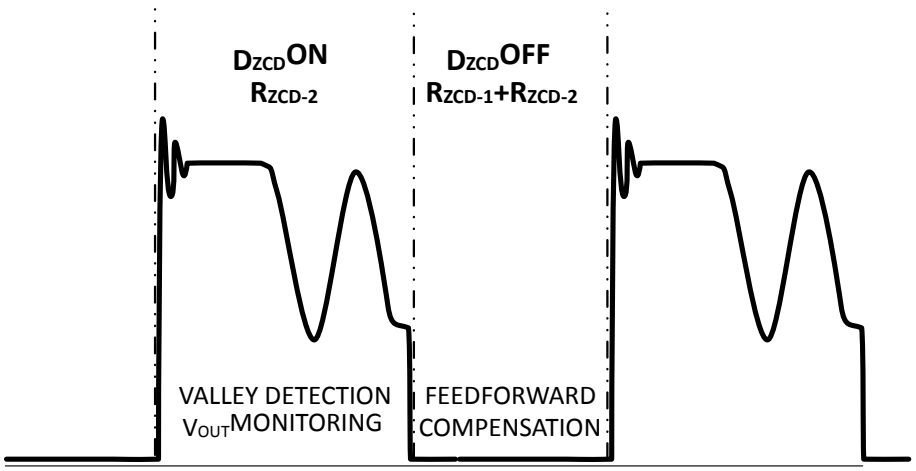
$$R_{ZCD-2} \leq 120\ \text{k}\Omega$$

Figure 10. Splitting of the R_{ZCD} resistor



In this way, the phase relative to the feedforward compensation is separated from the triggering and output voltage monitoring, Figure 11 shows the two different phases.

Figure 11. ZCD operational phases



When the primary Power MOSFET is in the ON state, the D_{ZCD} diode is open and the equivalent resistance is given by R_{ZCD-1} plus R_{ZCD-2}, line feedforward function continues to work properly and the current limitation does not depend on the input line voltage. While when the primary Power MOSFET is in an OFF state the D_{ZCD} diode is a short-circuit and the equivalent resistance is only R_{ZCD-2}. In this phase the ZCD pin senses the transformer demagnetization for quasi-resonant operation and a negative going edge triggers the Power MOSFET turn-on, furthermore the output voltage is monitored to realize the undervoltage and overvoltage protections.

6.2.5 UVP – OVP resistor selection

After the demagnetization of the transformer the voltage on the ZCD pin is sampled and held to get an accurate image of the output voltage to be used for overvoltage and undervoltage protection (OVP and UVP) sensing. OVP and UVP cannot be defined independently because they are in tracking. In order to avoid a conflict between the OVP and UVP thresholds and the output voltage range of the application, it is necessary to split the R_{OVP} resistance as shown in Figure 12.

As seen in Section 6.2.4 during this phase the diode D_{ZCD} is in conduction and the ZCD resistor is only R_{ZCD-2}. The D_{OVP} diode is open if the ZCD pin voltage is lower than the internal V_{UVP} threshold and the R_{UVP} resistor is chosen to set the level of UVP according to Equation 9.

Equation 9

(9)

$$R_{UVP} = \frac{\frac{N_{SEC}}{N_{AUX}} V_{UVP}}{V_{OUT-UVP} - \frac{N_{SEC}}{N_{AUX}} V_{UVP}} R_{ZCD-2}$$

Where $V_{OUT-UVP}$ is the UVP desired threshold value, V_{UVP} is an internal parameter of the device, N_{AUX} is the number of the auxiliary windings, N_{SEC} is the number of secondary side windings and R_{ZCD-2} is defined by Equation 8.

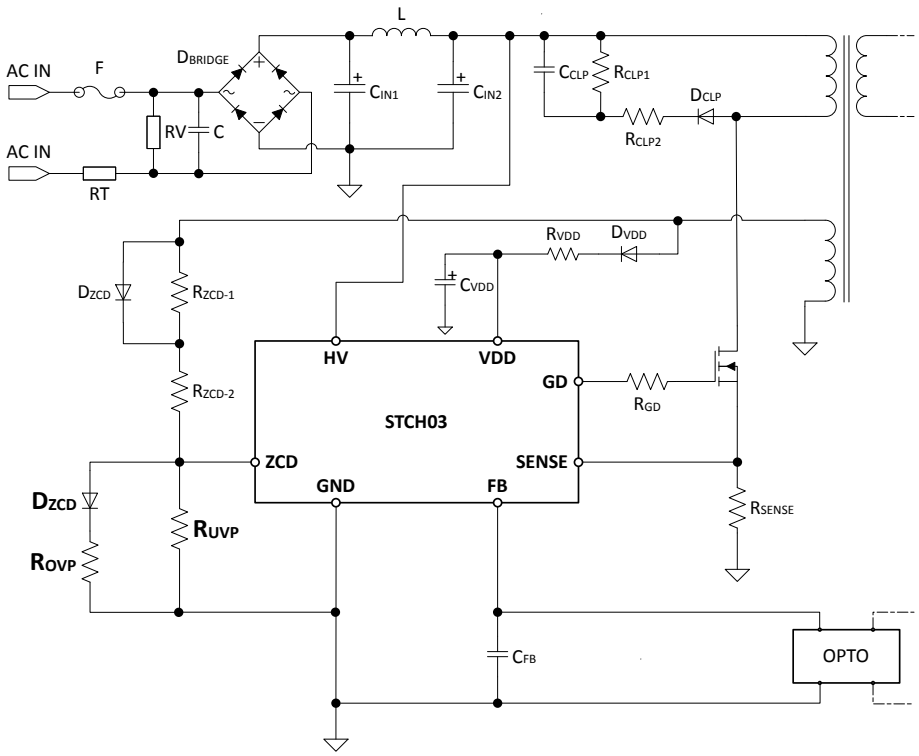
The D_{OVP} diode is a short-circuit when the ZCD pin voltage is greater than the internal V_{OVP} threshold and therefore the R_{UVP} and R_{OVP} resistors are connected in parallel. R_{OVP} resistor is chosen to set the level of OVP according to Equation 10.

Equation 10

(10)

$$R_{OVP} = \frac{\frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} V_{OUT-OVP} - V_{OVP}} R_{ZCD} - 2R_{UVP}}{R_{UVP} - \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} V_{OUT-OVP} - V_{OVP}} R_{ZCD} - 2}$$

Figure 12. Splitting of the OVP and UVP threshold



6.3 Snubber circuit

The capacitor C3, the resistor R1 // R2 and the diode D2 implement a snubber circuit to limit the leakage inductance voltage spike when the primary Power MOSFET is turned off. The clamping network ensures reliable power supply operation as it limits the maximum voltage on the primary Power MOSFET. The resistor R3 helps to reduce the residual ringing present across the primary Power MOSFET drain after the clamp action by damping the resonance oscillations between leakage inductance and equivalent drain capacitance at turn-off.

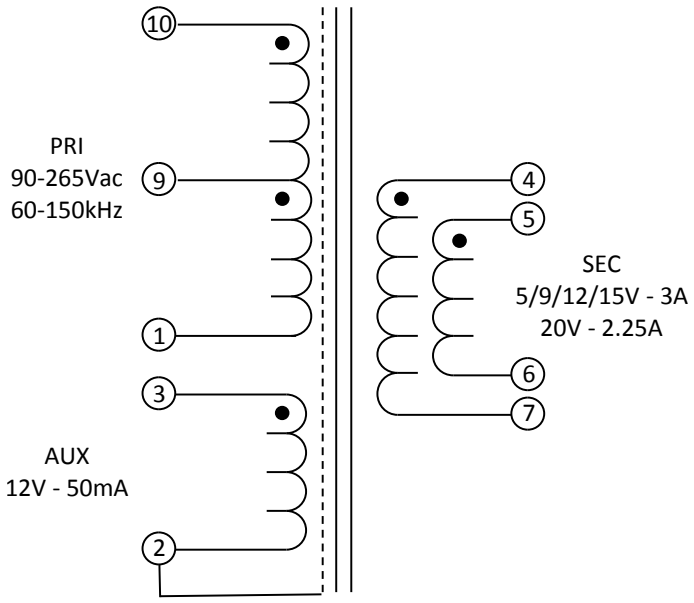
6.4 Transformer specification

The flyback transformer is designed in collaboration with Wurth Elektronik and its reference part number is 750344353rev6A. Table 3 shows the transformer main parameters and Figure 13 shows the transformer schematic. For more details refer to the supplier spec sheet (www.we-online.com).

Table 3. Transformer electrical specifications

Manufacturer	Wurth Elektronik
Part number	750344353rev6A
Core	RM8
Type of insulation	Reinforced
Coil former	Extended rail
Primary inductance	400 µH ±10%
Saturation current	2 A, 20% roll-off from initial value
Leakage inductance	10 µH max
Primary-to-secondary turns ratio	7.5 : 1 ±2%
Primary-to-auxiliary turns ratio	3.21 : 1 ±2%

Figure 13. Transformer electrical diagram



6.5 Synchronous rectifier controller and secondary Power MOSFET

The SRK1001 is a controller specially designed for synchronous rectification in flyback converters operating in QR or mixed CCM/DCM fixed frequency. In this application the SRK1001 is configured for QR operation.

This controller turns on the synchronous rectification Power MOSFET Q2 during the demagnetization period and the energy stored in the transformer primary inductance is transferred to the secondary side.

The current flows through SR Power MOSFET Q2 to the output capacitors C9 and C10, until the transformer is completely demagnetized. These capacitors ensure an ESR that is as low as possible and sufficient AC ripple capability. Capacitor C27 further reduces the output switching noise.

For a further understanding of SRK1001 operation, please refer to its datasheet (2).

The synchronous rectification Power MOSFET Q2 is a PowerFLAT N-channel 100 V Power MOSFET that utilizes STripFET F7 technology with $R_{DS(ON)}$ = 0.006 Ω. This technology features an enhanced trench-gate structure that lowers device on-state resistance, while also reducing internal capacitances and gate charge for faster and more efficient switching.

6.6 USB Power Delivery controller

STUSB4761 offers the benefits of a full hardware USB PD stack allowing robust, deterministic and safe negotiation in line with USB PD standards. It is ideal for provider application in which digital or software intelligence is limited or missing.

STUSB4761 main functions are to:

1. Detect the connection between two ports (attach detection),
2. Establish a valid Source-to-Sink connection,
3. Determine the attached device mode: Sink or Accessory,
4. Check cable power capabilities,
5. Negotiate a USB PD contract with a PD capable device,
6. Configure the output power path accordingly,
7. Regulate Voltage and Current according to PD contract,
8. Monitor VBUS, manage transitions, handle protections and ensure user and device safety

Additionally, the STUSB4761 offers customizable Power Data Objects (PDO) and UVLO / OVLO protections, an integrated discharge path, a VBUS current mirror and is natively robust to High Voltage surge, including on the CC pins.

In the EVLSTCH03-45WPD evaluation board, the STUSB4761 is used with its default factory setting except for Voltage UVLO for SRC_PDO1 set to -10%, summarized in the table below:

Table 4. STUSB4761 configuration

PDO #	PD Power (default)(1)	PD Power (OTP)(1)	Voltage UVLO (2)	Voltage OVLO (2)
SRC_PDO1	5 V - 3 A	2 A	-10%	+10%
SRC_PDO2	9 V - 3 A	2 A	-5%	+10%
SRC_PDO3	12 V - 3 A	2 A	-5%	+10%
SRC_PDO4	15 V - 3 A	2 A	-5%	+10%
SRC_PDO5	20 V - 2.25 A	2 A	-5%	+10%

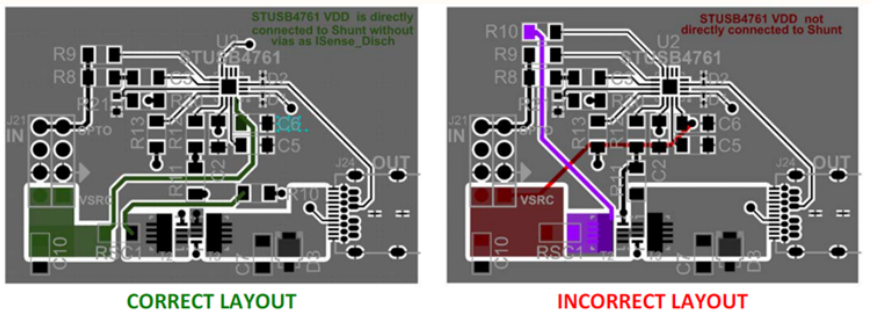
1. *PD Power (PDP): The output power of a Source, as specified by the manufacturer and expressed in Fixed Supply PDOs.*
2. *UVLO / OVLO accuracy: +/- 2% across temperature range*

The on-board temperature is monitored: in case of over-temperature conditions, (by default 70°C) the STUSB4761 advertises lower power profiles.

VBUS current used for regulation is measured thanks to a 10 mΩ (default) shunt resistor between VDD and ISENSE_DISCH pins. In case the measured VBUS current reaches the regulation threshold (+12.5% above the SRC current from the PDO selected by the sink), the STUSB4761 enters in CC mode: voltage is decreased down to the undervoltage (UVLO) condition defined for the selected contract.

To guarantee the regulation accuracy, one must follow the shunt layout recommendations as shown in Figure 14 below. A more detailed description of how to route the STUSB4761 PCB can be found in the AN5430 Application Note (3).

Figure 14. **STUSB4761 layout recommendations**



STUSB4761 NVM configuration can be customized statically to align PD controller behavior according to final application requirements. Customization applies to various parameters such as number of PDO, voltage, current, discharge time, protection thresholds, etc…

Parameter customization is possible:

- Either by direct access through I²C interface,
- Or by using specific commands packaged as ST proprietary unstructured VDM when STUSB4761 is connected in debug accessory mode (OrientedDebug Accessory.SRC state)

A more detailed description of temperature adaptive power, factory settings and customization can be found in the STUSB4761 datasheet or product page (4).

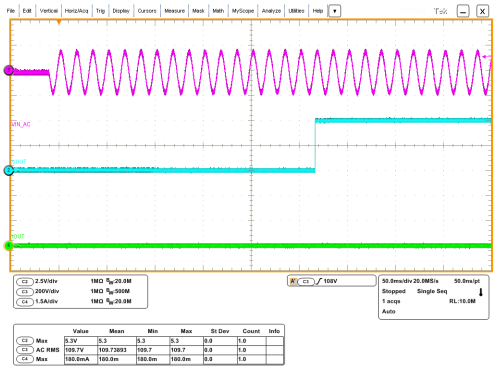
7 Typical waveforms

In this section the converter operating waveforms are shown, in particular the waveforms of the primary and secondary are reported in various line and load conditions.

7.1 Start-up waveforms

The following figures show the startup of the converter at 115 V_{AC} and 230 V_{AC} under no load and full load conditions. The output voltage begins to increase after a short delay from the presence of the input voltage (< 300 ms). No abnormal oscillation in the output is present.

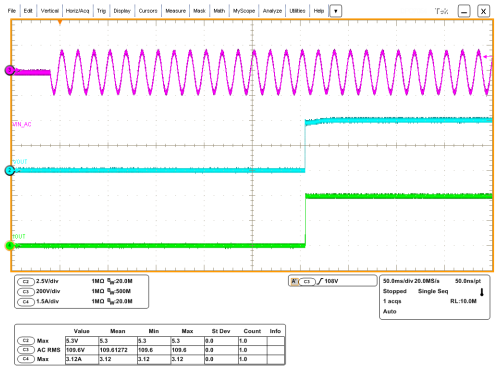
Figure 15. Start-up waveforms at 115 V_{AC} - No load



Violet = V_{IN} 200 V/div, Blue = V_{OUT} 2.5 V/div,

Green = I_{OUT} 1.5 A/div

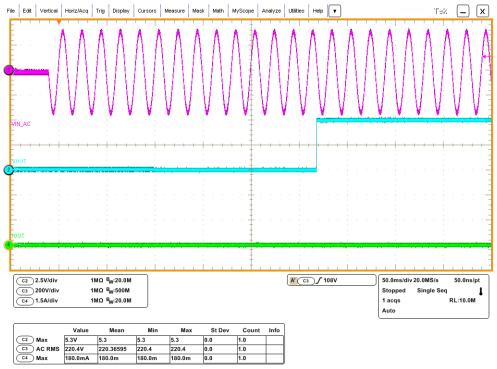
Figure 16. Start-up waveforms at 115 V_{AC} - Full load



Violet= V_{IN} 200 V/div, Blue = V_{OUT} 2.5 V/div,

Green = I_{OUT} 1.5 A/div

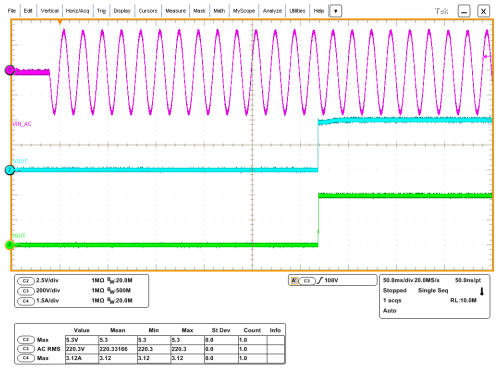
Figure 17. Start-up waveforms at 230 V_{AC} - No load



Violet = V_{IN} 200 V/div, Blue = V_{OUT} 2.5 V/div,

Green = I_{OUT} 1.5 A/div

Figure 18. Start-up waveforms at 230 V_{AC} Full load



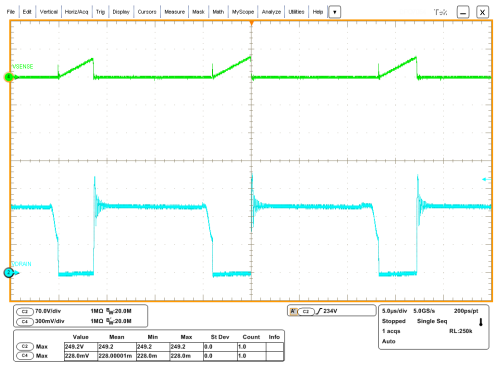
Violet = V_{IN} 200 V/div, Blue = V_{OUT} 2.5 V/div,

Green = I_{OUT} 1.5 A/div

7.2 Primary drain voltage and current sense voltage

The following figures shows the drain voltage and the current sense pin voltage waveforms of the flyback converter at 90 V_{AC} and 265 V_{AC} under full load condition.

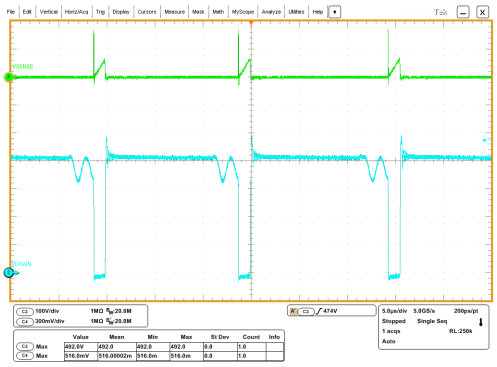
Figure 19. Flyback primary side waveforms at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 70 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 249.2 V

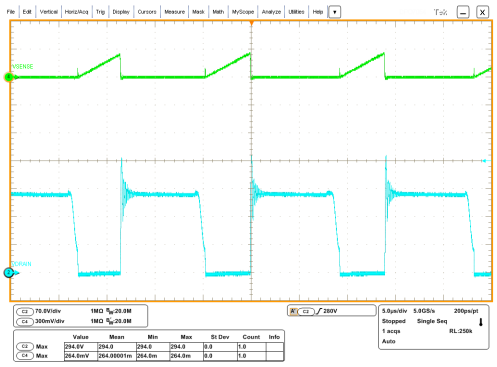
Figure 20. Flyback primary side waveforms at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 492 V

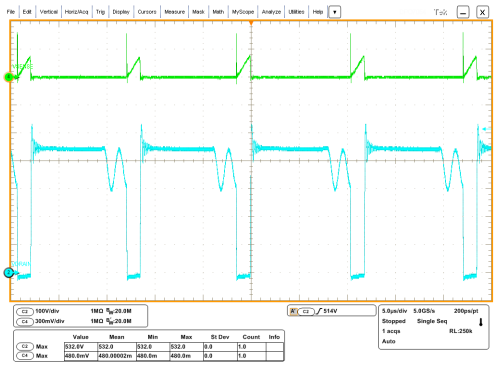
Figure 21. Flyback primary side waveforms at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 70 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 294 V

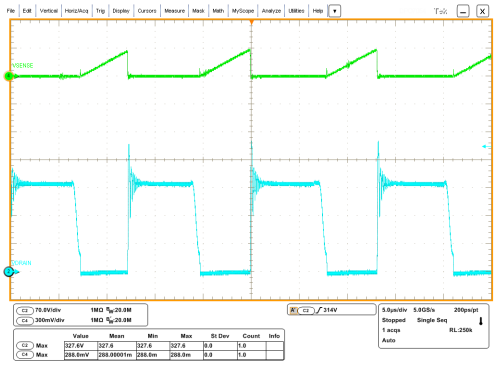
Figure 22. Flyback primary side waveforms at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 532 V

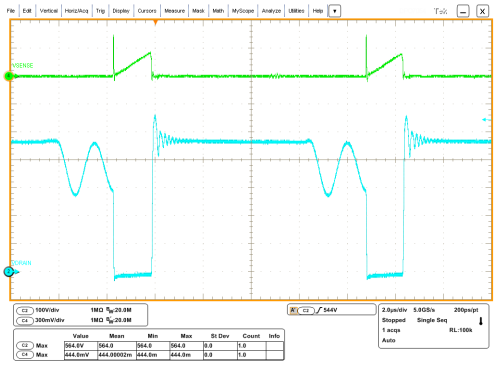
Figure 23. Flyback primary side waveforms at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 70 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 327.6 V

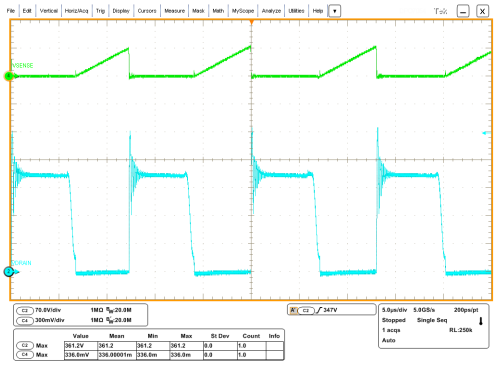
Figure 24. Flyback primary side waveforms at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 564 V

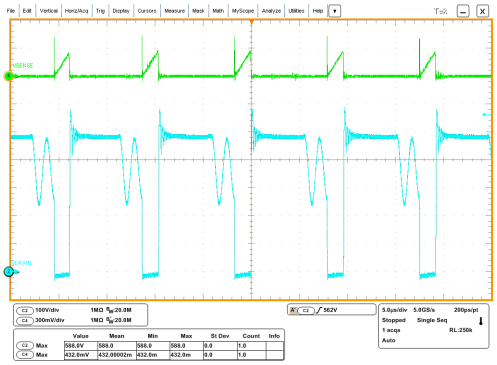
Figure 25. Flyback primary side waveforms at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 70 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 361.2 V

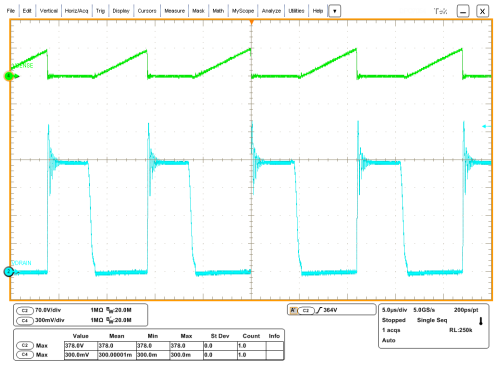
Figure 26. Flyback primary side waveforms at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 588 V

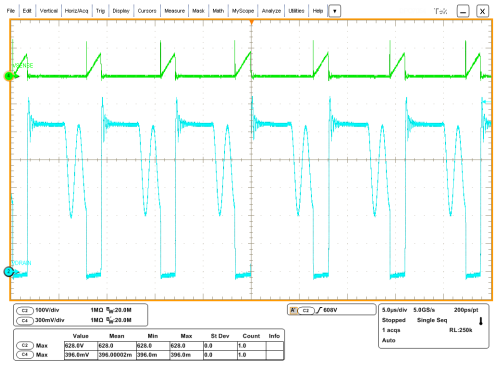
Figure 27. Flyback primary side waveforms at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 70 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 378 V

Figure 28. Flyback primary side waveforms at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 265 V_{AC})



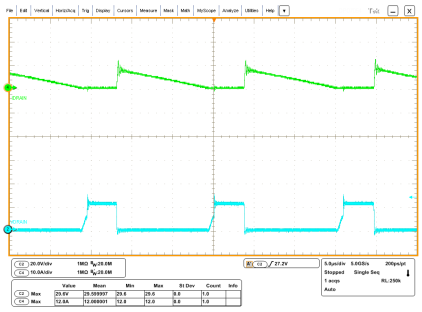
Blue = V_{DS} 100 V/div, Green = V_{SENSE} 300 mV/div ;

V_{DS-MAX} = 628 V

7.3 Secondary drain voltage and current

The following figures show the drain voltage and the drain current waveforms of operation of the flyback converter at 90 V_{AC} and 265 V_{AC} under full load condition.

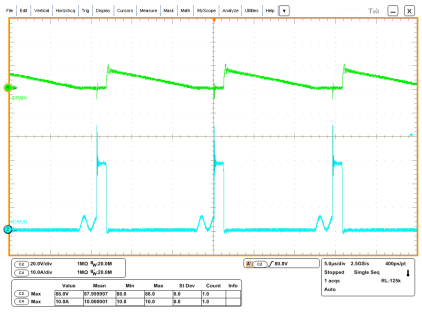
Figure 29. Flyback secondary side waveforms at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 20 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 29.6 V

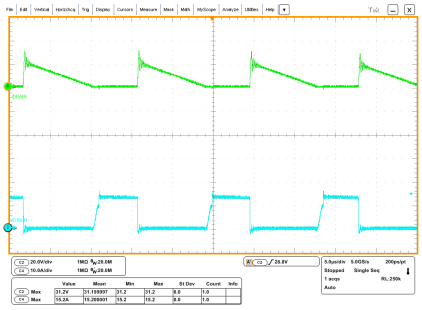
Figure 30. Flyback secondary side waveforms at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 88 V

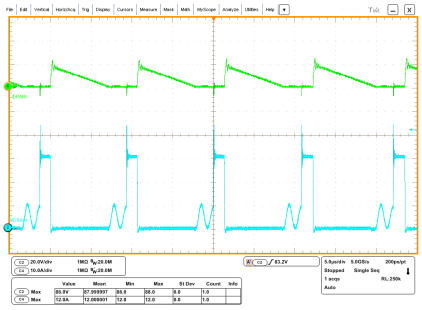
Figure 31. Flyback secondary side waveforms at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 20 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 31.2 V

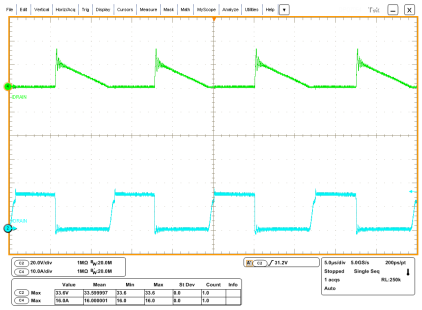
Figure 32. Flyback secondary side waveforms at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 88 V

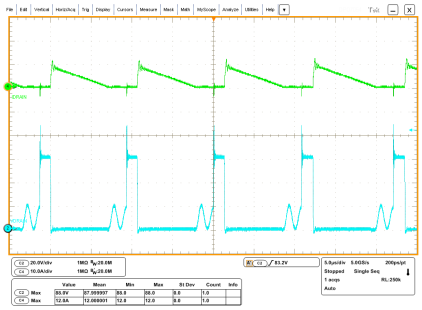
Figure 33. Flyback secondary side waveforms at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 20 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 33.6 V

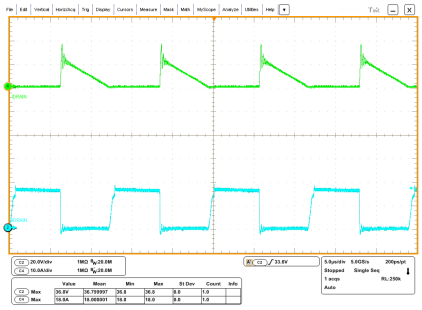
Figure 34. Flyback secondary side waveforms at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 87.2 V

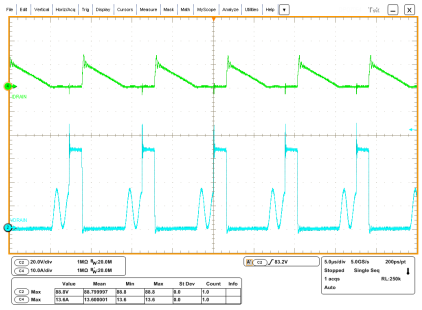
Figure 35. Flyback secondary side waveforms at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 20 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 36.8 V

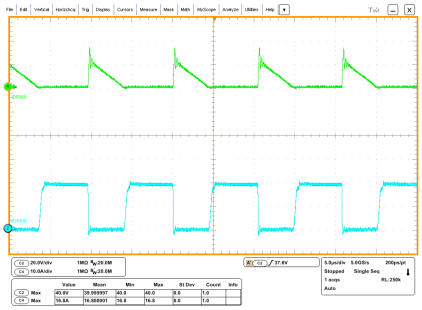
Figure 36. Flyback secondary side waveforms at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 265 V_{AC})



Blue = V_{DS} 100 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 88.8 V

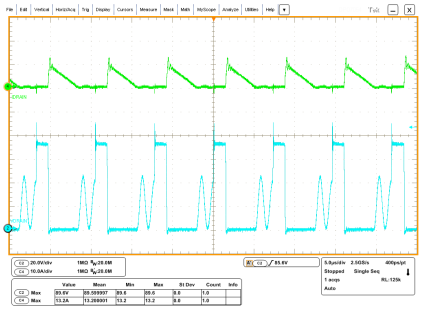
Figure 37. Flyback secondary side waveforms at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 90 V_{AC})



Blue = V_{DS} 20 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 40 V

Figure 38. Flyback secondary side waveforms at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 265 V_{AC})



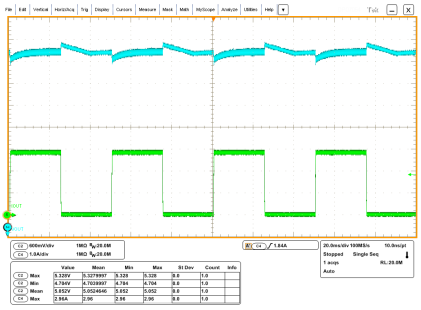
Blue = V_{DS} 100 V/div, Green = I_{DS} 10 A/div ;

V_{DS-MAX} = 89.6 V

7.4 Load transient response

The following figures show the load transient response waveforms of the flyback converter subjected to repetitive dynamic load transitions zero to full load at 115 V_{AC} and 230 V_{AC}.They show no abnormal oscillation in the output and the overshoot and undershoot values are acceptable.

Figure 39. Dynamic load transient zero to full load at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



Blue = V_{OUT}1 V/div, Green = I_{OUT} 1 A/div

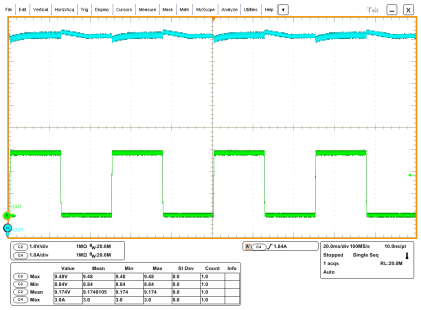
$V_{OUT-MAX}$ = 5.32 V ; $V_{OUT-MIN}$ = 4.7 V

Figure 40. Dynamic load transient zero to full load at V_{OUT} = 5 V - I_{OUT} = 3 A(V_{IN} = 230 V_{AC})

Blue = V_{OUT} 1 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 5.32 V ; $V_{OUT-MIN}$ = 4.7 V

Figure 41. Dynamic load transient zero to full load at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



Blue = V_{OUT} 1 V/div, Green = I_{OUT} 1 A/div

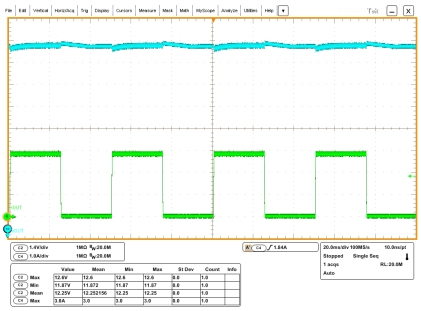
$V_{OUT-MAX}$ = 9.48 V ; $V_{OUT-MIN}$ = 8.84 V

Figure 42. Dynamic load transient zero to full load at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})

Blue = V_{OUT} 1 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 9.44 V ; $V_{OUT-MIN}$ = 8.84 V

Figure 43. Dynamic load transient zero to full load at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



Blue = V_{OUT} 1.4 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 12.6 V ; $V_{OUT-MIN}$ = 11.87 V

Figure 44. Dynamic load transient zero to full load at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})

Blue = V_{OUT} 1.4 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 12.54 V ; $V_{OUT-MIN}$ = 11.87 V

Figure 45. Dynamic load transient zero to full load at V_{OUT} = 15 V- I_{OUT} = 3 A (V_{IN} = 115 V_{AC})

Blue = V_{OUT} 1.7 V/div, Green = I_{OUT} 1 A/div

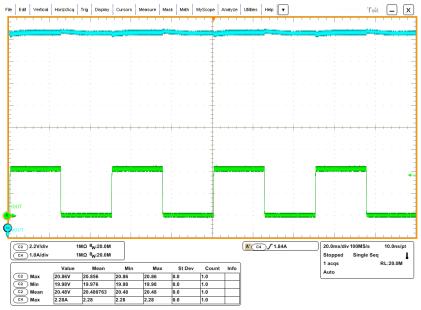
$V_{OUT-MAX}$ = 15.71 V ; $V_{OUT-MIN}$ = 14.89 V

Figure 46. Dynamic load transient zero to full load at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})

Blue = V_{OUT} 1.7 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 15.71 V ; $V_{OUT-MIN}$ = 14.89 V

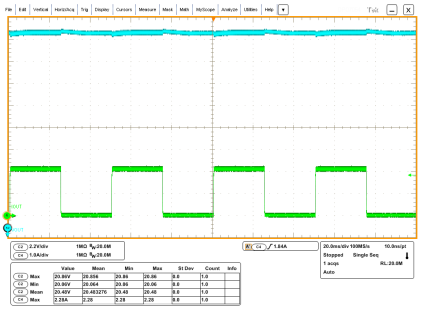
Figure 47. Dynamic load transient zero to full load at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 115 V_{AC})



Blue = V_{OUT} 2.2 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 20.86 V ; $V_{OUT-MIN}$ = 19.89 V

Figure 48. Dynamic load transient zero to full load at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 230 V_{AC})



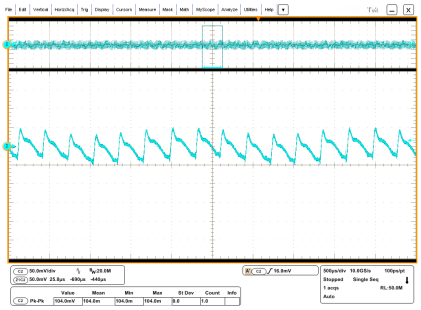
Blue = V_{OUT} 2.2 V/div, Green = I_{OUT} 1 A/div

$V_{OUT-MAX}$ = 20.86 V ; $V_{OUT-MIN}$ = 20.86 V

7.5 Output voltage ripple

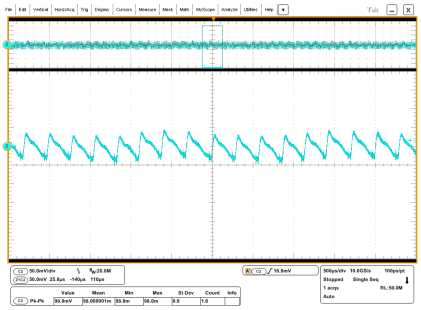
The following figures show the output voltage ripple waveforms of the flyback converter at 115 V_{AC} and 230 V_{AC} under full load condition.

Figure 49. Output voltage ripple at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



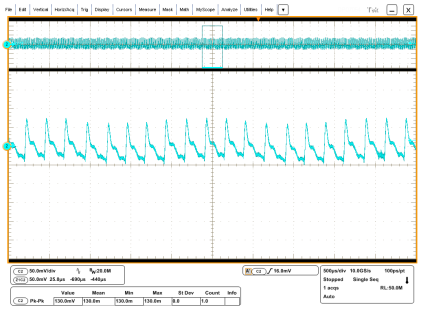
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 104 mV

Figure 50. Output voltage ripple at V_{OUT} = 5 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})



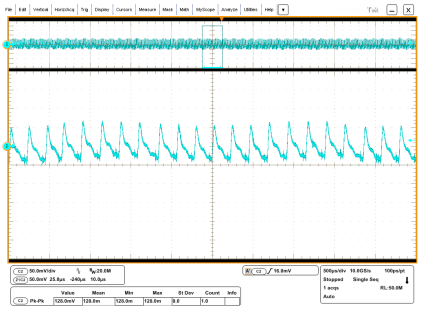
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 98 mV

Figure 51. Output voltage ripple at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



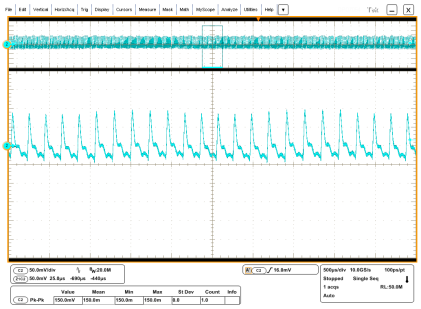
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 130 mV

Figure 52. Output voltage ripple at V_{OUT} = 9 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})



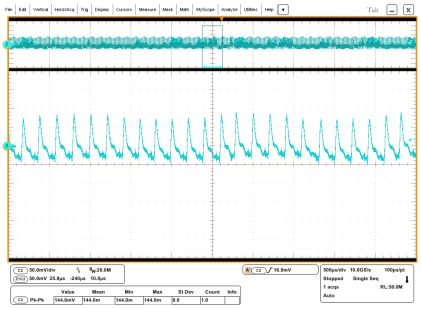
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 128 mV

Figure 53. Output voltage ripple at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



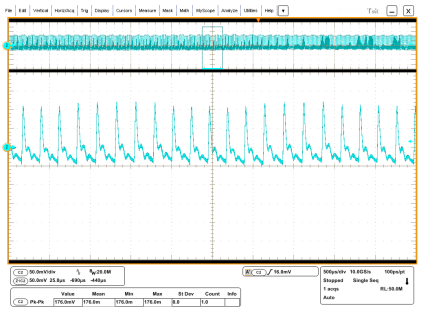
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 150 mV

Figure 54. Output voltage ripple at V_{OUT} = 12 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})



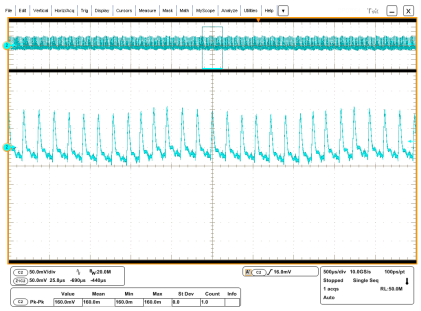
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 144 mV

Figure 55. Output voltage ripple at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 115 V_{AC})



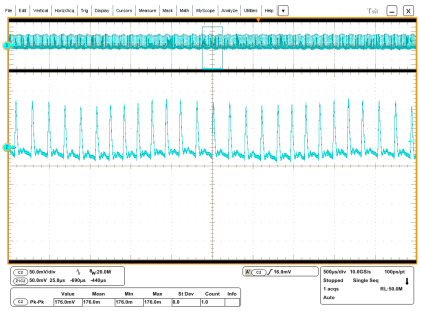
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 176 mV

Figure 56. Output voltage ripple at V_{OUT} = 15 V - I_{OUT} = 3 A (V_{IN} = 230 V_{AC})



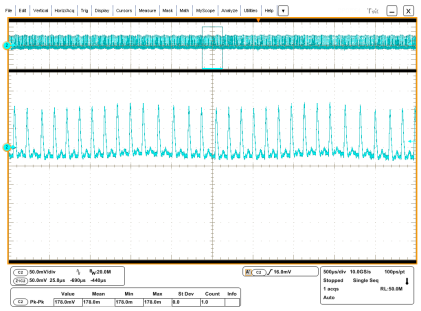
Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 160 mV

Figure 57. Output voltage ripple at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 115 V_{AC})



Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 176 mV

Figure 58. Output voltage ripple at V_{OUT} = 20 V - I_{OUT} = 2.25 A (V_{IN} = 230 V_{AC})



Blue = V_{OUT} 50 mV/div AC ; $V_{OUT-PKPK}$ = 178 mV

8 Efficiency and no-load consumption measurements

The energy efficiency of the adapter meets all DOE and UE CoC requirements, since the 4 points average efficiency and efficiency at 10% of rated load are always higher than the most stringent EU CoC rev. 5 - Tier 2 (2016).

The adapter efficiency and no-load consumption are measured at nominal input voltages and in the various operating profiles.

8.1 Efficiency performance at 115 V_{AC}

Table 5. Efficiency measurements summary at V_{IN} = 115 V_{AC} / 60 Hz

Efficiency @ V_{IN} = 115 V_{AC} / 60 Hz					
% of rated power	Output profile				
	5V	9V	12V	15V	20V
25%	87.92	90.18	90.32	90.22	89.48
50%	88.38	90.80	90.97	90.99	90.72
75%	87.97	90.65	90.92	91.03	90.91
100%	87.39	90.35	90.70	90.81	90.61
Avg eff. %	**87.92**	**90.50**	**90.73**	**90.76**	**90.43**
EU CoC rev. 5 - Tier 2 limit	**81.84**	**87.30**	**88.30**	**88.85**	**88.85**
10%	**85.36**	**86.97**	**86.99**	**87.33**	**85.53**
EU CoC rev. 5 - Tier 2 limit	**72.48**	**77.30**	**78.30**	**78.85**	**78.85**

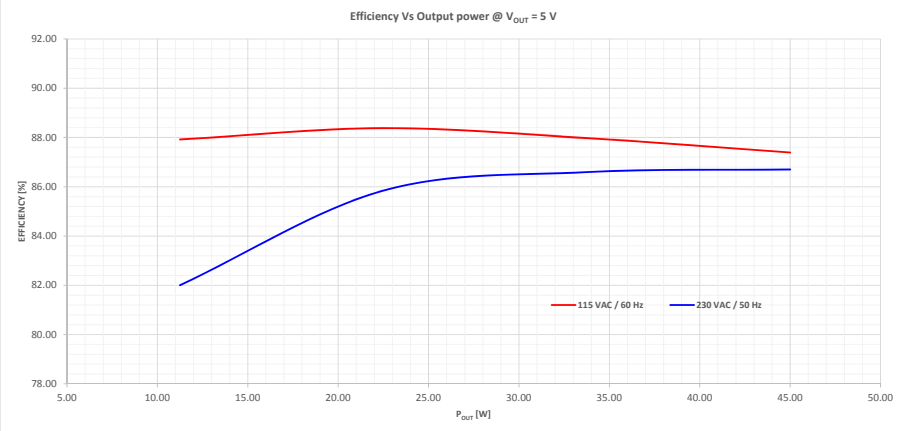
8.2 Efficiency performance at 230 V_{AC}

Table 6. Efficiency measurements summary at V_{IN} = 230 V_{AC} / 50 Hz

Efficiency @ V_{IN} = 230 V_{AC} / 60 Hz					
% of rated power	Output profile				
	5V	9V	12V	15V	20V
25%	82.00	87.07	88.06	88.66	87.88
50%	85.84	89.48	90.23	90.14	90.27
75%	86.59	90.15	90.89	91.31	91.14
100%	86.70	90.39	91.16	91.62	91.58
Avg eff. %	**85.29**	**89.27**	**90.09**	**90.43**	**90.22**
EU CoC rev. 5 - Tier 2 limit	**81.84**	**87.30**	**88.30**	**88.85**	**88.85**
10%	**74.90**	**78.71**	**80.65**	**82.01**	**80.74**
EU CoC rev. 5 - Tier 2 limit	**72.48**	**77.30**	**78.30**	**78.85**	**78.85**

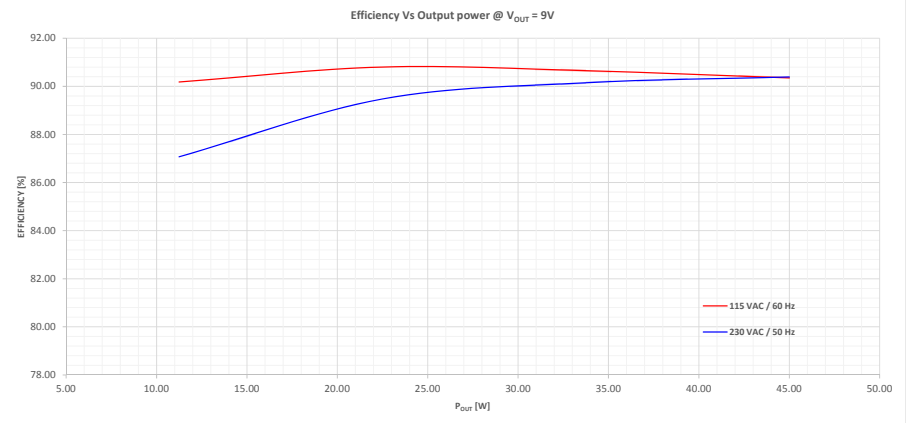
8.3 Output profile 5 V / 3 A

Figure 59. Efficiency vs. output power at V_{OUT} = 5 V



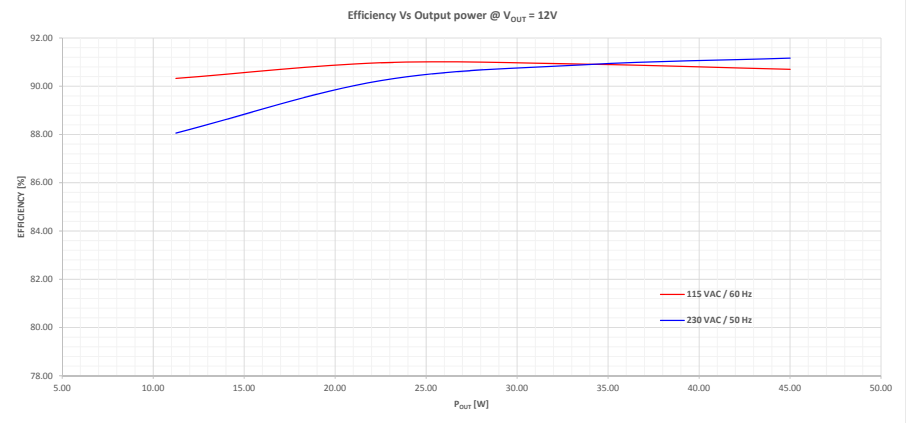
8.4 Output profile 9 V / 3 A

Figure 60. Efficiency vs. output power at V_{OUT} = 9 V



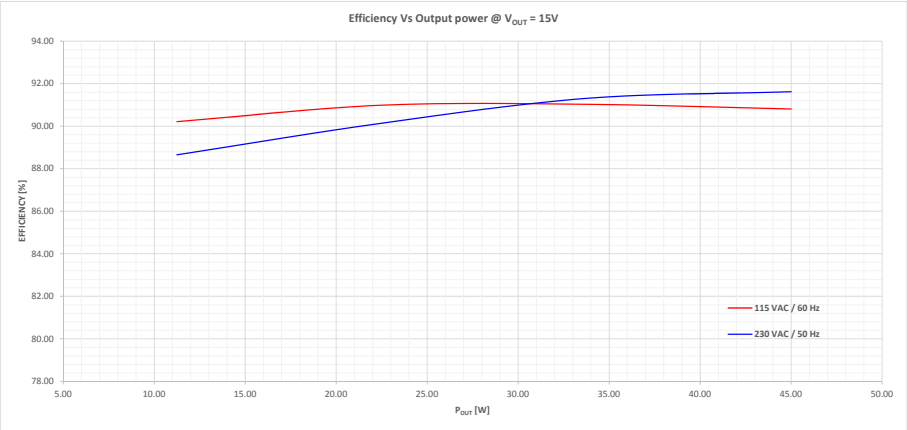
8.5 Output profile 12 V / 3 A

Figure 61. Efficiency vs. output power at V_{OUT} = 12 V



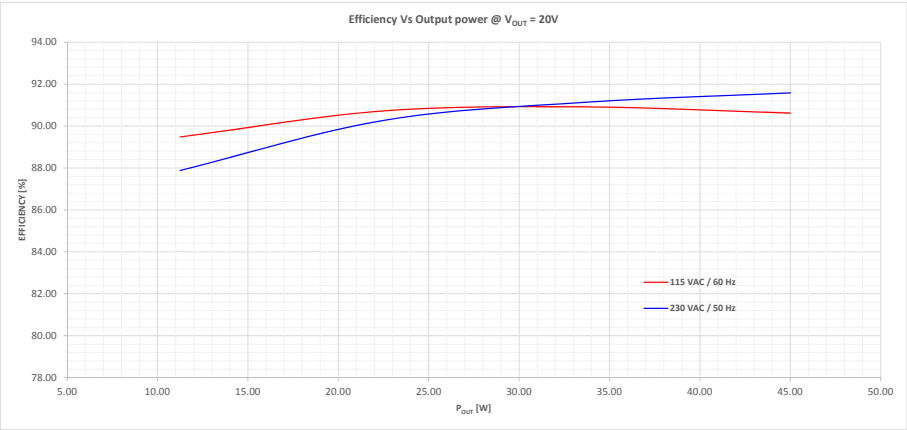
8.6 Output profile 15 V / 3 A

Figure 62. Efficiency vs. output power at V_{OUT} = 15 V



8.7 Output profile 20 V / 2.25 A

Figure 63. Efficiency vs. output power at V_{OUT} = 20 V



8.8 No-load consumption performance

The no-load consumption is measured at nominal input voltage with the USB Type-C interface board for output voltage selection disconnected from the adapter. In this way, the output voltage profile is set by default to 5 V / 3 A.

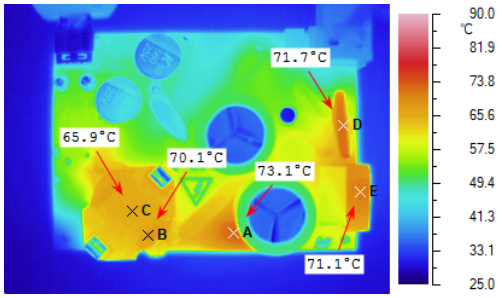
Table 7. No-Load consumption measurements

Input voltage VIN	No-load consumption [mW]
115 V_{AC} / 60 Hz	14.71
230 V_{AC} / 50 Hz	18.42

9 Thermal measurements

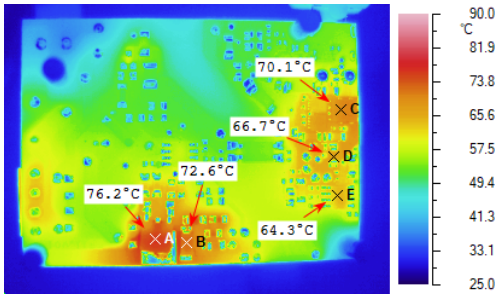
A thermal analysis of the board was performed with an infrared thermal imaging camera. The test was conducted with the output voltage profile selected to 15 V and full load. The board was submitted at minimum voltage and maximum voltage and after 30 minutes while the input voltage minimum and maximum input voltage 90 V_{AC} and 265 V_{AC} respectively.

Figure 64. Thermal image at 90 V_{AC} (top side)



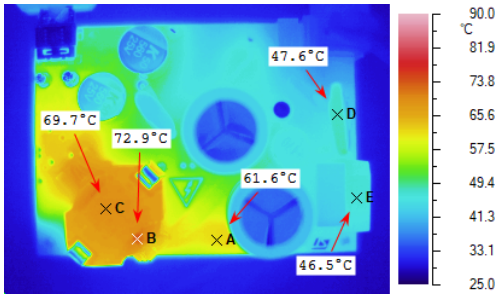
V_{OUT} = 15 V ; I_{OUT} = 3 A

Figure 65. Thermal image at 90 V_{AC} (bottom side)



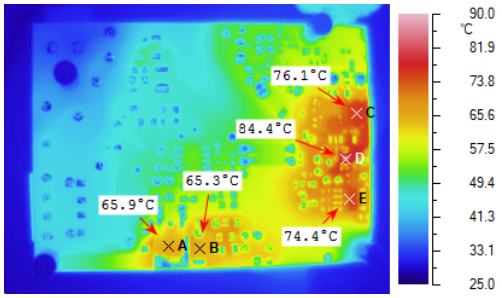
V_{OUT} = 15 V ; I_{OUT} = 3 A

Figure 66. Thermal image at 265 V_{AC} (top side)



V_{OUT} = 15 V ; I_{OUT} = 3 A

Figure 67. Thermal image at 265 V_{AC} (bottom side)



V_{OUT} = 15 V ; I_{OUT} = 3 A

10 Conducted EMI

A pre-compliance test for EN55022 – Class B European regulation for domestic equipment is performed, measuring the line conducted noise emissions at nominal mains voltages and full load.

The various measurements shown below have been performed using the average EMI detector configuration of the EMC analyzer receiver.

The Class B limits for domestic equipment are more severe compared to the Class A requirements, dedicated to information technology equipment. The lower limit in the graphs refers to the Class B average measurement set-up.

The results show a comfortable margin between the measurements and the required limits.

10.1 Output profile: 5 V / 3 A

Figure 68. EMI measurements for 5 V output profile, Line scan (115 V_{AC})

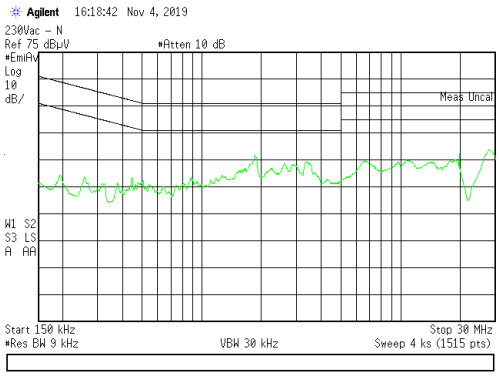


Figure 69. EMI measurements for 5 V output profile, Line scan (230 V_{AC})

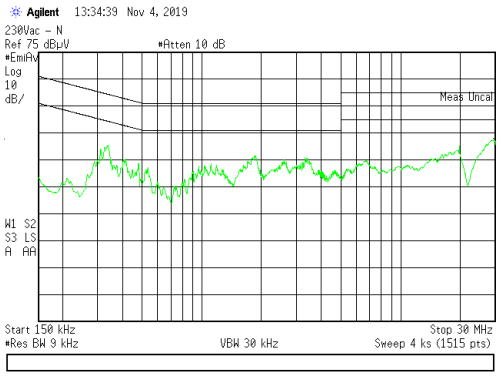


Figure 70. EMI measurements for 5 V output profile, Neutral scan (115 V_{AC})

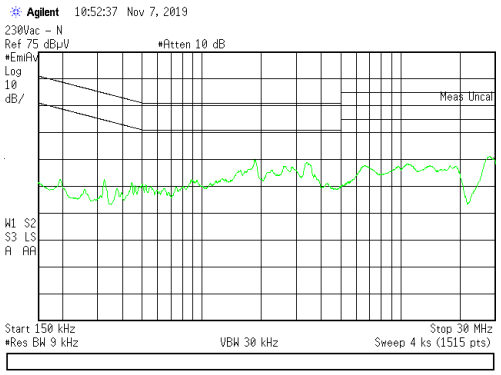
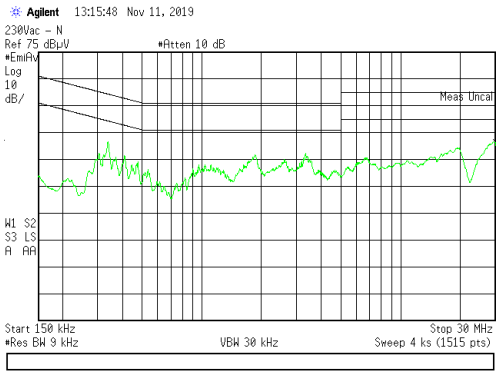


Figure 71. EMI measurements for 5 V output profile, Neutral scan (230 V_{AC})



10.2 Output profile: 9 V / 3 A

Figure 72. EMI measurements for 9 V output profile, Line scan (115 V_{AC})

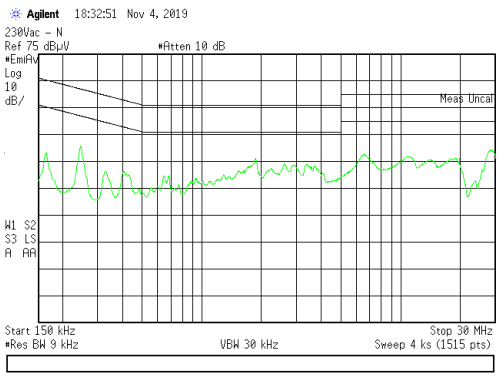


Figure 73. EMI measurements for 9 V output profile, Line scan (230 V_{AC})

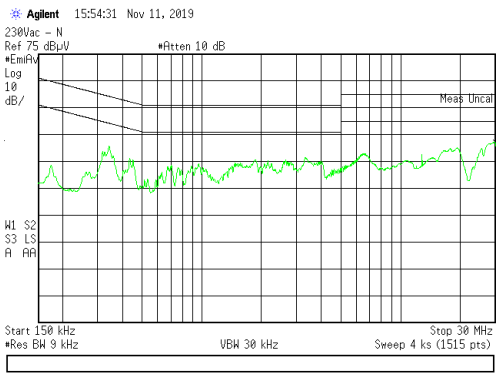


Figure 74. EMI measurements for 9 V output profile, Neutral scan (115 V_{AC})

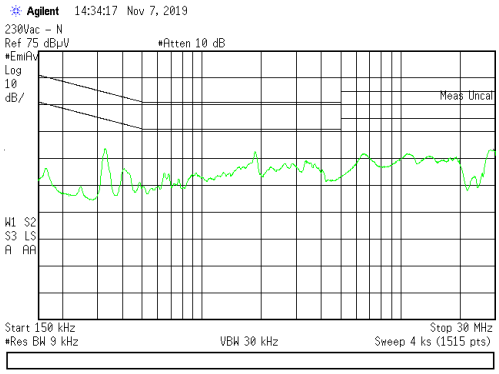
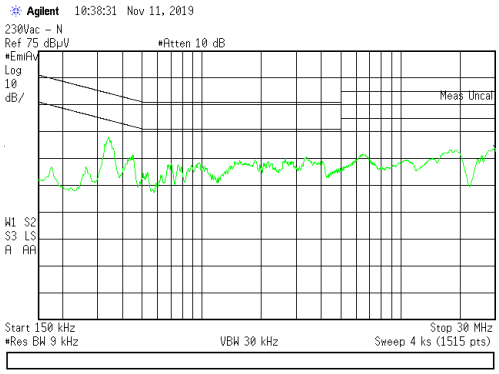


Figure 75. EMI measurements for 9 V output profile, Neutral scan (230 V_{AC})



10.3 Output profile: 12 V / 3 A

Figure 76. EMI measurements for 12 V output profile, Line scan (115 V_{AC})

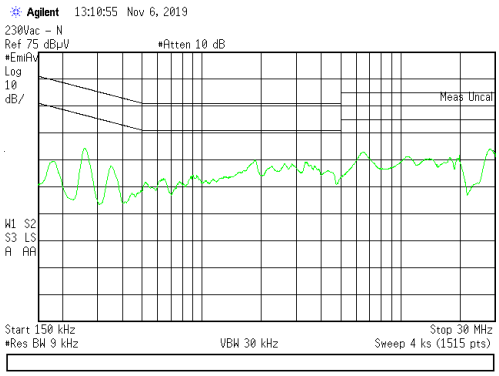


Figure 77. EMI measurements for 12 V output profile, Line scan (230 V_{AC})

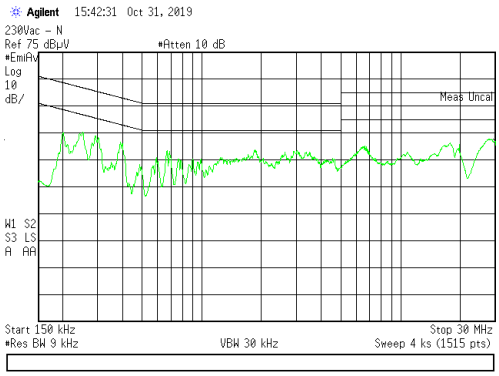


Figure 78. EMI measurements for 12 V output profile, Neutral scan (115 V_{AC})

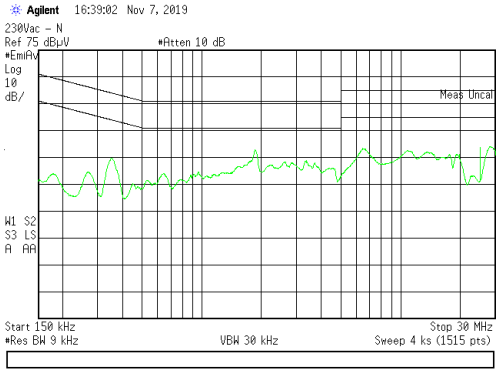
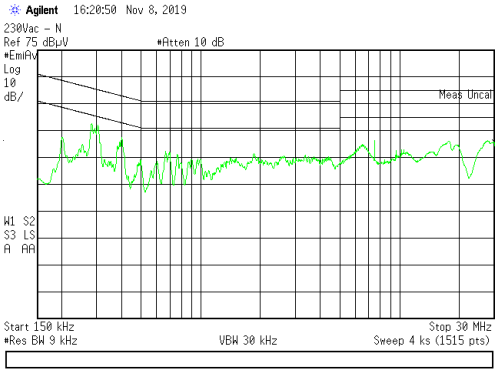


Figure 79. EMI measurements for 12 V output profile, Neutral scan (230 V_{AC})



10.4 Output profile: 15 V / 3 A

Figure 80. EMI measurements for 15 V output profile, Line scan (115 V_{AC})

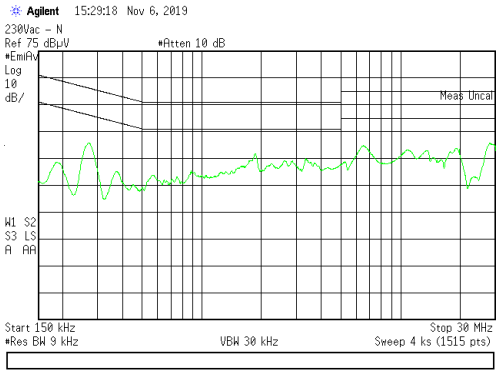


Figure 81. EMI measurements for 15 V output profile, Line scan (230 V_{AC})

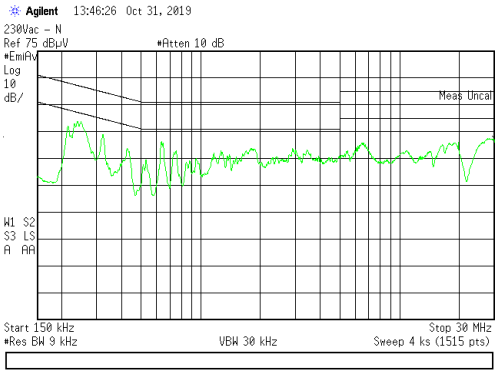


Figure 82. EMI measurements for 15 V output profile, Neutral scan (115 V_{AC})

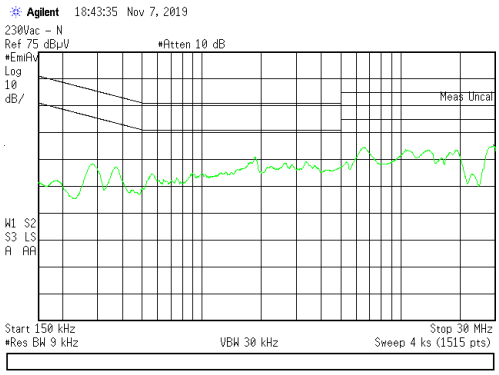
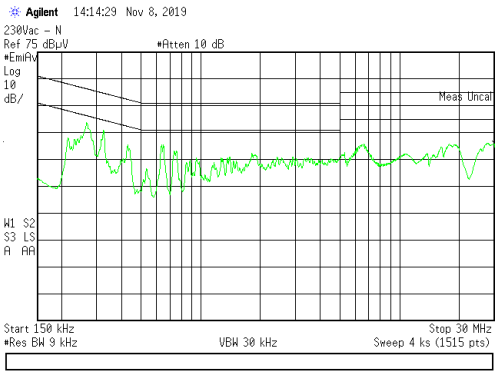


Figure 83. EMI measurements for 15 V output profile, Neutral scan (230 V_{AC})



10.5 Output profile: 20 V / 2.25 A

Figure 84. EMI measurements for 20 V output profile, Line scan (115 V_{AC})

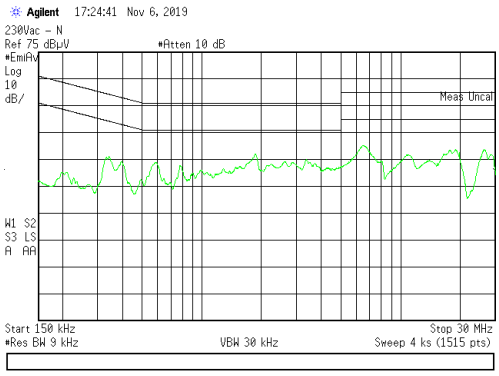


Figure 85. EMI measurements for 20 V output profile, Line scan (230 V_{AC})

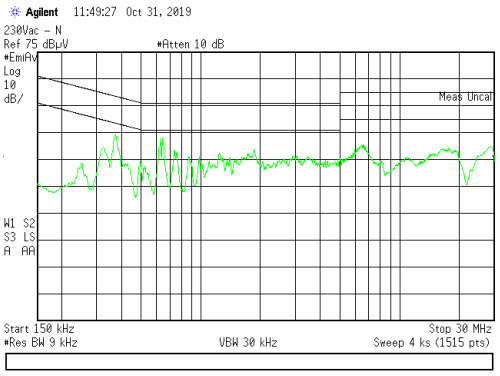


Figure 86. EMI measurements for 20 V output profile, Neutral scan (115 V_{AC})

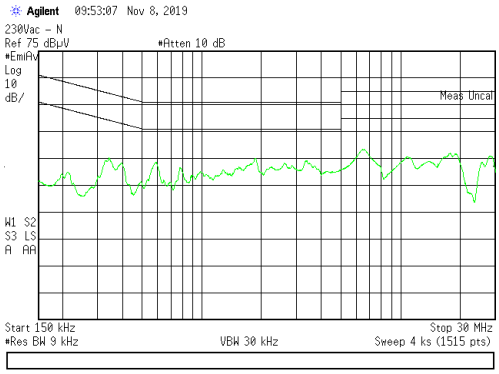
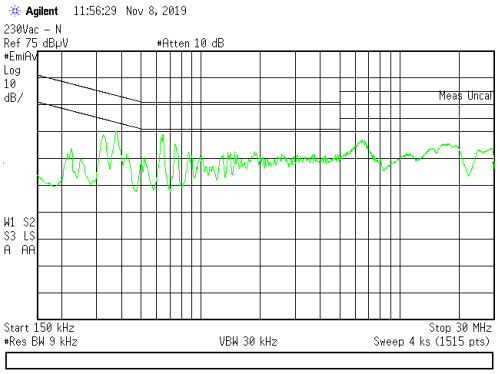


Figure 87. EMI measurements for 20 V output profile, Neutral scan (230 V_{AC})



11 Reference

(1) STCH03 Datasheet: available at www.st.com
(2) SRK1001 Datasheet: available at www.st.com
(3) AN5430 " The STUSB4761 PCB routing guidelines" : available at www.st.com
(4) STUSB4761 Datasheet: available at www.st.com

Revision history

Table 8. **Document revision history**

Date	Version	Changes
19-Feb-2020	1	Initial release.

Contents

List of tables

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