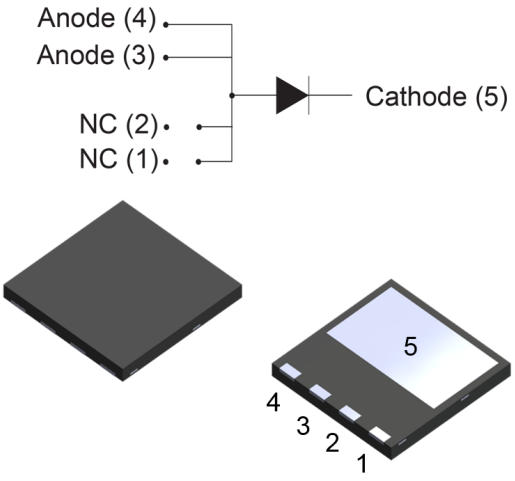
Thermal behavior and printed circuit board assembly recommendations for STMicroelectronics PowerFLAT 8x8 HV package

Introduction

The PowerFLAT 8x8 HV package has been developed to answer compactness requirements for low profile applications. This less-than-1 mm thickness package can be easily inserted in the thinnest power supply while showing good thermal behaviour, comparable to DPAK. In addition to thermal aspects, this application note gives some guidelines on soldering process, showing how to mount this flat package and easily withstand thermo-mechanical stresses.

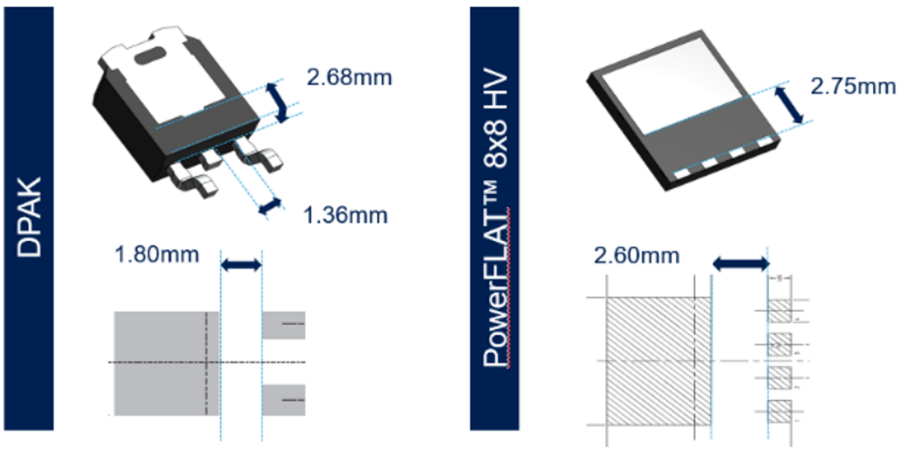
Figure 1. PowerFLAT 8x8 HV package configuration



PowerFLAT™ 8x8 HV

Furthermore, the PowerFLAT 8x8 HV package offers a greater distance between body pad and leads to ensure higher creepage distance than DPAK.

Figure 2. PowerFLAT 8x8 HV creepage



1 Thermal considerations

1.1 Thermal resistance

The thermal resistance of a semiconductor device defines the device's capability to dissipate the heat generated by the chip during operation. This parameter allows us to calculate the junction temperature, taking into account the device environment (load current, ambient temperature, mounting conditions, etc.).

For SMDs, the thermal resistance between junction and ambient, called $R_{th(j-a)}$ or $R_{th(j-pcb)}$, highly depends on the copper surface used under the tab. Figure 3 and Figure 4 below show an example of the relationship between $R_{th(j-a)}$ and the copper surface under the tab for an FR4 board - 35 and 70 µm copper thicknesses for a PowerFLAT 8x8 HV compared to other packages.

Power dissipation can be improved by using a PowerFLAT 8x8 HV compared to a PowerFLAT 5x6.

In regards to DPAK, this thinner and lighter package is showing very similar thermal dissipation.

Figure 3. Thermal resistance junction to ambient versus copper surface under tab (typical values, epoxy printed board FR4, e_{Cu} = 35 µm)

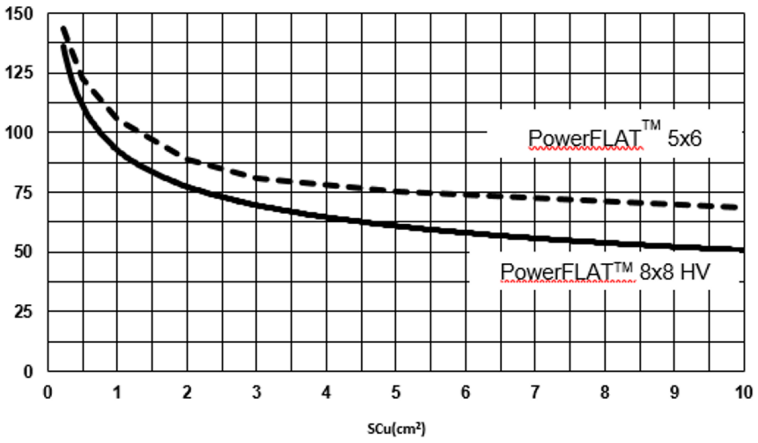
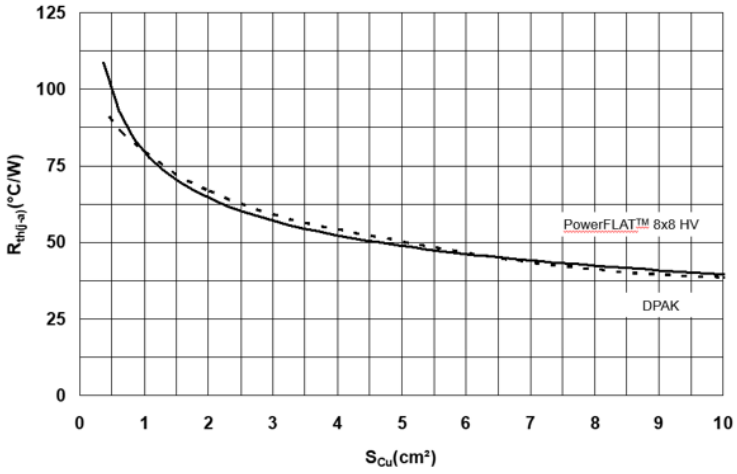


Figure 4. Thermal resistance junction to ambient versus copper surface under tab (typical values, epoxy printed board FR4, e_{Cu} = 70 µm)

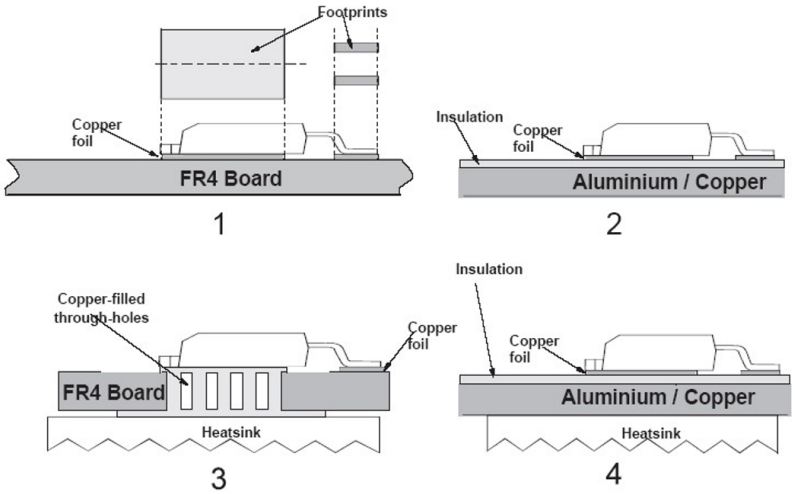


1.2 Mounting techniques and $R_{th(j-a)}$

$R_{th(j-a)}$ varies based on the printed circuit board technology employed. As shown in Figure 5, several technologies can be used depending on the performance required in the design. Four techniques are commonly used:

- FR4 - copper
- IMS (insulated metal substrate)
- FR4 board with copper-filled through-holes + heatsink
- IMS + heatsink

Figure 5. Mounting techniques for power SMDs



As the FR4 board is commonly used in surface mounting techniques, there are several ways of overcoming its low thermal performance:

- The use of large heat spreader areas (heatsink) at the copper layer of the PCB
- The use of copper-filled through-holes in addition to an external heatsink for even better thermal management

However, due to its power dissipation limitation, using the FR4 board with these techniques is only advisable for currents up to 8 A max.

Another technology available today is IMS - Insulated Metallic Substrate. This offers greatly enhanced thermal characteristics for surface mount components. IMS consists of three different layers:

- (I) base material which is available as an aluminum or copper plate
- (II) thermal conductive dielectric layer
- (III) copper foil, which can be etched as a circuit layer

If a higher power has to be dissipated, an external heatsink can be applied, which allows a significant reduction of $R_{th(j-a)}$.

The designer should carefully examine the appropriate mounting method to be used based on the power dissipation requirements. The board type will influence the thermal performance of the system. Table 1 shows the $R_{th(j-a)}$ for each mounting technique. The $R_{th(j-a)}$ values were not measured in similar conditions for PowerFLAT packages, but similar values can be expected.

Table 1. $R_{th(j-a)}$ for DPAK

Mounting method	$R_{th(j-a)}$
	DPAK
FR4 with minimum footprint	90 °C/W
FR4 with 10 cm² heatsink on board	40 °C/W
FR4 with copper filled holes and external heatsink	13 °C/W
IMS (40 cm^2) floating in air	9 °C/W
IMS with external heatsink	4.5 °C/W

1.3 T_j determination by measurement of top package temperature

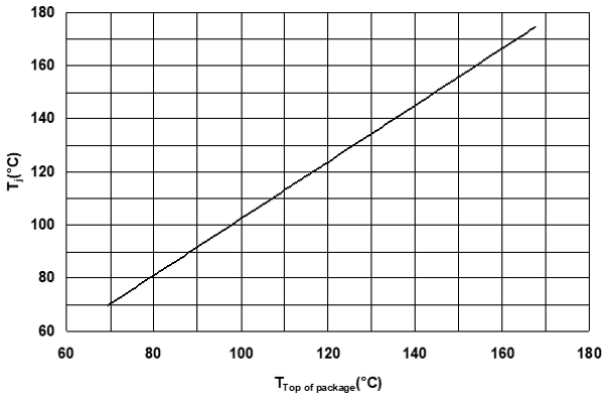
In conventional package such as a TO220 through-hole package, the device's junction temperature can be estimated from a measurement of the case temperature and $R_{th(j-c)}$ specified in datasheet by the relation:

- $T_j = T_c + P * R_{th(j-c)}$

In the case of the PowerFLAT 8x8 HV, the $R_{th(j-c)}$ concept is not suitable due to the complexity to measure a reliable case temperature (no access to the exposed pad).

As described in JESD51-2, the junction temperature of the dice can be estimated by a measurement of the top of package temperature. The Figure 6 below illustrates the variation between the diode junction temperature got by V_F diode reading and the top of package temperature obtained by thermal camera. This curve shows a low difference between junction temperature and measured top of package temperatures for a STPSCxH065DLF. The worst case appears at maximum junction temperature and leads to a difference of 7%. Obviously, this result may vary a bit depending on the PCB configuration but this characterization could be reproduced on applicative PCB.

Figure 6. Junction temperature versus maximum top of package temperature (typical values, mounted on epoxy printed board FR4 with recommended footprint, e_{Cu} = 70 µm)



2 PowerFLAT 8x8 HV PCB mounting process

The surface mount assembly is a 5-step process:

1. Solder paste printing
2. Component placement on the board
3. Reflow soldering
4. Cleaning (optional)
5. Final solder joint inspection

2.1 Printed circuit board recommendations

PCB solderable metallization

There are two common plated solderable metallization finishing which are used for PCB surface mount devices. In either case, it is required that the plating is uniform, conforming and free of impurities to ensure consistent solderability.

The first metallization finishing consists of an organic solderable preservative (OSP) coating over the copper pad. The organic coating assists in reducing oxidation to preserve the copper metallization for soldering.

The second metallization is NiAu (electroless nickel plating over the copper pad, followed by immersion gold). The thickness of the nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. For the immersion gold process, the gold thickness is self-limited, but should be thick enough to prevent Ni oxidation (typically above 0.05 µm) and thin enough to represent more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment, which may affect the reliability of the solder joint.

PCB design

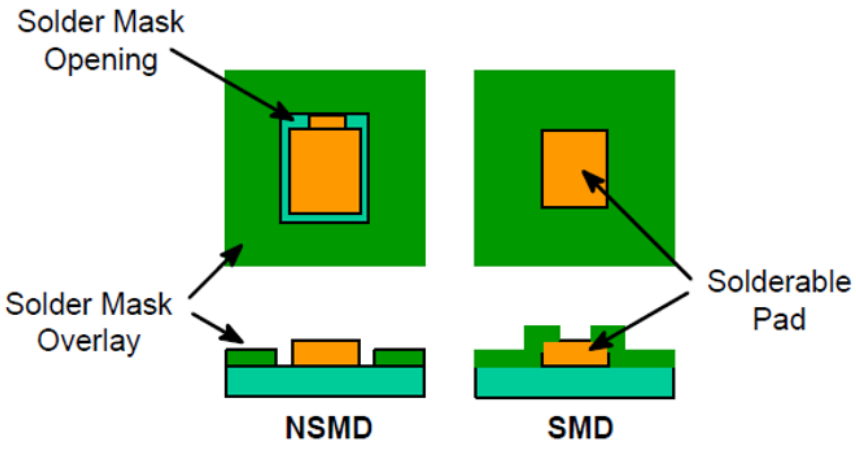
We recommend closed vias in the design, in order to control the amount of solder paste during screen printing. Position of tracks and open vias in the solder area should be well balanced. Symmetrical layout is recommended to avoid tilt caused by asymmetrical solder paste quantities.

- Non solder mask defined (NSMD)
- Solder mask defined (SMD)

As their title indicates, NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 7.

With SMD pads, the solder mask restricts the flow of solder paste to the top of the metallization, preventing the solder from flowing along the sides of the metal pad. This is different from the NSMD pads, where the solder will flow around both the top and the sides of the metallization.

Figure 7. Comparison between SMD and NSMD pads

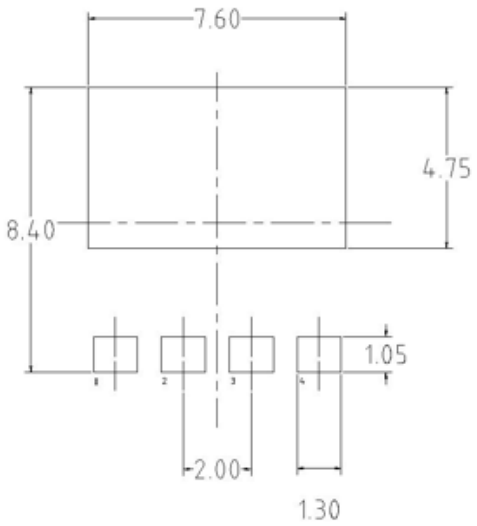


Both configurations can be used.

Typically, NSMD pads are preferred since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of tighter tolerance than the solder masking process.

PCB solderable pad design recommendations for PFLAT packages are shown in Figure 8.

Figure 8. PowerFLAT 8x8 HV PCB footprint



The dimensions of the PCB solderable pads should be greater than the package pads to ensure correct solder fillet aspect. This ratio is designed for optimal reliability, and to allow component self-centering during reflow.

2.2 Solder paste printing

Solder type

We recommend the use of solder paste with fine particles (type 3 or type 4, meaning that the particle are measuring from 20 to 45 µm), as well as solder paste containing halide-free flux ROL0 in accordance with ANSI/J-STD-004.

For lead- free solders Sn-Ag-Cu, alloy SnAg1.0Cu0.5 is preferred, but any SnAgCu alloys with 1 to 4% Ag and <1% Cu should be suitable.

Solder screening on the PCB

Stencil screening the solder on the PCB is commonly used in the industry. Recommended stencil thicknesses are 0.075 mm to 0.127 mm (0.003 inch to 0.005 inch) and the sidewalls of the stencil openings should be tapered approximately 5° to ease the release of the paste when the stencil is removed from the PCB.

For a typical lead PCB terminal, we recommend a stencil opening to footprint ratio of 90%.

For central exposed pad, it may vary depending on package dimensions, but solder coverage should vary from 50 to 80%.

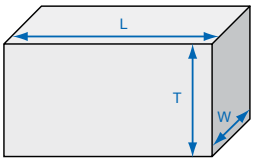
For PowerFLAT, as described later in this document, we evaluated an opening from 45 to 75%, without significant differences in terms of voids (but of course solder thickness differs depending on stencil opening and stencil thickness).

The stencil opening under the package's exposed pad must be divided into smaller openings. This reduces the risk of solder voiding and allows the solder joint for the leads to be at the same height as the exposed pad.

To ensure a safe and repeatable stencil printing process, some generic design rules for stencil design should be followed, as described here below.

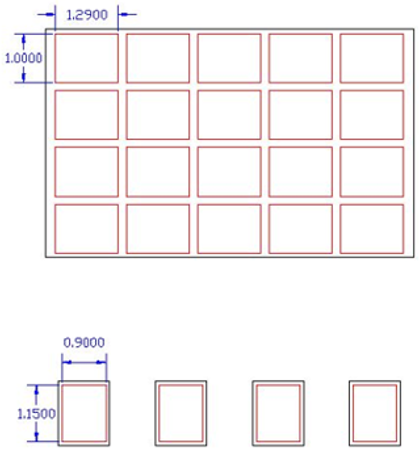
- General design rule
  - Stencil thickness (T) = 75 ~ 125 µm
  - Aspect ratio = W/T ≥ 1.5
  - Aspect area = (L x W) / (2T (L + W))

Figure 9. Stencil opening dimensions



Recommended stencil design openings is shown in Figure 10. Stencil openings are drawn in red lines (PCB solderable pads are in black).

Figure 10. **PowerFLAT 8x8 HV stencil opening recommendation**



2.3 Component placement

Manual placement is not recommended.

We recommend to use pick-and-place equipment with the standard tolerance of +/- 0.05 mm or better. The package will tend to center itself and correct for slight placement errors during the reflow process due to surface tension of the solder joint.

Adequate placement force should be used (3.5 N for example for most of packages).

Too strong, a placement force can lead to squeezed-out solder paste and cause solder joint to short.

Too low, a placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or non-centered packages.

2.4 Reflow profile recommendation

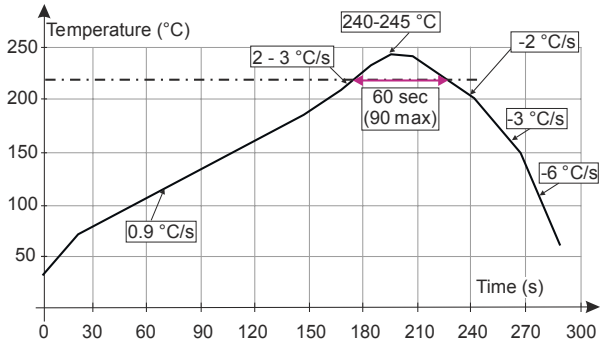
The soldering process causes significant thermal stress to a semiconductor component. This has to be minimized to assure a reliable and extended lifetime of the device.

PowerFLAT 8x8 HV, like many other SMD plastic packages, can be exposed to a maximum temperature of 260 °C for 10 seconds. Overheating during the reflow soldering process may damage the device. Therefore any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical heating profiles for lead-free solder (ST Ecopack) are given for small packages, either for mounting on an FR4 or on metal-backed boards (IMS). This is applicable to PowerFLAT 8x8 that is considered as a "small" package according to the JEDEC J-STD-020E. Please refer to the IPC / JEDEC J-STD-020E standard for further information about “small” and “large” component definitions.

Note: The soldering profiles defined in the JEDEC J-STD-020E standard are used for reliability assessment and typically describe the warmest profiles used for component mounting, not the necessary temperatures to achieve good soldering.

Wave soldering is not advisable for SMD power packages (and thus for PowerFLAT) because it is almost impossible to contact the whole package slug during the process.

Figure 11. ST Ecopack recommended soldering reflow profile for PCB mounting



For each individual board, the appropriate heat profile has to be adjusted experimentally. The current proposal is just a starting point. In every case, the following precautions have to be considered:

- Always preheat the device. The purpose of this step is to minimize the rate of temperature rise to less than 3 °C per second (recommended 2 °C/s) in order to minimize the thermal shock on the component.
- Dry out section, after preheating, to ensure that the solder paste is fully dried before starting the reflow step. Also, this step allows the temperature gradient on the board to be evened out.
- Peak temperature should be at least 30 °C higher than the melting point of the solder alloy chosen to ensure reflow quality. In any case the peak temperature should not exceed 260 °C.

Voids pose a difficult reliability problem for large surface mount devices. Voids under the package result in poor thermal contact and the high thermal resistance can lead to component failure.

2.5 Thermal cycling evaluations performed by STMicroelectronics

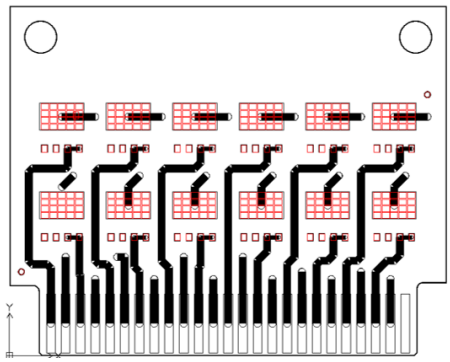
Evaluations are performed to assess ability of PowerFLAT package mounted on PCB to fulfill quality requirements.

2.5.1 Evaluation description

The PCBs are designed for PowerFLAT 8x8 HV with solderable pad dimensions recommended in this document. PCBs with 4 layers are designed (70 um Cu layer thickness on external sides, 35 um Cu internal layers – total is 4 layer PCBs) to evaluate PCBs with different mechanical characteristics. Solderable pads are designed as NSMD, and covered with NiAu plating.

PCB and PowerFLAT components generate a daisy chain, resistance is measured at initial stage, and resistance drift is measured every 500 cycles. Figure 12 provides the design of the PCBs.

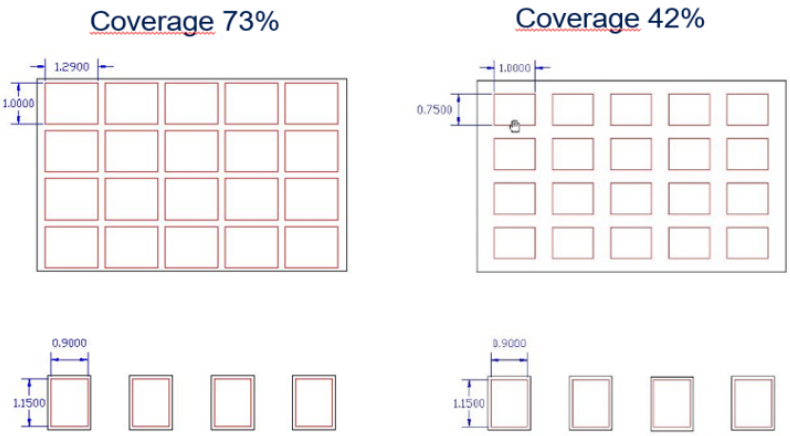
Figure 12. PCB design



The components are mounted on the PCBs with 2 different stencil designs, described in Figure 13. Opening ratio of 73% and 42% are designed for central exposed pad in order to evaluate pad opening impact on reliability (opening ratio is the ratio between stencil opening and PCB land dimension).

Stencils with 100 µm thickness is evaluated. The solder paste used is SnAg1.0Cu0.5 solder alloy, type 4 paste.

Figure 13. Stencil openings single pad

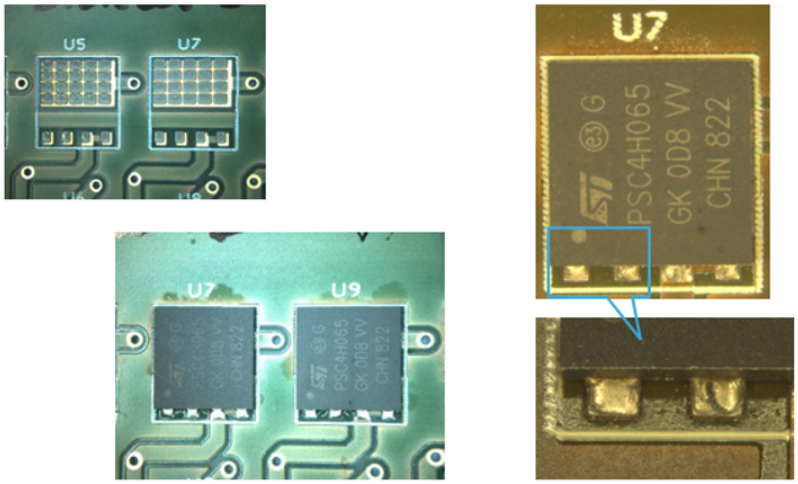


The reflow profiles used are the standard JEDEC profiles and an optimized reflow under vacuum in order to reach void level (< 1% compare to 30% voids under a single pad) in our evaluation, but it is intentionally not optimized to reflect reliability behavior of a solder joint in conditions not necessarily optimized for a PowerFLAT package.

2.5.2 Results

Assembly on PCB yield is 100%; no issue encountered.

Figure 14. Assembly pictures



The “standard reflow” is the recommended JEDEC reflow profile without any optimization. For this reason, the void level is up to 30%. As mentioned earlier, this reflow profile is optimized with vacuum during reflow, then the void levels observed are quite different and down to < 1%, refer to Figure 15, Figure 16 and Figure 17. Below are some pictures of the voids inside the solder joint layer (from < 1% to 30 % voids in the central pad). On this study, the leg with a stencil opening of 73% of the coverage with an optimized reflow under vacuum give the best results in term of cumulated voids under the central pad. Then, a reflow profile optimization can be done without vacuum by fine-tuning key parameters described in paragraph Section 2.4 .

Figure 15. Voids results and picture

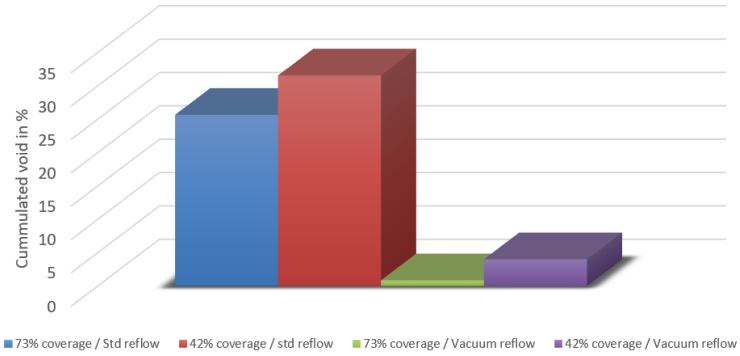


Figure 16. X-rays showing solder joint voids (standard and vacuum reflow)

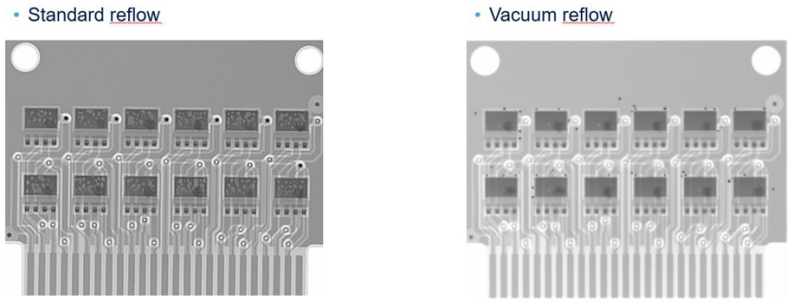
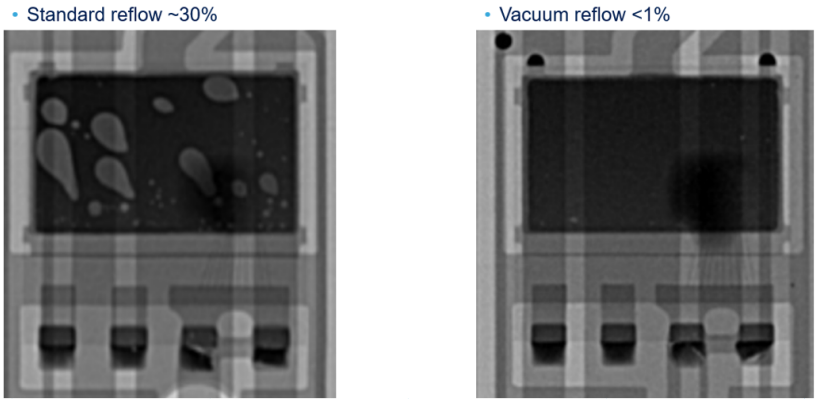
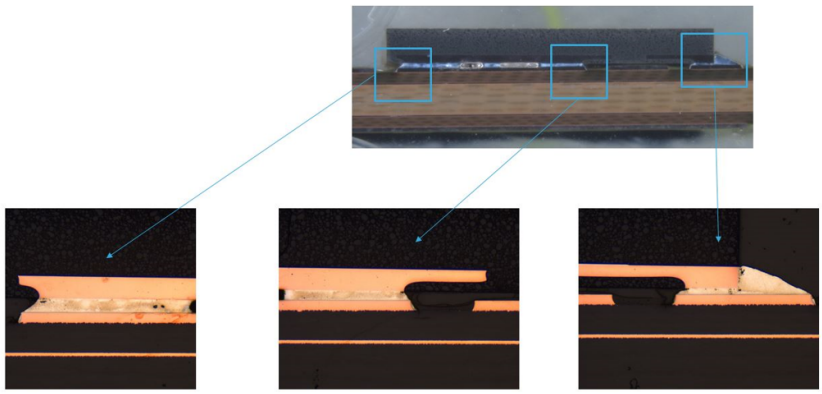


Figure 17. X-rays showing solder joint voids (standard reflow 30% and vacuum reflow < 1%)



The cross section views of the package mounted on a PCB show correct solder joints.

Figure 18. Cross section view



After the MSL1 cycles preconditioning level (as per IPC/JEDEC J-STD-033*), and 2000 cycles of thermal cycling (-65/150 °C / 2 cycles / hour), no failure are noted Table 2.

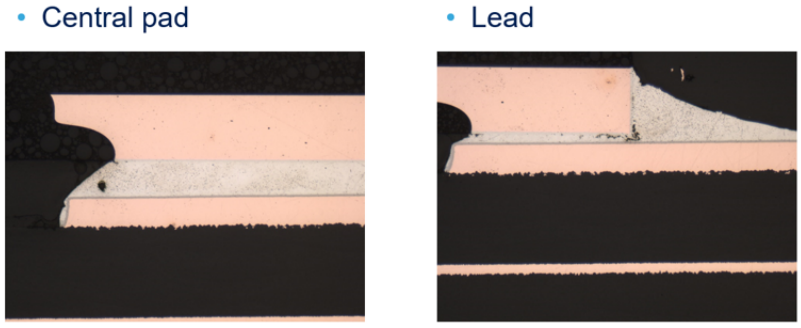
The thermal cycling is stopped after 2000 cycles then we can not highlight the benefit of low solder voids rate on the thermo-mechanical stress.

Table 2. Thermal cycling results

Reflow	Stencil pad opening in %	Results MSL1 + TC 2000 cycles
Standard	73 %	0/24
Standard	42 %	0/24
Vacuum	73 %	0/24
Vacuum	42 %	0/24

The physical analysis is conducted for each case and showed no crack in the solder joint under leads and central pad, as highlighted in Figure 19 below.

Figure 19. Physical analysis sample after 2000 cycles



3 Conclusion

Housing SiC diodes in our PowerFLAT 8x8 HV contributes to extract the best compactness for hardware design with a similar thermal performance than DPAK for a thinner and lighter package.

This evaluation confirmed that PowerFLAT 8x8 HV assembly on a printed circuit board is a safe and reliable process, and allows at least 2000 thermal cycles (-65/+150°C) without issues. For applications requiring better behavior, some optimization may be done like reflow profile under vacuum to ensure a stronger solder joint with fewer void.

We noticed also that the stencil opening ratio under the central pad does not have a major influence on void levels, although we recommend a design with more than 50% opening ratio to avoid excessive tilt.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
27-Jan-2020	1	Initial release.

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