Application note

Current Sensing in motion control applications

Introduction

The most common method to read the current flowing in a motor is to use a resistor connected on the source of each low side MOSFET of the power stage. The value of these resistors ranges from few milliohms to hundreds of milliohms, depending on the target current in the motor. Such small values help reduce the power dissipation, but imply small voltage drops. In order to properly acquire the small signal coming from the sense resistors, an amplification network is sometimes required.

This application note describes how to configure and size the amplifying network, providing some handy formulas.

1 Amplification for current sensing

1.1 List of definitions

Table 1 reports all the acronyms used in this application note.

Table 1. List of acronyms and definitions

Acronym	Definition
HS	High side MOSFET. When closed, it connects the load to the positive supply voltage. Refer to Figure 1.
LS	Low side MOSFET. When closed, it connects the load to the GND. Refer to Figure 1 .
Half bridge	Structure composed by one HS and one LS MOSFET connected together. Refer to Figure 1.
Full bridge	In this configuration each side of the load is connected to a half bridge: the full bridge can force the current in the load in both directions.
GND	Ground voltage. It is the reference or common voltage of the circuit.
R_S	Sense resistor or shunt resistor, placed on the source of the low side MOSFET, in order to measure the value of the current flowing in the load. Refer to Figure 1.
PWM	Pulse Width Modulation: it is a driving technique which uses a square wave with a modulated duty cycle in order to change the amount of current flowing through an inductive load.
DC	Direct current: more generally refers to currents and voltages which do not change in the time.
Op-amp	Operational amplifier.
GBWP	Gain Bandwidth Product of an operational amplifier.
SR	Slew Rate of the operational amplifier output.
ADC	Analog to Digital converter.
MCU	Microcontroller Unit.
PCB	Printed Circuit Board.

1.2 Sense resistor configuration

The typical configuration used for the current sensing is represented in Figure 1. The current can be sensed only when the low side MOSFET is turned on. According to the direction of the current in the inductive load, the voltage signal on the sense resistor can be positive or negative, as shown in Figure 2.

Figure 1. Basic configuration for current sensing using a sense resistor

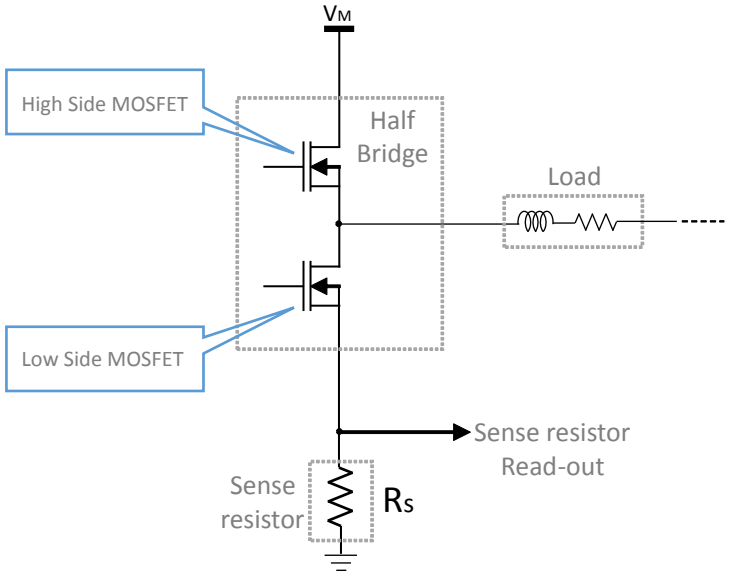
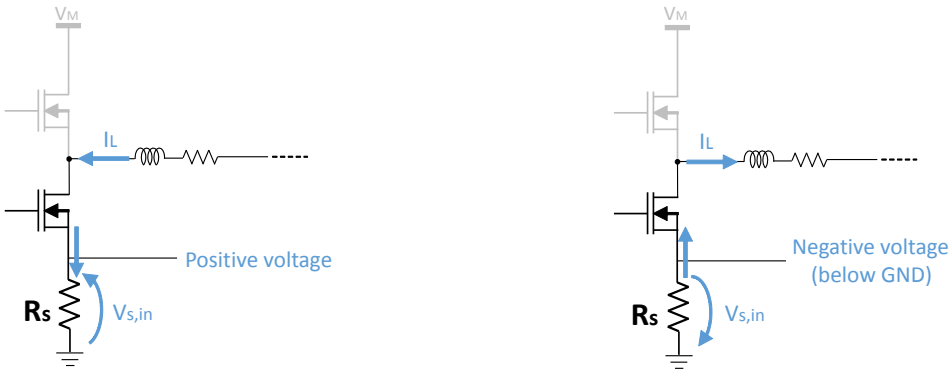


Figure 2. Representation of the voltages on the sense resistor according to the load current



Some current control methods just consider the positive voltage on the sense resistor in order to have an estimation of the current flowing in the motor phases, for example a peak current controller described in Section 1.2.1 . Some other control algorithms, e.g. Field Oriented Control, require the measurement of both positive and negative voltages on the sense resistor R_S. This application note focuses on this second configuration and explains how to acquire and condition bipolar signals, in order to make them compatible with the input of an ADC referred to GND.

1.2.1 Unipolar current sensing example

The unipolar current sensing refers to a current controller which monitors only the positive value of voltage on the sense resistor and regulates the current in the load according to this value. A typical example is the control of the peak current. The power stage uses the PWM technique in order to limit the peak of the current flowing in the load. Usually this kind of control uses a single sense resistor common to more than one half bridge; as an example consider Figure 3, where two half bridges are connected together in order to form a full bridge configuration, but only one sense resistor is used. The same image explains the meaning of on-time (T_{ON}) and off-time (T_{OFF}). The waveforms related to the peak current control are shown in Figure 4.

Figure 3. Current in the power stage during on-time and off-time

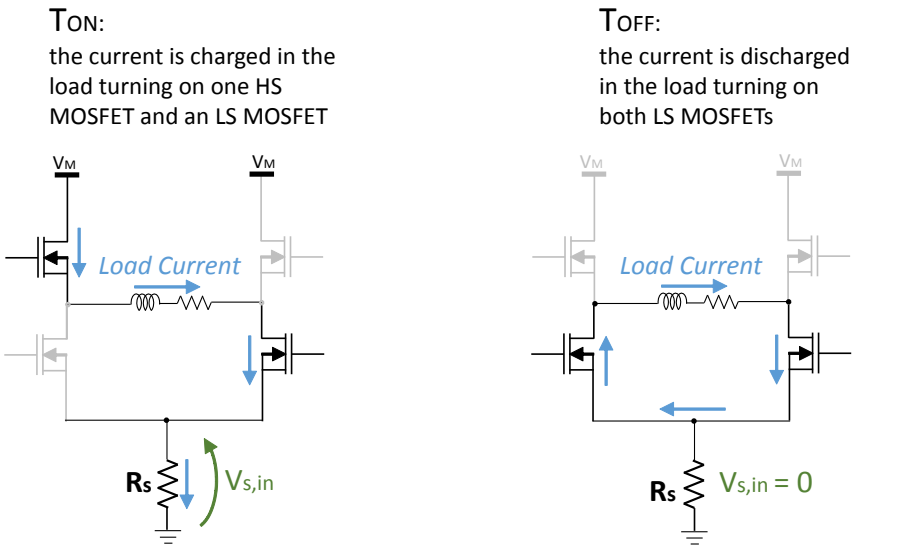
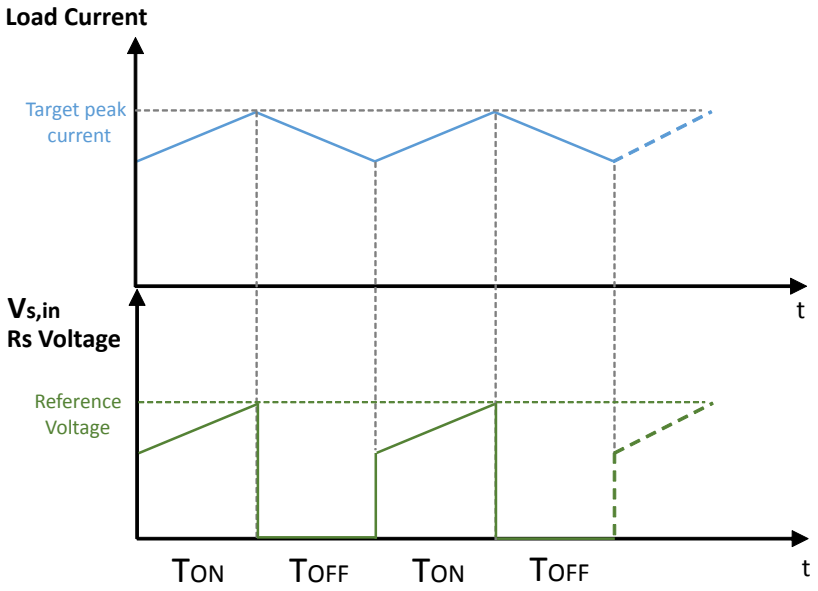


Figure 4. **PWM current control based on the current peak**



When a T_{ON} is performed, the current in the load increases: the voltage on the R_S increases as well. When the voltage reaches the target value, a T_{OFF} is triggered, discharging the current in the load for a fixed amount of time. Switching between T_{ON} and T_{OFF} allows to control the current in the load, and its level can be controlled just monitoring the positive value of the sense resistor's voltage and comparing it with a reference.

1.2.2 Bipolar current sensing

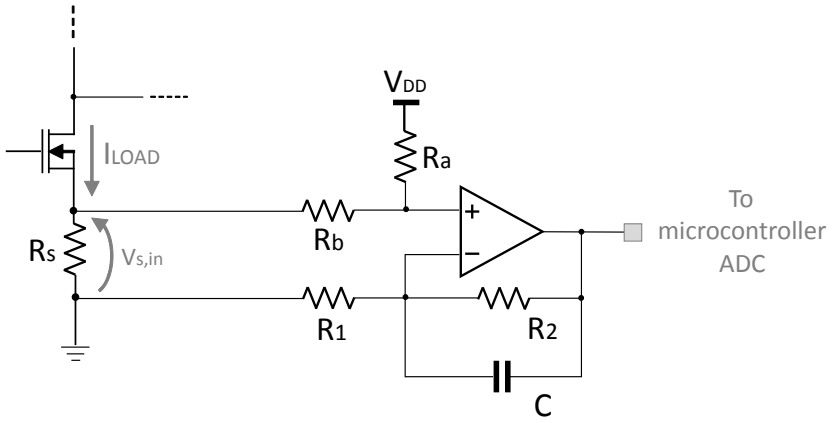
Other algorithms need to monitor the profile of the current in order to control it. Since the current can vary from a positive value to a negative one, the current flowing through the sense resistors generates both positive and negative voltage values. Consider for example a power stage in which each half bridge is connected to a sense resistor: when the LS of the half bridge is turned on the current flows in the sense resistor. According to the direction of the current, the voltage drop can be positive or negative (as depicted in Figure 2). The current is sampled at each PWM cycle, i.e. every time the LS turns on, and the profile of the current can be tracked. The control algorithm can calculate the PWM driving signals, according to the current profiles measured. While the positive voltages on the sense resistor can be directly acquired, negative signals (below GND reference) need a voltage translation before sampling, as explained in Section 1.3 .

1.3 Amplification network schematic for bipolar current sensing

The signal coming from the sense resistor is usually sampled by a microcontroller using an ADC: the input dynamic range of the ADC ranges from GND to V_{DD}, where V_{DD} is the supply voltage of the ADC. The signal of the sense resistor ranges from $– I_{max} \cdot R_S$ *to* $+ I_{max} \cdot R_S$, where I_{max} is the maximum current of the application and R_S is the sense resistor's value. In order to match the two ranges, a level shifting is needed before amplifying the signal.

The circuit proposed for current sensing is represented in Figure 5: referring to the image, R_a and R_b operate the signal level shifting.

Figure 5. Schematic of the amplification network



In case of zero current in the sense resistor, the ADC input should be at $V_{DD}/2$ (in the middle of the dynamic range), so the following relation must be satisfied:

Equation 1

(1)

$$\boldsymbol{V_{DD}} \cdot \frac{\boldsymbol{R_b}}{\boldsymbol{R_a} + \boldsymbol{R_b}} \cdot \left(1 + \frac{\boldsymbol{R_2}}{\boldsymbol{R_1}}\right) \approx \frac{\boldsymbol{V_{DD}}}{2}$$

R_a and R_b are supposed to be much greater than R_S, so this latter can be neglected in the formula. Satisfying Eq. (1) ensures a proper bias of the amplifier; then the gain of the amplifier must be adjusted in order to fit the application requirements (further details are provided in Section 1.3). The resistors' values can be sized to meet the selected gain *G*, according to the following equation:

Equation 2

(2)

$$V_{s,in} \cdot \frac{R_a}{R_a + R_b} \cdot \left(1 + \frac{R_2}{R_1}\right) \approx G \cdot V_{s,in}$$

Eq. (1) and Eq. (2) can be combined together to find a set of values for resistors in order to have the signal at the ADC input centered at $V_{DD}/2$ and amplified by a given gain *G*:

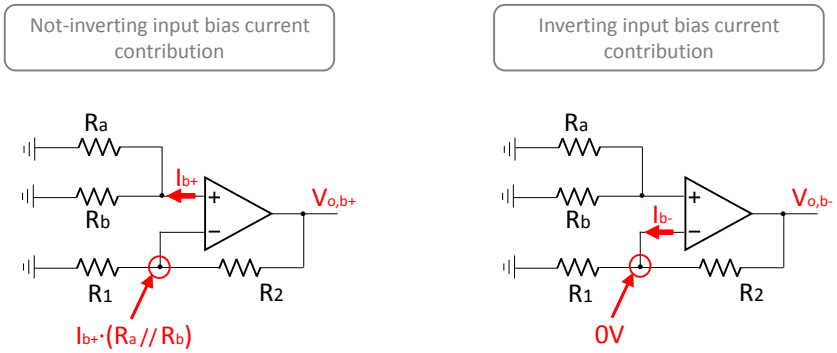
Equation 3

(3)

$$\begin{cases} \frac{R_a}{R_b} = 2G \\ \frac{R_2}{R_1} = G - 0.5 \end{cases}$$

Moreover, the bias current of the op-amp can introduce an error: in fact, the circuit presented in Figure 5 can be analyzed, considering the bias currents one at a time, as shown in Figure 6.

Figure 6. Equivalent circuit of the bias currents contributions



The resulting output due to bias currents is the sum of two contributions: $V_{o,b}+$ and $V_{o,b-}$:

$$\begin{cases} V_{o,b+} = I_{b+} \cdot \left(R_a // R_b\right) \cdot \left(1 + \frac{R_2}{R_1}\right) \\ V_{o,b-} = - I_{b-} \cdot R_2 \end{cases}$$

In order to cancel the error introduced by bias currents, one contribution must compensate the other one, thus $V_{o,b}+ = -V_{o,b}-$. Considering that in most of the op-amps the two bias currents have the same value ($I_{b+} = I_{b-}$), it is possible to compensate the error choosing the resistors as stated in the following equation:

Equation 4

(4)

$$V_{o,b+} = -V_{o,b-} \Longrightarrow \frac{R_a R_b}{R_a + R_b} = \frac{R_1 R_2}{R_1 + R_2}$$

According to Eq. (4), Eq. (3) can be rewritten as:

Equation 5

(5)

$$\begin{cases} \frac{R_a}{R_b} = 2G \\ \frac{R_2}{R_1} = G - 0.5 \\ \frac{R_b}{R_1} = 1 - \frac{0.5}{G} \end{cases}$$

1.4 Gain selection and dynamic performance

The gain *G* of the amplifier should be adjusted in order to exploit the entire dynamic range of the ADC that is sampling the signal. Usually the dynamic range is equal to the voltage supply of the microcontroller V_{DD} (a typical value is 3.3 V). Considering a maximum target current for the application I_{max}, that can be positive or negative as shown in Figure 2, it is possible to calculate the maximum gain G_{max} as follows:

Equation 6

(6)

$$G_{max} = \frac{V_{DD}}{2 \cdot I_{max} R_S}$$

Using a gain greater than G_{max} results in a saturation of the ADC at higher currents. The trade-off to be considered for gain selection is given by the gain-bandwidth product (GBWP) of the selected op-amp. Choosing a higher gain reduces the bandwidth of the system; the following relation can be used in order to estimate the bandwidth of the system:

Equation 7

(7)

$$BW = \frac{GBWP}{1 + \frac{R_2}{R_1}}$$

The Slew Rate (*SR*) of the op-amp should be considered as well: this parameter is crucial especially when the load current approaches its maximum value I_{max}.The output of the op-amp continuously switches, with an output variation equal to $\Delta V_{OUT} = I_{max} \cdot R_S \cdot G$. The slew rate of the op-amp determines the minimum settling time ($T_{settling}$) to be waited in order to have the output stable after the LS MOSFET is turned on

Equation 8

(8)

$$T_{settling} > \frac{I_{max} \cdot R_S \cdot G}{SR}$$

The op-amp should be chosen in order to have a very small settling time compared to the PWM period driving the motor.

Another aspect to be considered is the noise coming from the switching of the power stage. In order to improve the noise filtering while ensuring the integrity of the signal coming from the sense resistor, a capacitor C can be added in the feedback loop of the op-amp, as shown in Figure 5. The cut-off frequency of the low pass filter is given by:

Equation 9

(9)

$$f_{LP} = \frac{1}{2\pi R_2 C}$$

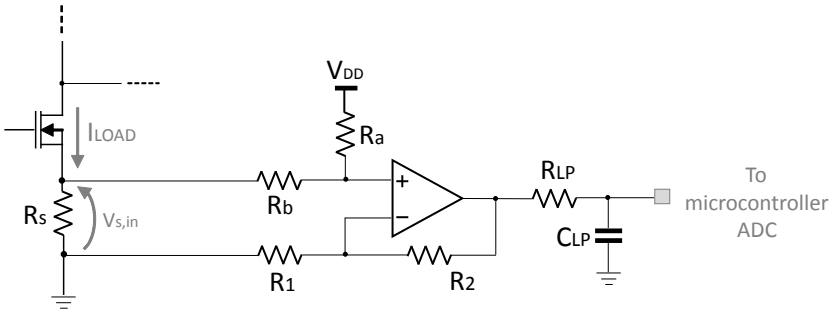
The capacitor should be selected according to the application parameters (such as the PWM frequency of the driver) and to be effective, the cutoff frequency f_{LP} stated in Eq. (9) should be smaller than the frequency limitation introduced by the op-amp (*BW* in Eq. (7)). It should be noted that the capacitor is in the feedback loop, so its value must be properly selected in order to guarantee the stability of the op-amp. When stability of the loop cannot be guaranteed, the low pass filter can be implemented removing the capacitor from the feedback loop and using an RC filter on the op-amp output (Figure 7). This solution can be used if the ADC input is a high impedance input, so the signal is not attenuated by the partition between the ADC input resistance and R_{LP}. Referring to Figure 7, the low-pass cut-off frequency is given by:

Equation 10

(10)

$$f_{LP,o} = \frac{1}{2\pi R_{LP} C_{LP}}$$

Figure 7. **RC low-pass filter added on the operational amplifier output**



1.5 Numerical example

This paragraph summarizes the concepts explained previously using a numerical example. The first parameter to be considered is the maximum current of the application. Let's assume for this example that I_{max}=10A. A reasonable value of the sense resistor R_S could be 20 mΩ; this guarantees that the maximum voltage drop on it is 0.2 V and thus the maximum power is 2W. Actually the average power is smaller, because the sense resistor dissipates only when the LS MOSFET is turned on. Choosing a resistor with a power rating of 2W ensures a safe margin from the thermal point of view.

Knowing the I_{max} and the R_S, it is possible to find the maximum amplification gain using Eq. (6): assuming V_{DD} = 3.3 V (typical digital voltage for microcontrollers) G_{max} = 8.25. Keeping some margin on the amplified signal, we can select G = 7.5 and using Eq. (5) we find:

$$\begin{cases} \frac{R_a}{R_b} = 15 \\ \frac{R_2}{R_1} = 7 \\ \frac{R_b}{R_1} \approx 0.933 \end{cases}$$

Selecting R_1 = 2 kΩ, it is possible to select the other resistors among the commercial values available:

- R_2 = 14 kΩ
- R_a = 30 kΩ
- R_b = 2 kΩ

It can be seen that the ratio R_b/R_1 is an approximate value, however the impact of this mismatch is reduced using an op-amp with low bias current inputs. A suggested part number is the TSV99x family. The TSV991, TSV992 or TSV994 op-amp (single, dual or quad respectively) are rail to rail input/output with a 20 MHz GBWP and a SR = 10 V/µs. The stability is guaranteed for closed loop gains greater than 4: there are no stability issues in this case, since the closed loop gain is 1+ R_2/R_1=8.

The bandwidth of the entire amplification network is given by Eq. (7) and it is BW = 2.5 MHz. According to Eq. (8), the minimum settling time of the op-amp is 150 ns. After the LS MOSFET turns on, the ADC should wait at least 150 ns before sampling the signal. Eventually considering for this example a PWM frequency of 25 kHz, the settling time is much smaller than the period of 40 µs, thus a proper sampling can be achieved.

2 Improved circuit

The amplification network described in Section 1 and represented in Figure 5 and Figure 7 shows some disadvantages:

1. In most cases the values found using Eq. (5) are not available in commercial format, so approximation in the resistors' values leads to a mismatch error
2. The common mode is not rejected, so parasitic elements on the GND path can introduce errors in the readout

In order to overcome these disadvantages, the circuit represented in Figure 5 and Figure 7 can be improved adding one more resistor, as explained hereafter.

2.1 Improved schematic diagram

The schematic of the improved solution is represented in Figure 8. The signal coming from the sense resistor is acquired as a differential signal. The ground reference is split between the power GND, which the sense resistor is referred to, and the signal GND, which is the reference for the amplified signal and the ADC. In fact, when high currents flow through the GND path, a common mode voltage is generated on the sense resistor, due to parasitic inductances distributed on the path (see Figure 9). If not rejected, the common mode voltage is amplified as a signal and it can introduce an error. The differential configuration depicted in Figure 8 allows to overcome this issue. As shown in Figure 8, the different GND paths must be kept separated and connected together just in one point of the PCB, usually the GND of the main power supply. Moreover, the two traces coming from the sense resistor must be treated as differential traces: they are connected as close as possible to the sense resistor terminals and run symmetrically and side by side towards the op-amp.

Figure 8. Improved schematic for current sensing network

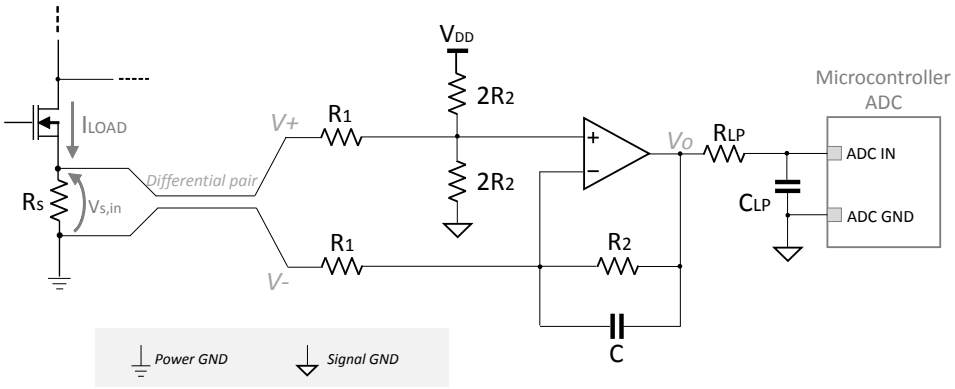
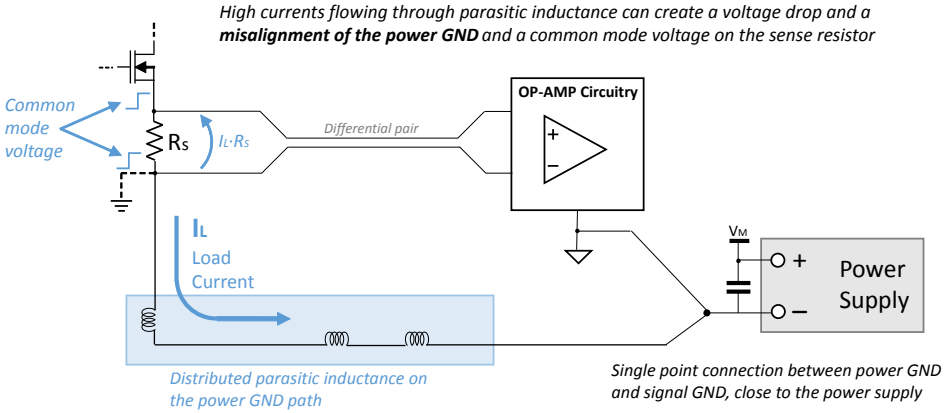


Figure 9. GND connections and parasitic elements on the power GND path



The op-amp network is sized in order to obtain the same gain on the inverting input and non-inverting input; referring to Figure 8, *V+* and *V-* must have the same gain, as stated in Eq. (11) (DC transfer for *V+*signal) and Eq. (12) (DC transfer for *V-*signal).

Equation 11

(11)

$$V_{o,+} = \frac{R_2}{R_1 + R_2} \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot V_+ = \frac{R_2}{R_1} \cdot V_+$$

Equation 12

(12)

$$V_{o,-} = -\frac{R_2}{R_1} \cdot V_-$$

Combining Eq. (11) and Eq. (12) it is possible to find the gain *G* for this amplification network:

Equation 13

(13)

$$G = \frac{V_o}{V_{s,in}} = \frac{(V_{o,+} + V_{o,-})}{(V_+ - V_-)} = \frac{R_2}{R_1}$$

Each differential signal (i.e. every signal generated by the current flowing in the power stage) is amplified according to Eq. (13), while each common mode signal (i.e. every signal coming from ground misalignment) is rejected.

Then, it can be verified that when $V_{s,in}$ = *0 (*no current is flowing in the sense resistor), the output V_o is equal to VDD/2 (considering that $R_S << R_1$):

Equation 14

(14)

$$V_o|_{V_{s,in}=0} \approx V_{DD} \cdot \frac{(R_1 \parallel 2R_2)}{2R_2 + (R_1 \parallel 2R_2)} \cdot \left(1 + \frac{R_2}{R_1}\right) = \frac{V_{DD}}{2}$$

It should be noted that the resistors' configuration on the input pins of the op-amp ensures the compensation of the bias currents of the op-amp.

According to the numerical example in Section 1.4 , where a gain G = 7.5 is required, the following resistors can be selected: R_1 = 2 kΩ, R_2 = 15 kΩ and consequently , $2R_2$ = 30 kΩ. The simplified relation between components allows to easily find commercial values matching the requirements.

The equations reported in section Section 1.4 are valid also for the circuit proposed in Figure 8, and can be applied in order to determine the maximum gain, the bandwidth and the settling time of the system.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
17-Oct-2019	1	Initial release.

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