AN5395

Application note

How to drive an external power amplifier with STM32WB series MCUs

Introduction

STM32WB series microcontrollers (MCUs) can support an external power amplifier (PA) to provide higher output power.

This document details the modifications to implement in the Cortex®-M4 firmware, to allow the external PA to be driven by the MCU. These modifications are based on the SKY66118-11 PA from Skyworks Solutions (maximum output power = 20 dBm).

1 Hardware

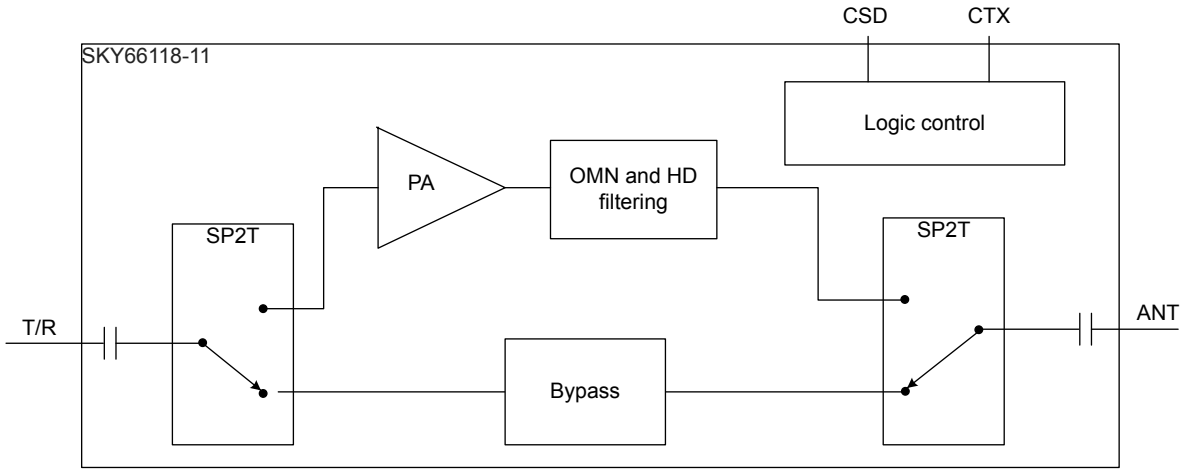
This document applies to the STM32WB series Arm® Cortex® core-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The following SKY66118-11 pins must be managed (see the figure and the table below):

- CTX pin, to switch the PA in transmission or reception
- CSD pin, to enable or disable the PA
- VCTRL pin, to control the output power (1.6 V < V_{CTRL} < 3.6 V), not represented in the figure below

Figure 1. SKY66118-11 block diagram



Note: ANT = Antenna, HD = harmonics distorsion, OMN = Output matching network, PA = power amplifier, SP2T = single pole 2 throw switch, T/R = transmit/receive

Refer to the SKY66118-11 datasheet available on Skyworks web site for more details.

Table 1. SKY66118-11 CSD and CTX pins

Mode	Description	CSD	CTX
0	All off (Sleep mode)	0	0 or 1
1	Transmit mode	1	1
2	Bypass mode	1	0

The CTX pin must be connected to GPIO PB0 (Port B, pin 0) of the microcontroller. The CSD pin is connected to another GPIO.

2 Firmware

CTX pin

For the CTX pin, add the following code to the Cortex-M4 firmware, in the initialization section of the GPIOs.

```
GPIO_InitTypeDef  GPIO_InitStruct;

 // Enable GPIOB clock for CTX pin
 __HAL_RCC_GPIOB_CLK_ENABLE();

 // configure the GPIO PB0 in AF6 to be used as RF_TX_MOD_EXT_PA
 GPIO_InitStruct.Pull      = GPIO_NOPULL;
 GPIO_InitStruct.Mode      = GPIO_MODE_AF_PP;
 GPIO_InitStruct.Speed     = GPIO_SPEED_FREQ_HIGH;
 GPIO_InitStruct.Alternate = GPIO_AF6_RF_DTB0;
 GPIO_InitStruct.Pin       = GPIO_PIN_0;
 HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
```

The CTX signal is managed by the hardware, hence there is nothing to add for this functionality.

Check that, in the Cortex-M4 firmware, PB0 is not used by another resource (for example, on the Nucleo board in the P-NUCLEO-WB55 pack, PB0 is used by LED2). If this occurs, this resource must be disabled.

CSD pin

The GPIO to be connected to the CSD pin must be configured in the Cortex-M4 firmware, in the initialization section of the GPIOs (PA0 example):

```
// Enable GPIOA clock for CSD pin */
  __HAL_RCC_C2GPIOA_CLK_ENABLE();
  __HAL_RCC_GPIOA_CLK_ENABLE( );

// configure the GPIO which will be managed by M0 stack to enable Ext PA
GPIO_InitStruct.Pull  = GPIO_NOPULL;
GPIO_InitStruct.Mode  = GPIO_MODE_OUTPUT_PP;
GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_HIGH;
GPIO_InitStruct.Pin   = GPIO_PIN_0;
HAL_GPIO_Init(GPIOA, &GPIO_InitStruct);
```

The Cortex-M4 firmware must inform the Cortex-M0+ firmware about the GPIO to be managed with the function:

- `SHCI_C2_ExtpaConfig((uint32_t)GPIOA, GPIO_PIN_0, EXT_PA_ENABLED_HIGH, EXT_PA_ENABLED);`

  when the PA is used.

- `SHCI_C2_ExtpaConfig((uint32_t) GPIOA, GPIO_PIN_0, EXT_PA, EXT_PA_ENABLED_HIGH, EXT_PA_DISABLED);`

  when the PA is not used.

Note: The selected PA must have a turn-on time lower than 300 µs.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
30-Sep-2019	1	Initial release.
16-Apr-2020	2	Updated: • Section 1 Hardware • Section 2 Firmware • Classification of the document
28-Jul-2025	3	Updated document title and Section 2: Firmware. Minor text edits across the whole document.

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