ACEPACK SMIT module package guidelines for mounting and thermal management

Introduction

STMicroelectronics is introducing a new module package called ACEPACK SMIT. This package is a surface mount power module, which is over-molded with an epoxy molding compound. The semiconductor chips are connected on a direct bonded copper (DBC) ceramic substrate. The DBC structure is composed of three layers: copper, alumina substrate, and copper. The alumina layer provides the required insulation with a specified voltage of 3400 V RMS.

The behavior of a semiconductor device depends on the temperature of its silicon chip. This is the reason why the electrical parameters are given at a specified temperature.

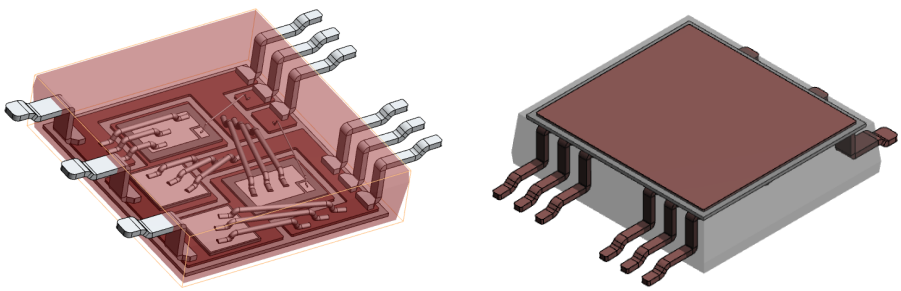
To achieve the performance of these devices, the temperature has to be limited by managing the heat transfer between the chip and the ambient atmosphere. The aim of this application note is to provide guidelines for the package mounting, handling and soldering. Also it provides thermal considerations linked to heatsink types and assembly methods.

The ACEPACK SMIT is design to be surface-mounted on a printed circuit board, while having its opposite top side connected to an external heatsink. This in order to extract the maximum power dissipation out of the device and optimize thermal performance. This module embeds a range of power devices containing thyristors, rectifier diodes (silicon or silicon carbide), and transistors such as MOSFETs (Si or SiC) and IGBTs.

The main applications where the ACEPACK SMIT fits are:

- On-board battery chargers
- EV chargers
- UPS
- Power converters for data centers
- Renewable energy
- Motor drive systems

Figure 1. ACEPACK SMIT package overview



Note: ACEPAK SMIT is a registered and/or unregistered trademark of STMicroelectronics International NV or its affiliates in the EU and/or elsewhere.

1 Package information

1.1 Package dimensions and packing

The ACEPACK SMIT has the following dimensions.

Figure 2. ACEPACK SMIT package outline

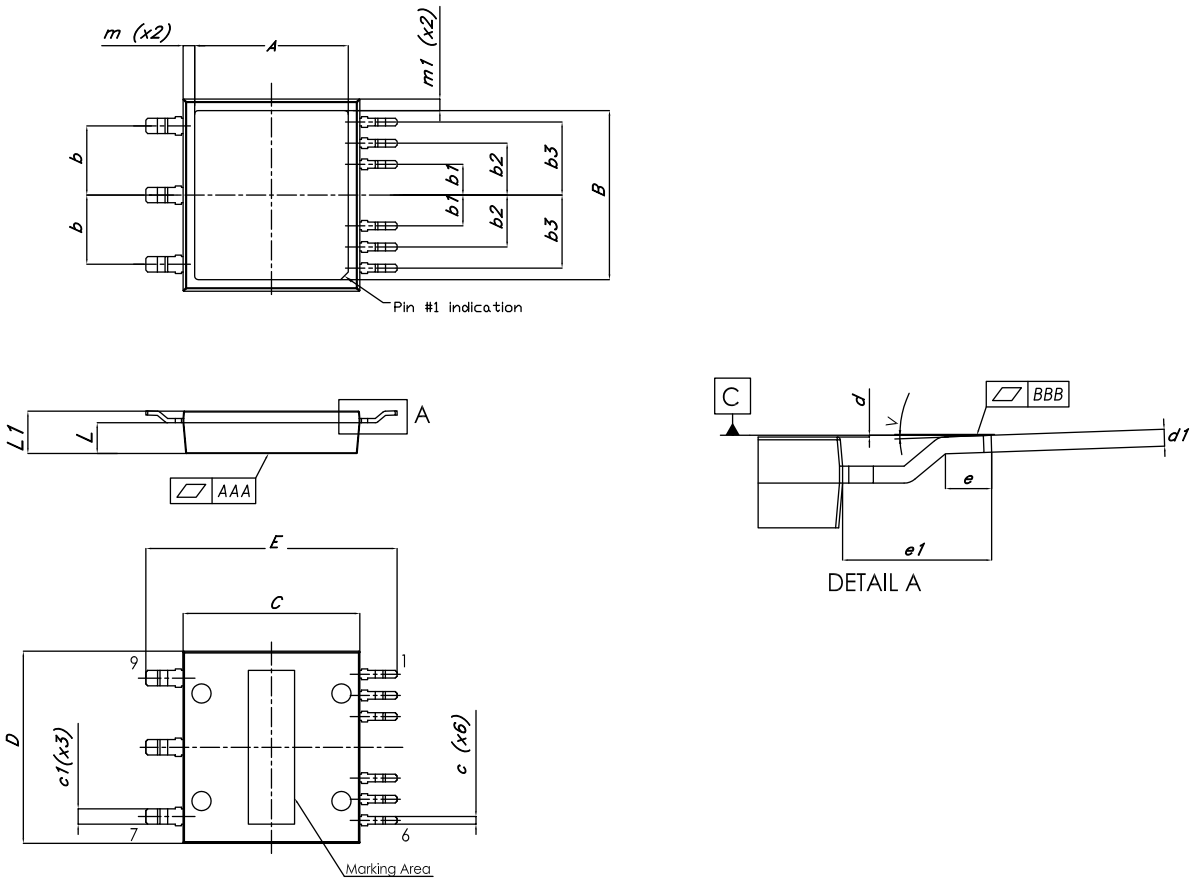
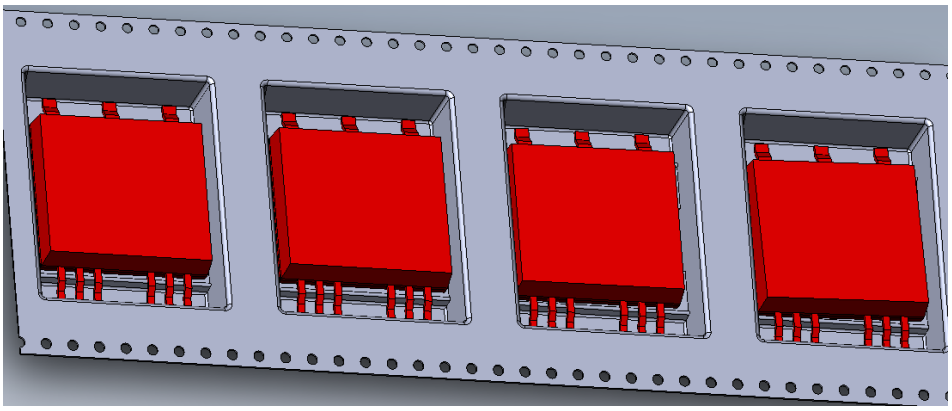


Table 1. ACEPACK SMIT package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	19.50	20.00	20.50
B	21.50	22.00	22.50
C	22.80	23.00	23.20
D	24.80	25.00	25.20
E	32.20	32.70	33.20
b		9.00	
b1		4.00	
b2		6.75	
b3		9.50	
c	0.95	1.00	1.10
c1	1.95	2.00	2.10
d	0		0.15
d1	0.45	0.55	0.65
e	1.30	1.50	1.70
e1	4.65	4.85	5.05
L	3.95	4.00	4.05
L1	5.40	5.50	5.60
m	1.3	1.55	1.8
m1	1.3	1.55	1.8
V	0°	2°	4°
AAA	0.01		0.05
BBB	0		0.1

ACEPACK SMIT products will be available in tape and reel packing, with 200 units per reel (reel is 13 inches, tape width is 56 mm, pitch between pockets is 36 mm).

Figure 3. ACEPACK SMIT picture in carrier tape



1.2 Moisture sensitivity

The ACEPACK SMIT is a moisture package. It is necessary to control the moisture content of the component (exposure to ambient air cause penetration of moisture into a package molding compound). Moisture absorption leads to moisture concentration inside of the component, which may be high enough to damage the package during the reflow process.

Therefore, it is required to dry moisture-sensitive components, seal them in a moisture-resistant bag, and only remove them immediately before assembly on the printed circuit board (PCB). The permissible time (floor life time, from opening the moisture barrier bag until the final soldering process) that a component can remain outside of the moisture barrier bag is a result of the sensitivity of the component to ambient humidity (moisture sensitivity level, MSL). The most commonly applied standard IPC/JEDEC J-STD-020E defines the MSL level, as shown in Figure 4.

Figure 4. Moisture sensitivity levels

LEVEL	FLOOR LIFE[4]		SOAK REQUIREMENTS[3]				
			STANDARD		ACCELERATED EQUIVALENT[1]		
					eV 0.40-0.48	eV 0.30-0.39	
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696[2] +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192[2] +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96[2] +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72[2] +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48[2] +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA

ACEPACK SMIT products are classified as MSL level 3. This means that the maximum floor life outside of the moisture barrier bag before reflow on PCB should not exceed 1 week (with 30 °C/60% relative humidity).

If the components have been exposed to ambient air for longer than this specified time, the components have to be baked before the assembly process. Please refer to IPC/JEDEC J-STD-033 for details. Please note that baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth.

1.3 Component solderability

The leads of the ACEPACK SMIT are plated with pure tin (10 µm minimum Sn plating). It ensures good solderability on the PCB pad openings, even after a long storage time. On the ACEPACK SMIT, the cut edges of the pins are also tin plated (unlike most of the SMD packages). This ensures wettability of the solder also on the pin edges (this is also called wettable flanks).

Tin plating performed is compatible with Pb-containing and Pb-free soldering processes.

2 Printed circuit board assembly

ACEPACK SMIT is a surface mount package. The assembly on the PCB consists of the following steps:

- Solder pastes printing
- Component placement on the PCB
- Reflow soldering
- Cleaning (optional)
- Final solder joint inspection

2.1 Printed circuit board recommendations

2.1.1 Material

There is no specific requirement related to PCB material for an ACEPACK SMIT package. STMicroelectronics performed evaluations with a PCB using FR4 material, as it is a commonly used material. Regarding the PCB thickness, as for thermal considerations (see detailed in Section 3 Heatsink attachment to package and Section 4 Thermal resistance measurements of this document) it is required to attach a heatsink at the top of the package. A thick PCB of 1.6 mm or above could be used to ease heatsink attachment, as it increases the PCB stiffness.

2.1.2 Copper

STMicroelectronics performed evaluations with 70 µm (2Oz/ft2) base, copper thickness on both sides of the PCB to accommodate the high currents required by the application. Final PCB copper thickness, including plating, is usually reaching 100 µm.

2.1.3 PCB pad design

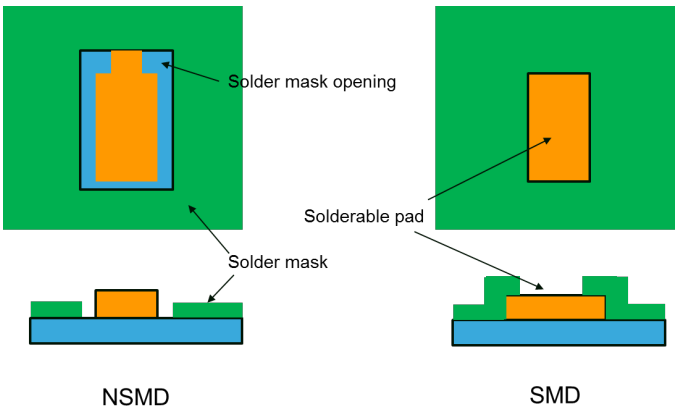
There are two different types of PCB pad configurations commonly used for surface mount packages:

- Non solder mask defined (NSMD)
- Solder mask defined (SMD)

The NSMD contact pads have the solder mask pulled away from the solderable metallization. For the SMD, pads have the solder mask over the edge of the metallization.

Using the SMD pads, the solder mask restricts the flow of solder paste to the top of the metallization. This prevents the solder from flowing along the sides of the metal pad. This is different from the NSMD pads where the solder flows around both the top and the sides of the metallization.

Figure 5. Solder mask design



The NSMD pads are preferred since defining the location and size of the copper pad. It is easier to control with respect to the solder mask. The copper etching process is suitable for tighter tolerance than the solder masking process. For NSMD, the solder mask openings are smaller than copper pads by typically 80 µm.

2.1.4 PCB solderable metallization

Solder paste must wet the solder pads. In general, all finishes are well-proven for surface mount technology for assembly.

From a package point of view, it is difficult to recommend a certain PCB pad finish, which always meets all requirements. The choice of the finish also depends on.

- the board design
- the pad geometry
- the various components mounted on the board
- the process conditions

It should be chosen accordingly to the specific needs of the customer.

STMicroelectronics usually recommends two PCB finishing types. In both cases, the plating must be uniform, conforming, and free of impurities, in order to ensure a consistent solderability.

The first metallization finish consists of an organic solderable preservative (OSP) coating over the copper pad. The organic coating assists in reducing oxidation to preserve the copper metallization for soldering.

The second metallization is NiAu (commonly electroless plated nickel over the copper pad, followed by immersion gold). The allowable internal material stresses determined the thickness of the nickel layer, and the temperature excursions the board is subjected to throughout its lifetime. In the case of an immersion a gold process, the gold thickness should be thick enough to:

- prevent Ni oxidation (typically above 0.05 µm)
- thin enough to represent more than 5% of the overall solder volume

Having excessive gold in the solder joint can create gold embitterment, which may affect the reliability of the solder joint.

2.1.5 Footprint

STMicroelectronics recommends the footprint shown in Figure 6 to achieve correct soldering.

For PCB design, it is recommended to keep a good balance between the top and bottom layers, copper ratios. It minimizes PCB warpage, and may generate stress in the solder joints.

The ACEPACK SMIT has a thermal pad facing upward in order to accept a heatsink. Instead of other SMD power packages, which have a thermal pad soldered onto the PCB.

The amount of heat that transferred across the components leads is negligible compared to the heat flow through the heatsink. As a consequence, PCB traces design have almost no influence on the thermal performance of the application.

Figure 6. Recommended footprint (mm)

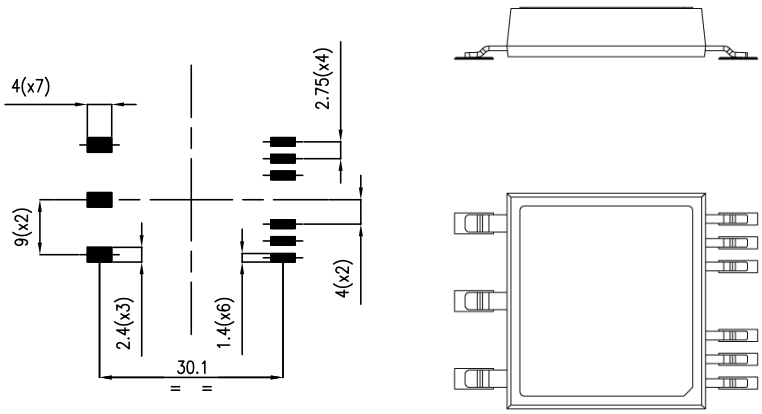
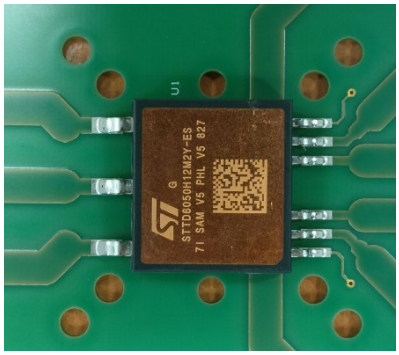


Figure 7. **ACEPACK SMIT sample mounted on test PCB**



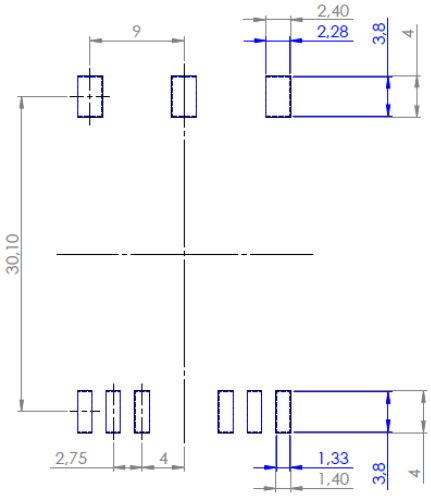
2.1.6 Screenprinting stencil

Stencil, screening the solder on the PCB, is commonly used in the industry. A stainless steel stencil should be used with a thickness of 150 µm to allow sufficient paste volume.

To ensure a safe and repeatable stencil printing process, some generic design rules for stencil design should be followed: stencil thickness should be >1.5, for example, and the aspect ratio between opening should be respected. It is not described here as no issue may be expected due to large pads dimensions.

ST recommends a stencil opening to footprint ratio of 90%, as shown on Figure 8 (stencil openings are drawn in blue dotted lines, while the PCB solderable pad is in black lines).

Figure 8. **Stencil opening recommendation**



The sidewalls of the stencil openings may be tapered approximately 5° to ease the release of the paste when the stencil mask is removed from the PCB.

2.1.7 Solder paste

We recommend using a solder paste with fine particles (type 3 or 4, meaning particle dimensions from 20 to 45 µm). And also a solder pastes containing halide-free flux ROL0 according to ANSI/J-STD-004.

Higher paste types (finer) can be used if you need to mount much smaller packages on the same PCB.

For lead-free solders SnAgCu, any SnAgCu alloy with 1% to 4% Ag and < 1% Cu should be convenient. STMicroelectronics used SnAg3Cu0.5 for its evaluations (LOCTITE LF318 97SCAG88.5 BU, no clean, Pb free solder paste).

2.1.8 Placement

Manual placement should be avoided, as the device must be placed parallel to the PCB surface in order not to squeeze the solder paste on one side.

There are no minimum placement force requirements since the weight of the device alone is sufficient to ensure a good contact with the solder paste.

Typical placement accuracy of pick and place machines is +/-50 µm. This is more than sufficient for such a large package (furthermore, the self-alignment effect caused by the surface tension of the liquid solder ensures the self-centering of the package).

If any components have to be placed on both PCB sides, the side with ACEPACK SMIT must be processed as last, as wetting forces could not hold the ACEPACK SMIT package during a second reflow.

2.1.9 Reflow profile

Forced convection oven is the preferred method for reflow.

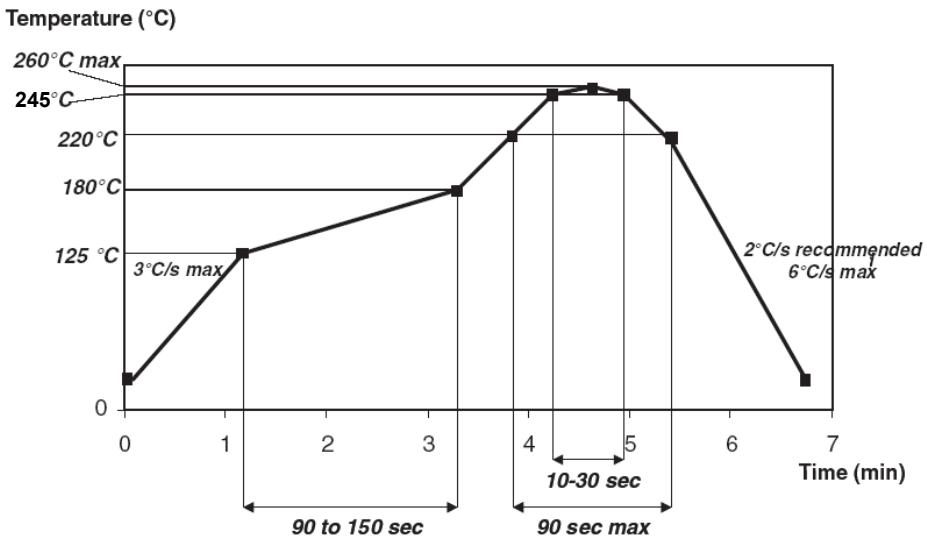
The soldering process causes high thermal stress to a semiconductor component. This has to be minimized to ensure a reliable and extended lifetime of the device.

The package is following IPC/JEDEC J-STD-020E requirements, and thus can be exposed to a maximum temperature of 245 °C for 10 seconds. Overheating during the reflow soldering process may damage the device, therefore any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical leadfree solder heating profiles (ST ECOPACK) are given in Figure 1 for mounting on an FR4 PCB.

Please refer to the IPC/JEDEC J-STD-020E standard for further information about “large” components definition.

Note: Soldering profile defined in the IPC/JEDEC J-STD-020E standard is used for reliability assessment. It describes the warmest profiles used for components mounting, and not the necessary temperatures to achieve good soldering.

Figure 9. Recommended soldering reflow profile



This profile is given as a starting point only. It must be adjusted depending on the PCB size and thickness, the overall weight, the position of the surrounding packages as well as on the reflow oven specification.

The following precautions have to be considered:

- Always preheat the device. The purpose of this step is to minimize the rate of temperature rise to less than 3 °C/sec in order to minimize the thermal shock on the components.
- Dry out the section, after preheating, to ensure that the solder paste is fully dried before starting the reflow step. This step also allows the temperature gradient on the PCB to be evened out. As the ACEPACK SMIT package is massive, soaking time is important in this case to ensure a homogeneous temperature distribution on the PCB.

Peak temperature should be at least 30 °C higher than the melting point of the solder alloy to ensure reflow quality. In any case, the peak temperature should not exceed 260 °C.

2.1.10 Wave soldering

Wave soldering is not recommended for the ACEPACK SMIT package.

The ACEPACK SMIT package is a surface mount package. The wave soldering is not the most suitable process to solder correctly the whole lead tip surface.

But the main reason is related to the package top side: due to the DBC exposed copper, and during the wave soldering, some Sn wets the copper surface, which necessarily generates topology on the package surface, as surface tensions generate a much thicker tin layer at the center of the package compared to the edge.

Consequently, this uneven surface generates additional thermal resistance between the package top surface and the heatsink (it requires the use of a thicker thermal compound or thermal pad layer).

3 Heatsink attachment to package

3.1 Thermal resistance

The thermal resistance of a semiconductor assembly is the parameter, which characterizes its resistance to the heat flow. The junction generates it during operation. A temperature exceeding the maximum junction temperature curtails the electrical performance and may damage the device.

The maximum dissipated power capability is:

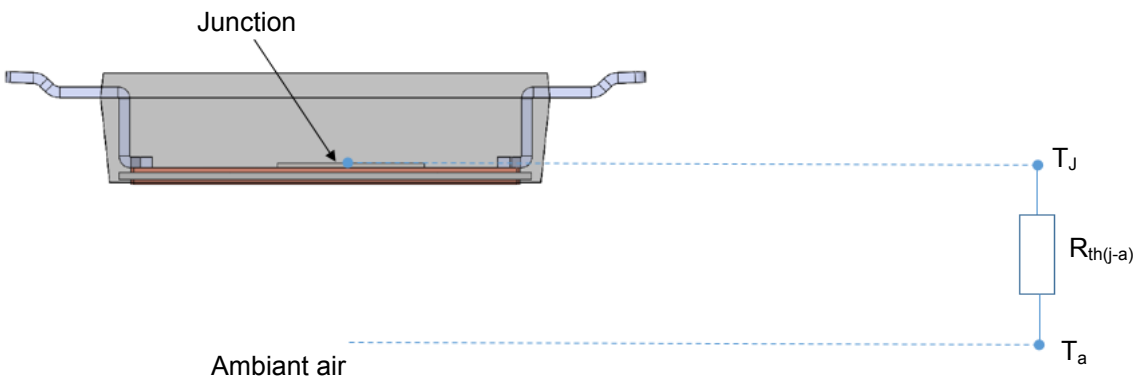
$$P_{max} = \frac{T_j max - Ta}{R_{th(j-a)}}$$

Where:

- T_j max is the maximum junction temperature of the semiconductor in °C
- T_a is the ambient air temperature in °C
- $R_{th(j-a)}$ is the thermal resistance between junction and ambient air/coolant in °C/W

The $R_{th(j-a)}$ value depends on the materials between the junction and ambient air.

Figure 10. Thermal equivalent diagram



3.2 Thermal path

The ACEPACK SMIT package is designed to have a heatsink pad located on the top of the device, in order to connect to a heatsink.

This pad is electrically insulated from all package pins (RMS 3400 V minimum insulation). So, the heatsink does not necessarily require further electrical insulation from accessible conductive surfaces.

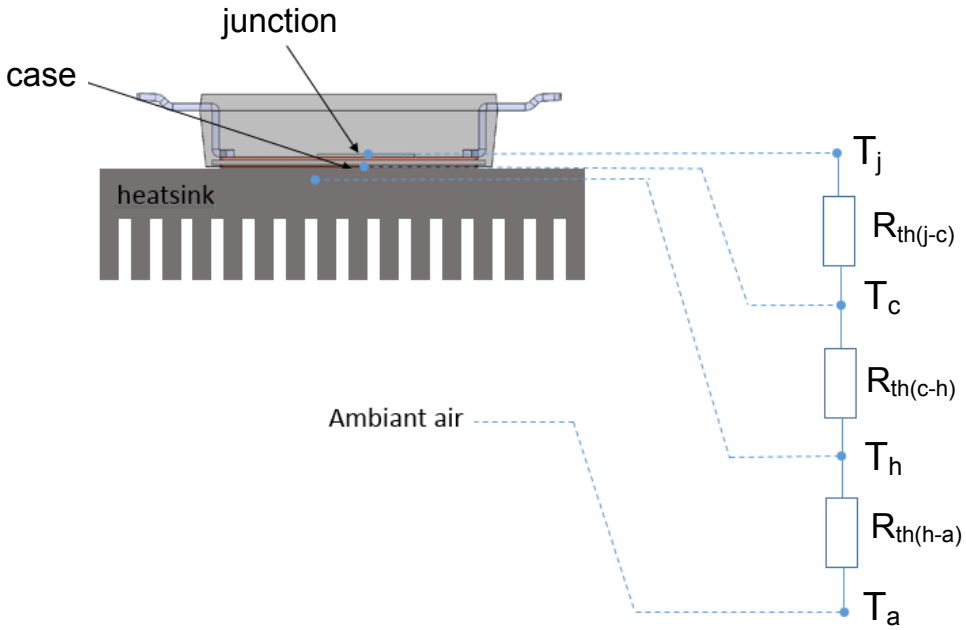
The ACEPACK SMIT package is designed to ensure a thermal path from the die junction (where the heat is generated) to the thermal pad. It is kept as high thermally conductive as possible.

The purpose of the heatsink is to keep the thermal path resistance from the device to the ambient environment. That receives this heat (whether it is water or air) also as low as possible.

Therefore, the total thermal resistance from junction to ambient is the sum of:

- The junction-to-package thermal resistance, defined by the package design ($R_{th(j-c)}$).
- The thermal resistance of the thermal pad or compound used between the device and the heatsink ($R_{th(c-h)}$)
- The thermal resistance of the heatsink between the thermal pad/compound and the ambient environment ($R_{th(h-a)}$).

Figure 11. Thermal equivalent diagram with external heatsink



3.3 Thermal compound

The purpose of this thermal compound is to ensure a good contact between the device surface and the heatsink. This purpose is to provide also in specific cases electrical insulation between the package and the heatsink. In the case of customer application requirements, the insulated thermal interface can be implemented. As an example, it reinforces insulation, in addition to the internal ACEPACK SMIT one.

However, to minimize thermal resistance, it is critical to ensure that the two surfaces of the device and the heatsink are in perfect contact. Due to surfaces roughness and planarity imperfections, a thin layer of thermal compound between the two layers to fill the gaps between the two surfaces is required.

Many compounds are commercially available and may provide this function. STMicroelectronics has successfully evaluated the HTCP20S compound from Electrolube.

3.4 Thermal pad

In the case where several ACEPACK SMIT devices share the same heatsink surface, some gaps could appear between the top surface packages and the heatsink surface. This is due to a height difference between the packages and parallelism issues.

These small gaps increase significantly the contact resistance with the heatsink, and a simple compound may not reliably fill them.

In this case, it is safer to use soft thermal pads with a thickness able to compensate the geometrical issues.

As there is no requirement for electrical insulation, electrically conductive material may be used, which offers a better thermal conductivity than electrically insulating materials.

3.5 Heatsink

Different types of heatsinks provide different $R_{th(j-a)}$ values, leading to limit the maximum allowed power dissipation in the dice for a fixed ambient/coolant temperature.

Two main categories of heatsinks may be used:

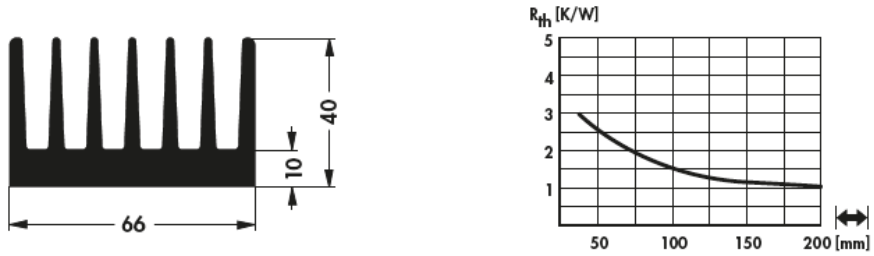
- **Heatsinks air cooled by natural convection:** This solution provides the poorest thermal dissipation, but is the simplest solution to design and includes the cheapest materials. Heatsink is usually an extruded aluminum part, attached to the cooling side of the device. The heatsink thermal performance is proportional to the difference between the package temperature and the air temperature used for cooling. It is also proportional to the area of the exchange surfaces (aluminum to air). Higher heatsink fins and longer/larger extruded profiles, lower the thermal resistance. A sufficient room above the heatsink is required for a sufficient convection of the ambient air.

Heatsink dimensioning estimation example:

For a given thermal resistance $R_{th(j-c)}$ of 0.5 °C/W, we get from the diagram that a 2.5 °C/W resistance is expected from case to ambient air $R_{th(c-a)}$. This if a 50 mm long heatsink is used (refer to Figure 12. Passive heatsink Fischer Elektronik SK100 50 datasheet). So, a total of 3.2 °C/W assuming 0.2 °C/W thermal resistance from thermal compound.

If we consider a maximum junction temperature of 120 °C and an air temperature of 40 °C, this allows a maximum dissipation of $(T_j - T_a)/R = 80/3.2 = 25$ W.

Figure 12. Passive heatsink Fischer Elektronik SK100 50 datasheet

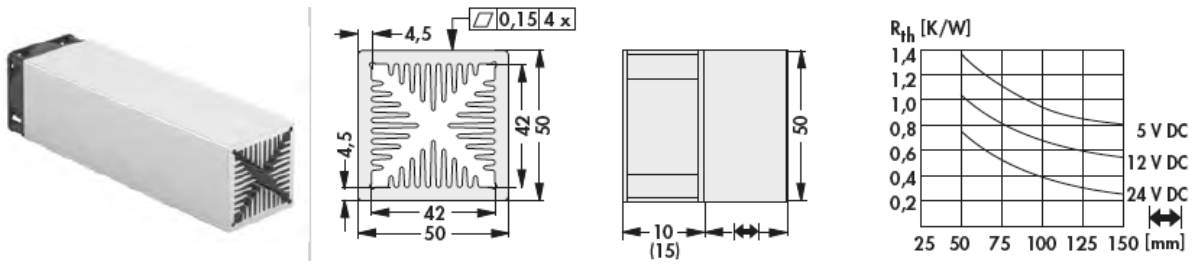


- **Heatsinks air cooled by forced convection:**Forcing the air flow on the above heatsinks drastically improve the heat exchange, up to several times, depending on the air flow. Tubular heatsinks can be used to improve the heat exchange as the air flow is guided along a large exchange area.

Heatsink estimation example:

Using the below heatsink type (refer to Figure 13. Forced convection heatsink Fischer Elektronik LAM5 100 datasheet), with a length of 100 mm and a 24 V fan, we can expect a thermal resistance of 0.4 °C/W. It gives a maximum theoretical allowed dissipation of 80/0.4=200 W in the same conditions.

Figure 13. Forced convection heatsink Fischer Elektronik LAM5 100 datasheet



These heatsink designs are provided as examples, but of course many other designs are available. Application designers can use different heatsinks like the liquid cooled heatsink, which provide significantly better thermal performances.

3.6 Heatsink attachment

3.6.1 Attachment requirements

A sufficient pressure must be applied between the package and the heatsink to achieve a good thermal contact and a maximum heat transfer. Thermal compound can be added to help filling the potential roughness gaps between the heatsink and the package. But pressure is still needed to squeeze the compound and reduce the space between the two parts. At the expense of the overall thermal performances degradation, we can use, alternatively, a smooth thermal interface films or gap filler.

As far as possible, stress on the PCB and the leads should be avoided, as thermal cycles occurring during the product life could induce cracks in the solder joints.

The PCB must be mechanically linked to the heatsink, to avoid vibrations.

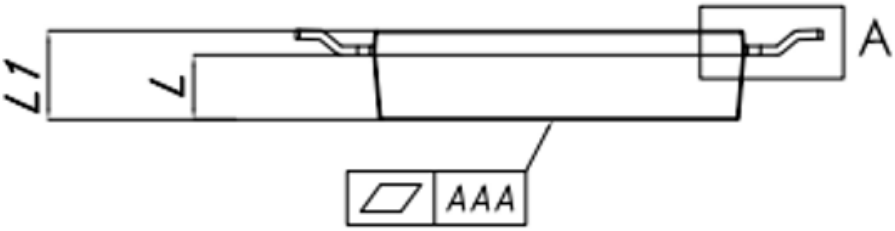
3.6.2 Issue

The package top surface must touch the heatsink surface, and simultaneously the PCB surface must be attached to the heatsink.

If several packages are used on a single PCB, they must simultaneously contact the heatsink.

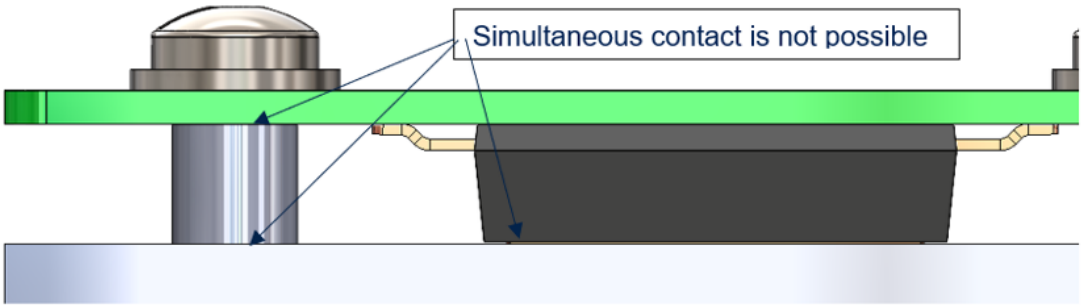
As there is a tolerance on the package height and heatsink/housing manufacturing, this is impossible without flexibility or adjustment in the final assembly.

Figure 14. PCB profile view



ACEPAKSMIT height tolerance: L1 = 5.5 mm +/- 0.1.

Figure 15. Contacts view



3.6.3 TIMs and gap fillers

The ACEPAK SMIT package has very high thermal performances. Unless necessary (for example to increase creepage distance), TIMs should be avoided as they greatly decrease the overall thermal conductivity of the system.

Gap fillers degrade the performances, especially when used in large gaps.

The best results are achieved using thermal grease alone to compensate for the surface roughness, and a sufficient pressure between the package and the heatsink.

3.6.4 Simple screw attachment

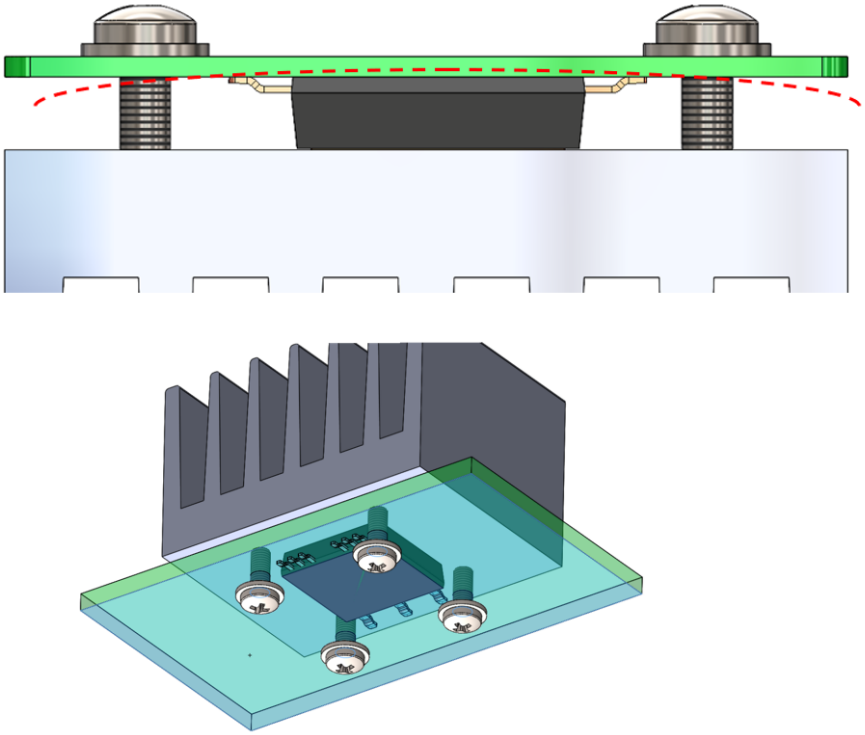
The easiest way to mount the heatsink on a PCB is by using screws. STMicroelectronics recommends using four screws.

For example, four M4 screws are located on corners of a 30x30 mm square pattern, centered around the ACEPACK SMIT package.

However, this method may generate mechanical stress on the assembly, leading to PCB bending, even with limited torque applied to the screws.

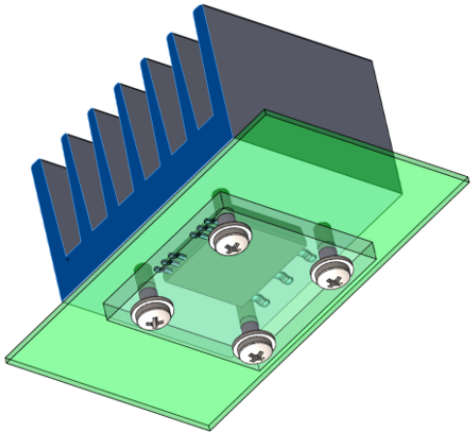
PCB design and material may also impact the stiffness of the PCB. To reduce these parameters impact, we suggest applying the above mounting conditions only if the PCB is very thick (above 4 mm).

Figure 16. Simple heatsink attachment



In order to limit the PCB warpage, a counter-plate can be attached on the back of the PCB, refer to Figure 18. Any material can be used. The presence of tracks in contact with the counter-plate is not allowed using metal.

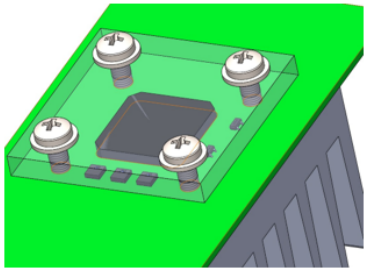
Figure 17. **Heatsink assembly with counterplate**

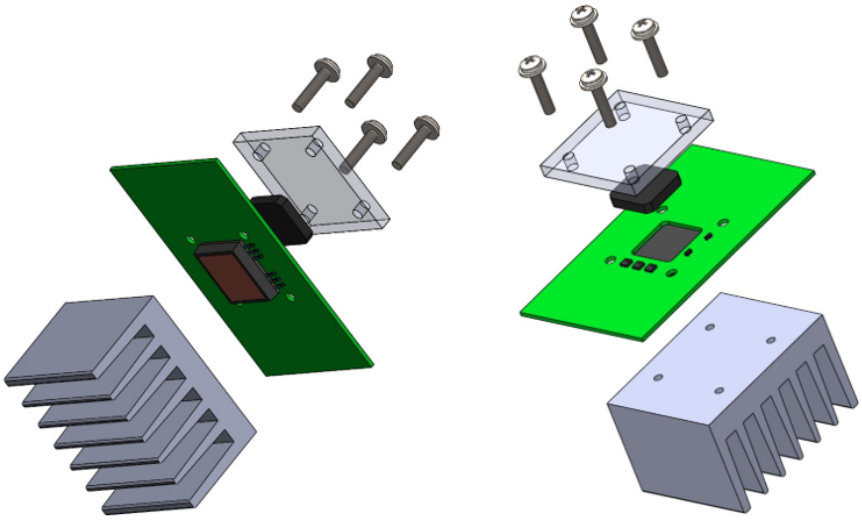


To avoid the stress applied on the PCB, the following assembly is recommended: A square hole in the PCB located below the ACEPACK SMIT device holds a spacer slightly thicker than the PCB (for example 2 mm for a 1.6 mm PCB). The counter-plate apply pressure directly on the package backside without pressing on the PCB itself.

Using a sufficiently thick spacer can limit significantly the impacted area on the PCB back side, and able to place components on the bottom side of the PCB (see Figure 18). It depends on customer requirements.

Figure 18. **Heatsink assembly with counterplate and spacer + hole in PCB**





3.6.5 Spacers considerations

Adding spacers limits the PCB warp when the screws are tightened.

However, the height of the spacers is critical: too low, the remaining stresses on the PCB and leads are important. Too high, there is no contact between the package and the heatsink.

Figure 19. Spacers lower than package height

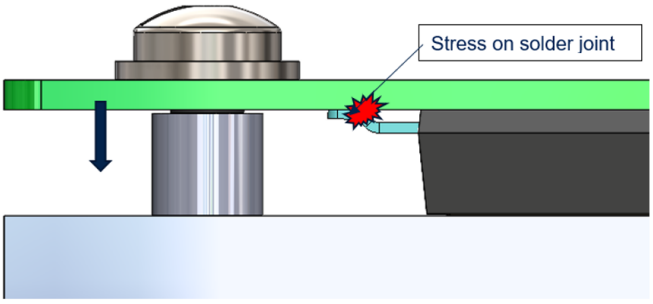
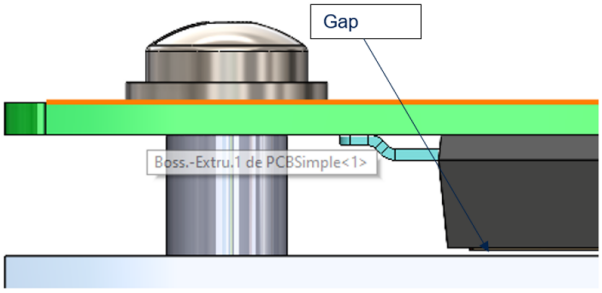


Figure 20. Spacers higher than package height



If zero stress on solder joints is a requirement, the spacer height should be calculated to have a 0+ gap with the worst case tolerances (spacer height = max package height). As a worst-case gap equal to the full package height range is to be expected, a gap filler is mandatory. This solution keeps the stress at the minimum possible level, but have a lower thermal performance.

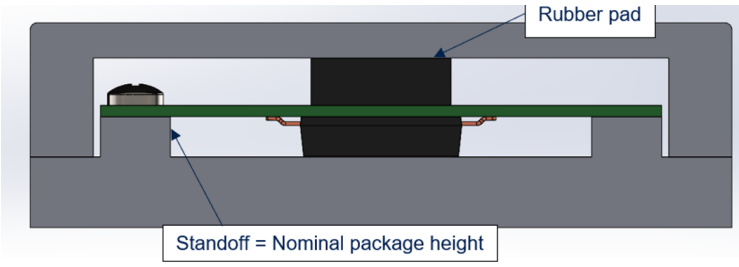
Alternatively, the spacer height can be set to a value slightly lower than the minimum package height. In this case, no gap occurs, and a simple thermal grease can be used. However, this causes stress on the solder joints when the package has the maximum possible height.

Using the housing cover to apply pressure

The cover of the device housing can be used to apply some pressure between the package and the heatsink. A flexible material must be used as a spring to accommodate the possible tolerances.

The shorter the distance between the package and the PCB mounting points, the higher is the remaining stress on the solder joints.

Figure 21. Housing cover

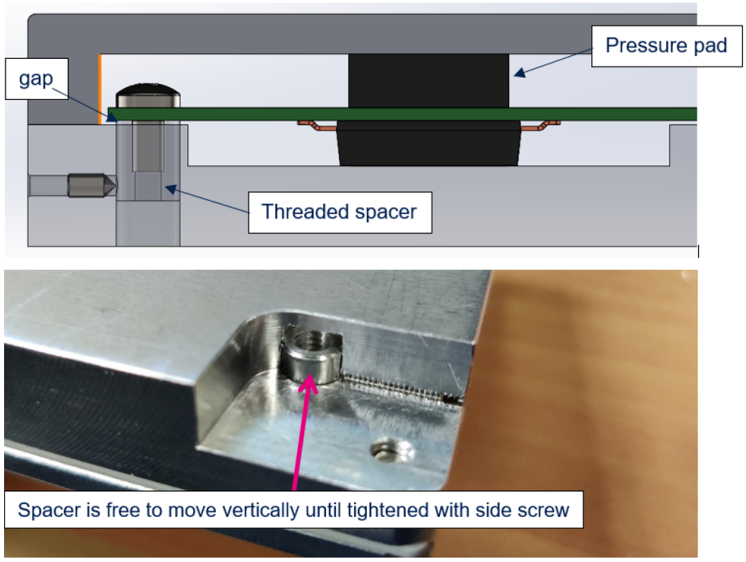


Adjustable PCB mounting for zero stress on package leads

Using adjustable PCB attachments allows the PCB to have the package topside touching the heatsink surface without creating stress on the PCB:

1. Threaded spacers are mounted on the PCB
2. The spacers are inserted into mounting holes drilled in the heatsink
3. The PCB remains free to move vertically while the cover is mounted. Pressure is applied on the device
4. Spacers are immobilized after cover mounting using, for example, headless screws.

Figure 22. Adjustable PCB mounting



Effect of the stress on the solder joints.

There is no way to suppress completely the stress on the solder joints if several packages are soldered on the same PCB, like on most designs. Whether this stress may affect the solder joints reliability is a common concern.

The following experiment has been carried out to check a worst-case scenario.

- A controlled stress condition has been created, by applying a pronounced deformation to the PCB
- Thermal cycling was applied to the parts under stress. (4 parts, 1000 cycles, -55/+150 °C)
- Electrical tests and analysis (SAM, cross section) of the solder joints has been performed to check the possible damages to the solder joints.

Test conditions:

ACEPAKSMIT packages were mounted on standard FR4 circuit boards, using the recommended footprint.

The PCB thickness was 1.6 mm.

The PCB has been attached to a heatsink using spacers 0.3 mm shorter than the package height, which is much more than the expected mechanical tolerances in a standard application.

Pressure was applied to the backside of the PCB using a screw until the package came in contact with the heatsink.

Spacers were placed on a 40x40mm pattern centered on the package.

Figure 23. **ACEPAKSMIT package mounted with a 0.3mm gap (pressure screw loosened)**

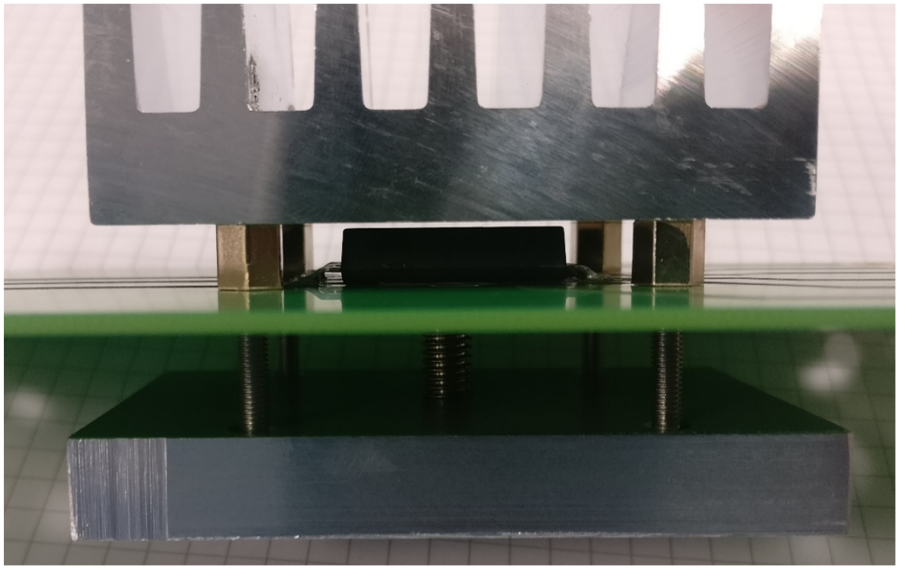
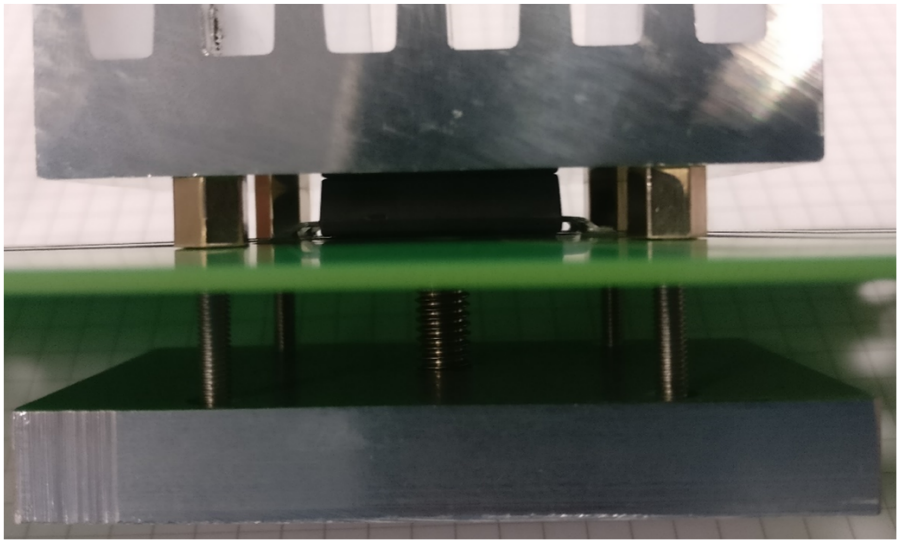


Figure 24. **ACEPAKSMIT package mounted with an initial gap of 0.3mm (pressure screw tightened)**



Results after cycling:

- All parts tested electrically OK. No drift in any parameter was encountered
- No visible difference between the stressed parts and unstressed parts solder joints. (SAM, X-ray, cross sections)
- As the mechanical tolerances in real applications should be much tighter, this “worst case” evaluation indicates that the remaining stress in the solder joints should be acceptable for most of the applications.

4 Thermal resistance measurements

4.1 Product description

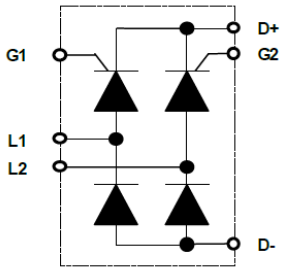
Thermal resistance measurements were performed on product STTD6050H-12M2Y, which is a single-phase SCR-diode bridge rectifier.

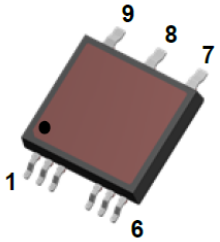
This product is composed of four silicon dice (two diodes and two thyristors), and is described here below.

Both diodes are identical, as well as both thyristor dice. The coupling thermal resistance between each die can be neglected. Even if the dice are identical. This is due to the DBC layout (mainly the dimension of the copper pad on the DBC ceramic), we can notice small $R_{th\ junction–case}$ differences between the dice.

In the following pictures, we named thyristor dice (T1, T2) as well as diode dice (D1, D2).

Figure 25. STTD6050H-12M2Y draft product description





Pin #	Name	Description
1	NC	Not connected
2	G1	Gate SCR1
3	G2	Gate SCR2
4	D-	Output minus
5	D-	Output minus
6	D-	Output minus
7	L2	AC Line 2
8	L1	AC Line 1
9	D+	Output plus

Application

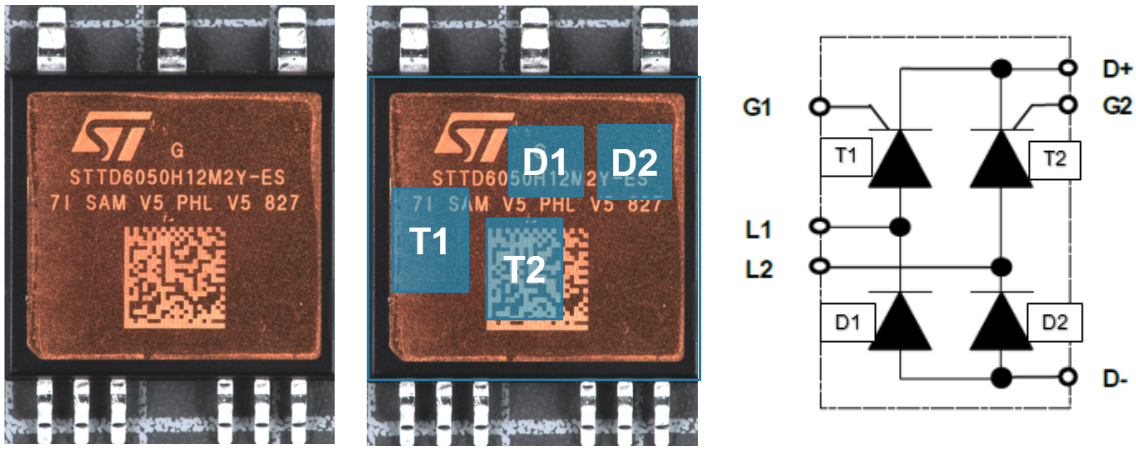
- Single phase controlled bridge rectifier
- On-Board and Stationary Chargers
- AC DC converter for SMPS or motor drive
- AC current from 32 A up to 80 A_{RMS}

Features

- Embed two TN6050H-12 and two STBR6012
- 1200 V symmetrical blocking voltage
- 150°C max. junction temperature T_J
- 1000V/µs noise immunity / static dV/dt
- SMD with isolated top cooled tab
- Insulated tab-to-leads package,
  - UL recognition to build
- Connection pins opposite to cooling side
- ECOPACK®2 compliant component
- AEC-Q101 Automotive grade
- Meet IEC 60664-1
  - 250V_{AC} pollution degree 3
  - 600V_{AC} pollution degree 2

Symbol	Value	Unit
$I_{F(RMS)}$, $I_{T(RMS)}$	60	A
V_{DRM} , V_{RRM}	1200	V
V_{DSM} , V_{RSM}	1400	V
I_{GT}	50	mA
T_J	150	°C

Figure 26. Optical and X-ray view from the top heatsink metallization tab



4.2 Thermal resistance junction – case $R_{th(j-c)}$ measurement

The same principle as for $R_{th(j-a)}$ applies here, but $R_{th(j-c)}$ defines the temperature difference between the silicon junction and package case.

So, $R_{th(j-c)} = (T_j - T_c)/Pdissipated$.

For each die, a thermal calibration is performed (to define a correlation between junction temperature and forward voltage of the diode, or V_T of the thyristor).

When the defined conditions are applied (Pdissipated is applied), we can then compute T_j.

The package case temperature is measured, which allows us to compute the $R_{th(j-c)}$ of each silicon die. Usually the packages are placed on “infinite” heatsink, and T_{case} is measured through a thermocouple placed below each die.

The purpose of this document is to provide information about $R_{th(j-a)}$.

For the $R_{th(j-a)}$ measurement, we cannot place a thermocouple below each die.

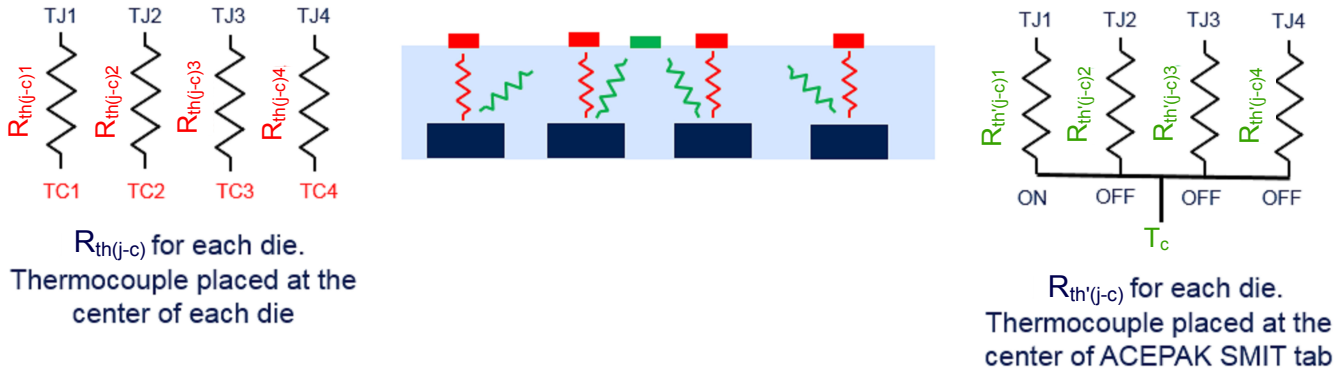
As previously mentioned, due to the excellent performance of the package, the coupling thermal resistance between the dice is negligible.

The consequence is that a thermocouple placed at the center of the case measures temperature, which is quite different from a thermocouple placed below each die.

$R_{th'(j-c)}$ is defined as the $R_{th(j-c)}$ with case temperature measured at the center of the package.

When measurements are performed, it is important to check the $R_{th'(j-c)}$ if we intend to compare $R_{th(j-a)}$ measurements with $R_{th(j-c)}$ measurements.

Figure 27. $R_{th(j-c)}$ and $R_{th'(j-c)}$ definitions



The table below lists the typical values measured for $R_{th(j-c)}$ and $R_{th'(j-c)}$.

Table 2. $R_{th(j-c)}$ measurements

		Min	Avg	Max
$R_{th(j-c)}$	D1	0.49	0.50	0.52
	D2	0.52	0.54	0.56
	T1	0.57	0.64	0.68
	T2	0.54	0.60	0.65
$R_{th'(j-c)}$	D1	0.75	0.77	0.77
	D2	0.93	1.03	1.18
	T1	0.89	0.98	1.02
	T2	0.64	0.70	0.72

$R_{th'(j-c)}$ has been also measured for different forces applied on the package (on one thyristor and one diode).

We observe in this case that the thermal resistance starts to be stable when the force applied on the package is above 40N.

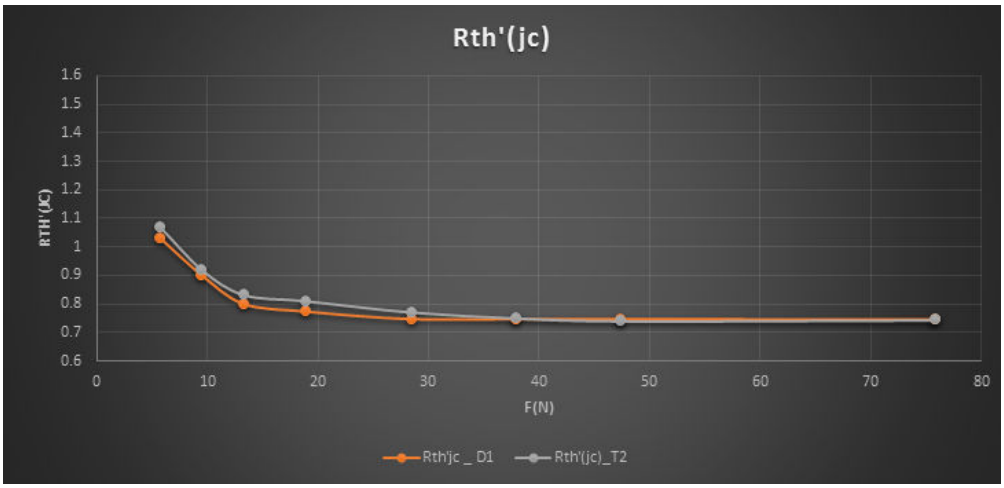
The package experiences a force by a piston with a diameter of 7 mm. So, 40N is equivalent to a pressure of 1.04N/mm² on the ACEPACK SMIT package.

This measurement is performed by placing the package on a cooled heatsink (with controlled temperature). Then, the contact between the top surface package and the water ensure the heatsink.

We know that the additional thermal resistance brought by water presence may reach up to 0.1 °C/W.

The results shown here below are aligned with previous measurements and simulations performed, with 0.1 °C/W uncertainty.

Figure 28. $R_{th'(j-c)}$ function of force applied on package

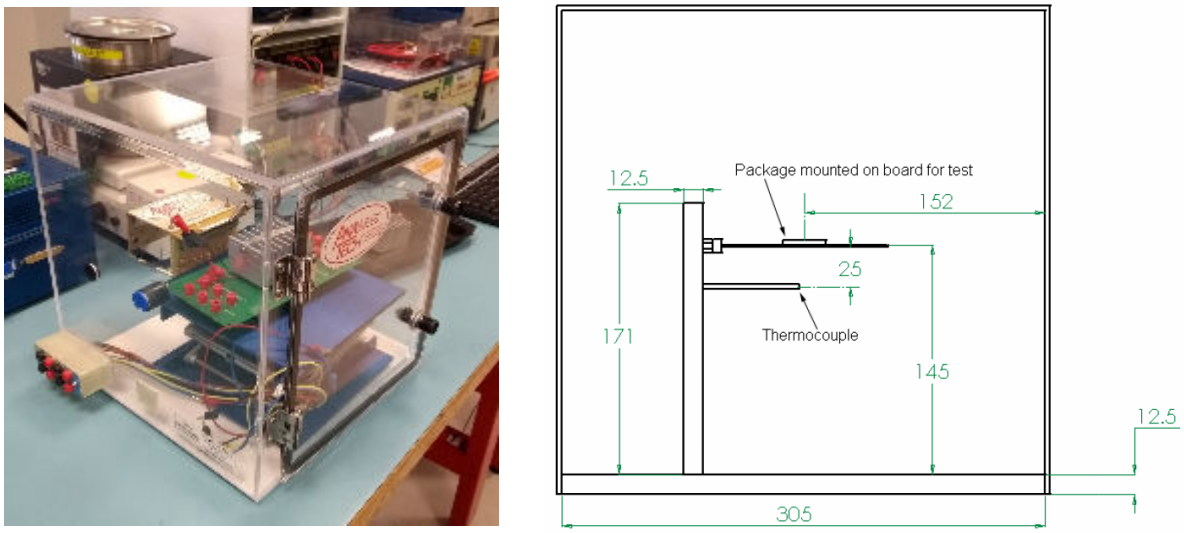


4.3 Measurements of junction to ambient thermal resistance

$R_{th(j-a)}$ measurements have been performed using a passive heatsink.

The test conditions used were the standard ones (using normalized still air chamber EVN-12, JEDEC JSD51-2).

Figure 29. Air chamber drawing and picture

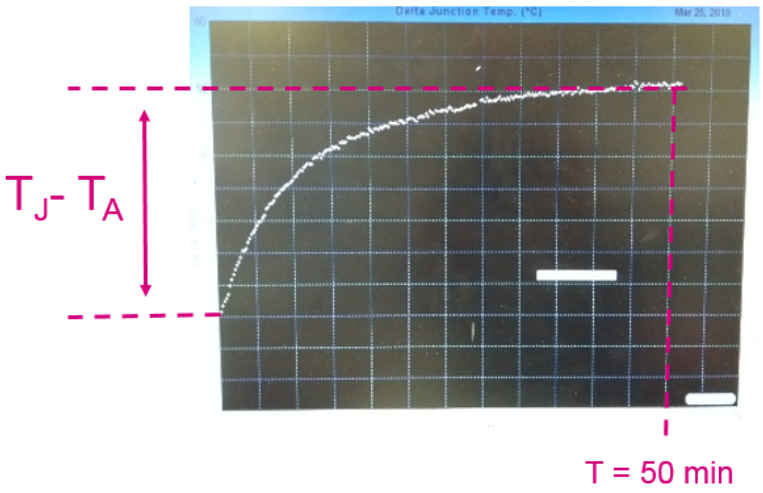


Only diode D1 was conducting when the $R_{th(j-a)}$ was characterized, by measuring its junction temperature.

Temperature in the laboratory was 25 °C and the supply current flowing through ID1 was 15 A with a heating time of 1 hour.

The diode was cooled down to 25 °C between each measurement.

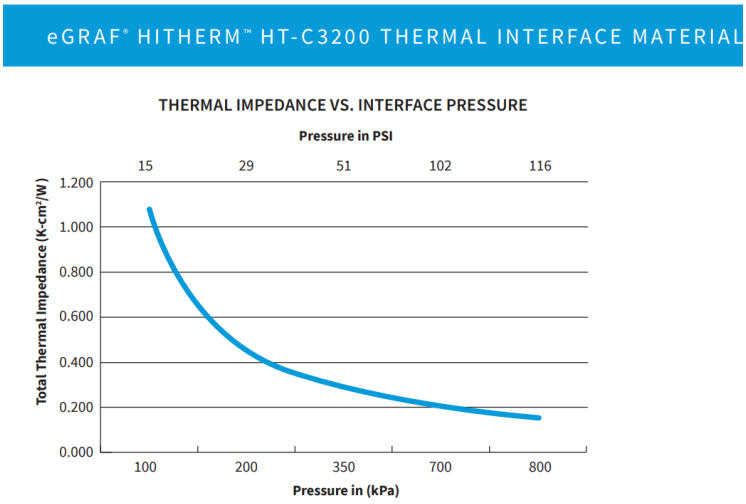
Figure 30. Junction temperature measurement



We used a Fischer Electronik passive heatsink (reference SK100 50, with Rth of 2.5 °C/W according to the supplier datasheet). Then we evaluate two thermal interface materials:

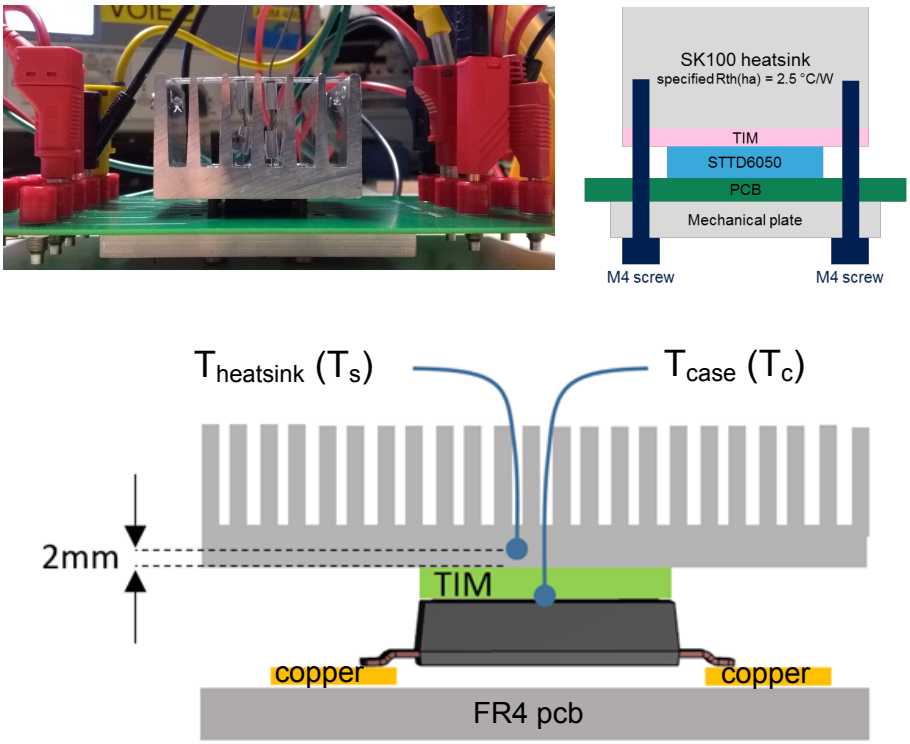
- a thermal compound from Electrolube (reference HTCP20S, which is electrically non conductive, with 2.5 W/mK thermal conductivity)
- a thermal pad from Neograf (reference HT-C3200, with thermal conductivity provided in here below table)

Figure 31. Neograf HT-C3200 thermal properties



The ACEPACK SMIT package was mounted on PCB, with the heatsink attached through the use of M4 screws, and thermocouples were placed on the case, and inside of the heatsink.

Figure 32. $R_{th(j-a)}$ measurements description



$R_{th(j-a)}$ was computed according to screw torque variation.

Above 0.4N.m torque, $R_{th(j-a)}$ becomes stable, which indicates that the pressure applied on the thermal interface material is good enough.

We recommend a typical screw torque of 1N.m (0.8N.m minimum) in order to ensure a correct mounting process. This with the M4 screws, as an indicative value (as various parameters like screw material, heatsink material, etc. may influence the required torque).

$R_{th(j-a)}$ can be computed as the sum of $R_{th(j-c)}$, Rth(c-h), and $R_{th(h-a)}$, with $R_{th(c-h)}$. This is representing the thermal resistance of the TIM, and $R_{th(h-a)}$ as the thermal resistance of the heatsink.

$R_{th(j-c)}$ was measured at 0.8 °C/W.

According to the inputs provided by the materials suppliers, $R_{th(c-h)}$ can be estimated around 0.3 °C/W for thermal compound (HTCP) and 0.1 °C/W for thermal pad (HT-C3200).

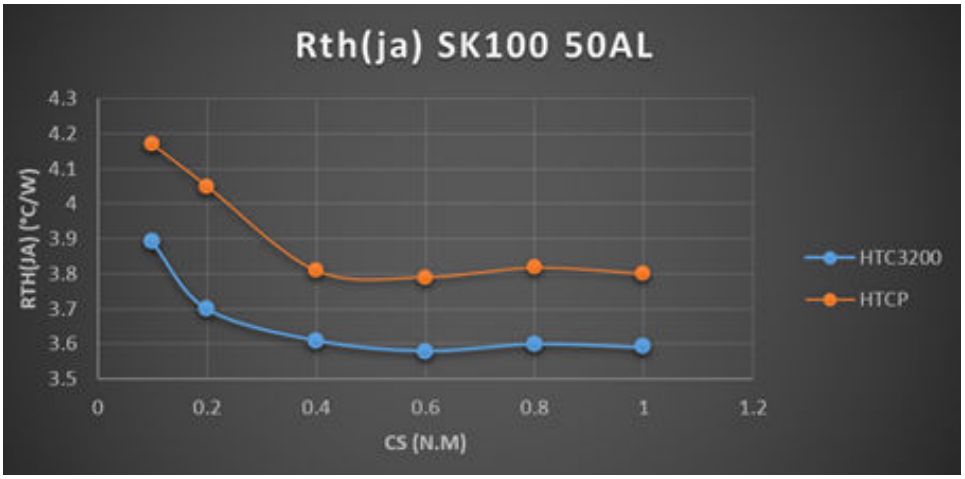
The heatsink was supposed to have a $R_{th(c-h)}$ of 2.5 °C/W according to the supplier datasheet.

We should have found 3.6 °C/W (for the configuration with thermal compound interface), and we measured 3.8 °C/W.

We consider our measurement accuracy is around +/-0.1 °C/W, so this experimental result, even if not perfectly aligned with the suppliers datasheets, seems reasonable.

As the gap between two TIM is confirmed to be 0.2 °C/W, there is a significant possibility that the heatsink datasheet is slightly optimistic.

Figure 33. $R_{th(j-a)}$ versus torque screw



We would like to remind the reader that these results are valid with a selected passive heatsink. It is clear that a better thermal resistance performance may be obtained by selecting a more performing heatsink.

5 Conclusion

This paper provides recommendations and metrics information in order to design with the ACEPACK SMIT package in suitable mounting conditions.

Experimental results show that the thermal performance fulfills the requirements with an individual device junction-to-case resistance Rth(j-c) of about 0.5 °C/W including the internal DBC insulator and a global junction-to-ambient resistance Rth(j-a) as low as 3 °C/W in the entire air cooling system while this last resistance Rth(j-a) can be reduced to 1 °C/W using liquid forced cooling methods.

Therefore, the ACEPACK SMIT embeds power devices rated from 50 A to 200 A with a blocking voltage up to 1200 V; this will help to design power systems up to 20 kW, for instance in battery chargers, motor drive and power converters for data centers and renewable energy.

Even if not extensively described in this application note, for more thermally demanding applications, some forced convection heatsinks or forced liquid cooled heatsinks extend the usage of the ACEPACK SMIT power module.

Revision history

Table 3. Document revision history

Date	Revision	Changes
04-Nov-2019	1	Initial release.
21-Mar-2023	2	Added Section 3.6 Heatsink attachment chapter. Minor text changes.

Contents

1 **Package information** 2
1.1 Package dimensions and packing 2
1.2 Moisture sensitivity 4
1.3 Component solderability 4
2 **Printed circuit board assembly** 5
2.1 Printed circuit board recommendations 5
2.1.1 Material 5
2.1.2 Copper 5
2.1.3 PCB pad design 5
2.1.4 PCB solderable metallization 6
2.1.5 Footprint 6
2.1.6 Screenprinting stencil 7
2.1.7 Solder paste 8
2.1.8 Placement 8
2.1.9 Reflow profile 8
2.1.10 Wave soldering 9
3 **Heatsink attachment to package** 10
3.1 Thermal resistance 10
3.2 Thermal path 10
3.3 Thermal compound 11
3.4 Thermal pad 11
3.5 Heatsink 12
3.6 Heatsink attachment 13
3.6.1 Attachment requirements 13
3.6.2 Issue 13
3.6.3 TIMs and gap fillers 14
3.6.4 Simple screw attachment 14
3.6.5 Spacers considerations 16
4 **Thermal resistance measurements** 19
4.1 Product description 19
4.2 Thermal resistance junction – case $R_{th(j-c)}$ measurement 20
4.3 Measurements of junction to ambient thermal resistance 22
5 **Conclusion** 26
Revision history 27

List of figures

Figure 1. ACEPACK SMIT package overview . . . 1
Figure 2. ACEPACK SMIT package outline . . . 2
Figure 3. ACEPACK SMIT picture in carrier tape . . . 3
Figure 4. Moisture sensitivity levels . . . 4
Figure 5. Solder mask design . . . 5
Figure 6. Recommended footprint (mm) . . . 6
Figure 7. ACEPACK SMIT sample mounted on test PCB . . . 7
Figure 8. Stencil opening recommendation . . . 7
Figure 9. Recommended soldering reflow profile . . . 8
Figure 10. Thermal equivalent diagram . . . 10
Figure 11. Thermal equivalent diagram with external heatsink . . . 11
Figure 12. Passive heatsink Fischer Elektronik SK100 50 datasheet . . . 12
Figure 13. Forced convection heatsink Fischer Elektronik LAM5 100 datasheet . . . 12
Figure 14. PCB profile view . . . 13
Figure 15. Contacts view . . . 13
Figure 16. Simple heatsink attachment . . . 14
Figure 17. Heatsink assembly with counterplate . . . 15
Figure 18. Heatsink assembly with counterplate and spacer + hole in PCB . . . 15
Figure 19. Spacers lower than package height . . . 16
Figure 20. Spacers higher than package height . . . 16
Figure 21. Housing cover . . . 16
Figure 22. Adjustable PCB mounting . . . 17
Figure 23. ACEPAKSMIT package mounted with a 0.3mm gap (pressure screw loosened) . . . 18
Figure 24. ACEPAKSMIT package mounted with an initial gap of 0.3mm (pressure screw tightened) . . . 18
Figure 25. STTD6050H-12M2Y draft product description . . . 19
Figure 26. Optical and X-ray view from the top heatsink metallization tab . . . 20
Figure 27. $R_{th(j-c)}$ and $R_{th'(j-c)}$ definitions . . . 21
Figure 28. $R_{th'(j-c)}$ function of force applied on package . . . 22
Figure 29. Air chamber drawing and picture . . . 22
Figure 30. Junction temperature measurement . . . 23
Figure 31. Neograf HT-C3200 thermal properties . . . 23
Figure 32. $R_{th(j-a)}$ measurements description . . . 24
Figure 33. $R_{th(j-a)}$ versus torque screw . . . 25

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved