Three output isolated flyback converter evaluation board with the VIPer26K, designed for the STCOMET smart meter and PLC system

Introduction

The STEVAL-VP26K01F three output isolated flyback converter evaluation board is based on the VIPER267KD HV converter and is specifically designed to supply the STCOMET smart meter and powerline communication system.

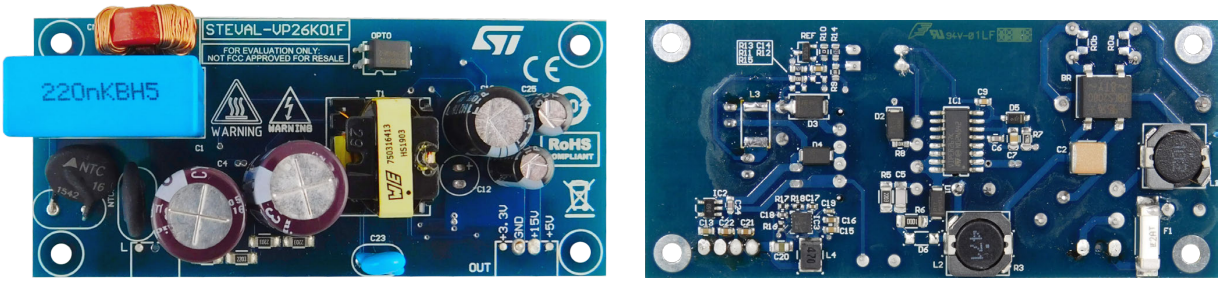
The VIPER267KD is an offline high-voltage converter with a 1050 V avalanche-rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, current limiting with a 700 mA fixed set point, on-board soft-start, safe auto-restart after a fault condition and low standby power.

The power supply provides 15 V at 550 mA_{RMS} (700 mA peak) to supply the powerline modem (PLM) and the analog circuitry, as well as post-regulated 5 V at100 mA and 3.3 V at 200 mA supplies for digital circuitry and other low voltage parts, which are generated by a dedicated DC/DC converter connected to the 15 V rail.

The power supply is designed to operate over a wide 90 V_{AC} to 264 V_{AC} input voltage range, but can also withstand a maximum AC main up to 440V_{AC} and even continue to function (with limited performance) with incorrect phase-to-phase connections in a three-phase network.

The board can be used in a standalone configuration for a standard meter platform, or in conjunction with the dedicated EVLKSTCOMET10-1 development kit; the PCB is specially designed to fit inside a real meter.

Figure 1. STEVAL-VP26K01F evaluation board top and bottom



1 Features and specifications

Table 1. **STEVAL-VP26K01F electrical specifications**

Parameter	Min.	Typ.	Max
Operative AC Main Input voltage	90 V_{AC}	-	264 V_{AC}
Overvoltage AC main	-	-	440 V_{AC}
Mains frequency	50 Hz	-	60 Hz
Output Voltage 1 – VOUT1	14 V	15 V	16 V
Output Current 1 – IOUT1	10 mA	-	550 mA (rms)
	-	-	700 mA (peak)
Output Voltage 2 – VOUT2	4.75 V	5 V	5.25 V
Output Current 2 – IOUT2	10 mA	60 mA	100 mA
Output Voltage 3 – VOUT3	3.1 V	3.3 V	3.5 V
Output Current 3 – IOUT3	-	100 mA	200 mA
Maximum peak power	-	-	11.66 W
Maximum rms power	-	-	9.4 W
Efficiency at full load	-	78.7%	-
Ambient operating temperature	-40 °C	-	85 °C

1.1 Schematic diagrams

Figure 2. **STEVAL-VP26K01F schematic - main PSU**

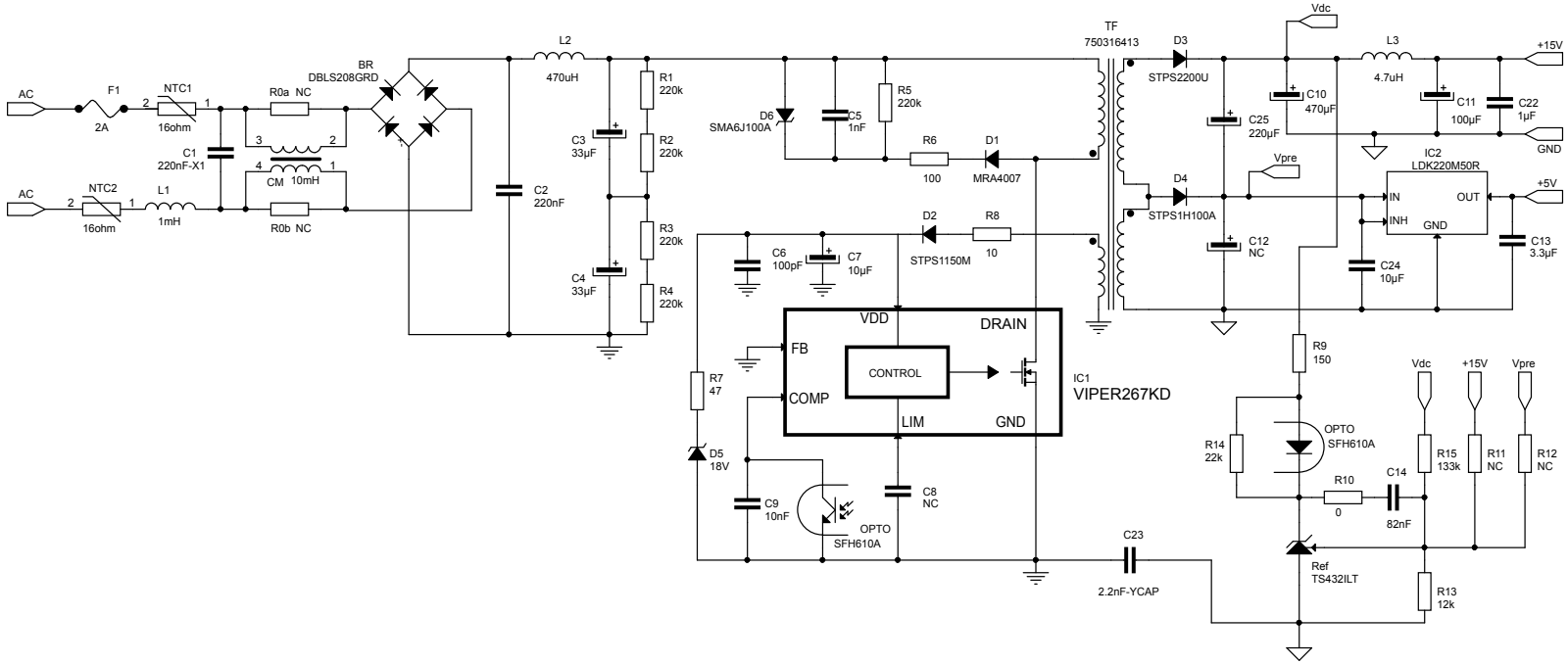
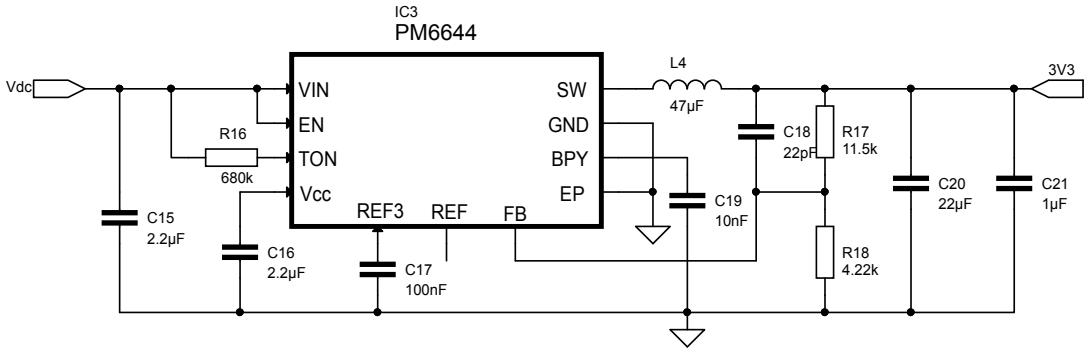


Figure 3. **STEVAL-VP26K01F schematic - dedicated DC/DC for 3V3 rail**



1.2 Bill of materials

Table 2. **STEVAL-VP26K01F bill of materials**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	R0a	-	not mounted	-	-
2	1	R0b	-	not mounted	-	-
3	5	R1, R2, R3, R4, R5	220kΩ ±5% - 0.33W - 200V	Thick film resistor SMD	Panasonic	ERJ-P08J224V
4	1	R6	100Ω ±5% - 0.33W - 200V	Thick film resistor SMD	Panasonic	ERJP08J101V
5	1	R7	47Ω ±1% - 0.5W	Thick film resistor SMD	Panasonic	ERJP06F47R0V
6	1	R8	10Ω ±1% - 0.2W	Thick film resistor SMD	Panasonic	ERJP03F10R0V
7	1	R9	150Ω ±1% - 0.1W	Thick film resistor SMD	TE Connectivity	CRG0603F150R
8	1	R10	0Ω ±1% - 0.1W	Thick film resistor SMD	TE Connectivity	CRG0603ZR
9	1	R11	133kΩ ±1% - 0.1W	Thick film resistor SMD	Vishay	CRCW0603133KFKEA
10	1	R12	-	not mounted	-	-
11	1	R13	12kΩ ±5% - 0.1W	Thick film resistor SMD	Panasonic	ERJ3GEYJ123V
12	1	R14	12kΩ ±1% - 0.2W	Thick film resistor SMD	Panasonic	ERJP03F1202V
13	1	R15	-	not mounted	-	-
14	1	R16	680kΩ ±1% - 1/16W	Thick film resistor SMD	TE Connectivity	CRG0402F680K
15	1	R17	11.5kΩ ±0.1% - 0.1W	Thin film resistor SMD	TE Connectivity	CPF0402B11K5E1
16	1	R18	4.22kΩ ±0.1% - 0.1W	Thin film resistor SMD	TE Connectivity	RN73C1E4K22BTG
17	1	C1	220nF - 440Vac	Film X1 capacitor	Kemet	PHE844RD6220KR06L2
18	1	C2	220nF - 630V	MLCC capacitor	Murata	GRM55DR72J224KW01L
19	2	C3, C4	33µF - 350V	Elcap	Nichicon	UCY2V330MHD1TO
20	1	C5	1nF - 630V	MLCC	TDK	C3216C0G2J102JT
21	1	C6	100pF - 50V	MLCC	Murata	GRM1885C1H101JA01D
22	1	C7	10µF - 25V	MLCC	TDK	C2012X5R1E106K125AB
24	1	C9	10nF - 100Vdc	MLCC	Murata	GCM188R72A103KA37D
25	1	C10	470µF - 25V	Elcap low ESR	Rubycon	25ZLH470MEFC10X12.5
26	1	C11	100µF - 25V	Elcap 100uF-25V	Rubycon	25YXF100MEFC6.3X11
27	1	C12	-	-	-	Not connected
28	1	C13	3.3µF - 10V	MLCC	Murata	GRM188R61A335KE15D
29	1	C14	82nF - 50V	MLCC	KEMET	C0603C823K5RACTU
30	2	C15, C16	2.2µF - 35V	MLCC	TDK	C1608X5R1V225K080AC
31	1	C17	100nF - 50V	MLCC	TDK	C1005X5R1H104K050BB

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
32	1	C18	22pF - 50V	MLCC	Vishay	VJ0402A220JNAAJ
33	1	C19	10nF - 50V	MLCC	Murata	GRM155R71H103KA88D
34	1	C20	22µF - 6.3V	MLCC	Murata	GRM21BR60J226ME39L
35	2	C21, C22	1µF - 25V	MLCC	Murata	GRM188C81E105KAADD
36	1	C23	2.2nF 250Vac	Ceramic X1/Y1 capacitor	Murata	DE2E3KY222MA2BM01
37	1	C24	100pF - 50V	MLCC	Murata	GRM1885C1H101JA01D
38	1	C25	100µF - 35V	Elcap	Rubycon	35ZLH100MEFC6.3X11
39	1	D1	1A - 1000V	Power rectifier diode	ON Semiconductor	MRA4007T3G
40	1	D2	1A - 150V	Signal schottky	ST	STPS1150A
41	1	D3	2A - 200V	Power schottky	ST	STPS2200U
42	1	D4	1A - 100V	Power schottky	ST	STPS1H100A
43	1	D5	18V	Zener diode	Vishay	MMSZ5248B-V-GS08
44	1	D6	-	not mounted	-	-
45	1	BR	1200V - 2A	Bridge rectifier	Taiwan Semiconductor	DBLS208G RD
46	1	TF	-	Flyback transformer	Wurth Elektronik	750316413-R02
47	1	L1	1mA	Power induction	Wurth Elektronik	7447713102
48	1	L2	470µA	Power induction	Wurth Elektronik	7447713471
49	1	L3	4.7µA	Power induction	Wurth Elektronik	74455047
50	1	L4	47µA	Power induction	Wurth Elektronik	7440459470
51	1	CM	10mH	Common Mode choke	Wurth Elektronik	744821110
52	1	IC1	-	HV Offline driver	ST	VIPER267KD
53	1	IC2	5V - 200mA	LDO	ST	LDK220M50R
54	1	IC3	350mA	Step down regulator	ST	PM6644
55	1	REF	-	Reference	ST	TS432ILT
56	1	OPTO	-	Optocoupler	Vishay	SFH610A-2
57	2	NTC1, NTC2	16Ω	inrush current limiter	EPCOS	B57236S160M
58	1	F1	2A	Fuse	Littlefuse	0461002.ER
59	1	OUT	4-way	Female connector	Molex	0022152046
60	1	IN	3-way	Female connector	Molex	0022162030

1.3 Transformer

Table 3. Transformer characteristics

Manufacturer	Wurth Elektonik
Part number	750316413 rev2
Core	E16
Primary Inductance	1.5 mH ±10%
Saturation current	700 mA (20% roll-off from initial)
Leakage inductance	50 µH max

Manufacturer	Wurth Elektonik
Primary-to-auxiliary turns ratio	5.38 ±1%
Primary-to-sec1 turns ratio	7.78 ±1%
Primary-to- sec2 turns ratio	11.67 ±1%

Figure 4. Dimensional drawing, pin placement (distances, bottom view) and electrical diagrams

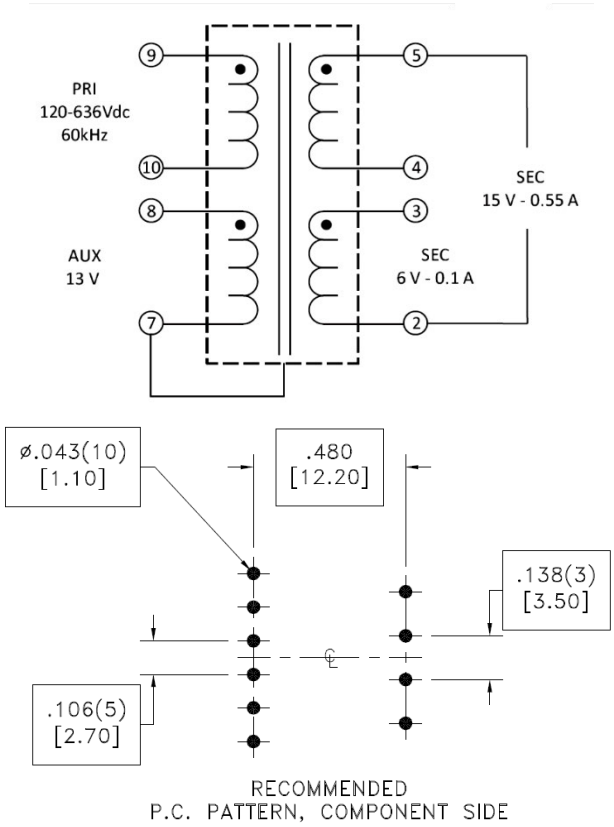
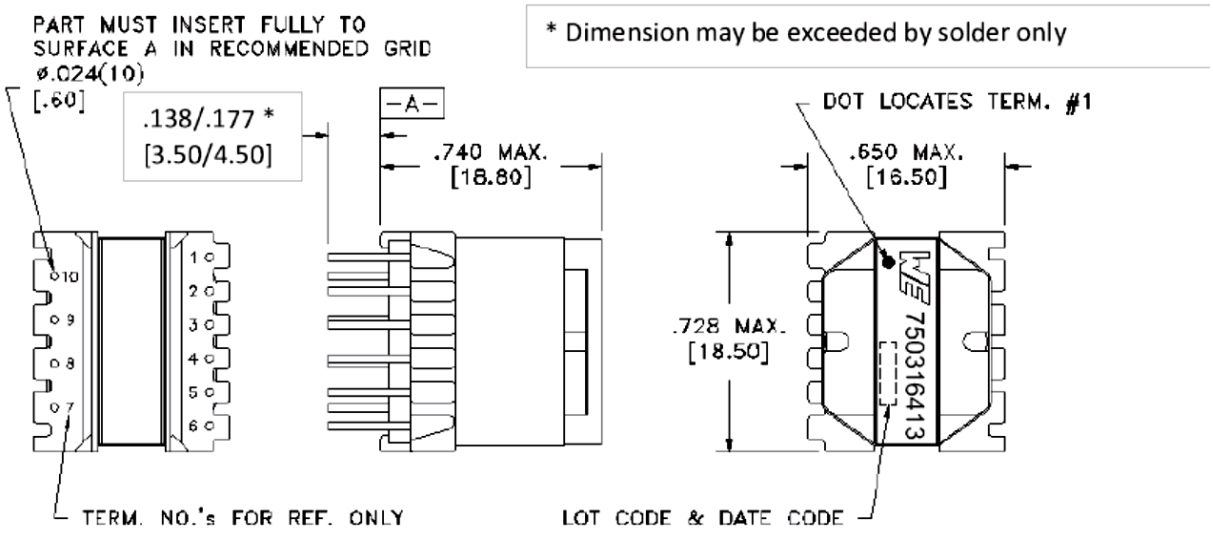


Figure 5. Dimensional drawing and pin placement diagram (bottom, side and top view)



2 Circuit description

2.1 Input stage and filtering

The input stage is designed to allow the power supply to sustain operation at up to $440V_{AC}$. It consists of a fuse (F1) to prevent catastrophic failure and two input NTC to limit the inrush current of the capacitors at plug-in and to protect the bridge rectifier (BR). The total required resistance of the NTC is divided into two in order to ensure safe operation of the NTC components without exceeding the allowed voltage rate across them.

The total bulk capacitance consists of series two capacitors for a total voltage rating above the maximum operative rectified input voltage (about $620V_{DC}$); resistors R1 to R4 ensure equal voltage sharing between the capacitors.

Special care has been placed on filtering conducted converter noise to make render powerline communication less sensitive to the switching power supply. Both differential and common mode filters have been implemented.

2.2 Snubber network

The clamping network (R5-C5-D1), limits the peak of the leakage inductance voltage spike by dissipating the associated energy at MOSFET turn-off to ensure reliable power supply operation.

Resistor R2 helps to further reduce the ringing of the transformer, damping the resonance oscillations at turn-off between leakage inductance and equivalent drain capacitance.

A Transil (D6) is also used to limit the drain voltage in case of excessive voltage.

2.3 HV converter

The core of the power supply is the VIPER267KD offline high-voltage converter with 1050 V avalanche-rugged power section with a maximum $R_{DS(on)} \leq 8.5\ \Omega$, and a current-mode 60 kHz fixed frequency PWM controller.

The device includes several features which considerably reduce the overall BoM cost and improve system reliability.

Control is achieved adjusting the voltage on COMP pin, which transfers the output voltage information via the optocoupler. The capacitors and the pin is used for appropriate loop compensation.

During normal operation, the V_{DD} pin is powered by the output of the auxiliary winding of the transformer, which is rectified by diode D2 and capacitor C7. Resistor R8 is used to filter the auxiliary spikes at turn-off, and limit voltage fluctuation on the pin. Capacitor C6 is used to filter any narrow voltage spikes entering the V_{DD} pin. A clamp network consisting of R7 and D5 is connected across the V_{DD} pin to avoid transient voltages exceeding the AMR of the pin.

The LIM pin, which is used to adjust the cycle-by-cycle current limitation, is left floating because maximum current limitation is required. In case of high noise conditions, a 100nF to 470nF capacitor can be connected between the pin and GND without impacting the functionality of the pin.

2.4 Output stage

The secondary of the transformer is designed for a two-output option: the secondary windings are wound using a stack arrangement to improve the cross regulation of the non-regulated output.

The first secondary signal is rectified by diode D3 and filtered by output capacitor C10, which is designed to ensure enough AC ripple capability to avoid overheating of the component. The L3-C11 post filter is used to further reduce the residual output ripple, whereas the capacitor C22 is used to further reduce the output switching noise.

The other secondary signal is rectified by diode D4 and capacitor C24. As this output is not directly connected to the feedback loop, an LDO is used to provide a stable and precise +5V output.

Capacitor C25 is connected between the cathodes of the diodes to further reduce the cross regulation between the regulated output and the unregulated one.

The output voltage is sensed by voltage divider R15 and R13 and compared with the internal 1.24V reference of the shunt voltage reference TS432; its output is then converted via the optocoupler into a current control signal for the primary PWM IC.

The 3.3V output is achieved using a step-down regulator based on the PM6644, which allows the creation of a low cost synchronous buck converter based on constant on-time (COT) architecture.

3 Performance data

3.1 Output voltage characteristics

The line and load regulation of the board is measured at the PCB output connectors for both 115 V_{AC} and 230 V_{AC}.

Table 4. Load regulation at 115 V_{AC}

I_{OUT1} [mA] 15	I_{OUT2} [mA] 5	I_{OUT3} [mA] 3.3	V_{OUT1} [V]	V_{OUT2} [V]	V_{OUT3} [V]
10	10	100	15.12	5.05	3.30
10	60	100	15.12	5.04	3.30
10	100	100	15.12	5.04	3.30
700	10	100	15.11	5.03	3.29
700	60	100	15.21	4.03	3.28
700	100	100	15.21	5.02	3.28
10	10	200	15.23	5.04	3.24
10	60	200	15.21	4.03	3.24
10	100	200	15.21	5.03	3.24
700	10	200	15.22	5.03	3.23
700	60	200	15.08	5.03	3.23
700	100	200	15.20	5.02	3.23

Table 5. Load regulation at 230 V_{AC}

I_{OUT1} [mA] 15	I_{OUT2} [mA] 5	I_{OUT3} [mA] 3.3	V_{OUT1} [V]	V_{OUT2} [V]	V_{OUT3} [V]
10	10	100	15.20	5.05	3.29
10	60	100	15.19	5.03	3.29
10	100	100	15.18	5.04	3.29
700	10	100	15.17	5.03	3.29
700	60	100	15.18	5.04	3.29
700	100	100	15.19	5.02	3.29
10	10	200	15.22	5.04	3.24
10	60	200	15.23	5.05	3.24
10	100	200	15.25	5.03	3.24
700	10	200	15.23	5.02	3.23
700	60	200	15.23	5.03	3.23
700	100	200	15.23	5.02	3.23

3.2 Efficiency and light load measurements

The efficiency and the light load consumption of the converter are measured at nominal input voltages (115 V_{AC} and 230 V_{AC}).

Table 6. Efficiency at typical and maximum load

Output condition	Efficiency	
	115 V_{AC}	230 V_{AC}
15V@550mA / 5V@60mA / 3.3V@100mA	77.15%	79.92%
15V@700mA / 5V@100mA / 3.3V@200mA	72.37%	76.45%

Table 7. Load consumptions at minimum load (P_{OUT} = 0.16W)

Input voltage	Input power
115V_{AC}	270 mW
230V_{AC}	390 mW

4 Typical waveforms

In TX mode, the load on output 1 changes from 10 to 700 mA with a 1-Hz repetition rate and 70% duty cycle. Output 2 and output 3 are loaded at typical values (60 mA and 100 mA respectively).

During PLM operation, it is important that the output voltage remains regulated within specification limits to ensure correct operation of the PLM power amplifier (see Figure 6 and Figure 7). The output voltage is quite stable and clean with no abnormal oscillation during load changes and the steady-state values are within specification with very good margin.

Figure 6. Output voltage and current at 115 V_{AC}

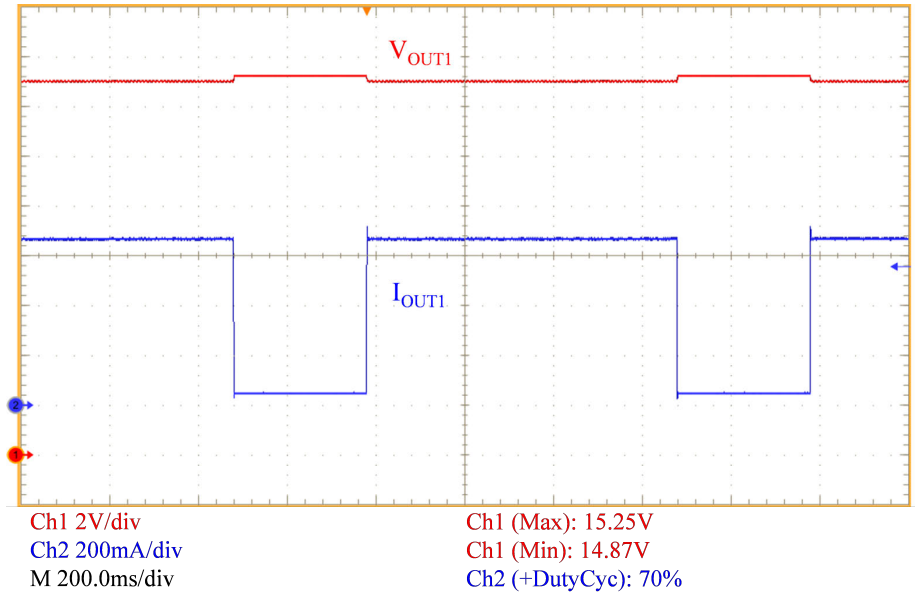
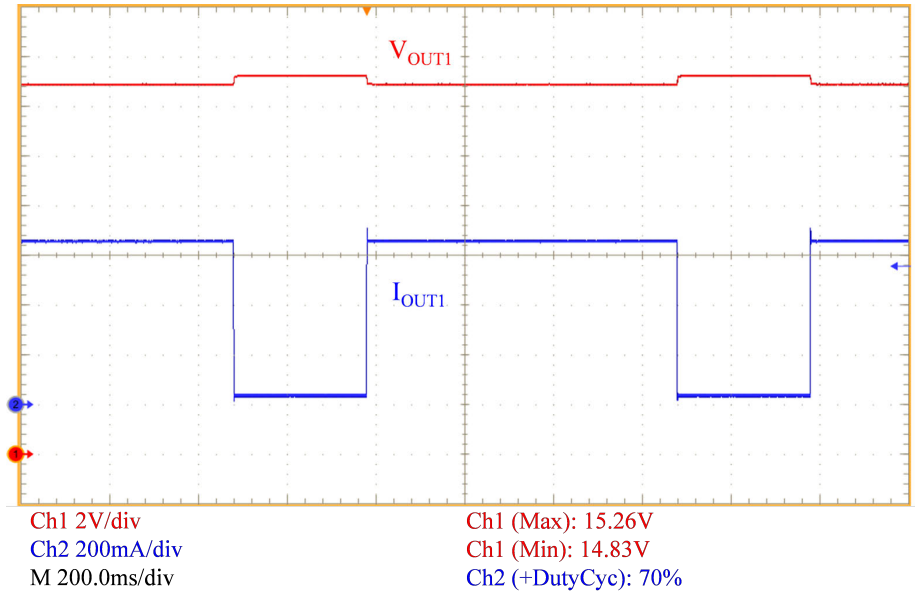
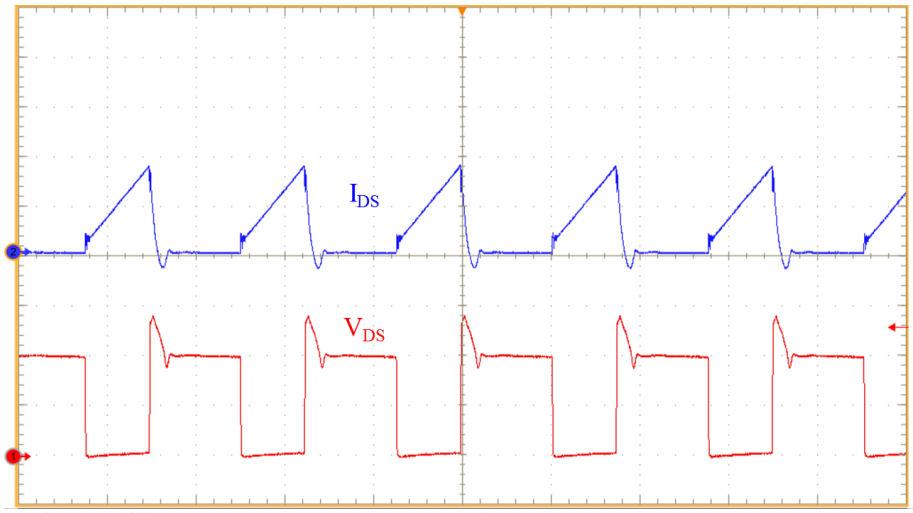


Figure 7. Output voltage and current at 230 V_{AC}



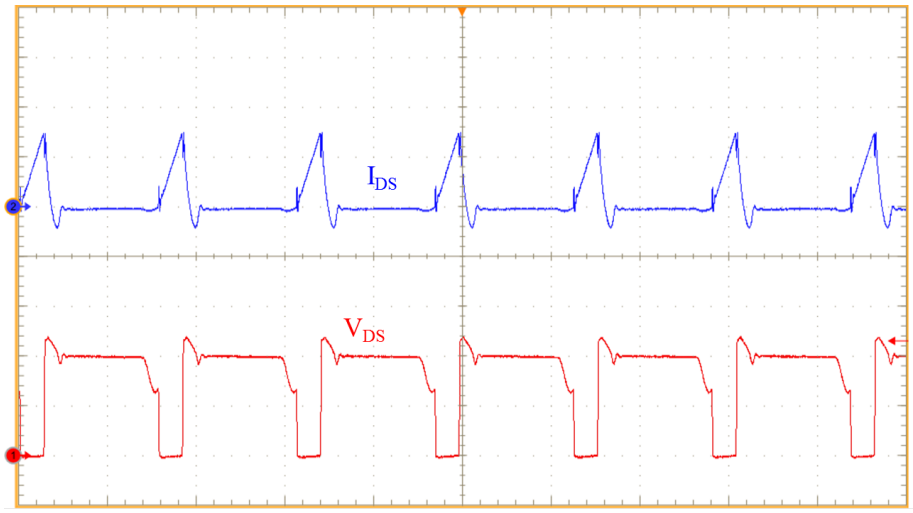
The drain voltage and the drain current waveforms are reported for the two nominal input voltages and at 440V_{AC} also (see figures Figure 8 to Figure 10).

Figure 8. Drain voltage and drain current at 115 V_{AC}



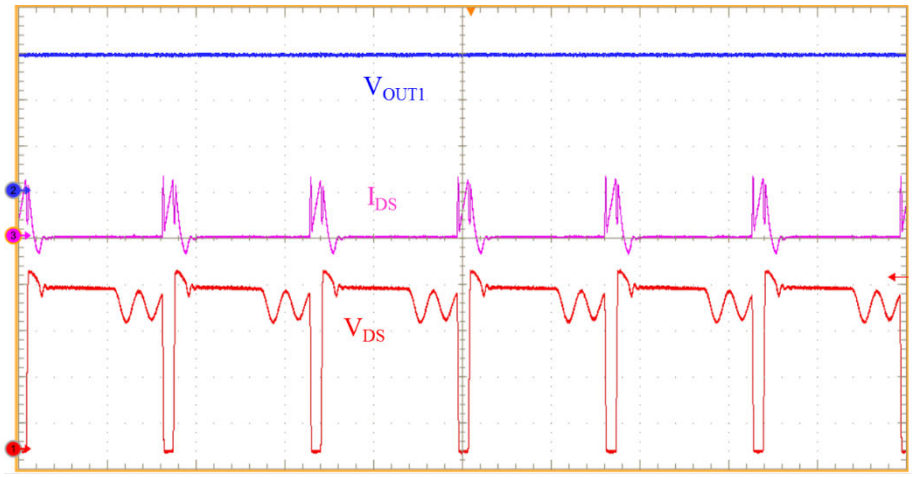
Ch1 100V/div
Ch2 300mA/div
M 10.0µs/div
Ch1 (Max): 280V
Ch2 (Max): 500mA
Ch2 (Freq): 59.35 kHz

Figure 9. Drain voltage and drain current at 230 V_{AC}



Ch1 100V/div
Ch2 300mA/div
M 10.0µs/div
Ch1 (Max): 475V
Ch2 (Max): 456mA
Ch2 (Freq): 59.35 kHz

Figure 10. **Drain voltage and drain current at 440 V_{AC}**

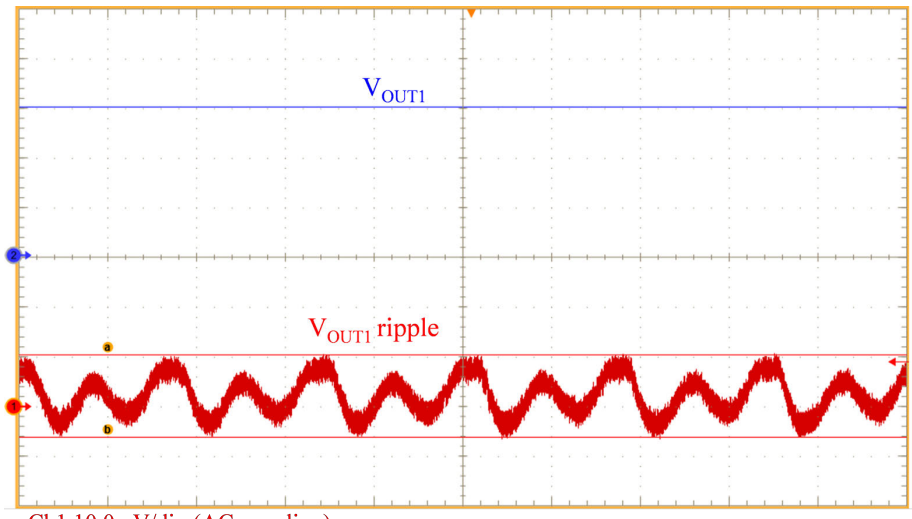


Ch1 200V/div
Ch2 5V/div
Ch3 300mA/div
M 10.0µs/div

Ch1 (Max): 772V
Ch2 (Mean): 14.8V
Ch3 (Max): 396mA

The output voltage ripple at the 15 V output at nominal input voltage and full load is also measured. It must be very low in order to ensure good sensitivity during the PLM operation (see figures Figure 11 and Figure 12). The measured value is extremely low, resulting in the range of about 0.1% of the nominal output voltage.

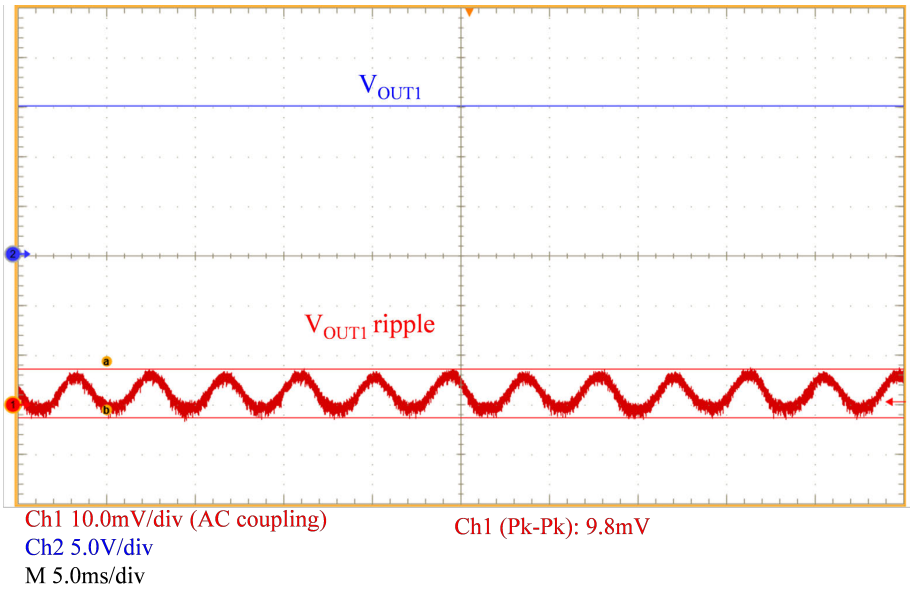
Figure 11. **Output voltage ripple at 115 V_{AC}**



Ch1 10.0mV/div (AC coupling)
Ch2 5.0V/div
M 5.0ms/div

Ch1 (Pk-Pk): 16.58mV

Figure 12. **Output voltage ripple at 230 V_{AC}**



5 Noise measurements

The pre-compliance tests for conducted noise emissions as per EN55022 (Class B) European normative were performed using a Quasi-Peak detector and an Average detector of the conducted art nominal mains voltage, and compared with the associated limits.

Figure 13 and Figure 14 show that the tests returned a very good margin between the measurements and the respective limits.

Figure 13. LINE conducted disturbance

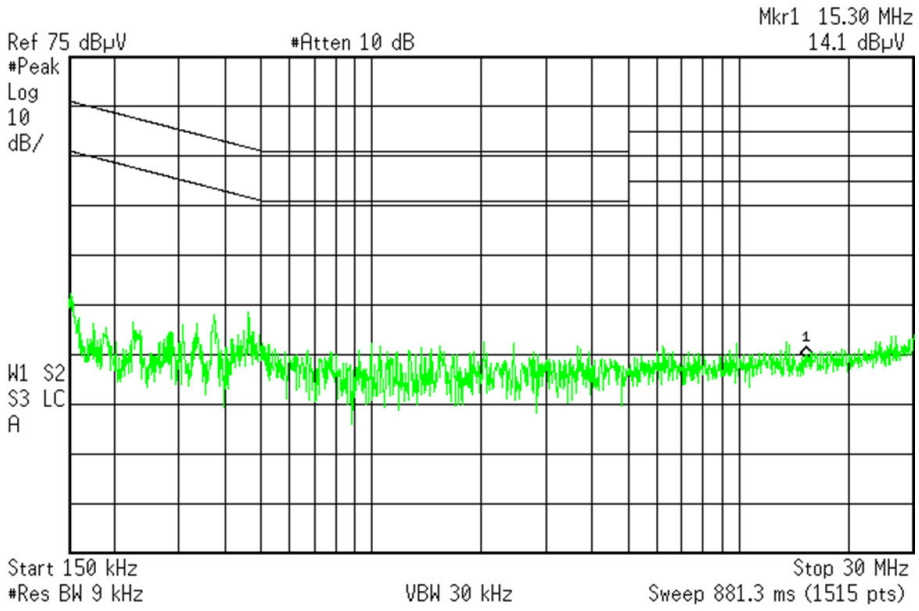
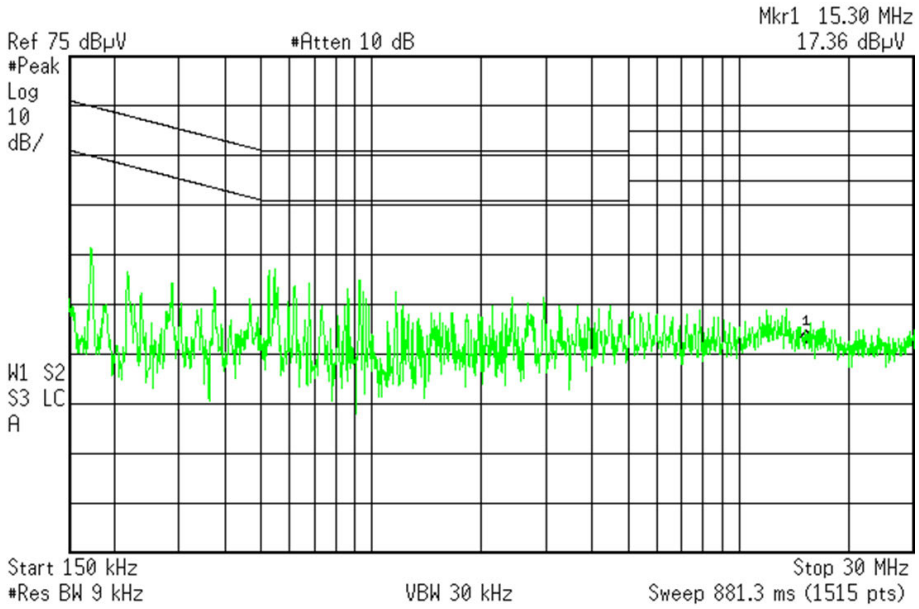


Figure 14. NEUTRAL conducted disturbance



6 Conclusion

A three output isolated flyback converter reference design for smart meter and PLC systems using the VIPER267KD was tested and we demonstrated that the the input filter setup, the compliance with the European standards for smart metering PLC applications and for Electromagnetic compatibility and the overall performances of the board make it suitable for use in any PLC system.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
06-May-2019	1	Initial release.

Contents

List of figures

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