STM32L5 Series microcontroller ultra-low-power features overview

Introduction

The STM32L5 Series microcontrollers are ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M33 with FPU core.

The STM32L5 Series microcontrollers use an innovative architecture to reach ultra-low-power consumption figures provided by their high flexibility and advanced set of peripherals providing high energy efficiency for applications.

With the integration of the ART accelerator instruction cache, the STM32L5 Series microcontrollers can operate at frequencies up to 80 and 110 MHz, and achieve 120 and 165 DMIPS performance at 80 and 110 MHz respectively, while maintaining extremely low dynamic power consumption.

The STM32L5 Series microcontrollers feature FlexPowerControl, which increases flexibility in power mode management while at the same time reducing the overall application power consumption.

The STM32L5 Series microcontrollers embed a high number of smart, high performs peripherals, a large set of advanced andlow-power analog features, and several peripherals tuned for Low-power modes. Thanks to the batch acquisition sub-mode (BAM), these microcontrollers optimize the consumption when data is transferred through communication peripherals, while the rest of the device is kept in Low-power mode.

The combination of low-power design and processing performance allows these devices to achieve an industry leading EEMBC® ULPBench™ score, up to 370 ULPMark™.

Based on the STM32F and STM32L families, the STM32L5 Series microcontrollers embed several innovations which minimize power consumption in the different modes, while maintaining most of the existing peripherals and an excellent pin-to-pin compatibility to allow easy migration from existing families.

Note that the pin-to pin compatibility does not apply to the STM32L5 Series microcontrollers supporting the built-in SMPS.

Thanks to their built-in internal voltage regulator and voltage scaling, the consumption in active modes is kept to a minimum whatever the external supply voltage. This makes these devices particularly suited for mobile battery-supplied products, down to 1.71 V.

Furthermore, some STM32L5 Series microcontrollers embed a built-in SMPS step down converter which is a very power-efficient DC/DC non-linear switching regulator improving power performance when the VDD voltage is high.

In addition, their multi-voltage domains allow the product to be supplied at low voltage (thus reducing consumption) while the analog-to-digital and digital-to-analog converters can operate with a higher supply and reference voltage, up to 3.6 V.

The STM32L5 Series microcontrollers support a battery backup domain to keep the RTC running, and a set of 32 registers, each 32 bits wide which are retained in case of power loss. This optional backup battery can be charged when the main supply is present.

The STM32L5 Series microcontrollers support seven main low-power modes, each of them with several sub-mode options. This allows the designer to achieve the best compromise between low-power consumption figure, shortened start-up time, available set of peripherals and maximum number of wakeup sources.

The STM32L5 Series microcontrollers with a "Q" suffix (such as STM32L5xxxxQ) support the use of an optional internal SMPS, thus enabling the design of very efficient and low power applications.

The STM32L5 Series microcontrollers with "P" suffix (such as STM32L5xxxxP) support the use of an optional external SMPS.

1 General information

This document applies to the STM32L5 Series based Arm® Cortex®-M33 core microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Energy-efficiency processing

The high processing performance in Run mode (expressed in DMIPS/MHz) is achieved thanks to the use of a Cortex®-M33 core associated with the interfaces of its memories. To ensure full performance operation at maximum operating frequency the STM32L5 Series microcontrollers embed the ART accelerator instruction cache (ICACHE), which masks the Flash memory access wait state, and it is possible to achieve 1.5 DMIPS/MHz, whatever the system clock frequency.

The high energy efficiency, expressed as mA/DMIPS, is obtained by dynamically adapting the internal supply voltage to the operating frequency. This method is called “under-volting”.

The STM32L5 Series microcontrollers offer dynamically selectable voltages and frequency ranges:

- Range 0 for system frequency up to 110 MHz
- Range 1 for system frequency up to 80 MHz
- Range 2 for system frequency up to 26 MHz with improved efficiency:
  - up to 20 % higher than Range 0, when LDO is used
  - up to 30% higher than, Range 0, when SMPS is used.

This is achieved by supplying the logic with the internal low-power regulator. In this mode the peripherals with independent clocks can still run on the internal high-speed oscillator (HSI) at 16 MHz. Those peripherals are I^2C, USART, LPUART1, LPTIM.

Figure 1 shows the typical current consumption of the STM32L5 Series microcontrollers, as a function of system frequency, using different Run modes. LPRun stands for low-power run.

Figure 1. Current consumption in Run and LPRun with ICACHE on, 2-ways

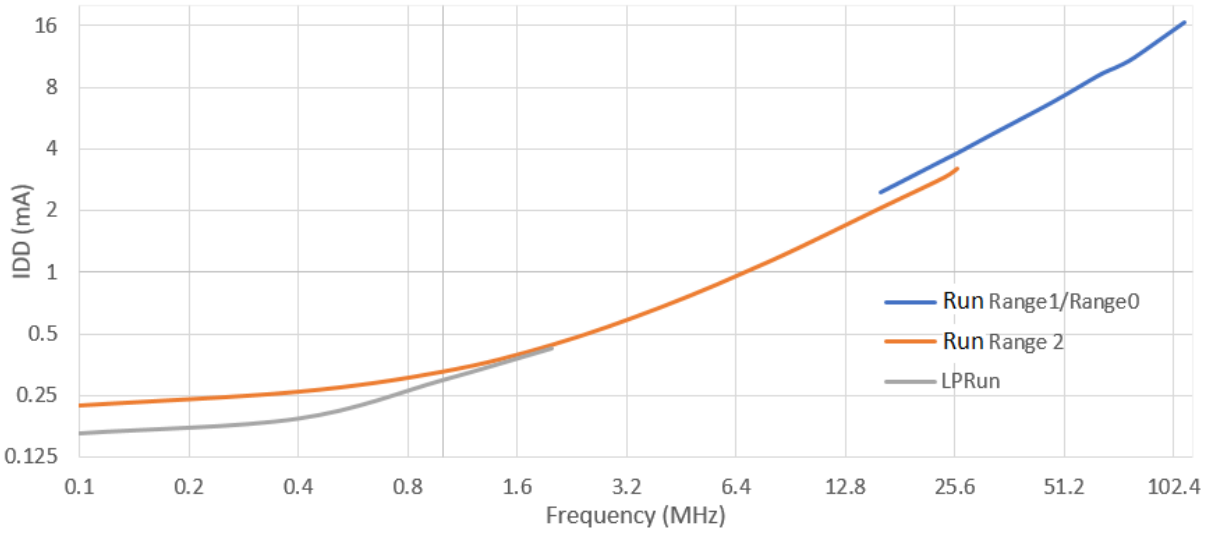
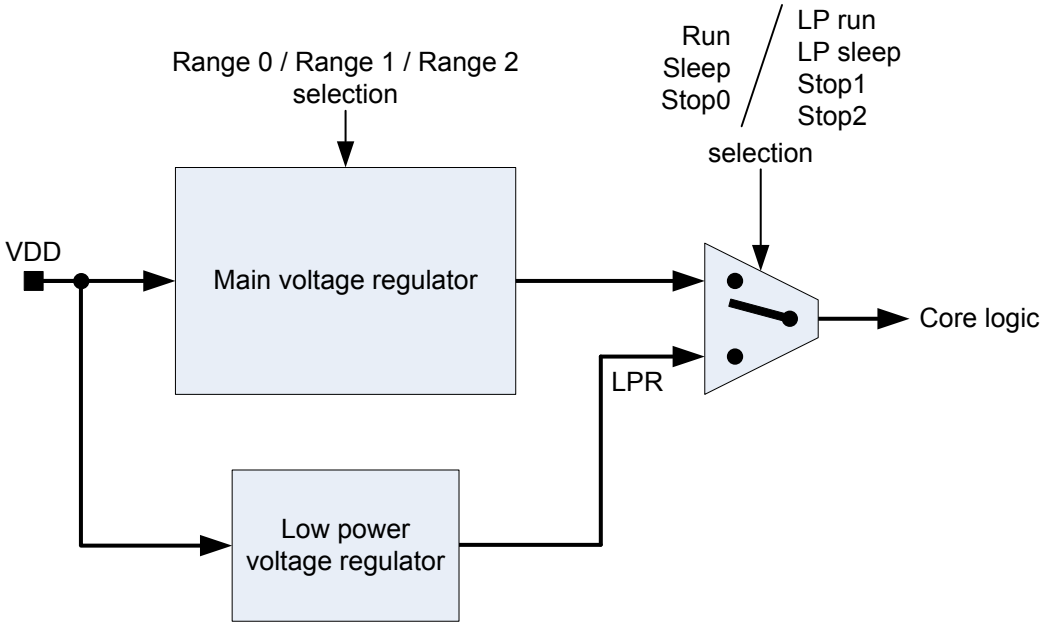


Figure 2 shows the power distribution from the internal LDO regulator in the different power modes.

Figure 2. Power distribution architecture



The STM32L5 Series microcontrollers have a built-in SMPS step down converter. It is a power-efficient DC/DC non-linear switching regulator that improves power performance when the VDD voltage is high enough. The SMPS is used in Run, Sleep and Stop 0 modes. It supplies the main voltage regulator which itself provides the V_{core}.

Note: The SMPS is available on STM32L5xxxxQ devices only.

Figure 3 shows the typical current consumption of a STM32L5 Series microcontroller in Run mode, as a function of system frequency, when SMPS is used.

Figure 3. Current consumption in Run with ICACHE on , 2-ways, SMPS

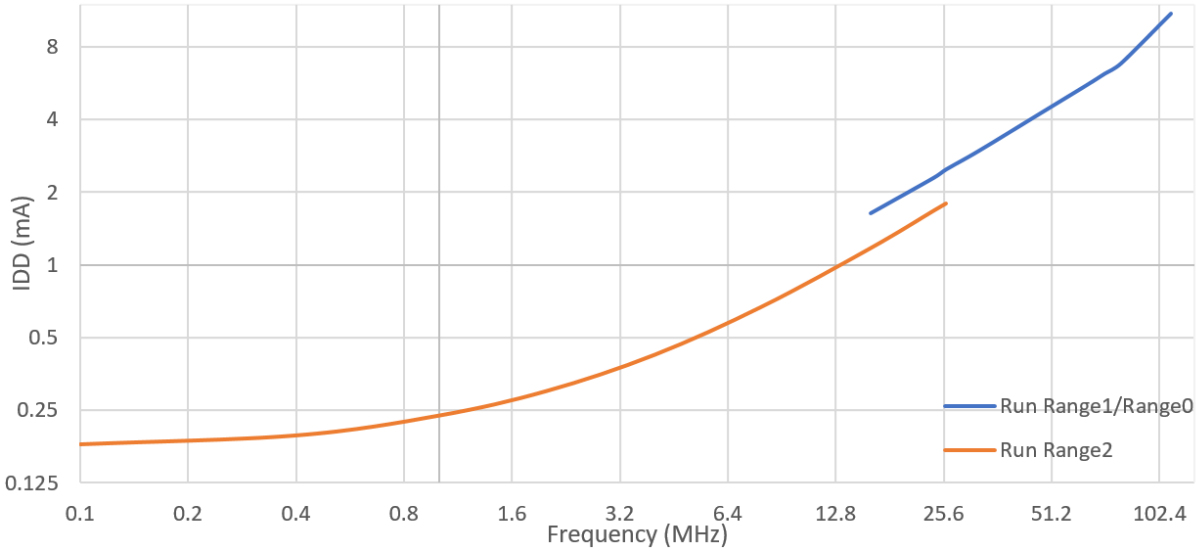


Figure 4. Current consumption in Run with ICACHE on, 2 -ways, SMPS versus LDO

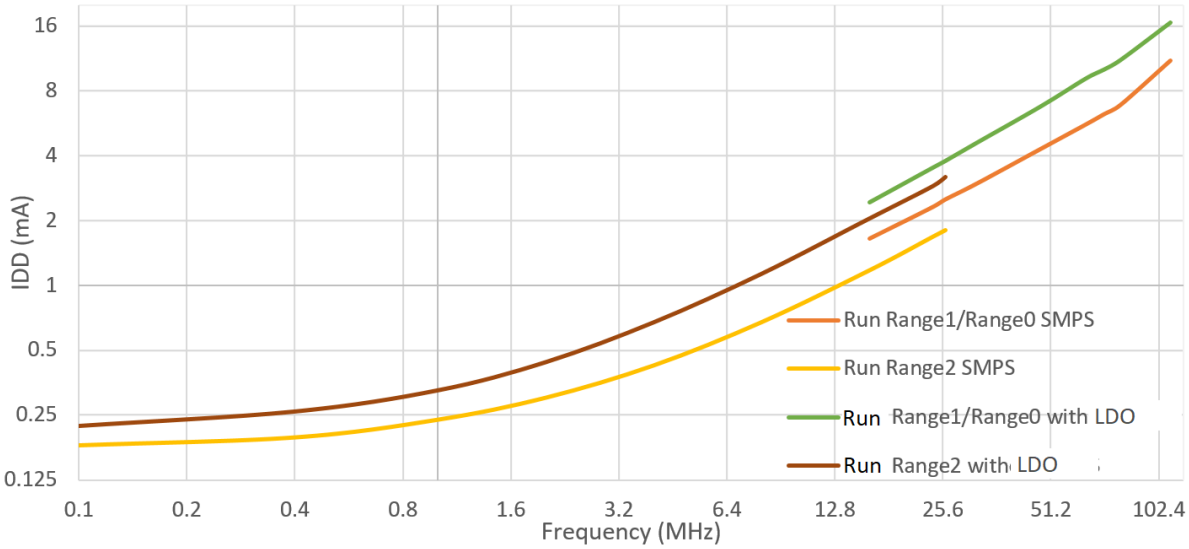


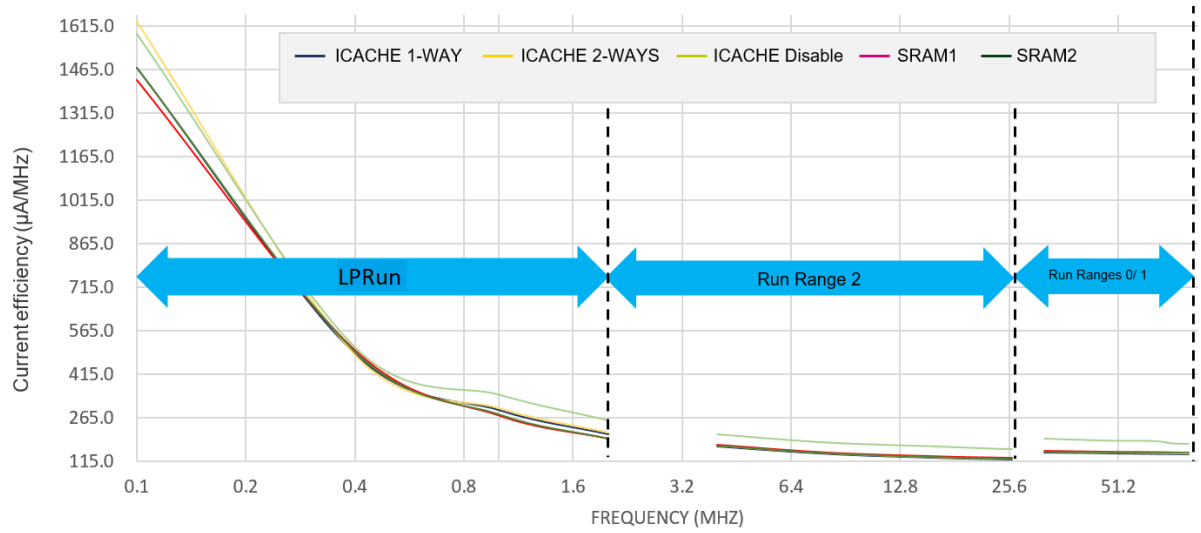
Figure 4 shows the typical current consumption of a STM32L5 Series microcontroller in Run mode, as a function of system frequency, for both SMPS and bypass (LDO) configurations.

The lowest power consumption is achieved when running from internal SRAM. When running from the internal Flash memory, the instruction cache tends to reduce the number of accesses to the memory thus reducing the overall current consumption.

Figure 5 shows the consumption of the STM32L5 Series microcontrollers using LDO for four main memory configurations:

- Execution from the internal Flash memory, ICACHE enabled 1-way
- Execution from the internal Flash memory, ICACHE enabled 2-ways
- Execution from the internal Flash memory, ICACHE disabled
- Execution from the internal SRAM1, Flash memory disabled
- Execution from the internal SRAM2, Flash memory disabled.

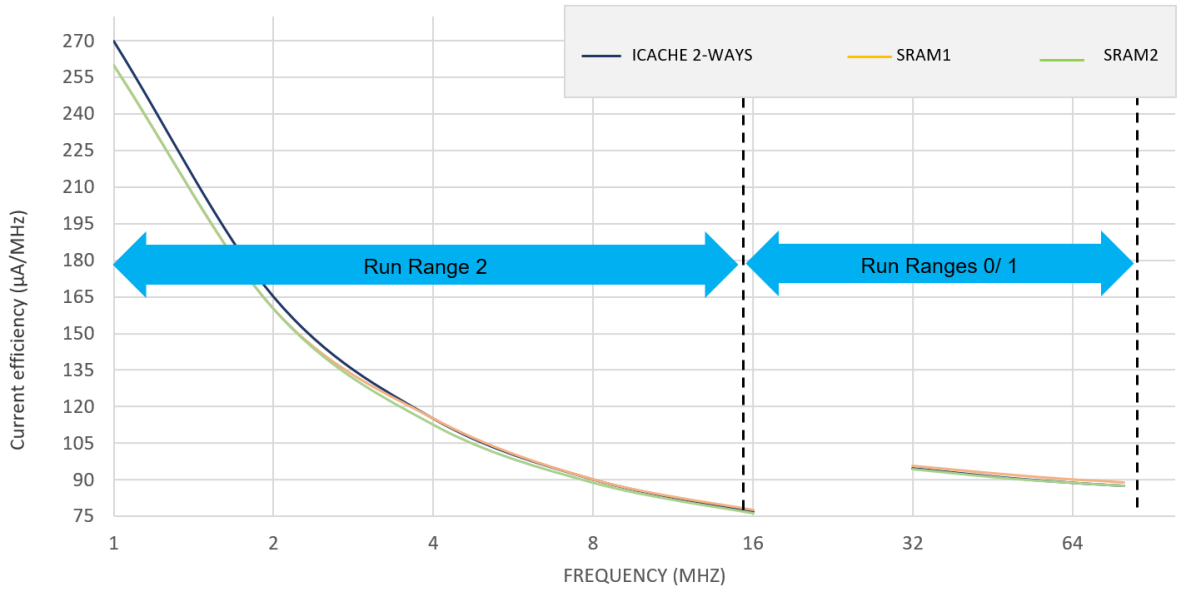
Figure 5. Current efficiency for different memory configurations, LDO



Note: In LPRun, the low-power regulator is used instead of the main voltage regulator.

Figure 6 shows the consumption of the STM32L5 Series microcontrollers using SMPS for three memory configurations:

Figure 6. Current efficiency for different memory configurations, SMPS



Note: In LPRun mode, the SMPS cannot be used. It is bypassed. In this case, the low-power regulator is used to provide V_{core}.

The location of the executable code and data within the memory system impacts not only the current consumption but also the overall computation performances. As an example, Table 1 details the overall performances measured on the STM32L5 Series microcontrollers running the system clock at 110 MHz on a more complex algorithm, such as CoreMark® from EEMBC® organization.

Table 1. STM32L5 Series microcontrollers performance with system clock at 110 MHz

Configuration	mA/MHz		CoreMark/MHz	CoreMark/mA		Comments
	LDO	SMPS		LDO	SMPS	
ICACHE Disabled	0.171	0.117	1.53	8.95	13.08	-
ICACHE 1-WAY	0.146	0.098	3.92	26.85	40	-
ICACHE 2-WAYS	0.152	0.102	3.97	26.12	38.92	-
SRAM1 and SRAM2	0.152	0.1	4.01	26.38	40.1	Code in SRAM2, data in SRAM1

The ICACHE makes it possible to reach almost the same performance, both in computation (CoreMark® per MHz) and current consumption (CoreMark® per mA), as if the same program is run from the internal SRAM.

Table 2 gives the impact on performance, measured on an STM32L5 Series microcontrollers, for different Run modes.

Table 2. STM32L5 Series microcontrollers performance for different Run modes

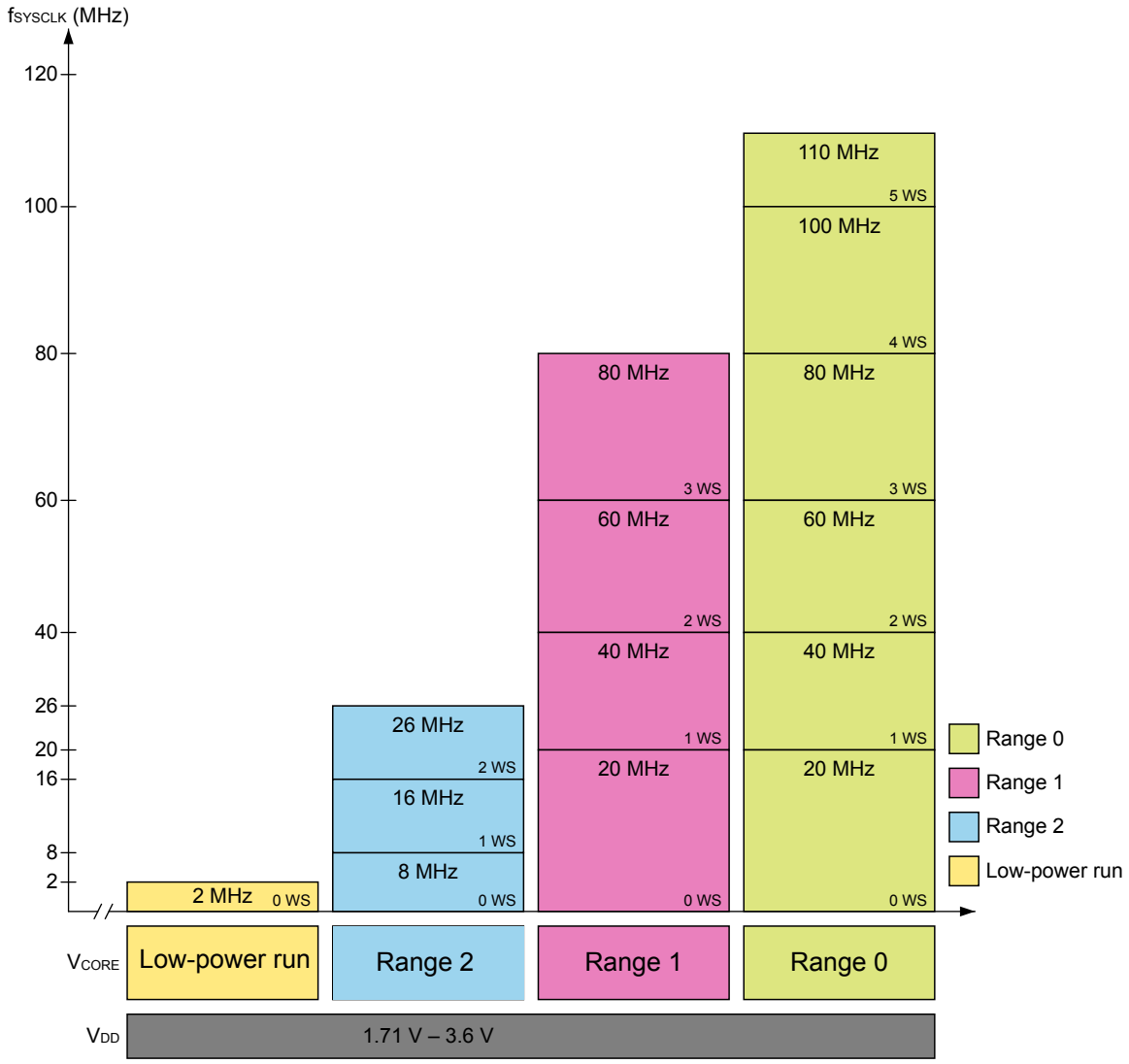
Run mode	Configuration	mA/MHz		CoreMark/ MHz	CoreMark/mA	
		LDO	SMPS		LDO	SMPS
Range 0 (110 MHz)	ICACHE Disabled	0.171	0.117	1.53	8.947	13.077
	ICACHE 1-way	0.146	0.098	3.92	26.849	40
	ICACHE 2-ways	0.152	0.102	3.97	26.118	38.922
Range 1 (80 MHz)	ICACHE Disabled	0.176	0.112	2.14	12.159	19.107
	ICACHE 1-way	0.138	0.085	3.96	28.696	46.588
	ICACHE 2-ways	0.143	0.088	3.99	27.902	54.341
Range 2 (26 MHz)	ICACHE Disabled	0.157	0.092	3.31	21.083	35.978
	ICACHE 1-way	0.119	0.07	3.99	33.529	57
	ICACHE 2-ways	0.123	0.072	4.01	32.602	55.694

Range 2 improves the efficiency (CoreMark® per mA) over Range 0 by almost:

- 20 % when the LDO is used
- 30 % when SMPS is used.

Figure 7 shows the Flash memory latency (number of wait states to be programmed in the Flash memory access control register), depending on regulator voltage scaling range and system clock frequency for the STM32L5 Series microcontrollers.

Figure 7. Flash memory latency vs Vcore range for the STM32L5 Series microcontrollers



3 FlexPowerControl description

FlexPowerControl reduces the application power consumption thanks to high flexibility in the power management, smart peripherals and architecture.

3.1 Numerous Low-power modes

The STM32L5 Series microcontrollers implement many different power modes, seven of them are Low-power modes.

On top of these modes, the power consumption can be modulated by selecting different clock sources and frequencies, as well as clocking off peripherals not in use.

In all these modes, except Shutdown, the safe power monitoring Brown-Out Reset (BOR) and the IWDG can stay active to guarantee safe execution.

Table 3 summarizes the features available for each mode and provides an indication of the current consumption.

3.1.1 Low-power run and Low-power sleep modes

Two Low-power active modes are available on the STM32L5 Series microcontrollers in addition to Sleep, Stop and Standby modes implemented on the STM32F Series microcontroller. These modes are the Low-power run and Low-power sleep.

They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off, or where the CPU is processing continuously at low speed to minimize current variations.

Several features have been put in place to reduce the current consumption:

- The core logic is supplied by the low-power voltage regulator to reduce the quiescent current .
- The Flash memory can be switched off (Power-down mode and clock gating) in Low-power sleep mode. It can also be switched off in Low-power run when the processor is executing from SRAM1 or SRAM2.
- The system clock is limited to a maximum of 2 MHz. The MSI internal RC oscillator must be selected as it supports several frequency ranges, with a small microcontroller total consumption down to 18 µA in low-power sleep Flash memory off at 100 kHz.

Batch acquisition sub-mode (BAM)

The STM32L5 Series microcontrollers support the power efficient batch acquisition sub-mode (BAM), in which data is transferred with communication peripherals, while the rest of the device is in Low-power mode.

This is achieved by entering Sleep or Low-power sleep mode with this configuration:

- Only the DMA, the communication peripheral(s) and the SRAM1 or SRAM2 clocks are enabled in Sleep (or Low-power sleep) mode.
- The Flash memory is off in Sleep (or Low-power sleep) mode: the Flash memory is in power-down and the Flash memory clock is gated off.
- If the system clock can be limited to 2 MHz, the main regulator is switched off (to enter Low-power sleep).

In Low-power sleep mode, the I^2C and USART / LPUART peripherals can still be clocked with HSI at 16 MHz. This allows BAM to be supported with the I^2C or USART at up to 1 Mbps speed.

3.1.2 Stop mode

The STM32L5 Series microcontrollers implements three Stop modes with full SRAM and peripheral retention capability and the ability to wake up in 1 µs by using of the MSI running at 48 MHz.

In these Stop modes, all the high-speed oscillators (HSE, MSI, HSI) are stopped, while the low speed ones (LSE, LSI) can be kept active. The peripherals can be set active, using the HSI clock when needed, to be able to wake up the device on some specific events (such as UART character reception or I^2C address recognition).

Stop 2 mode implements a dedicated mechanism to keep the retention current as low as possible while allowing a very fast wakeup of 6.19 µs from SRAM or 11.20 µs from Flash memory.

3.1.3 Standby mode

In Standby mode, the BOR is always enabled, ensuring that the device is under reset when the supply voltage drops below the selected functional threshold.

By default, the SRAM content is lost in Standby mode. However, it is possible to preserve, entirely or partially the content of the SRAM2, but this requires additional current consumption.

The configuration of external devices are kept by the use of pull-ups and pull-downs which are individually applied on each I/O during the Standby mode.

A wakeup from this mode is done thanks to one of the five wakeup pins, the reset pin or the independent watchdog. The RTC clocked by the low-speed oscillators (LSE or LSI) is also available in this mode, with wakeup capability.

3.1.4 Shutdown mode

This mode provides the lowest consumption, by switching off the internal voltage regulators, and by disabling the voltage power monitoring. A wakeup from this mode is done thanks to one of the five wakeup pins or to the reset pin. The RTC clocked by the low-speed external oscillator (LSE) is also functional in this mode, with wakeup capability.

Table 3. STM32L5 Series microcontrollers power modes overview

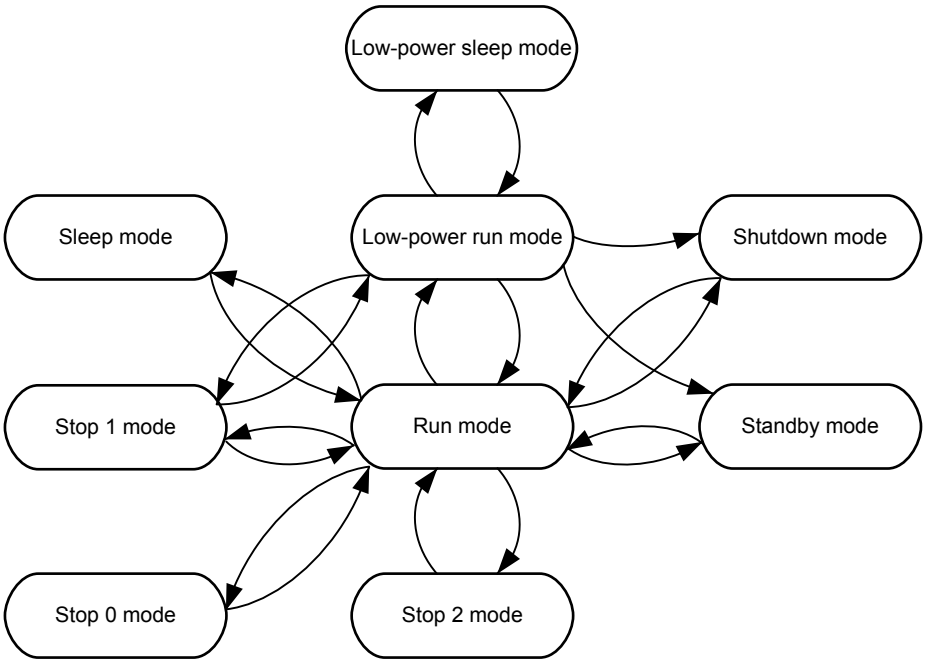
Mode	Regulator and SMPS mode (1)	CPU	Flash	SRAM	Clocks	DMA and Peripherals(2)	Wake up source
Run	Ranges 0/1 SMPS HP mode, if SMPS is used.	Yes	On(3)	On	Any	All	N/A
	Range 2 SMPS LP or HP mode, if SMPS is used					All except USB_FS, RNG	
LPRun	LPR	Yes	On(3)	On	Any except PLL	All except USB_FS, RNG	Any interrupt or event
Sleep	Ranges 0/1 SMPS HP mode, if SMPS is used.	No	On(3)	On(4)	Any	All	Any interrupt or event
	Range 2 SMPS LP or HP mode, if SMPS is used					All except USB_FS, RNG	
LPSleep	LPR	No	On(3)	On(4)	Any except PLL	All except USB_FS, RNG	Any interrupt or event
Stop 0(5)	MR	No	Off	On	LSELSI	BOR, PVD, PVMRTC, IWDGCOMPx (x=1,2), DAC1OPAMPx (x=1,2), USARTx (x=1...5)(6), LPUART1(6), I2Cx (x=1...4) (7), LPTIMx (x=1,2,3)	Reset pin, all I/Os BOR, PVD, PVMRTC, IWDGCOMPx (x=1..2), USARTx (x=1...5)(6), LPUART1(6), I2Cx (x=1...4)(7), LPTIMx (x=1,2),

Mode	Regulator and SMPS mode [1]	CPU	Flash	SRAM	Clocks	DMA and Peripherals[2]	Wake up source
						*** All other peripherals are frozen	USB_FS[8]
Stop 1	LPR	No	Off	On	LSELSI	BOR, PVD, PVMRTC, IWDGCOMPx (x=1,2), DAC1OPAMPx (x=1,2,3), USARTx (x=1...5)[6], LPUART1[6], I2Cx (x=1...4)[7], LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/OsBOR, PVD, PVMRTC, IWDGCOMPx (x=1..2), USARTx (x=1...5)[6], LPUART1[6], I2Cx (x=1...4)[7] LPTIMx (x=1,2), USB_FS[9]
Stop 2	LPR	No	Off	On	LSELSI	BOR, PVD, PVMRTC, IWDGCOMPx (x=1..2), I2C3[7], LPUART1[6], LPTIMx (x= 1,3) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVMRTC, IWDGCOMPx (x=1..2), I2C3[7], LPUART1[6], LPTIMx (x= 1,3)
Standby	LPR	Powered Off	Off	SRAM2 On	LSELSI	BOR, RTC, IWDG *** All other peripherals are powered off *** I/O configuration can be floating, pull-up or pull-down	Reset pin, Five I/Os (WKUPx)[8], BOR, RTC, IWDG
	OFF			Powered Off			
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off *** I/O configuration can be floating, pull-up or pull-down[8]	Reset pin Five I/Os (WKUPx)[10], BOR, RTC

1. *LPR means main regulator is OFF and low-power regulator is On.*
2. *All peripherals can be active or clock gated to save power consumption.*
3. *The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.*

4. *The SRAM1 and SRAM2 clocks can be gated on or off independently.*
5. *SMPS mode can be used in Stop 0 mode, but no significant power gain is expected comparing to the case where SMPS is bypassed.*
6. *U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.*
7. *I^2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.*
8. *I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.*
9. *USB_FS wakeup by resume from suspend and attach detection protocol event.*
10. *The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.*

Figure 8. Low-power modes possible transitions



3.2 Multi-supply and battery backup domain

The STM32L5 Series microcontrollers require a 1.71 V to 3.6 V operating supply voltage (VDD). Several peripherals are supplied through independent power domains: VDDA, VDDIO2, VDDUSB. Those supplies must not be provided without a valid operating supply on the VDD pin. The power domains are outlined in the table below.

Table 4. Power domains

Domain name	Voltage range	Description
VDD	1.71 V to 3.6 V	VDD is the external I/O power supply, the internal regulator (or the SMPS step down converter depending on the device) and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
VDDA	1.62 V (ADCs/COMPs) 1.8 V (DACs/OPAMPs) 2.4 V (VREFBUF) to 3.6 V	VDDA is the external analog power supply for: • A/D converters • D/A converters • voltage reference buffer • operational amplifiers • comparators. VDDA voltage level is independent from VDD voltage. VDDA must be connected to VDD when these peripherals are not used.
VDDSMPS	2 V to 3.6 V	VDDSMPS is the external power supply for the SMPS step down converter. It is provided externally through the VDDSMPS supply pin and must be connected to the same supply as VDD.
VLXSMPS	2 V to 3.6 V	VLXSMPS is the switched SMPS step down converter output.
V15SMPS(1)	2 V to 3.6 V	V15SMPS is the power supply for the system regulator. It is provided externally through the SMPS step down converter VLXSMPS output.
VDD12(2)	1.05 to 1.32 V	VDD12 is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and does not support any external load.
VDDUSB	3.0 V to 3.6 V	VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage. VDDUSB must be connected to VDD when the USB is not used. The VDDUSB power supply may not be present as a dedicated pin, but is internally bonded to VDD. For such devices, VDD has to comply the VDDUSB supply range when the USB is used.
VDDIO2	1.08 V to 3.6 V	VDDIO2 is the external power supply for 14 I/Os (Port G [15:2]). The VDDIO2 voltage level is independent from the VDD voltage and must be connected to VDD when PG [15:2] are not used.
VBAT	1.55 V to 3.6 V	VBAT is the power supply for RTC, external 32 kHz oscillator clock and backup registers (through power switch) when VDD is not present. VBAT is internally bonded to VDD for small packages without dedicated pin.

1. *The SMPS power supply pins are available only on a specific package with SMPS step down converter option.*
2. *The VDD12 power supply pins are available only on a specific package with external SMPS option.*

VREF-, VREF+ definition

VREF+ is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

When VDDA is less than 2 V, VREF+ must be equal to VDDA.

When VDDA is greater than 2 V, VREF+ must be between 2 V and VDDA.

VREF+ can be grounded when ADC and DAC are not active.

The internal voltage reference buffer supports two output voltages, which are configured with the VRS bit in the VREFBUF_CSR register:

- VREF+ around 2.048 V. This requires VDDA to be equal to or higher than 2.4 V.
- VREF+ around 2.5 V. This requires VDDA to be equal to or higher than 2.8 V.

On some packages, VREF- and VREF+ pins are not available. When not available on the package, they are internally bonded to VSSA and VDDA respectively.

When VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to related device datasheet for package pinout descriptions).

VREF- must always be equal to VSSA.

An embedded linear voltage regulator is used to supply the internal digital power Vcore, the digital peripherals and the memories.

In the STM32L5 Series microcontrollers with SMPS, the main regulator is fed by the SMPS output. The SMPS is a power efficient DC/DC non linear switching regulator that improves power performance when the VDD is high enough.

3.3 Supply monitoring

The STM32L5 Series microcontrollers include a sophisticated supply supervisor module with several programmable options. This module is active during both power-on, power-down and run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) retrieved from the non-volatile memory to perform the microcontroller initialization, even before the user reset phase. It is also during this period that VDD can be altered with glitches coming from the battery insertion or because of a weak power source.

The ultra-safe BOR circuitry guarantees that the reset is released only if the value of VDD is above the selected threshold, whatever the slope of the VDD ramp-up phase, so that the circuit is within its guaranteed operating conditions when the program execution starts. A reset is generated when VDD falls below the selected threshold. Five thresholds can be selected depending on the value stored in Flash memory option byte. The BOR minimum threshold is 1.71 V, guaranteeing that the microcontroller exits reset above 1.71 V supplying it with a reference voltage of 1.8 V ± 5%.

The BOR is enabled in all modes except Shutdown mode. In Shutdown mode, the power monitoring is disabled. As a consequence the switch to VBAT domain when VDD is not present (and vice-versa) is not supported in Shutdown mode.

In addition, a 7-level programmable voltage detector (PVD) is available to generate an early interrupt in case of a voltage drop.

Finally, the independent power supplies (VDDA, VDDUSB and VDDIO2) can be monitored by comparison with a fixed voltage threshold and generate an interrupt in case power drops below the threshold.

The PVD and PVM can wakeup from Stop modes.

In the STM32L5 Series microcontrollers, it is possible to monitor the upper VDD voltage thanks to the internal tamper.

A tamper event is generated when the VDD domain voltage exceeds a specified threshold.

3.4 A set of peripherals tailored for Low-power consumption

Some peripherals require special attention, either because of their intrinsic high consumption, or because they are always powered up.

The STM32L5 Series microcontrollers embed multiple 12-bit / 5 Msps ADCs. Each of these very fast and accurate converters can jeopardize the battery lifetime if left powered-up continuously, with a 1 mA typical consumption at 5 Msps. As the ADC consumption is roughly proportional to the acquisition frequency (around 200 µA / Msps), the application can choose between two solutions to control the power consumption:

- Performing the acquisition at low speed to limit maximum current.
- Performing the acquisition at maximum speed to switch in Ultra-low-power mode earlier.

When the acquisition is performed slowly, the ADC consumption itself is reduced to few tens of µA, drastically limiting the maximum current. This is mandatory when the power source provides a limited current. The drawback, if the CPU has no other task to perform during that time, it can increase the time the system spends in run or sleep mode (or Low-power run or Low-power sleep modes) versus the time spent in Ultra-low-power mode (Stop or Standby).

Several peripherals have been developed to operate even in Stop mode, with the system clock stopped, and the main oscillator and memory powered down as detailed below:

- A pair of ultra-low-power comparators is available to monitor analog voltages with a current as low as 350 nA. These comparators can wakeup the microcontroller as soon as the external voltage reaches the selected threshold and they can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general purpose use.
- The devices embed multiple DACs, with sample and hold capability supported in Stop 1 mode. In sample and hold mode, the DAC core converts data on a triggered conversion, then holds the converted voltage on a capacitor. When not converting, the DAC cores and buffer are completely turned off between samples and the DAC output is tri-stated, therefore reducing the overall power consumption.
- An RTC peripheral provides a clock/calendar with two alarms, includes a periodic wakeup unit and several application specific functions (such as timestamp, tamper detection). It can remain enabled in the lowest power mode (shutdown), when most of the chip is powered down, and wake up the full microcontroller in case of an alarm is triggered or tamper is detected, for instance. It also contains up to 128 bytes of backup registers to store contextual information when exiting from Standby mode, or to store sensitive information as they are protected by tamper detection, and readout memory protection. This peripheral has been designed using asynchronous design techniques to minimize its consumption.

  The RTC can be clocked by two low-power, low-speed clocks:

  – LSE: the external 32.768 kHz quartz oscillator supports four power consumption modes, combined with drive capability.
  – LSI: when high accuracy is not required, the RTC can be clocked by an internal 32 kHz oscillator, with extremely low consumption. The LSI clock can be divided by "128" in order to further reduce the consumption.
- The Low-power timer (LPTIM) is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to its diversity of clock sources, the LPTIM is able to keep running whatever the selected power mode. Given its capability to run even with no internal clock source, the LPTIM can be used as “Pulse Counter” which can be useful in some applications. Also, the LPTIM is capable of waking up the system from Low-power modes. This makes it suitable to build “Time-out functions” with extremely low-power consumption. The LPTIM introduces a flexible clock scheme that provides the required functionality and performance, while minimizing the power consumption.
- The low-power universal asynchronous receiver transmitter (LPUART) is an UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock. Even when the microcontroller is in Stop modes, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption.

  Several sources are available to wake up from Stop mode can be selected:

  – Wakeup on address match
  – Wakeup on Start bit detection
  – Wakeup on received byte.

- The I^2C is able to wake up the microcontroller from Stop modes (APB clock is off), when it is addressed. All addressing modes are supported. The HSI oscillator must be selected as the clock source for I2CCLK in order to allow wakeup from Stop. During Stop mode, the HSI is switched off. When a START is detected, the I^2C interface switches the HSI on, and stretches SCL low until HSI is woken up. HSI is then used for the address reception. In case of an address match, the I^2C stretches SCL low during the microcontroller wakeup time. The stretch is released when ADDR flag is cleared by software, and the transfer goes on normally. If the address does not match, the HSI is switched off again and the microcontroller is not woken up.
- The USART is able to wake up the microcontroller from Stop 0/1 mode when USART clock is HSI or LSE. Several wakeup sources can be selected to wake the microcontroller from Stop 0/1 mode:
  - Wakeup on address match
  - Wakeup on Start bit detection
  - Wakeup on received byte.
- The USB can wake up from Stop 0/1 mode with these events:
  - Resume from Suspend
  - Attach detection protocol event.

Table 5 summarizes the peripheral features over all available modes. Wakeup capability is detailed in gray cells.

Table 5. Functionality depending on the working mode

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (512 Kbyte)	O (1)	O(1)	O(1)	O(1)	-	-	-	-	-	-	-	-	-
SRAM1 (192 Kbytes)	Y	Y (2)	Y	Y(2)	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y	Y(2)	Y	Y(2)	Y	-	Y	-	O	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
OCTOSPI	O	O	O	O	-	-	-	-	-	-	-	-	-
OTFDEC	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brown-Out Reset reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	(4)	-	(4)	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
V_{DD} voltage monitoring, temperature monitoring	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / TAMP	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	8	8	8	8	8	O	8	O	8	O	8	O	3
USB, UCPD	O(7)	O(7)	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1, 2, 3, 4, 5)	O	O	O	O	O (5)	O(5)	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O(5)	O(5)	O(5)	O(5)	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O (6)	O(6)	-	-	-	-	-	-	-
I2C3	O	O	O	O	O(6)	O(6)	O(6)	O(6)	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
FDCAN1	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1, 3 (LPTIM1 and LPTIM3)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O (7)	O(7)	-	-	-	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
HASH hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
PKA	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(8)	5 pins (9)	(10)	5 pins(9)	-

1. *The Flash can be configured in Power-down mode. By default, it is not in Power-down mode.*
2. *The SRAM clock can be gated on or off.*
3. *Four Kbytes or full SRAM2 content is preserved depending on RRS[1:0] bits configuration in PWR_CR3 register.*
4. *Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.*
5. *UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.*
6. *I^2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.*
7. *Voltage scaling Ranges 0 and 1 only.*
8. *I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.*
9. *The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.*
10. *I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.*

Note: Refer to Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 165 DMIPS, up to 512 KB Flash memory, 256 KB SRAM, SMPS (DS12737) for the latest version of Table 5.

3.5 A versatile clock management

A reset and clock controller (RCC) peripheral manages the five possible clock sources of the STM32L5 Series microcontrollers.

Two external oscillators can be used for applications requiring high precision:

- The HSE clock (4 to 48 MHz high speed external clock), typically used to feed the PLL and to generate a CPU clock frequency of up to 110 MHz. On the STM32L5 Series microcontroller, it can also be configured in bypass mode for an external clock.
- The LSE (typically 32.768 kHz low speed external clock) normally used to provide a low-power clock source to the real time clock and can also be configured in bypass mode for an external clock.

Three internal oscillators can be selected for the following tasks:

- The LSI clock (32 kHz low speed internal clock) is used to drive the independent watchdog. The LSI clock accuracy has a ± 5 % accuracy. The LSI clock can be divided by 128 to output 250 Hz as source clock.
- The HSI clock (16 MHz high speed internal clock), trimmable by software, that can supply a PLL.
- Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach an accuracy greater than ± 0.25 %. In this mode, the MSI can feed the USB device, removing the need for an external high-speed crystal (HSE). The MSI can supply a PLL.
- The RC48, internal 48 MHz clock source (HSI48), is used to drive the USB FS, the SDMMC and the RNG. This clock can be output on the MCO.

Table 6. STM32L5 Series clock source characteristics

Clock Source	Use	Frequency	Consumption (Typical)	Accuracy	Trimming	
					Factory	User
HSE	Master clock (+RTC)	4-48 MHz	-	Crystal dependent, down to tens of ppm	Not applicable	
LSE	RTC, USART LPUART, LPTIM independent clock	32.768 KHz (typical)	250 nA	Crystal dependent, down to a few ppm		
HSI	Master clock Peripheral independent clock	16 MHz	155 µA	± 0.8 % typical over - 10 to + 85 °C + 0.1/ - 0.2 % typical over 1.62 to 3.6 V	Yes	Yes
LSI	RTC and IWDG	32KHz	110 nA	± 1.5 % typical over -40 to + 125 °C + 0.5/-1.5 % typical over 1.62 to 3.6 V	Yes	No
MSI	Master clock	100 kHz 200 kHz 400 kHz 800 kHz 1 MHz 2 MHz 4 MHz 8 MHz 16 MHz 24 MHz 32 MHz(1) 48 MHz(1)	0.6 µA 0.8 µA 1.2 µA 1.9 µA 4.7 µA 6.5 µA 11 µA 18.5 µA 62 µA 85 µA 110 µA 155 µA	Default mode: + 1.5/- 1 % typical over - 10 to + 85 °C + 1.5/- 5.5 % typical for 16 to 48 MHz over 1.62 to 3.6 V PLL-mode: better than 0.25 %	Yes	Yes
HSI48	USB, RNG	48 MHz	340 nA	± 3 % max over 15 to 85 °C VDD = 3.0 to 3.6 V ± 4.5 % max over -40 to +125 °C VDD = 1.65 to 3.6 V	Yes	USB PLL

1. *Only possible in Ranges 0/1.*

Note: See Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 165 DMIPS, up to 512 KB Flash memory, 256 KB SRAM, SMPS (DS12737) for detailed electrical characteristics.

In addition, the STM32L5 Series microcontrollers embed three PLLs:

- PLL
- PLLSAI1
- PLLSAI2.

Each PLL provides up to three independent outputs and can be fed by the HSI, the HSE or the MSI, with a maximum frequency of 110 MHz. The nine outputs can be independently configured:

- System clock
- ADC interface clock
- USB clock
- Serial Audio Interface SAI1 clock
- Serial Audio Interface SAI2 clock.

This removes the peripheral constraints on the system clock. Many other peripherals, when available, can be clocked independently from the system clock: USARTx (x= 1, 2, 3, 4, 5), LPUART and I^2Cx (x=1, 2, 3, 4) receive an independent clock. This makes it possible, for example, to reduce the system and APB bus frequencies and keep the communication peripheral baud rate constant, regardless of the system clock frequency.

All peripheral clocks can be individually enabled or disabled in Run,Low-power run, Sleep and Low-power sleep modes.

The price of a crystal oscillator may not be neglected in cost sensitive applications. For this reason, the STM32L5 Series microcontrollers offer several options to measure the internal oscillators.

Although HSI and MSI are factory trimmed, they can be further trimmed in 0.5 % steps during run time to compensate for frequency deviations due to temperature and voltage changes.

When LSE is present in the application, the MSI can be automatically calibrated using the LSE (PLL-mode configuration), making it possible to reach long-term LSE accuracy. This mode can provide the USB clock with the accuracy required to operate in device mode, saving the cost of a high-speed crystal oscillator.

Moreover, when the microcontroller exits from Stop modes the system clock can be configured to be either HSI or MSI at any frequency range. This enables an exit from Stop mode directly at 48 MHz, without waiting for a PLL starting time.

4 Conclusion

The main ultra-low-power features of the STM32L5 Series microcontrollers are presented in this application note. They show the benefits offered by this microcontroller family to reduce the current consumption in embedded systems.

The STM32L5 Series microcontrollers extend the STMicroelectronics ultra-low-power family already available with the STM32L0 and STM32L1, STM32L4 and STM32L4+ Series, offering a built-in SMPS step down converter and high processing performance without compromising the power consumption.

The rich set of peripherals of the STM32L5 Series microcontrollers cover a wide range of applications, while the available Low-power modes give full flexibility to adjust on-the-fly the consumption to any task.

Revision history

Table 7. **Document revision history**

Date	Version	Changes
12-Oct-2020	1	Initial release.

Contents

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