RHFL6000 application note

Introduction

The characteristics of the voltage transient on the output of a voltage regulator, as a consequence the transfer of energy related to an ion strike with the silicon, is a very critical issue in space applications. Large undershoots can cause erratic operation in memories and microprocessors, while overshoots of excessive amplitude can lead to the degradation - or even the destruction - of CMOS devices. As an example, for most FPGA the recommended operating voltage is 1.5 V and the max. limit 1.6 V (in some applications restricted to 1.575 V to keep further safety margin). This latter applies to both static and dynamic operating conditions.

The RHFL6000 is a low-drop linear regulator designed to be immune to the single events at its output. This feature is achieved through a dedicated internal circuitry embedded for minimizing the transient at the output and the adoption of particular layout rules. However, these steps are not sufficient to achieve the mentioned target. A properly designed PCB and the selection of parts having particular characteristics is essential.

This document provides guidelines about the rules that users should comply with to get output single events < 3.3% of the absolute V_{OUT} value with the RHFL6000. In particular, these rules refer to:

- The PCB design
- The selection of the parts mounted on it

1 PCB guidelines

For a voltage regulator, the generation of pulsed currents on the output, either long or short, is among the most salient effects consequent to the single events. These currents can in turn cause voltage spikes whose amplitude is dependent on the amount and nature of the PCB impedance of the paths they flow in. In this respect, the most critical path is the one to ground. According to Section B References the duration of the worst case SET arising into the RHFL6000 is limited to 300 nsec. During this interval, one of the main causes of variation of the output is the ground bouncing caused by the currents spikes (originated by the single event in question) flowing across the ground stray inductance. Therefore, it is essential in designing a PCB to take into account the mentioned effect with a layout aiming at minimizing the parasitic impedance of the connections to GND highlighted in the scheme of fig.1 (LWix, LWox, LWgnd) On the other hand, the inductances on V_{OUT}, LW_{OUT}, these, according to qualitative simulations, act along with C_{OUTX} as a low pass filter for the load and can thus be beneficial.

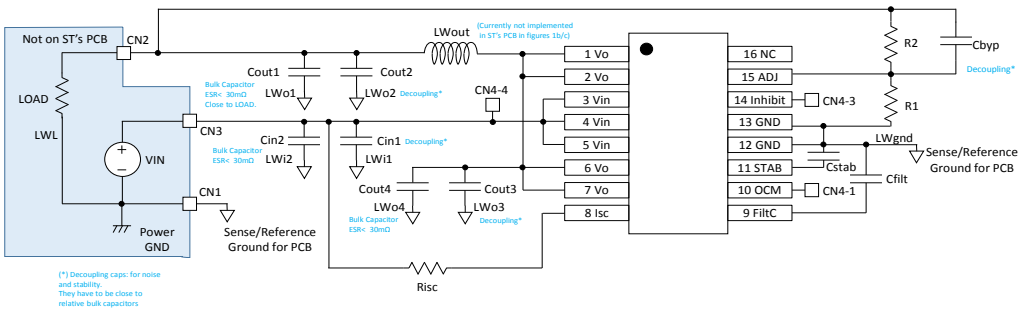
About the reduction of LWix, LWox, LWgnd, the best recommended practice is the adoption of a ground plane (at least). As it will be discussed in the Appendix, even better results can be achieved by splitting the ground in two separate planes, one for the power connections (POWER GND) and another for the Kelvin sense (SENSE GND). These two planes meet only close to the GND pin of the voltage regulator (that is thus assumed to be the “reference ground” of the system board).

For the second stray inductance considered, according to some qualitative simulations, a LWout of even some tens of nH, along with a suitable Cout, can significantly contribute to the SET mitigation for the load. An LWout of this value can be implemented on board by drawing the PCB track connecting the OUT pins to Cout1, Cout2 and Load properly.

Finally, a third rule concerns the selection of parts: these must be SMD.

A possible application scheme optimized according to the above indications is shown below. This is the board used by ST for testing the single events. Please notice that the PCB in figures 2/3 doesn’t have a power GND as the Power Supply and the Load are supposed to be connected externally through the header connectors (CN1, CN2, CN3).

Figure 1. Schematic of the board used by ST for the single event tests of the RHFL6000



Board used by ST for the single event tests of the RHFL6000: schematic see figures below, top and bottom view.

Figure 2. Layout of the board used by ST for the single event tests of the RHFL6000, top view

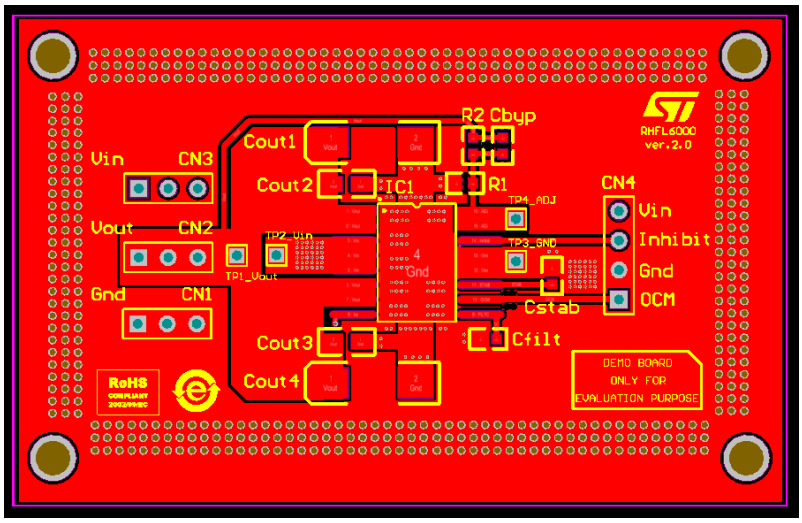
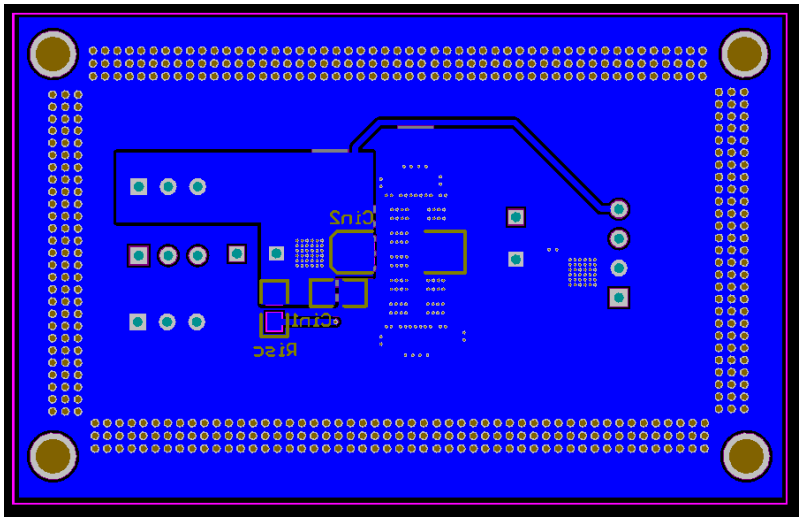


Figure 3. Layout of the board used by ST for the single event tests of the RHFL6000, bottom view



For the specific target of single event < 3.3% absolute V_{out} variation, additional rules to comply with are:

1. connect at each output port a 47 µF tantalum capacitor
2. in parallel to each bulk capacitor, connect a 100 nF, low-ESL capacitor for decoupling
3. at the output, the 100 nF cap should be mounted close to the load and, for C_{in}, close to the voltage regulator

2 Guidelines on parts selection

In line with the goal of limiting the stray inductances on GND, an important step concerns the parts selection. In this respect, table 1 shows the suggested BOM list of the components. This was adopted for the buildup of the testing PCB shown in and . In alternative, elements having similar characteristics are also suitable.

Table 1. Suggested BOM

Part	Value - package	Ordering information	Function	Manufactured	Radiospares Ref
CIN1, COUT2, COUT3	100 nF - 1206	12065F104K4T2A	Multilayer ceramic capacitors - SMD	AVX	698-3695
COUT1, COUT4	47 µF - ESR 35 mΩ - 7343-31	T520D476M016ATE035	Tantalum Capacitor - SMD	Kemet	692-5807
CIN2	100 µF - ESR 35 mΩ - 7343-31	TPME107K020R0035	Tantalum Capacitor - SMD	AVX	548-3494
CBYP	47 nF - 1210	1210J5000473KXT	Multilayer ceramic capacitors - SMD	Syfer Technology	774-0597
CFILT	22 nF - 1206	1206J5000223KXT	Multilayer ceramic capacitors - SMD	Syfer Technology	774-0556
Risc	8.2 kΩ - 1% - 0603	ERJP03F8201V	Resistor - SMD	Panasonic	721-7410

Additional guidelines

For a given capacitor, the ESL is made by two components: the first one is intrinsic, whilst the second is dependent on the mount on board (because it is related to the patterns followed on PCB by the single-event currents generated).

Therefore, in order to minimize the SETs, the following additional rules should be adopted:

- The capacitors should have the smallest possible physical size (meaning the highest possible capacitance-to-bulk volume ratio);
- Output capacitors must be physically soldered as close as possible to the output load
- Input capacitor must be located as close as possible to the chip;

In addition:

- for each I/O power terminal, it is essential to have a pair of capacitors the first of which for stability and energy storing (bulk cap.), the second for high-frequency signals bypassing;

- Finally note that, compared to a single element, an array of capacitors in parallel at both input/output terminals is expected to work better because the Equivalent Series Inductance is reduced.

For more information about the single event performances of this device, see Section B References.

A Appendix

A.1 Guidelines for grounding strategy for an optimum PCB

The generation of pulsed currents, either long or short, is among the most salient effects brought by a single event. In turn, any current exiting from the device can produce voltage spikes, depending on the amount of impedance seen on the pcb path crossed by it.

For this reason, some voltage spikes of considerable amplitude may arise during a single event.

A possible solution to minimize unwanted spikes is to split the ground plane in two: the sense GND and the power GND.

Ideally, the sense GND should be the one “clean” from noise, all low-power terminations should be connected to it. The power GND instead should be used to connect the power source(s).

- To achieve a good GND sensing, it is necessary to comply with the following rules:
  - Every node from which critical currents are expected to flow out during a single event (as the GND current originated by SE flowing out from the voltage regulator) should go to the GND reference node directly with the shortest path (also through multiple vias). This minimizes any spurious bouncing on the GND sense plane;
  - Vias buildup: in case vias are made of copper, an array of multiple structures works better compared to a single big one because of the resulting lower stray impedance;
  - Input/output capacitors: the terminals should be connected to the reference GND;
  - BOM: as already mentioned, use of good low-ESR, low-ESL parts.

B References

TRAD: Heavy Ions test report of RHFL6000 from STMicroelectronics, Sept 23, 2014.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
27-Aug-2018	1	Initial release.

Contents

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