AN5163

Application note

L9001 integration and performance evaluation

Introduction

L9001 is a highly configurable device which can easily fit in several applications with a limited number of external components. The device has many features that can be used to fulfill different application requirements. The purpose of this document is to describe these features in order to simplify the IC integration in what are considered to be the typical scenarios. Furthermore, application considerations are explained for the behaviour of the IC outside of the operative range described in the datasheet. As a reference the L9001 demo board will be used when needed.

1 Device description

The L9001 is a power management device targeting various automotive applications. This device contains three voltage regulators: VDD1, VDD2 and ADCLDO.

VDD1 is an asynchronous switch mode power supply with integrated FET and can be used as a pre-regulator for VDD2 regulator and/or to supply external devices (µC, transceiver, sensors, …). The regulated voltage can be configured to 3.3 V / 5 V or 6 V by a proper connection of CONF3 input pin. Current capability is up to 1 A, and the device provides an internal peak current limitation as protection. In addition VDD1 output voltage is monitored through VR1 pin and if the voltage goes outside the specified range, RSTN1 output is asserted low; when the fault disappears the output is released after the specified hold time.

VDD2 is a configurable power supply with integrated FET that can be used as BUCK regulator (also referenced as BUCK2 in this case) or as LDO regulator (also referenced as LDO2 in this case) to supply µC or µC core. In fact the regulated voltage is highly configurable and can be adjusted between 0.8 V and 5V by proper sizing of external divider on FB2 input pin. The BUCK/LDO choice is made instead with proper connection of CONF2 input pin. Current capability is up to 1A in BUCK mode and 300 mA in LDO mode and device provides an internal limitation according to the chosen option (BUCK / LDO). In addition VDD2 output voltage is monitored through FB2 pin and if the voltage goes outside of the specified range, RSTN2 output is asserted low; when the fault disappears the output is released after the specified hold time.

ADCLDO is a LDO power supply with integrated FET which can be used for external loads with low current demand. The regulated voltage can be configured to 3.3 V / 5 V by proper connection of CONF1 input pin. Current capability is up to 100 mA, and the device provides an internal current limitation as protection. In addition ADCLDO output voltage is monitored through VADC pin and if the voltage goes outside of the specified range, ADCMON output is asserted low; when the fault disappears the output is released after the specified hold time.

In addition to the described protection features of current limit and output voltage monitor, the device provides additional supervision and diagnosis functions: VS UV/OV, over temperature, watchdog and latch mode.

VS input voltage is monitored and if an undervoltage or overvoltage is detected with respect to the specified thresholds, the device enters a so called safe mode in which output voltages are switched off.

Device internal temperature is also monitored: when temperature increases over the specified threshold, the TWN output is asserted and, if the temperature is still increasing, the device enters a safe state.

The device has also a charge pump block which is used to ensure proper regulators functionality inside spec limits; undervoltage on CP also triggers device safe state.

The device integrates a watchdog functional block which constantly monitors the status of the microcontroller's oscillator. This is done by checking the synchronization of the microcontroller with an internal time signal whose period is configured by applying a specific capacitor at the input WDT. If the microcontroller signal, which is transmitted to the watchdog via the pin WDI, is not serving the watchdog correctly, the output pin WDO is asserted low for the specified time.

L9001 provides a feature, the so called latch state, to disable the system in case a systematic fault is repetitively detected on a charge pump structure, watchdog or thermal event. The separate fail counters and detection mechanism are explained in the device datasheet.

For low power applications the L9001 provides a LOW POWER-mode feature which drastically reduces the device power consumption while the attached loads are still supplied via bypass LDOs. This mode can be entered with STBY pin to high level as described in the dedicated section of this document. Load current is monitored in this mode and the main regulators will be automatically re-enabled in case of need.

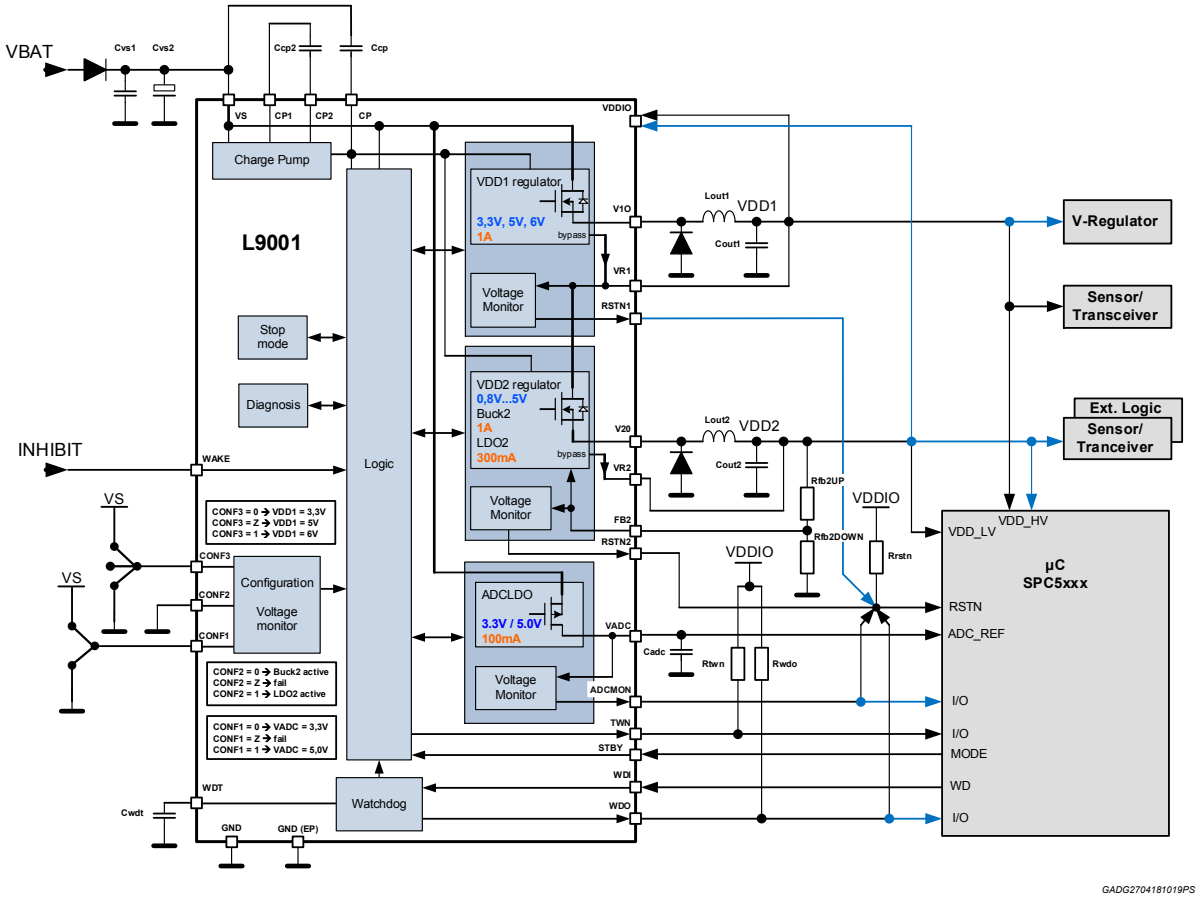
2 Application diagram

The L9001 provides several configurable blocks in order to fit many application scenarios.

The application diagram below refers to the case when both VDD1 and VDD2 regulators are used and VDD2 is configured as BUCK; so in this configuration CONF2 is fixed to GND but it's still possible to modify CONF1 and CONF3. In addition, VDDIO input needs to be connected to VDD1 or VDD2 output depending on the I/O voltage. Note that CONFx must be connected to VS after protection diode.

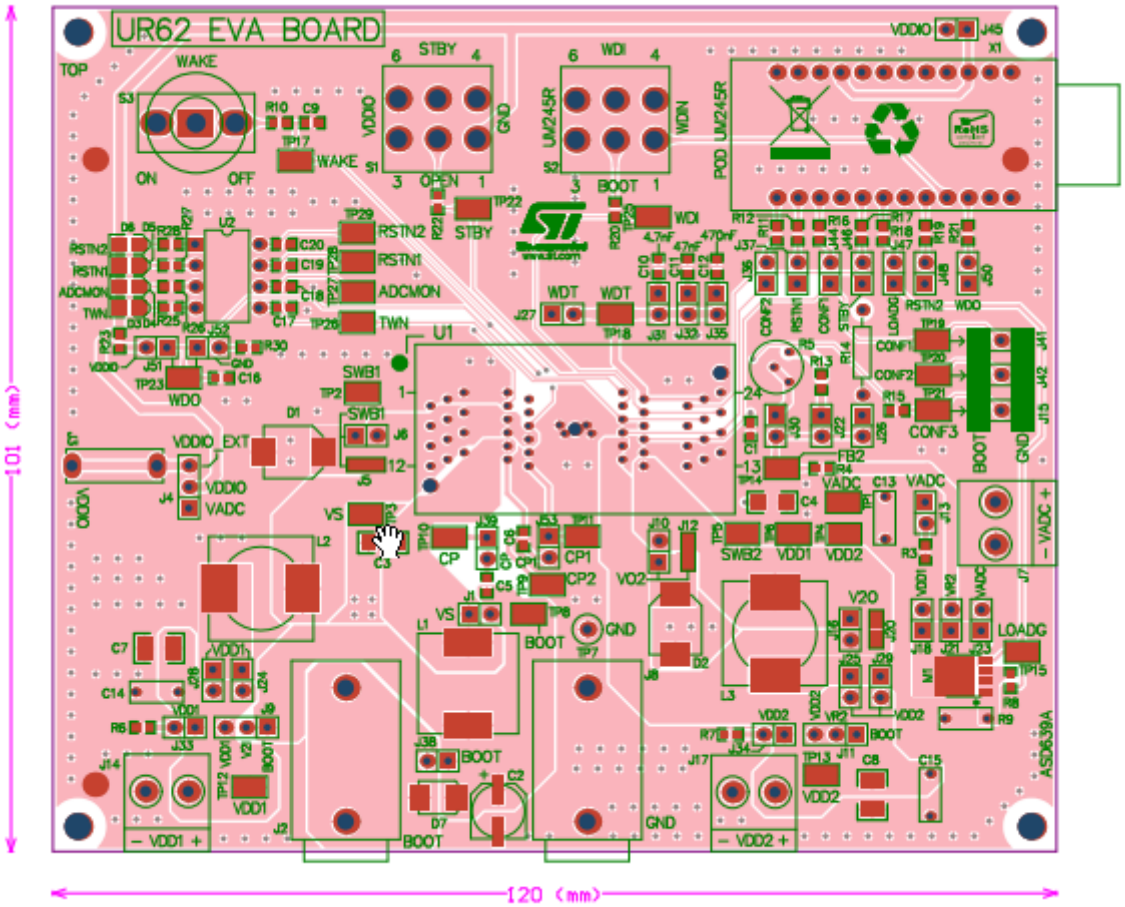
For details about configuration please refer to L9001 Datasheet and the dedicated section in this document.

Figure 1. L9001 Application configurability



As reference the demo board will be used.

Figure 2. **L9001 Demo board**



3 Functions description

3.1 Regulators

3.1.1 Power up/down sequences

L9001 is a very flexible power supply and, in order to give information about different applications, in this paragraph the power up and power down sequence will be described for different configurations, load conditions and setup.

For details about the configuration see the dedicated paragraphs.

- HW_b
  - Vdd1 = 5 V, vdd2 = 3.3 V as LDO2, VADC = 3.3 V
- HW_e
  - Vdd1 disabled; vdd2 = 3.3 V as LDO2, VADC = 5 V
- HW_c
  - Vdd1 = 5 V, vdd2 disabled, VADC = 3.3 V

Load conditions:

- No load
- Load
  - for VDD1= 5 V: 416 mA (12vΩ , 1.75W)
  - for VDD2 = 3.3 V LDO: 275 mA
  - for VADC = 3.3 V: 33 mA
  - for VADC = 5 V: 50 mA

Setup:

- WAKE and VS separated: VS = 12 V , WAKE forced on (5 V) and off
- WAKE and VS connected together [(a)] with ramp up, ramp down at VBAT (VS is the protected one)

Note: *[(a)] WAKE signal as digital input is also displayed in the scope pictures (threshold used for oscilloscope is 3.2 V unless shown along with the picture).*

3.1.1.1 *HW b*

Figure 3. Power sequence HW b, not loaded, VS=WAKE (th=3.1V), CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (1)

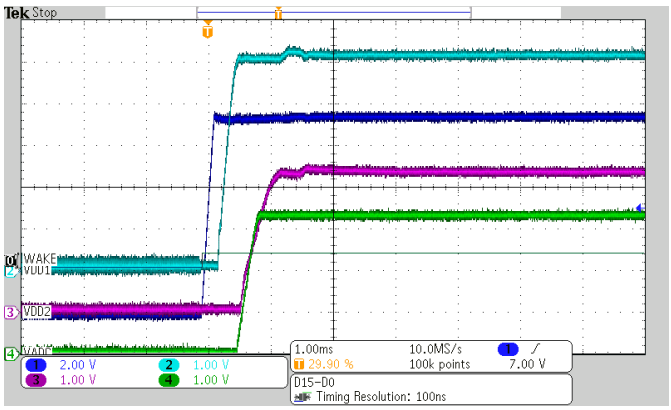


Figure 4. Power sequence HW b, not loaded, VS=WAKE (th=3.1V), CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (2)

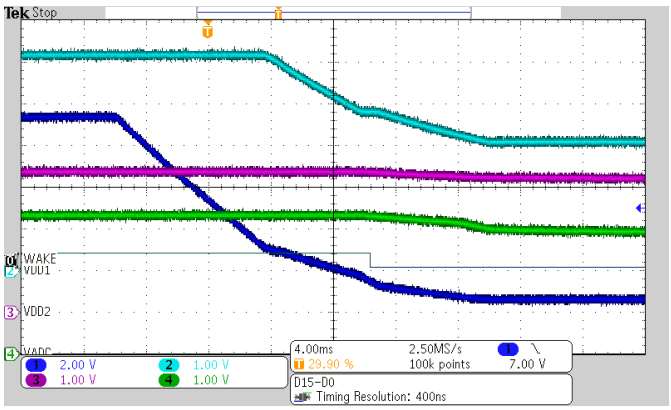


Figure 5. Power sequence HW b, loaded, VS=WAKE (th=3.1V), CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (1)

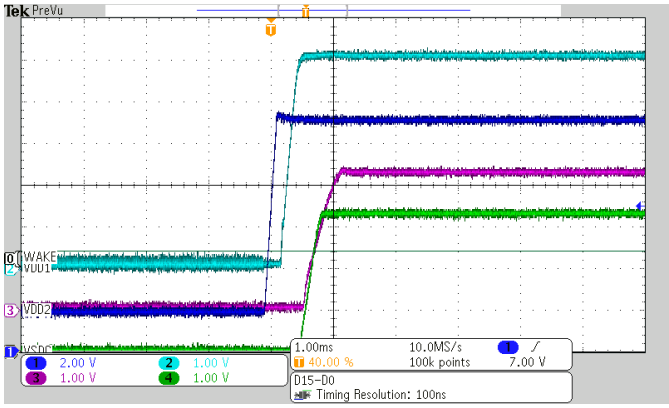


Figure 6. Power sequence HW b, loaded, VS=WAKE (th=3.1V), CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (2)

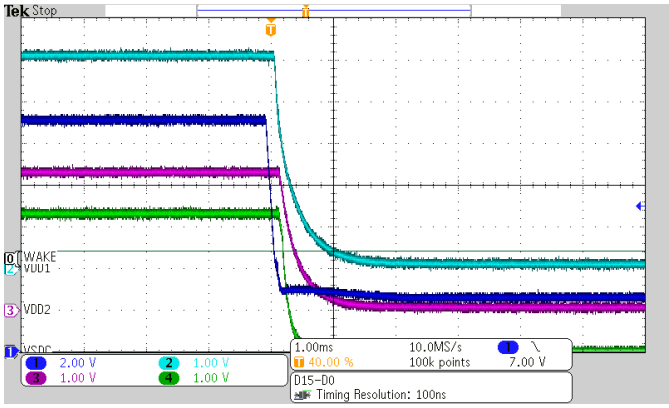


Figure 7. Power sequence HW b, not loaded, WAKE and VS separated, CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (1)

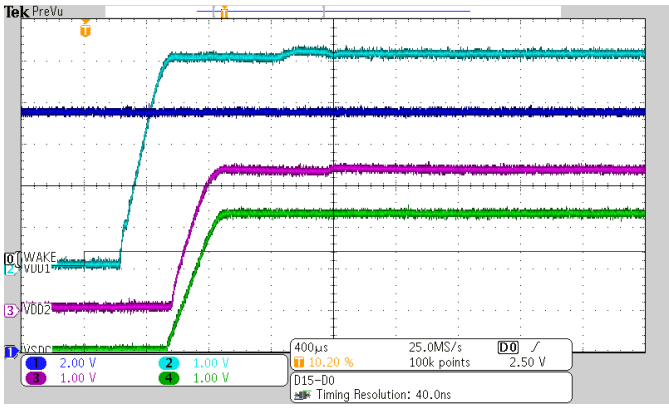


Figure 8. Power sequence HW b, not loaded, WAKE and VS separated, CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (2)

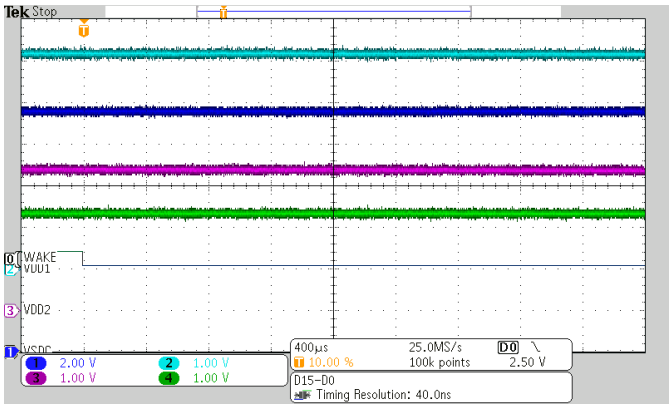


Figure 9. Power sequence HW b, loaded, WAKE and VS separated, CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (1)

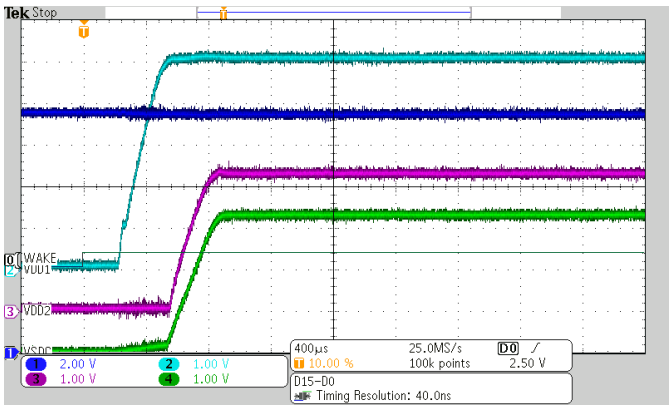
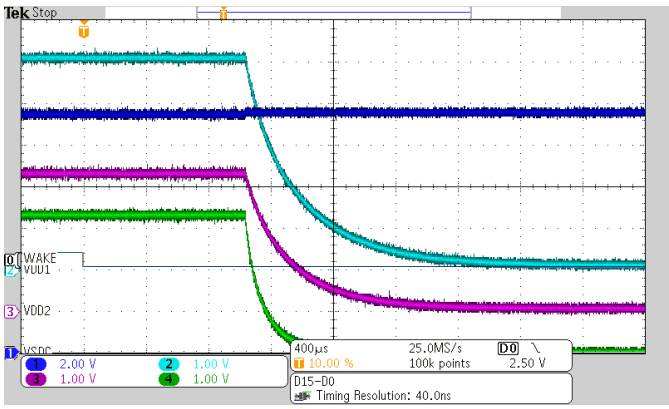


Figure 10. Power sequence HW b, loaded, WAKE and VS separated, CH1=VS, CH2=VDD1, CH3=VDD2, CH4=VADC (2)



3.1.1.2 *HW e*

Figure 11. Power sequence HW e, loaded, WAKE and VS separated, CH1=VS, CH2=WAKE, CH3=VDD2, CH4=VADC (1)

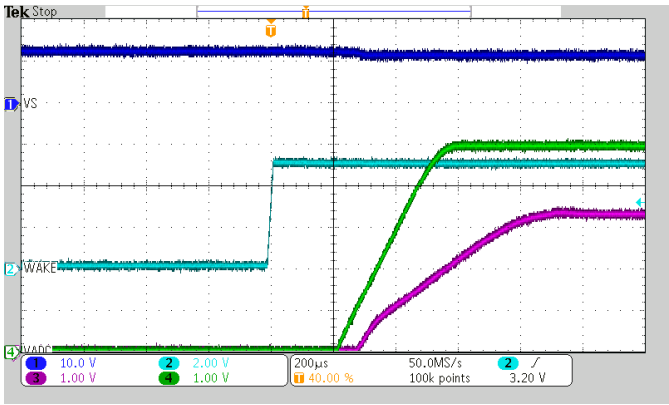


Figure 12. Power sequence HW e, loaded, WAKE and VS separated, CH1=VS, CH2=WAKE, CH3=VDD2, CH4=VADC (2)

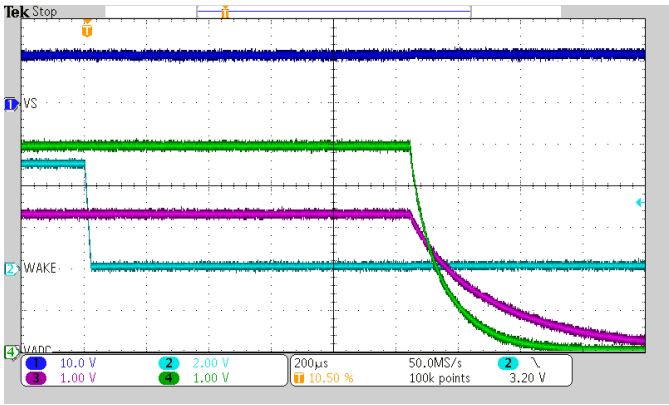


Figure 13. Power sequence HW e, loaded, WAKE = VS, CH1=VS (th = 3.1V), CH2=WAKE, CH3=VDD2, CH4=VADC (1)

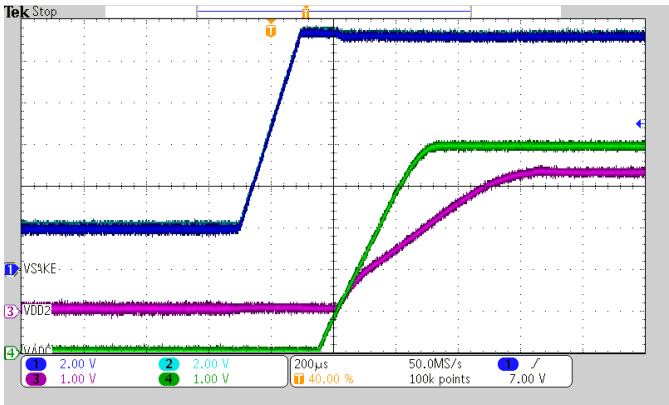
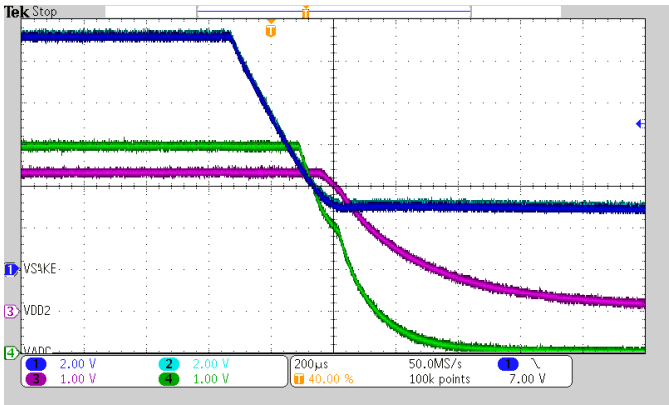


Figure 14. Power sequence HW e, loaded, WAKE = VS, CH1=VS (th = 3.1V), CH2=WAKE, CH3=VDD2, CH4=VADC (2)



3.1.1.3 *HW c*

Figure 15. Power sequence HW c, loaded, WAKE = VS (th = 3.1V), CH1=VS, CH2=WAKE, CH3=VDD1, CH4=VADC (1)

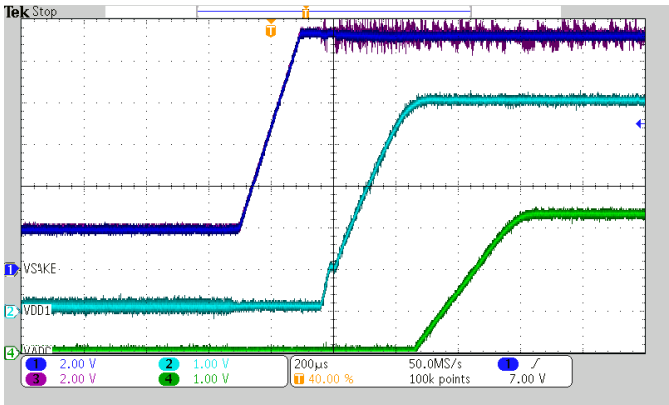


Figure 16. Power sequence HW c, loaded, WAKE = VS (th = 3.1V), CH1=VS , CH2=WAKE, CH3=VDD1, CH4=VADC (2)

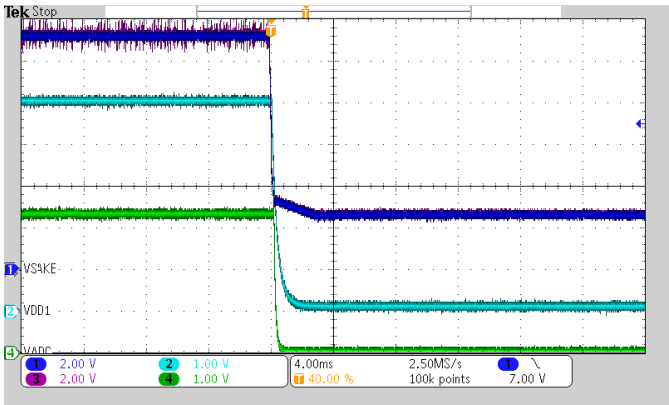


Figure 17. Power sequence HW c, loaded, WAKE and VS separated, CH1=VS, CH2=VDD1, CH3=WAKE, CH4=VADC (1)

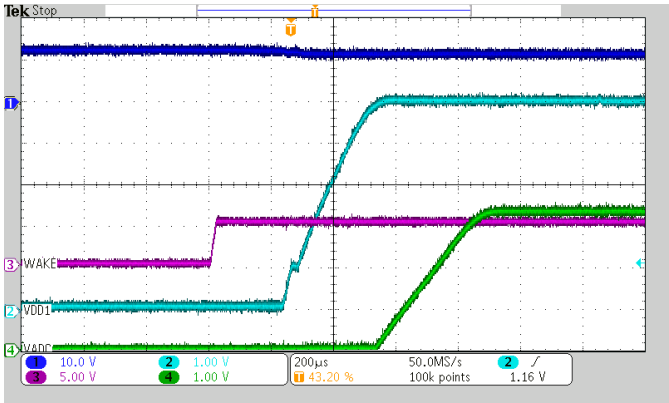
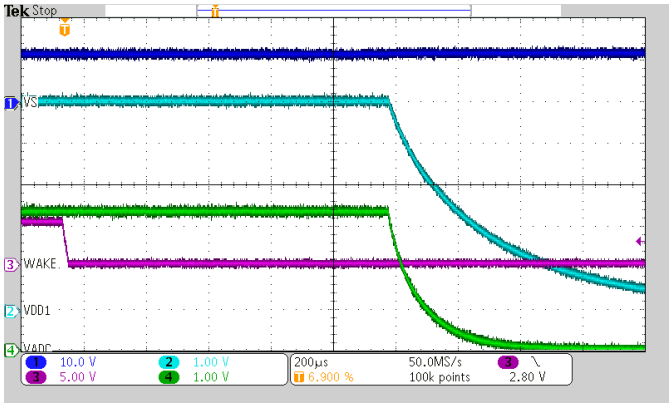


Figure 18. Power sequence HW c, loaded, WAKE and VS separated, CH1=VS, CH2=VDD1, CH3=WAKE, CH4=VADC (2)



3.1.2 VDD1 regulator

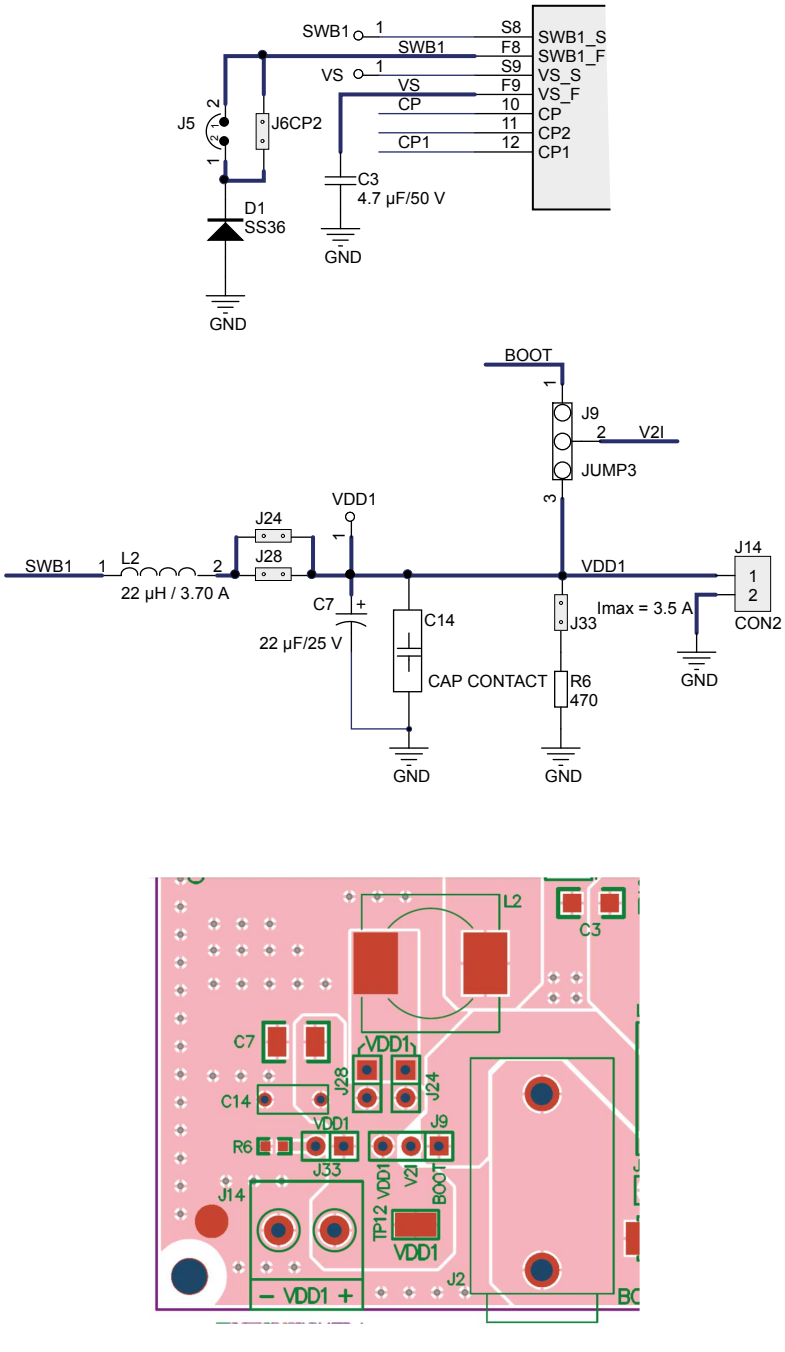
3.1.2.1 *Configuration*

VDD1 regulator is an asynchronous buck voltage regulator with integrated MOS that can used as pre-regulator for VDD2 or as direct MCU supply.

VDD1 regulator has in parallel a small bypass LDO regulator whose output is VR1; when output current goes below ILIM_BP1 the VDD1 output voltage increases as described in L9001 Datasheet.

In the next figure the application circuit with reference to application board snapshot is shown.

Figure 19. VPREREG external circuit and configuration selection



The regulator voltage can be selected as 3.3 V, 5 V or 6 V through the CONF3 input pin (see Table 1)

When the regulator operates at 5 V or 6 V, and input voltage is under 6.5 V, the output voltage may decrease due to RDSon of the internal MOS (see line regulation graphs for more details).

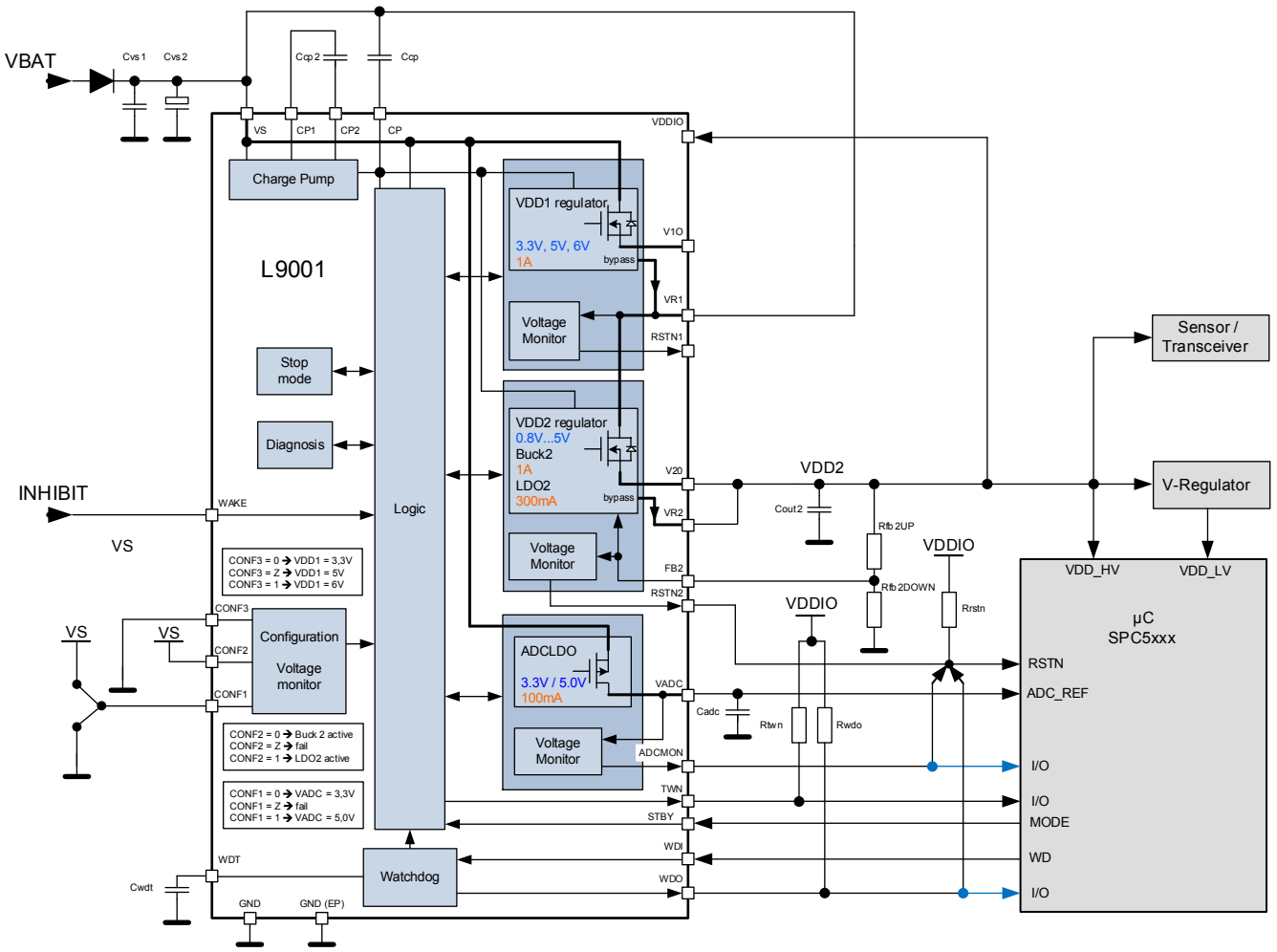
If the regulator is configured as 5 V, a sharpe line transient outside of the operative range could create overshoot at the regulator output above 5.5 V (see transient line paragraph for more details). If the microcontroller cannot sustain these spikes, an external protection should be placed.

Table 1. VDD1 configuration based on jumpers

Name	Setup	Condition	Note
J6-J5	open	VDD1 diode disconnected(allowed when VDD1 not used)	
	closed	VDD1 diode connected	
J9	P1 to P2	V2I connected to VS	VDD1 disabled
	P2 to P3	V2I connected to output of VDD1	VDD1 enabled
	OPEN	NOT ALLOWED	
J24-J28	open	Inductor disconnected (allowed when VDD1 not used)	
	closed	Inductor connected	
J15	P1 to P2	CONF3 to GND	VDD1 set to 3.3 V or VDD1 disabled
	P2 to P3	CONF3 to VS	VDD1 set to 6 V
	OPEN	CONF3 open	VDD1 set to 5 V

VDD1 can be also completely disabled if not needed by directly shorting VR1 pin to VS and connecting CONF3 to GND while leaving RSTN1 floating; in this case VREG2 is powered by VS.

Figure 20. Application diagram with VDD1 disabled and VDD2 configured as LDO



3.1.2.2 *Line*

In this paragraph line regulation plots for VDD1 are shown for the different regulation options in the VS range from 5.5 V to 18 V.

Figure 21. VDD1 line regulation (1)

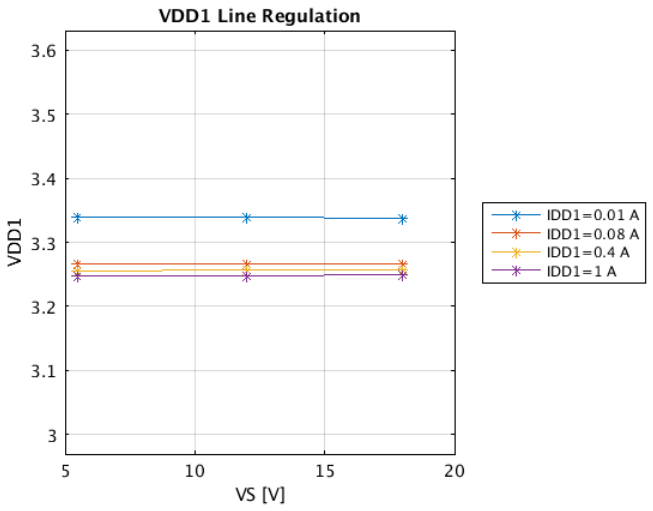


Figure 22. VDD1 line regulation (2)

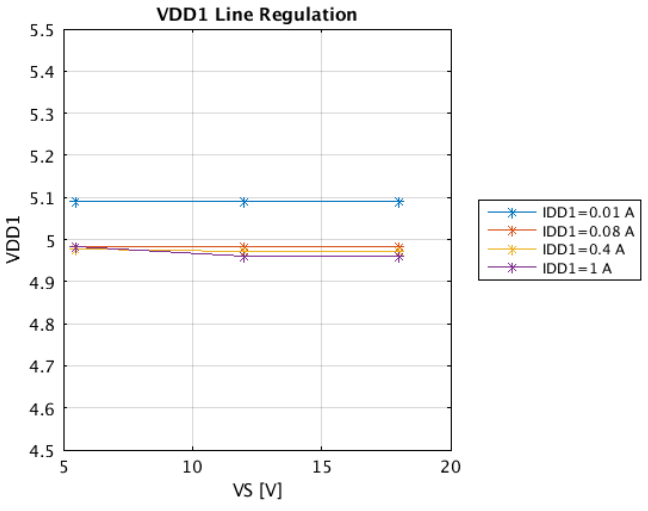
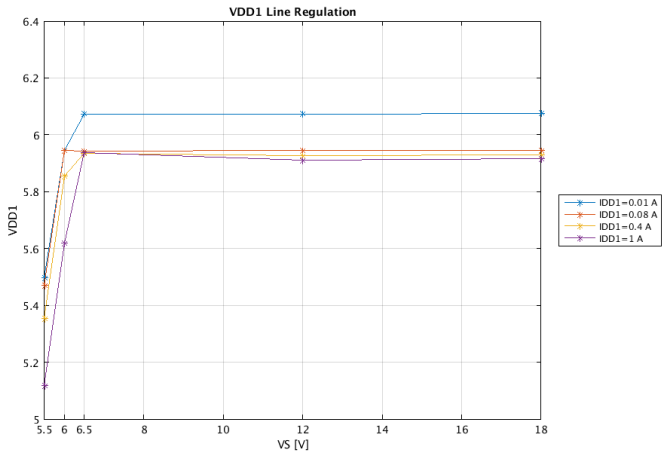


Figure 23. VDD1 line regulation (3)



3.1.2.3 *Load*

Figure 24. VDD1 load regulation (1)

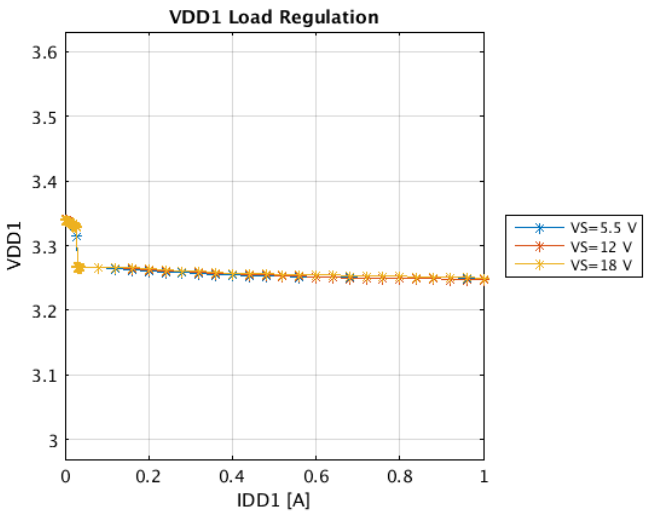


Figure 25. VDD1 load regulation (2)

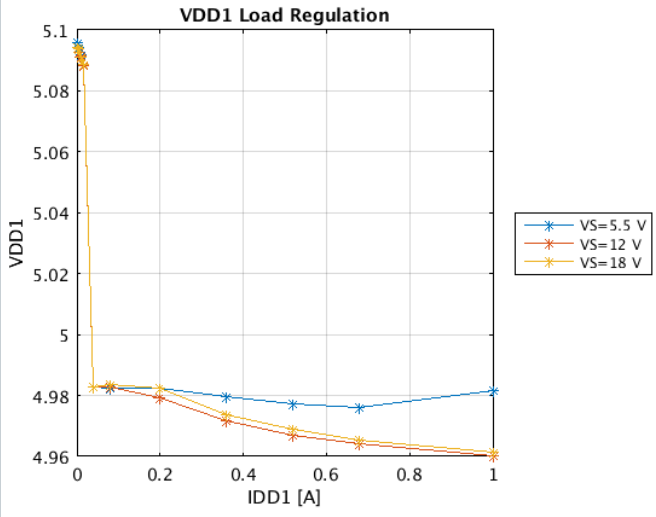
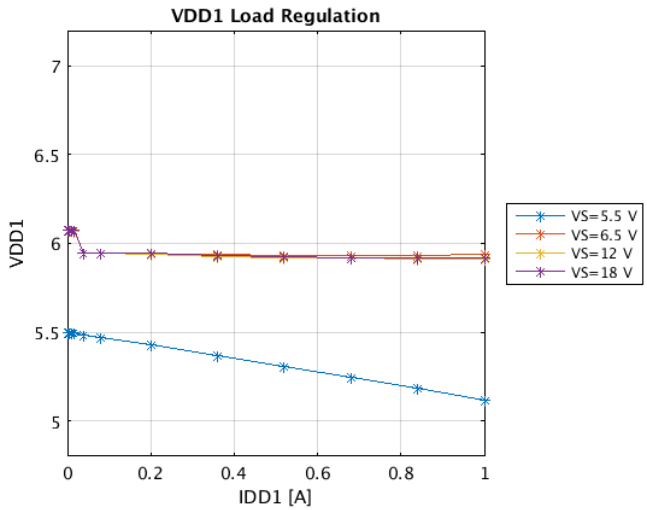
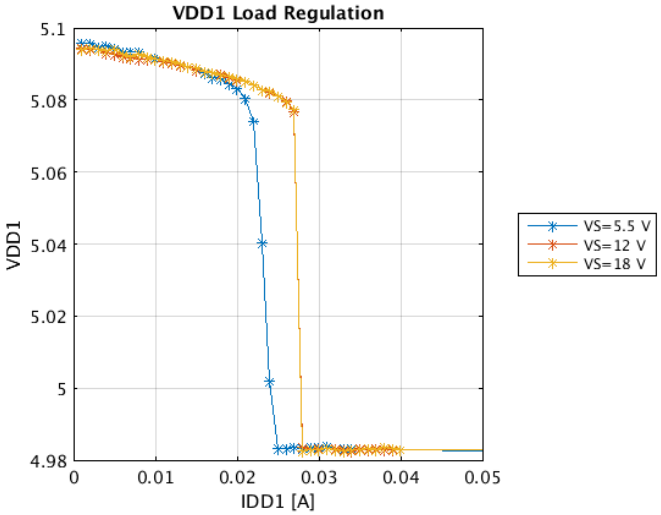


Figure 26. VDD1 load regulation (3)



A detailed view of the load regulation in the range across ILIM_BYP is shown in the next figure.

Figure 27. **VDD1 = 5V, Load regulation range 0 - 50 mA**



3.1.2.4 *Battery and load transient*

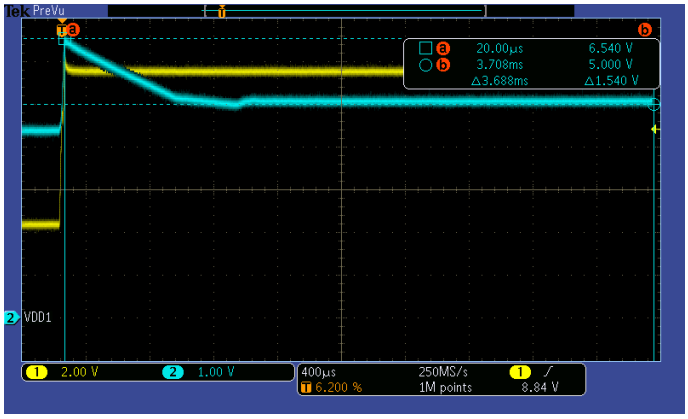
3.1.2.4.1 Line

From datasheet, Line transient is specified inside the operating range (5.5 V < VS < 18 V)

It's important to highlight here that, in case the application faces fast transient also outside of the above range, regulators output could have some overshoot also greater than 6.5 V (see the next figure for details).

If the regulator is used to directly power MCU, an external clamp must be used.

Figure 28. **Line transient outside operative range (VS : 4.2-> 12 V in 10 µs), CH1=VS, CH2=VDD1**



3.1.2.4.2 VDD1 load transient regulation

In this section typical response to load transient is shown when using external components recommended in the application diagram reported in the L9001 datasheet.

The load transition is specified in the datasheet for current greater than Ilim_bp1; in case the application requires transient in the full output current range, the regulator may have a slower response and the output voltage may significantly drop. In this case a possible solution would be to put an external fixed load R < Vnom/ Ilim1_bp1(max).

Otherwise it must be guaranteed at application level that when load transition happens the MCU is not reset and operation is not influenced by the output voltage change (IC reset could not be given anyway because of 200 µs typ filter time). For example, if current load is 1 A and then it decreases to 0 mA in 10 µs, the regulator output could exhibit an overshoot due to loop recovery and this could be eventually dangerous for the application. A proper action should be taken in order to maintain transient behaviour inside the required ranges.

To analyse performances of the regulator VDD1 a 2-steps current profile has been used. This kind of waveform simulates the typical wake up of a microcontroller.

The first current step (rise from 0 A to 50 mA in 10 µs) emulates the first phase of MCU waking up from sleep, where only a set of basic peripherals are switched on. The second step (from 50 mA to 400 mA) besides, takes into account the phase of the complete wake up occurred.

In the Figure 29 (VDD1 = 3.3 V, VS = 12 V, room temperature) it is reported the VDD1 transient load regulation in the case of Low Power disabled. The device is not entering in Low Power mode because the STBY pin is forced at low value. The same situation showed Figure 30 highlights the voltage drop on VDD1 on an increased scale (AC coupling mode). Besides, a case of IC exiting from low power mode is also reported: Figure 31 shows the case in which VDD1 is moving from Low Power to normal mode, because of the rising current profile applied (STBY pin was forced high).

As a result, for the application which needs to sustain sharp load transient across the whole working region the user may mount an additional cap on VDD1 output, whose value shall be trimmed in application based on the current profile needed during the transition sleep-normal mode.

Figure 29. VDD1 transient load response

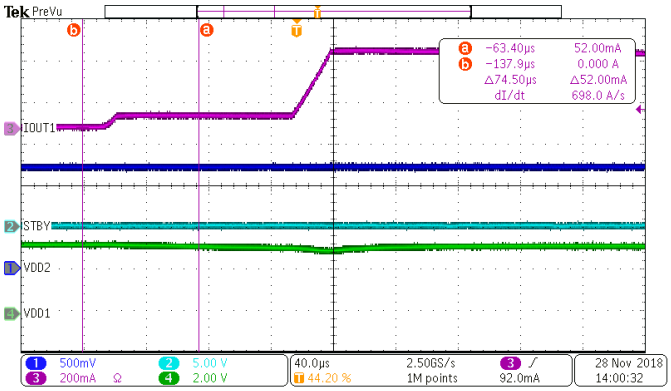


Figure 30. VDD1 transient load response CH4 in AC coupling

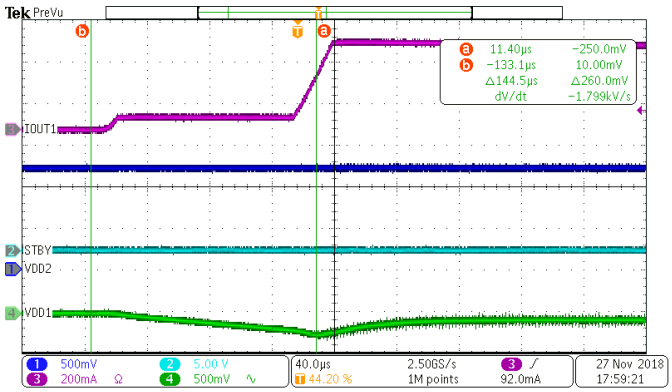
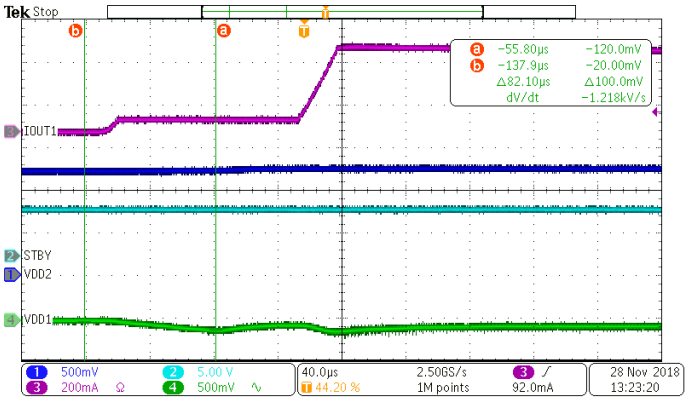


Figure 31. VDD1 transient load response when moving from Low Power to normal mode



3.1.2.5 *Efficiency plots*

In this paragraph efficiency plots for VDD1 are shown for the different regulation options in the output current range from 50 mA to 1 A.

Figure 32. Eff1 as function of load current, VDD1 = 3.3 V

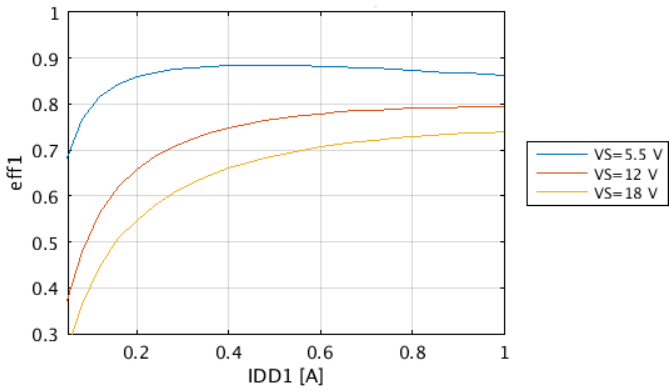


Figure 33. Eff1 as function of load current, VDD1 = 5 V

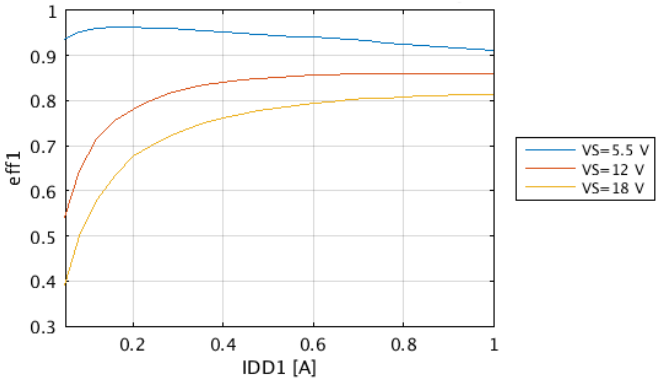
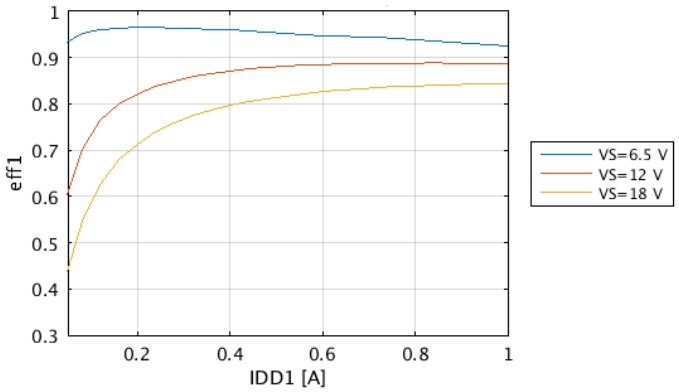


Figure 34. Eff1 as function of load current, VDD1 = 6 V



3.1.3 VDD2 regulator

VDD2 regulator is a BUCK/LDO configurable regulator with output voltage adjustable in a range 0.8 V to 5 V (3.3 V to 5 V in case of VR1 connection direct to VS)

3.1.3.1 *Configuration*

The BUCK or LDO mode is selected by CONF2 pin depending on jumper settings (see Figure 35. VDD2 external circuit and configuration selection)

Figure 35. VDD2 external circuit and configuration selection

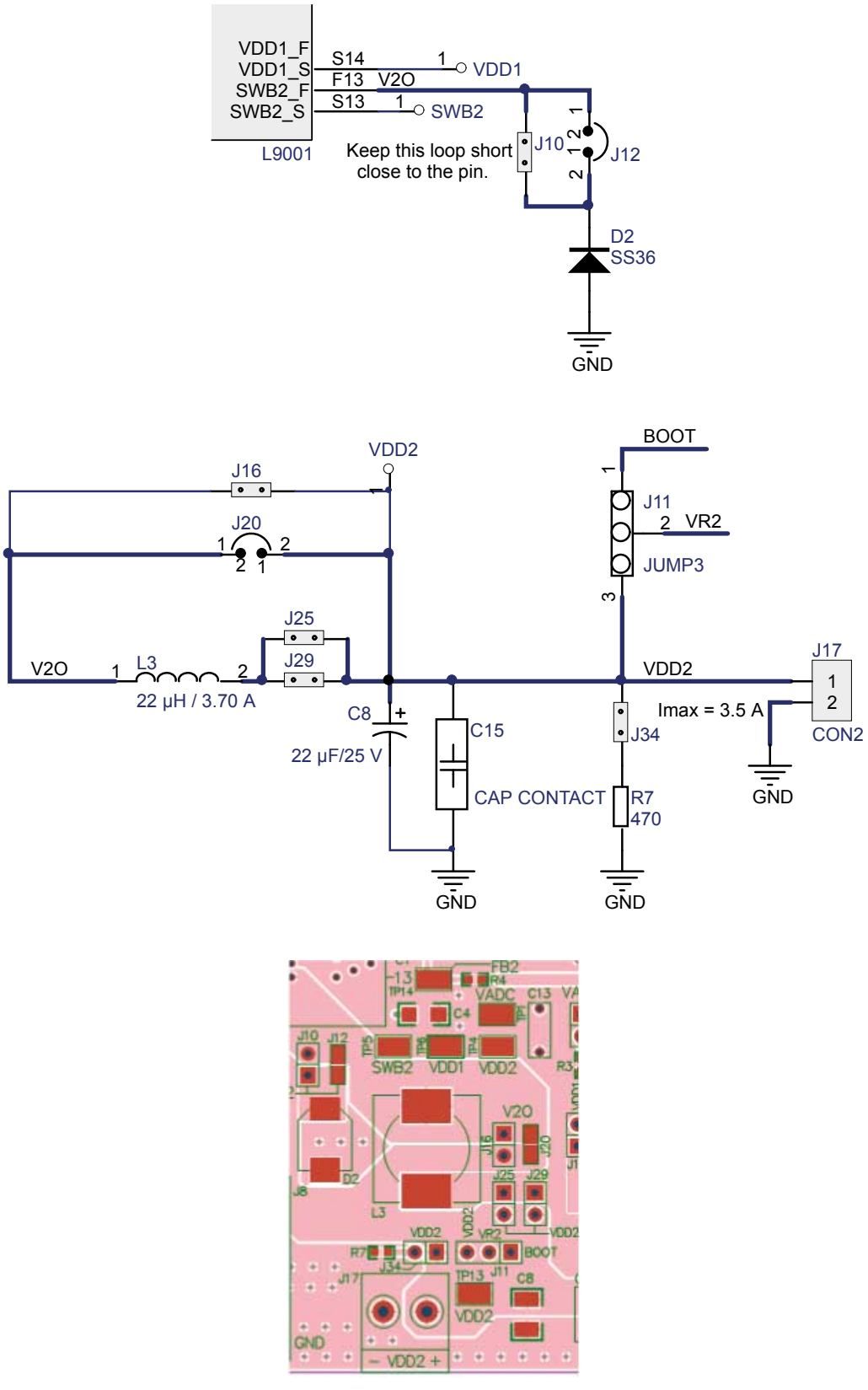


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Table 2. VDD2 configuration based on jumpers

Name	Setup	Condition	Note
J10-J12	open	VDD2 diode disconnected – LDO mode	
	closed	VDD2 diode connected – BUCK mode	
J42	P1 to P2	CONF2 to GND	VDD2 set BUCK mode
	P2 to P3	CONF2 to VS	VDD2 set to LDO mode
	OPEN	NOT ALLOWED	
J25-J29	Open	Inductor disconnected	VDD2 set to LDO mode
	Close	Inductor connected	VDD2 set BUCK mode
J16-J20	Open	VDD2 not connected to V20	VDD2 set BUCK mode
	Close	Inductor connected	VDD2 set BUCK mode
J11	P1 to P2	FB connected to VS through VR2+R4	VDD2 disabled
	P2 to P3	VR2 connected to VDD2	

The output voltage is selected by adjusting external divider on FB2 as shown in the equations below; for example on the Application Board the external feedback network values are chosen to generate a VDD2 = VDD_TGT where VDD_TGT = 1.2 V or VDD_TGT = 5 V[(b)] and FB2 = 0.8 V.

Note: *[(b)]The trimmer R5 can be adjusted to have 3.3 V output*

$$CASE\ \#\ 1 \rightarrow VDD2 = \frac{R_4 + R_{14}}{R_{14}} * \mathrm{FB2} \cong 5V \quad (1)$$

$$CASE\ \#\ 2 \rightarrow VDD2 = \frac{R_4 + R_{13}}{R_{13}} * \mathrm{FB2} \cong 1.2V \quad (2)$$

It's important to note that the nominal voltage designed with this calculation will be the regulator output voltage at high load; for small current load (below the ILIM_BYP2), the regulator enters bypass mode and so output voltage is increased above the nominal designed value VDD_TGT according to the FB2_byp parameter.

If the application requires a lower design value also at small load, the FB2 divider can be designed for example to regulate a value less than VDD_TGT in order to compensate the drift at low current.

Figure 36. VREG2 Feedback divider options

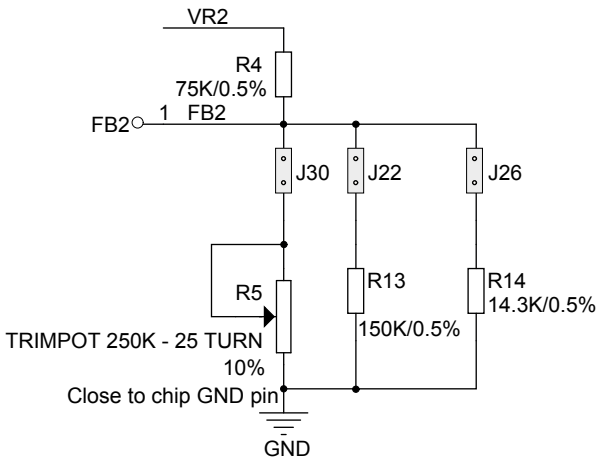

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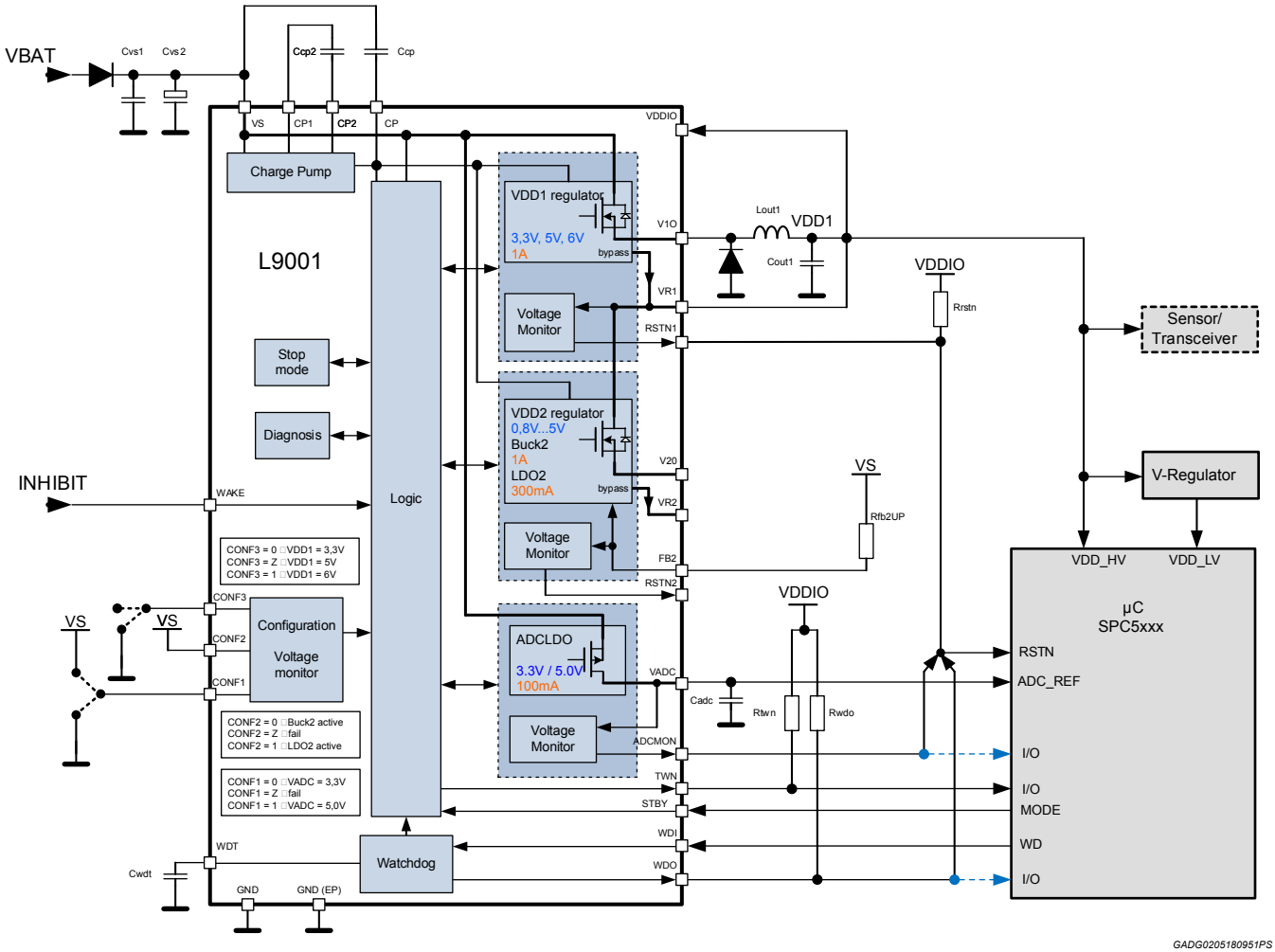
Table 3. VDD2 configuration based on jumpers J22, J26 and J30

Name	Setup	Condition	Note
J30	Open	VDD2 not connected to TRIM R5	
	Closed	VDD2 connected to R5	
J22	Open	VDD2 not connected to R13	
	Close	VDD2 connected to R13 (1.2 V opt)	
J26	P1 to P2	VDD2 not connected to R14	
	P2 to P3	VDD2 connected to R14 (5 V opt)	

The regulator can also be disabled by shorting FB2 pin to VS.
In this case the following setup is used at pin level:

- CONF2 = VS
- V20 = OPEN
- VR2 = OPEN
- FB2 = connected to VS (eventually w 10k pull up)
- RSTN2 = OPEN

Figure 37. Application diagram with VDD2 disabled



3.1.3.2 *LDO output cap considerations*

The regulator provides a soft start circuit which is able to gradually increase the output voltage with a controlled slope whose maximum slew rate is reported on DS.

Table 4. Soft start control

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SS2	Soft start control	LDO (20%-80% of VR2)			10.5	V/ms

This parameter is intended for all values of VDD2 output voltages and so the maximum is referred to the 5 V nominal output voltage which is the worst case because of the fixed soft start time on FB2.

In the following table it's shown the V/ms for various output voltage in linear mode:

Table 5. V/ms for various output voltage in linear mode

Nominal output voltage [V]	Max Slew rate [V/ms]	Avg Measured [V/ms]
5	10.5	8.5
3.3	8	5.5
1.2	3.5	1.9

If we assume capacitive load at startup, the regulator will increase its voltage linearly following the slew rate SR_Vo and so output cap will be charged with a current C_{out} * SR_Vo.

Increasing the output capacitor, the current requested to the regulator will increase and for a critical value of Cout, the regulator enters current limitation and slope is fixed to I_{lim}/C_{out}.

The drawback of increasing the C_{out} beyond the critical value (LDO mode) is that when the output voltage reaches the nominal value, the loop is unbalanced and output cap is still charged above the nominal output voltage until it recovers.

Calculation of critical capacitor is shown in the next table for measured I_{lim} of 0.35 A.

Table 6. LDO2 critical cap

Nominal output voltage [V]	Avg Measured [V/ms]	Critical Cap [µF]
5	8.5	41
3.3	5.5	63
1.2	1.9	184

For example in case of VDD2 = 3.3 V, a start-up with different capacitor values is shown.

Figure 38. Power up of LDO2 with Cout2 = 10 µF load capacitor

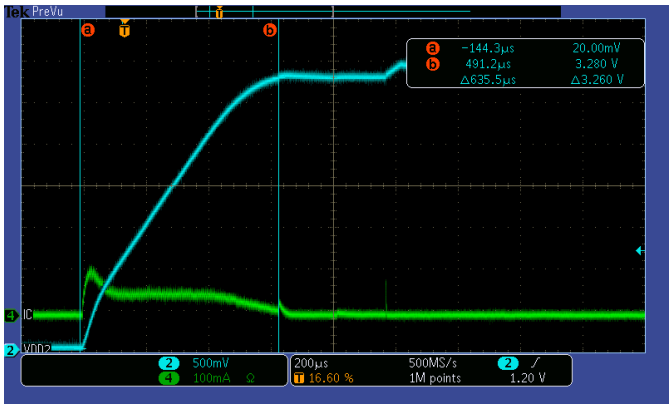


Figure 39. Power up of LDO2 with Cout2 = 22 µF load capacitor

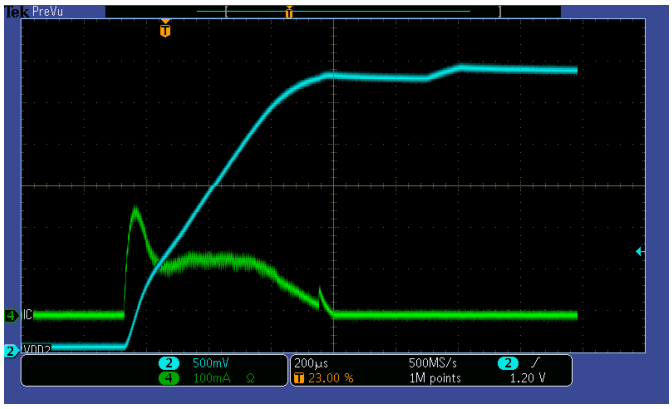
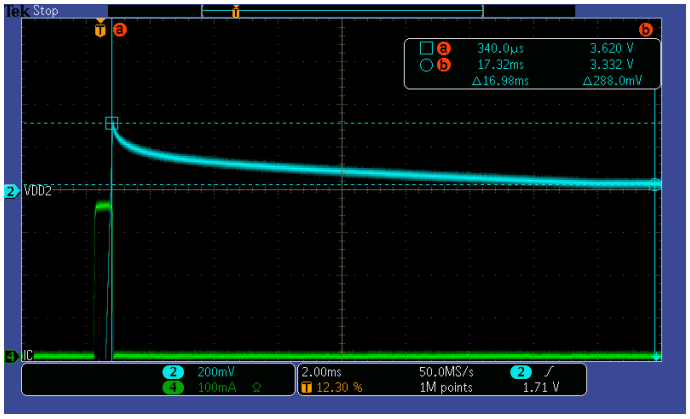


Figure 40. Power up of LDO2 with Cout2 = 67 µF load capacitor



3.1.3.3 *Line*

In this paragraph line regulation plots for VDD2 as BUCK2 are shown for the different regulation options (3.3 V and 5 V) in the VS range from 5 V to 18 V. As reference, also LDO at 3.3 V is shown.

Figure 41. VDD2 BUCK, line regulation (3.3 V)

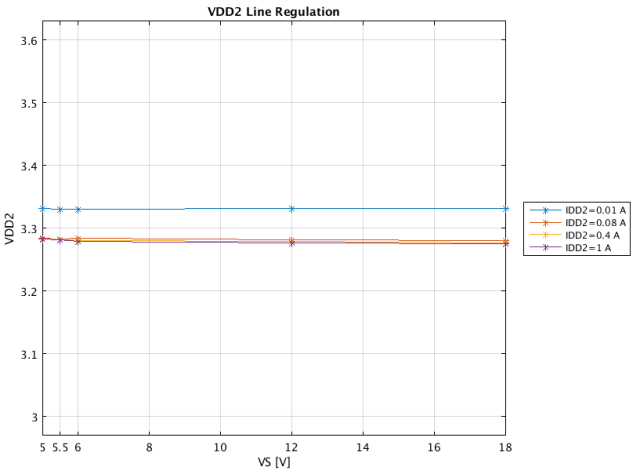


Figure 42. VDD2 BUCK, line regulation (5 V)

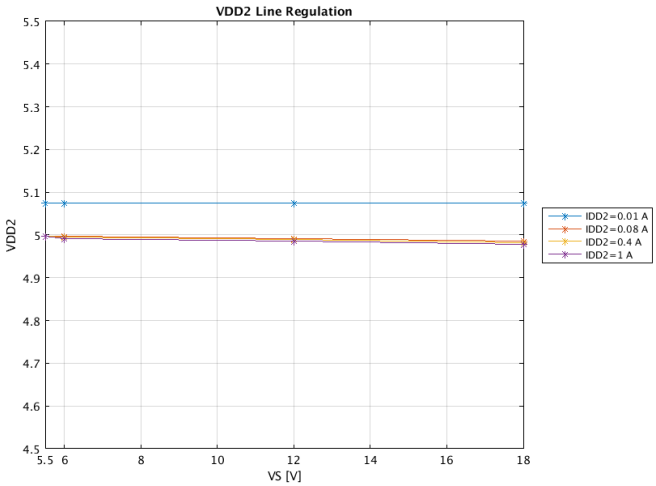
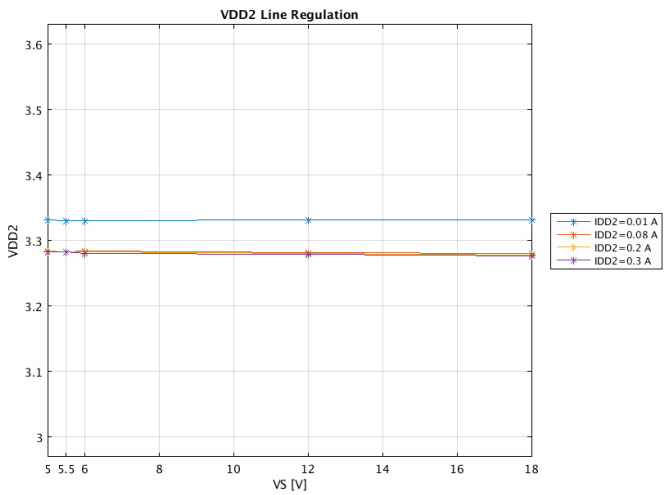


Figure 43. VDD2 LDO, line regulation



3.1.3.4 Load

Figure 44. VDD2, BUCK load regulation (1)

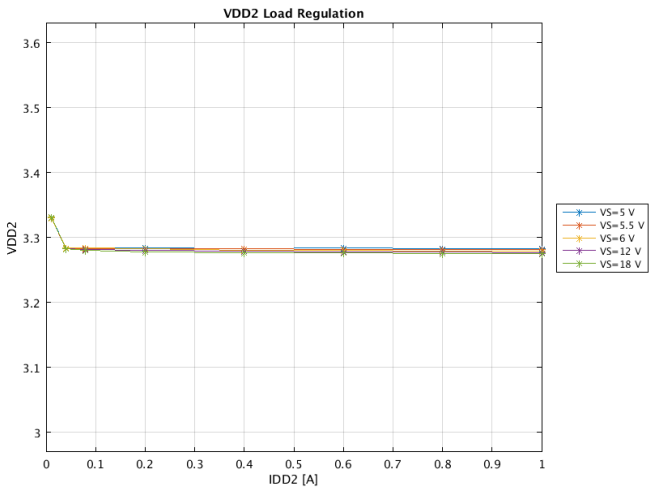


Figure 45. VDD2, BUCK load regulation (2)

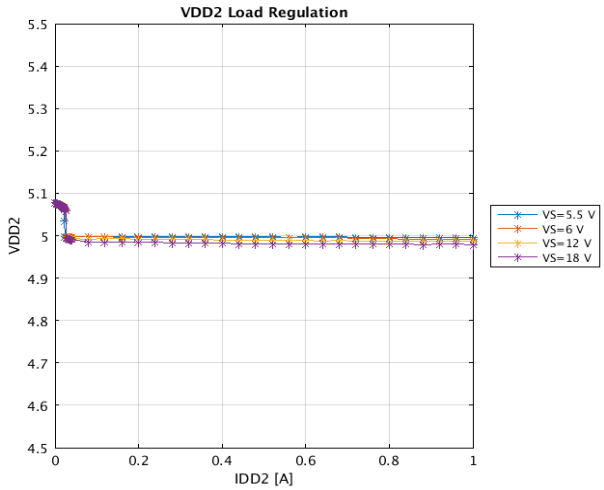
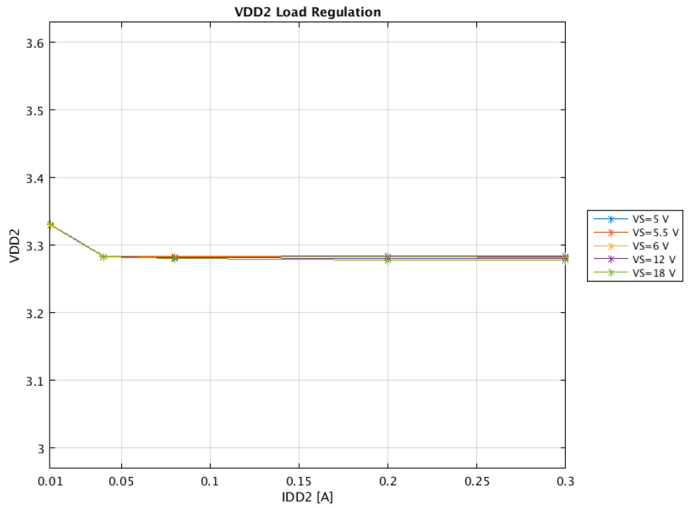


Figure 46. VDD2, LDO load regulation



3.1.3.5 *Battery and load transient*

3.1.3.5.1 Line

In case VDD2 is attached directly to battery, line transient could be relevant; in this case it can be applied the same consideration as Section 3.1.2.2 Line .

3.1.3.5.2 VDD2 load transient regulation

For VDD2 regulator, the user shall take care of avoiding transient load condition to generate uv/ov that can be an issue for the microcontroller as described also for VDD1 regulator (see Section 3.1.2.4.2); in particular when low nominal voltage is used (1.2 V) high capacitance may be needed to reduce the eventual voltage drop.

Also for regulator VDD2 the two steps current profile has been used, according to the consideration reported in Section 3.1.2.4.2 .

In the Figure 47 (VDD2 = 1.2 V, VS = 12 V, room temperature) it is reported the VDD2 transient load regulation in the case of Low Power disabled. The device is not entering in Low Power mode because the STBY pin is forced at low value. Moreover, the Figure 48 shows the case in which VDD2 is exiting from Low Power mode, during the rising current profile.

Figure 47. VDD2 load transient regulation no Low Power exiting (STBY low value)

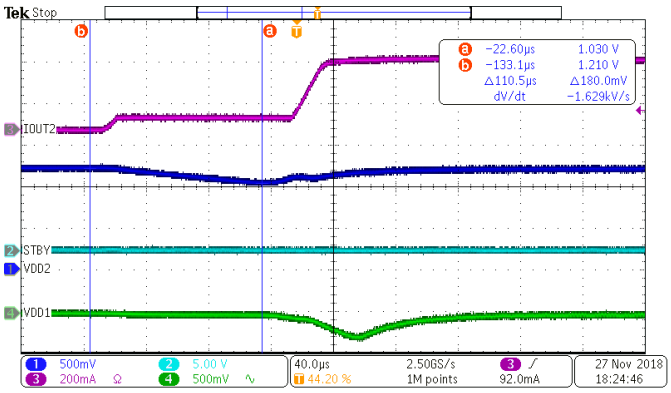
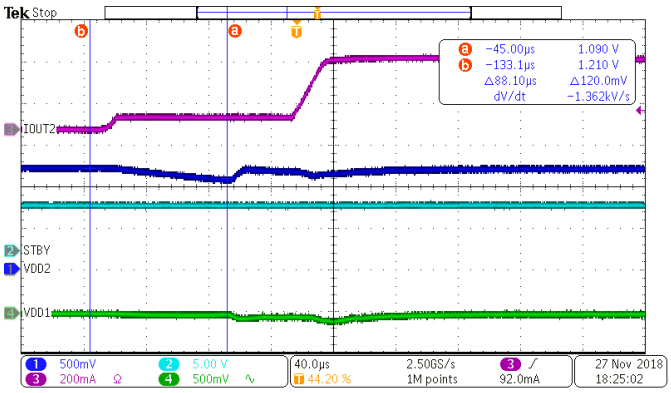


Figure 48. VDD2 transient load regulation Low Power exiting (STBY high value)



3.1.3.6 *Efficiency plots*

In this paragraph efficiency plots for VDD2 as BUCK2 are shown for the different regulation options (3.3 V and 5 V) in the output current range from 50 mA to 1 A.

Figure 49. VDD2 = 5 V efficiency plot

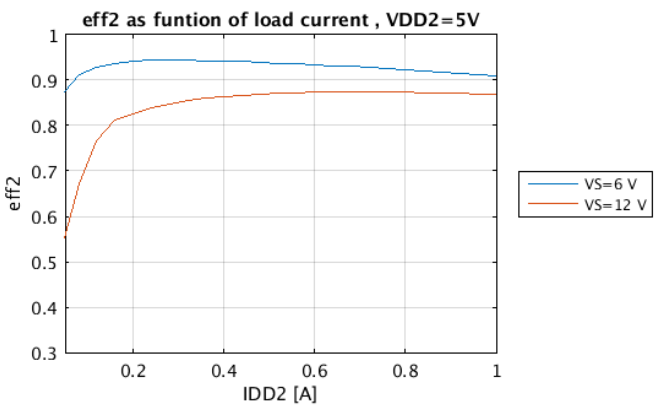
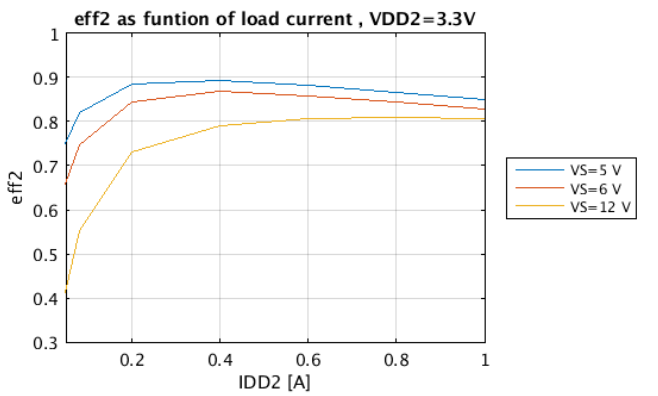


Figure 50. VDD2 = 5V efficiency plot



In case VDD2 is used as linear regulator, power dissipation could be evaluated with the following equation (where VR1={VS,VDD1} depending on the connection) :

$$Pd = (VR1-VDD2)*IDD2$$

3.1.4 ADCLDO

L9001 offers functional configurability for VADC voltage through CONF1 device pin:

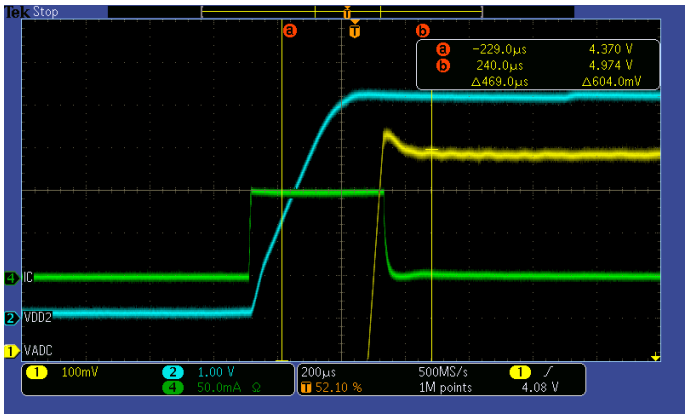
- CONF1 voltage connected to VS selects 5 V output
- CONF1 voltage connected to GND selects 3.3 V output

3.1.4.1 *Output cap considerations*

For ADCLDO it can be applied the same consideration as for LDO2.

For example if 10 µF are placed at the output in parallel to 1 µF as a stability capacitor, a small overshoot (about 60 mV) appears as depicted in Figure 51 (offset is placed on CH1).

Figure 51. ADCLDO power up with 10 µF cap



3.1.4.2 *Disable workaround*

VADC reg cannot be disabled; if it's not needed the following setup is used at pin level:

- VADC = min external cap (1 µF)
- CONF1 = VS (eventually w 10k pull up)
- ADCMON = OPEN

3.2 WD

L9001 has a configurable watchdog with adjustable timing.

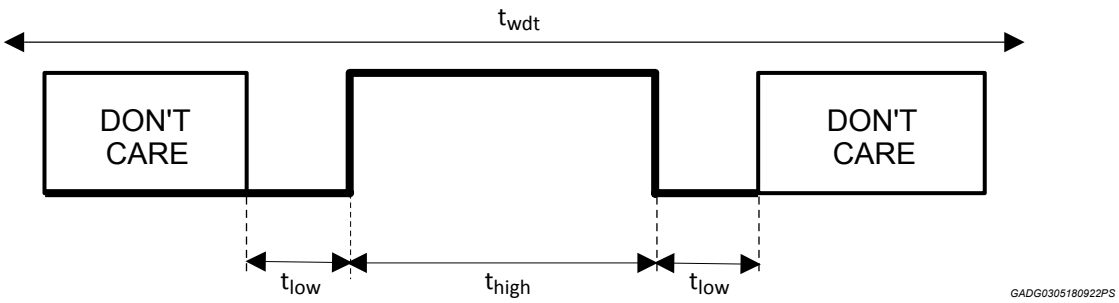
As soon as the reset of the active regulators is released and WD is enabled, the device opens a long window in which the watchdog must be served; if the WD is correctly served within this window (i.e. within the minimum time of the window duration), the device opens subsequent normal windows.

In order to serve the watchdog, WDI has to toggle from low state to high state within the expected window (see the below figure for details); if this is not accomplished, the device asserts WDO pin for t_{WDO} (16 ms typ).

t_{low} > twdi_l_max

t_{high} > twdi_h_max

Figure 52. Watchdog time diagram



The window duration t_{WDT} can be set by external capacitance at pin WDT. This capacitor establishes both the normal window and the long window reference working point:

- Normal window duration = t_{WDT}(47 nF) * Cwdt/47 nF
- Long window duration = 10 x Normal window duration

Besides, taking into account also the capacitor tolerance, the effective values t_{WDT}(Cwdt) and t_{WDT_lw}(Cwdt) are derived.

The following steps are required in order to calculate the generated windows:

1. Calculate t_{WDTRWP} i.e. the reference working point values (min, typ, max) using the formula:

   t_{WDTRWP}(Cwdt) = t_{WDT}(47 nF) * Cwdt/47 nF

2. Extract t_{WDT} tolerance from Cwdt tolerance using Figure 53
3. Calculate t_{WDT} timings using the following relationship:

   t_{WDT}(min) = t_{WDTRWP} (min) * (1-twdt_toll)

   t_{WDT}(max) = t_{WDTRWP} (max) * (1+twdt_toll)

For example if a Cwdt = 4.7 nF with 5% tolerance is placed on WDT pin:

1. t_{WDTRWP}(4.7 nF) = 3.5 ms | 4 ms | 4.5 ms (min|typ|max)
2. twdt_toll(Ctoll = 5%) = 0.14 from Figure 53
3. the values in the Table 7 and Table 8 are derived

So in this example, at startup the microcontroller must be correctly initialized and able to serve the WD within 30 ms ; after that, the WD must be served within the 3 ms window duration time.

The external capacitor must be chosen sufficiently high to allow that microcontroller could be initialized in order to correctly serve the long window within tWDT_lw (min).

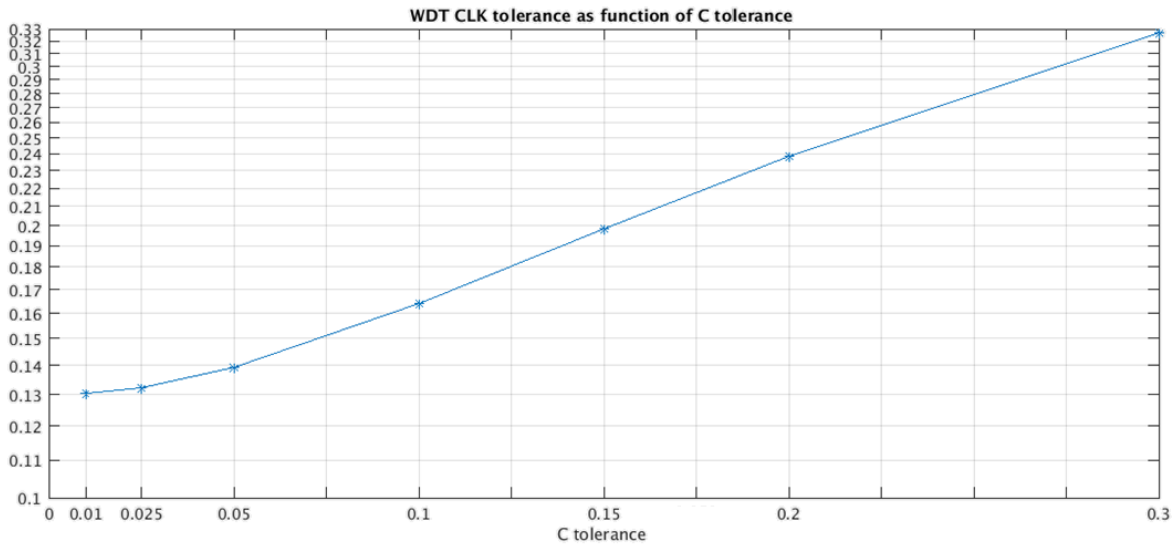
Table 7. Cwdt vs. t_{WDT} duration time

	t_{WDT} (min)	t_{WDT} (typ)	t_{WDT} (max)	Unit
Cwdt = 4.7 nF ±5%	3	4	5.2	ms

Table 8. Cwdt vs. tWDT_lw duration time

	t_{WDT_lw} (min)	t_{WDT_lw} (typ)	t_{WDT_lw} (max)	Unit
Cwdt = 4.7 nF ±5%	30	40	52	ms

Figure 53. t_{WDT} tolerance



The WD can be disabled by entering FLASH mode and this means apply on WDT pin a voltage grater than 8 V (for example VS); in this case WDI must be connected to GND.

If WD is not needed even at low VS battery (i.e. VS = 5.5 V) and no other voltages are present in the application above 8 V, both the WDI and the WDT pin can be connected to GND.

There is a slight difference between the previous connection of WDT (to VS) and the connection to GND: while in the first case the device switches to FLASH mode where WD_FC is permanently kept to 0, in the latter case, the device is still in ACTIVE mode but the WD counter and WD_FC are freezed and so the watchdog doesn't affect the device operation.

3.3 Low power mode

L9001 is capable of operating in a reduced consumption mode, the so called Low power mode.

In this mode the current consumption is reduced to **I_LPM** (see L9001 datasheet) considering only internal device consumption and excluding external load currents.

This value slightly changes with temperature and it's given for both the regulators enabled; in case one regulator is disabled (VDD1 or VDD2) the consumption is reduced of few tens of µA.

In case the FB2 is loaded with an external divider to regulate an output voltage greater than 0.8 V on VDD2, an additional contribution needs to be considered:

$$I_{LPM_{ext_div}} = VDD2 * \frac{1}{R_4 + R_{14}} \quad (3)$$

As described in DS, STBY input must be high in order to enter LPM but, once the IC is in the LPM, it could be low because the device only monitors the output current in order to exit from LPM (see L9001 datasheet for details). What is relevant here is that, as STBY input pin has an internal pull down, in case the STBY is kept to high level

during low power mode, an additional consumption of STBY_PD needs to be considered from VDDIO; in case VDDIO is connected to VDD1 or VDD2, this current must be considered as low power mode additional consumption from VS pin:

$$I_{LPM_{stby_pd}} = STBY_{PD} \quad (4)$$

For example, with HW b, the measured current in LPM is 165 µA with STBY = 0 @RT ≥ ILPM_extdiv = 33 µA as R5 = 24K in this case ≥ I_{LPM} =132 µA which is in line with L9001 datasheet; with HW c instead a value of 115 µA is measured (with STBY = 0) and as no ext divider is connected this is the ILPM which is reduced of less than 20 µA respect to the case when both regulators are connected.

Figure 54. Low power mode enter/exit

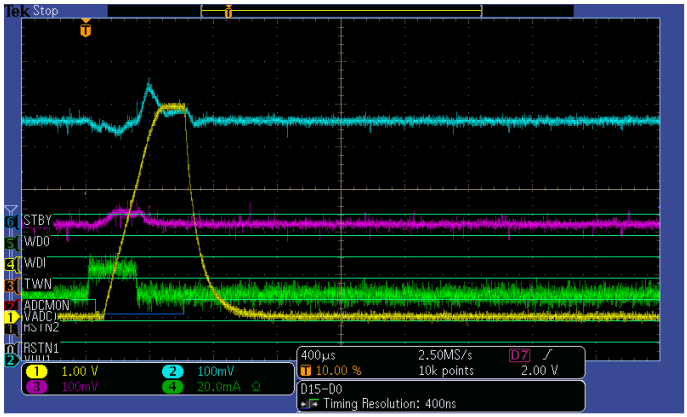


Figure 54 shows the behavior in entering and exiting the low power mode (D7 is used as waves time reference and for scope triggering) for configuration of VDD1 = 5 V, VDD2 = 1.2 V, VADC = 5 V, with no load applied on VDD1.

Table 9. Low power mode plot waves

SCOPE ID	Name	Offset [V]	Position [0=center]
CH1	VADC	0	-3
CH2	VDD1	4.5	-4
CH3	VDD2	0.9	-4
CH4	I(VDD2)	0	-3
D0	RSTN1	-	-
D1	RSTN2	-	-
D2	ADCMON	-	-
D3	TWN	-	-
D4	WDI	-	-
D5	WDO	-	-
D6	STBY	-	-

Before triggering, STBY pin is high and the device is in LPM (VADC output is off) and load on VDD2 is below ICMP1_h threshold; after triggering, I(VDD2) rises above the threshold ICMP1_h and so, after a certain time (about 100 µs) the device wakes from LPM and so VADC is switched on; then even if the load returns below the ICMP1_l threshold, the device holds the active mode for a certain time (about 400 µs) in order to reject spurious active to low power mode transitions. Only after this safe time, the LPM is entered again.

It's important to underline here that during the transition from LPM to ACTIVE mode the regulators need to switch from bypass to normal and so it must be ensured at application level that current slew rate is relatively slow until the output current is greater than Ilim_bypx (see paragraph Load for more information).

3.4 Latch mode

L9001 provides a feature, the so called latch state, to disable the system in case a systematic fault is repetitively detected on the charge pump structure, watchdog or thermal event. The separate fail counters and detection mechanism are explained in the device datasheet.

As example let's see what happens when latch mode is entered after 4 WD failures; in this case the outputs are switched off and a new power up sequence by WAKE or VS is needed to reactivate the device.

Note: In the following figures VDDIO is connected to VDD1, Cwdt = 47 nF); RSTNx and ADCMON are driven low immediately as shown (VDD2 loaded with 12 Ohm, VDD1 not externally loaded); TWN is not active.

The device consumption from VS supply measured on application board for HW b is about 3 mA.

In this example watchdog is never given and it is visible the long window of 400 ms repeated for 4 times.

Figure 55. Latch mode enter, CH1 = WAKE, CH2 = VDD1, CH3 = VDD2, CH4 = WDO (analog)

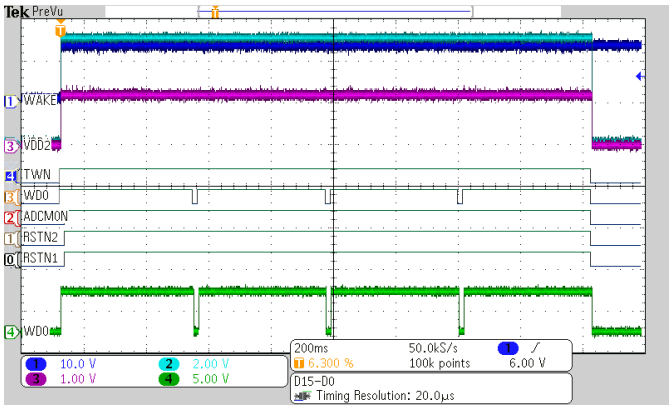
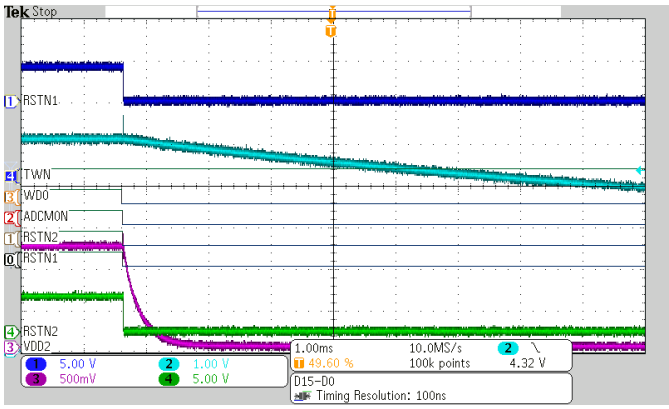


Figure 56. Latch mode enter, output behavior, CH1 = RSTN1, CH2 = VDD1, CH3 = VDD2, CH4 = RSTN2



3.5 Diagnosis output

TWN and WDO are open drain outputs and so require an external pull up resistor to the voltage rail connected to VDDIO.

A value of typ 5 kΩ is recommended as pull up resistor.

Even if RSTN1, RSTN2 and ADCMON have an internal pull up to VDDIO, an external stronger 5 kΩ pull up to VDDIO could be placed if needed.

4 Note and suggestions on layout

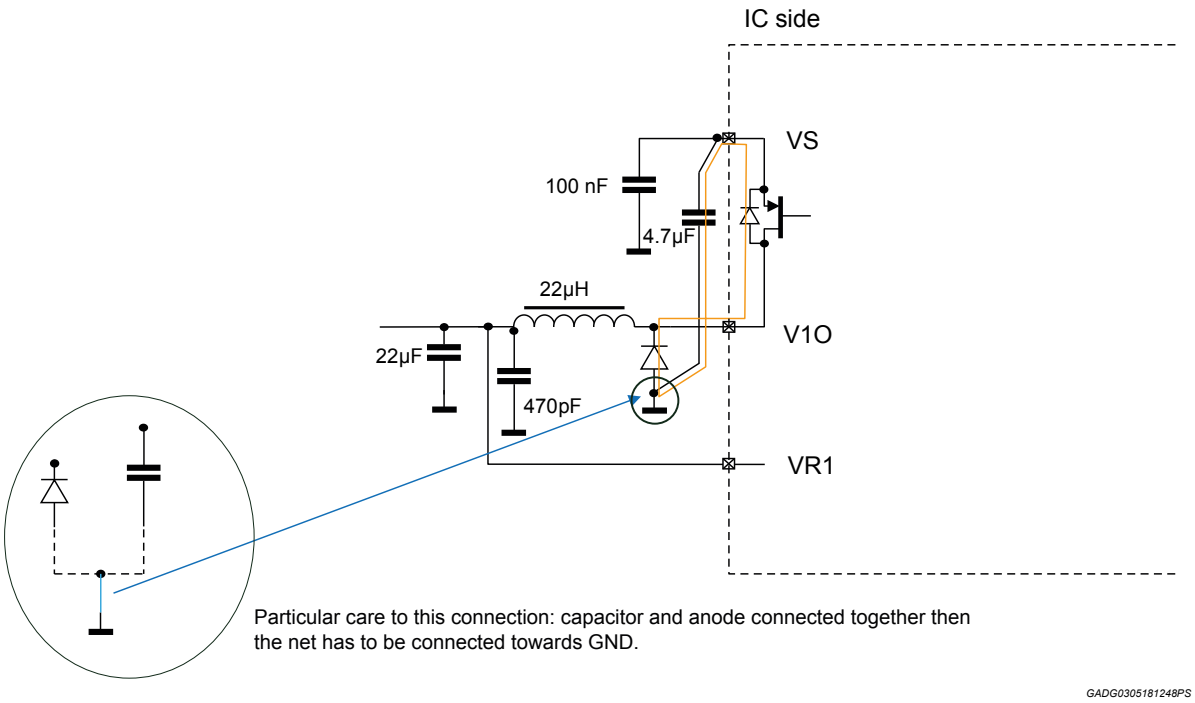
4.1 PCB layout guide line

4.1.1 VDD1 regulator

Particular care should be put on the routing of the connection between the anode of the recirculation diode and, the terminal of the noise bypass capacitor to the ground.

The connection should be realized not through independent paths but following the rule showed in Figure 57.

Figure 57. VDD1 buck regulator layout suggestions



4.1.2 VDD2 regulator

In order to have high flexibility, VDD2 has been implemented with an architecture compatible with both linear and buck configurations where the regulated voltage can be fully configurable through external feedback resistors, in (0.8-5 V) range; the following guidelines refer to buck configuration which is the most critical from the layout point of view; layout for linear case can be extrapolated as well.

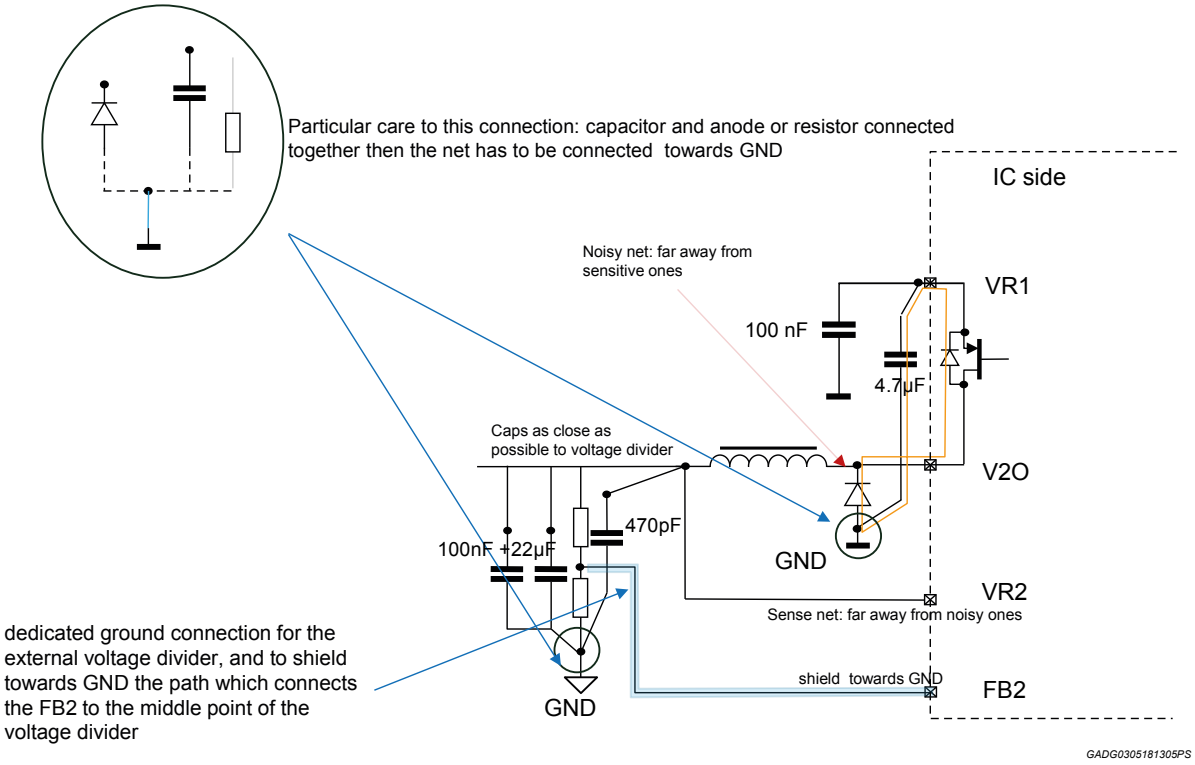
In order to guarantee the performances reported in the datasheet for these regulators, particular attention should be paid on managing external components placement and path routing.

Particular care should be put on the routing of the connection among the anode of the recirculation diode, the terminal of the noise bypass capacitor and the ground. The connection should be realized not through independent paths but following the rule showed in Figure 58.

In order to improve EMC performances, the external components should be placed to make the area of the loop highlighted in orange as small as possible.

Being the value of the regulated voltage dependent on the voltage on FB2, any accidental coupling effect on this net strongly affects the behavior of the regulator output. For this reason, ST recommends a dedicated ground connection for the external voltage divider, and to shield towards GND the path which connects the FB2 to the middle point of the voltage divider. The connection towards ground should be realized following the rule showed below.

Figure 58. VDD2 buck regulator layout suggestions



A Appendix

A.1 Test point list

Table 10. Test point list

Name	Description
TP1	ADCMON
TP2	RSTN1
TP3	RSTN2
TP4	VDDIO
TP5	CONF3
TP6	WAKE
TP7	SWB1
TP8	VS
TP9	CP
TP10	CP1
TP11	CP2
TP12	V2O
TP13	V2I
TP14	FB2
TP15	VDD2
TP16	CONF1
TP17	CONF2
TP18	VADC
TP19	TWN
TP20	WDI
TP21	STBY
TP22	WDT
TP23	WDO
TP24	GND

A.2 Reference documents

Table 11. Reference documents

Document name	Reference document	Revision
L9001 Datasheet	L9001	-
ASD639A_R2 layout.pdf	The file is attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it.	R2
ASD616A_R2 L9396 DEMO BOARD Schematic_R2.pdf	The file is attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it.	R2

Revision history

Table 12. **Document revision history**

Date	Version	Changes
25-Jan-2019	1	Initial release.

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