Migration of applications from STM32F0 Series to STM32G0 Series

Introduction

Designers of applications based on STM32 microcontrollers must be able to easily replace one microcontroller type with another from the same product family, or with products from a different family.

There are several reasons to migrate an application to a different microcontroller, among them the need to fulfill more demanding product requirements, such as increased memory size and the number of available I/Os, or cost reduction constraints, requiring a switch to smaller components and reduced PCB areas.

This application note analyzes the steps required to migrate from the STM32F0 to the STM32G0 Series, providing guidelines on the hardware and peripheral migration.

For a better understanding the user needs to be familiar with STM32 microcontrollers.

For additional information, refer to the product datasheets and to the following documents, available on www.st.com:

- AN3364: Migration and compatibility guidelines for STM32 microcontroller applications
- RM0091: STM32F0x1/STM32F0x2/STM32F0x8 advanced Arm®-based 32-bit MCUs
- RM0360: STM32F030x4/x6/x8/xC and STM32F070x6/xB advanced Arm®-based 32-bit MCUs
- PM0215: STM32F0xxx Cortex®-M0 programming manual
- PM0223: STM32L0 Series Cortex®-M0+ programming manual
- RM0444: STM32G0x1 line of advanced Arm®-based 32-bit MCUs
- RM0454: STM32G0x0 line of advanced Arm®-based 32-bit MCUs

This document will be regularly updated to provide information on new STM32G0 devices.

1 General information

This document applies to Arm®-based devices of STM32F0 Series and STM32G0 Series.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32G0 Series overview

Microcontrollers of the STM32G0 Series are based on Arm® cores(a). They include a set of peripherals with advanced features and optimized power consumption compared with those of the STM32F0 Series:

- Low-power timer (LPTIMER)
- Low-power universal asynchronous receiver transmitter (LPUART)
- Voltage reference buffer (VREFBUF)
- True random number generator, encryption hardware accelerator (TrueRNG, AES)
- UCPD (USB type-C power delivery)
- Securable Flash memory area
- Two timers 128 MHz capable

Note: The STM32G0 Series is divided to full featured STM32G0x1 line and value line STM32G0x0 where some features may be missing or limited. Always check the datasheet for definitive description.

3 Hardware migration

3.1 Pinout compatibility

STM32G0 devices use a different system of power distribution (single supply pair) compared with STM32F0 ones. Thanks to this change the spare pins can be used for other functionalities (see Table 1 for examples).

Table 1. Additional I/Os for STM32G071 vs. devices of the STM32F0 Series - Examples

Package	STM32G0 Series	STM32F0 Series	Difference in I/Os
LQFP64	STM32G071	STM32F071	+9
LQFP32	STM32G071	STM32F051	+5

As a consequence the two families are no longer pin to pin compatible, in case of replacement the PCB routing needs to be reworked.

The two device families are however quite similar from the programming point of view.

When the same peripheral and the same pin are present on both devices the functionality and alternate function mapping is the same. Efforts have been spent to keep (when possible) one alternate functionality for each peripheral.

STM32G0 and STM32F0 Series offer a similar range of packages as detailed in Table 2.

Table 2. Package types

Package pins	STM32F0 Series	STM32G0 Series
8	Not available	SO8N
20	TSSOP	TSSOP
28	UFQFPN	UFQFPN
32	LQFP / UFQFPN	LQFP / UFQFPN
48	LQFP / UFQFPN	LQFP / UFQFPN
64	LQFP / UFBGA	LQFP / UFBGA
80	Not available	LQFP
100	LQFP / UFBGA	LQFP / UFBGA

Note: WLCSP packages not included in this comparison as they depend upon die size, and hence require deeper redesign.

4 Boot mode selection

The boot configuration of the STM32G0 Series is based on that used in the STM32F0 Series. It implements the same features, including the empty check, which forces boot from System memory when the empty check flag is set (device is considered empty).

As an extension, the STM32G0 family implements BOOT_LOCK bit in option bytes (see Table 3), which forces booting from Main Flash memory regardless of the other options.

Empty check feature can be controlled also by content of EMPTY bit in the FLASH access control register.

Table 3. Boot mode configuration

BOOT_LOCK bit (1)	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit (2)	nBOOT0 bit (2)	Selected boot area
0(1)	x	0	0(2)	x(2)	Main Flash memory
0(1)	1	1	0(2)	x(2)	System memory
0(1)	0	1	0(2)	x(2)	Embedded SRAM
0(1)	x(2)	x(2)	1(2)	1(2)	Main Flash memory
0(1)	1(2)	x(2)	1(2)	0(2)	System memory
0(1)	0(2)	x(2)	1(2)	0(2)	Embedded SRAM
1(1)	x(1)	x(1)	x(1)	x(1)	Main Flash memory forced(1)

1. *STM32G0x1 only*
2. *STM32G0x and STM32F04/9x only*

Important difference is that while F0 has the BOOT_SEL bit, it's nBOOT_SEL bit on the G0 with the same default value but opposite default functionality. While on F0 the default configuration uses BOOT0 pin to select the boot area, the G0 by default uses the nBOOT0 bit. Together with empty check functionality the OB based selection is flexible enough while not occupying useful pins, especially on new 8 pin package.

5 Peripheral migration

5.1 STM32 product compatibility

STM32 microcontrollers embed a set of peripherals that can be classified in three categories:

1. Peripherals common to all products. They are identical, so have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
2. Peripherals shared by all STM32 products, with minor differences (in general to support new features), so the migration from one product to another is very easy and does not need any significant new development effort.
3. Peripherals that have been considerably changed from one product to another (e.g. with a new architecture, or implementing new features). For this category the migration requires a new development at application level.

STM32Cube HAL is compatible between the STM32F0 Series and the STM32G0 devices, there are slight differences in the low-layer APIs (LL).

Table 4 shows the STM32 peripheral compatibility between the STM32F0 Series and the STM32G0 devices.

Table 4. Comparison of peripherals between the two STM32 Series

Peripheral		STM32F0 Seriess	STM32G0 Serie(1)	STM32G0Bx/Cx
Power supply		See Table 6. Power control peripheral, STM32F0 vs. STM32G0		
Core		Cortex M0	Cortex M0+	
Maximum frequency		48 MHz	64 MHz	
Flash memory		Up to 256 Kbyte	Up to 128 Kbyte	Up to 512 Kbyte
SRAM		Up to 32 Kbyte	Up to 32 Kbyte - Parity Up to 36 Kbyte - Parity	Up to 128kB with parity Up to 144kB no parity
Timers	General purpose	5 x 16-bit	5 x 16-bit + 1 x 32-bit	6 x 16-bit + 1 x 32-bit
	Advanced	1	1	
	Basic	2	2	
	Low power	Not available	2	
ADC		1 Msps	2.5 Msps	
DAC		Up to 2 channels (2)	2 channels	
AES		Not available	Key sizes of 128 or 256 bits (only crypto parts)	
TSC		Up to 24 capacitive sensing channels (2)	Not available	
DMA	Number of independently configurable channels (requests)	Up to 12 (2)	7	12
DMAMUX		Not available	1 DMA request multiplexer	
True RNG		Not available	1	
GPIO		Same interface		
USB		Full speed USB 2.0	Not available	Full speed USB 2.0 device and host
UCPD		Not available	USB Type-C power delivery interface	
RTC, TAMP		One peripheral	Split into two peripherals	

Peripheral	STM32F0 Seriess	STM32G0 Serie(1)	STM32G0Bx/Cx
COMP	2	2	3
I2C	2	2	3
CAN	CAN protocols version 2.0A and B	Not available	CAN protocols v2.0 A/B, CAN FD 1.0
USART	Up to 8	Up to 4	6
LPUART	Not available	1	2
Backup registers	5		
SPI	Up to 2		3

1. *Except STM32G0Bx/Cx devices*
2. *Check the actual number on the datasheet of the device used in your application.*

The following sections detail the differences between the two Series.

5.2 System architecture

The Cortex-M0+ processor is binary-compatible with the Cortex-M0.

Table 5. Comparison of Cortex cores

Feature	M0	M0+	Advantages of M0+ vs. M0
Pipeline	Three-stages	Two-stages	Improved response time and efficiency
Performance efficiency (CoreMark®/MHz)	2.33	2.46	Lower power, higher performance
Memory protection	Not available	Memory protection unit	Makes system more secure by: • Separating processes • Preventing tasks from corrupting stack or data memory used by other tasks • Preventing unprivileged tasks from accessing peripherals that can be critical tothe system security
Relocatable vector table	Not supported	Supported	Enables the relocation of the interrupt vector table anywhere in the memory. Enables different applications to use their own vector table.
Unprivileged/ privileged mode execution	Not supported	Supported	Allows atask, such as the system calling in an operating system, to execute with more privileges than the user task or an application.

5.3 Memory mapping

The peripheral address mapping has been changed in the STM32G0 Series compared to the STM32F0 Series. The main change concerns the GPIOs, which have been moved from the APB bus to the IOPORT interface to allow them to operate at the maximum speed.

5.4 Power control peripheral

The power control of the STM32G0 Series is slightly different from the one of the STM32F0 Series, the differences are summarized in Table 6. The programming interface is almost unchanged.

Table 6. Power control peripheral, STM32F0 vs. STM32G0

PWR	STM32F0x1/x2 devices	STM32F0x8 devices	STM32G0 Series
Power supplies	• V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins. • V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively. • V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. • V_{DDIO2} = 0 to 3.6 V, only available on STM32F07x and STM32F09x.	• V_{DD} = 1.8 V ±8%: external power supply for I/Os. Provided externally through V_{DD} pins. • V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. VDDA and VSSA must be connected to V_{DD} and V_{SS}, respectively. • V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. • V_{DDIO2} = 0 to 3.6 V, only available on STM32F07x and STM32F09x.	• V_{DD} = 1.6 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins. • V_{DDA} =1.62 V (ADC and COMP) / 1.8 V (DAC) / 2.4 V (VREFBUF) to 3.6 V: V_{DDA} voltage level is identical to V_{DD} voltage as it is provided externally through V_{DD} pin. • V_{BAT} = 1.55 to 3.6 V: power supply for RTC, TAMP, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. • V_{DDIO2} = 1.6 to 3.6 V, only available on STM32G0B1xx and STM32G0C1xx (1)
Power supply supervisor	• Integrated POR /PDR circuitry • Programmable voltage detector (PVD)	Power ON reset must be controlled externally through the dedicated NPOR pin.	• Integrated POR /PDR / BOR circuitry • Programmable voltage detector (PVD)
Low-power modes and wakeup sources	Sleep mode • Any peripheral interrupt / wakeup event Stop mode • Any EXTI line event/interrupt Standby mode • WKUPx pins rising edge • RTC alarm / autowakeup • External reset in NRST pin • IWDGreset	Sleep mode • Any peripheral interrupt / wakeup event Stop mode • Any EXTI line event/ interrupt	Sleep mode • Any peripheral interrupt /wakeup event Low power run mode • Clearing LPR bit Low power sleep mode • Any peripheral interrupt /wakeup event Stop 0 and 1 modes • Any EXTI line event/interrupt Standby mode • WKUPx pins rising edge • RTC /TAMP event • External reset in NRST pin • IWDG reset Shutdown mode • WKUPx pins rising edge • RTC /TAMP event • External reset in NRST pin

1. *For STM32G0x0 are 2 V minimum, no BOR*

5.5 Reset and clock controller (RCC) interface

Table 7. RCC peripheral, STM32F0 vs. STM32G0

RCC	STM32F0	STM32G0
HSI48	High speed internal oscillator at 48 MHz (1)	High speed internal oscillator at 48 MHz (2)
HSI 14	High speed internal oscillator dedicated to ADC	Not available
HSI	8 MHz RC factory-trimmed	16 MHz RC factory-trimmed
LSI	40 kHz RC	32 kHz RC
HSE	4 to 32 MHz	4 to 48 MHz
LSE	32.768 kHz	
PLL	Main PLL	Three independent clock outputs (extra PLL outputs for I2S, ADC, RNG, USB, FDCAN and TIM1/15 clocks)
System clock source	HSI48, HSI,HSE or PLL	HSI, HSE, PLLRCLK, LSI or LSE
System clock frequency	• Up to 48 MHz • 8 MHz after reset based on HSI	• Up to 64MHz • 16MHz after reset based on HSI16
APB frequency	Up to 48 MHz	Up to 64 MHz
RTC clock source	LSI, LSE or HSE clocks divided by 32	
MCO clock output	MCO (PA8): SYSCLK, HSI, HSE, HSI14, HSI48, PLLCLK, LSE, LSI	MCO (PA8, PA9, PF2, PD10) & MCO2 (PB2, PA10, PA15, PD7) SYSCLK, HSI16, HSE, LSE, PLLR, LSI, HSI48 (2), PLLQ & PLLP
LSCO clock output	-	LSI, LSE - Available also in Stop0, Stop1 and Standby modes
Internal oscillator measurement and calibration	Internal/external clock measurement inputs: • TIM14 inputs: RTCCLK, HSE/32, MCO • HSI48 can becalibrated on the run by mean of CRS using a reference clock. (1)	Internal/external clock measurement inputs • TIM14 inputs: RTCCLK, HSE/32, MCO, MCO2 • TIM16 inputs: LSI, LSE, MCO2 • TIM17 inputs: HSE/32, MCO, MCO2, HSI48/256

1. *Available only on STM32F04x, STM32F07x and STM32F09x devices.*
2. *Only available on STM32G0Bx and STM32G0Cx, where the USB interface is implemented.*

5.6 Interrupt vectors

Table 8. Interrupt vectors for STM32F0 and STM32G0 Series

Position	STM32F0	STM32G0
0	WWDG	WWDG
1	PVD_VDDIO2	PVD
2	RTC	RTC/TAMPER
3	FLASH	FLASH
4	RCC_CRS	RCC/CRS(1)
5	EXTI0_1	EXTI0_1
6	EXTI2_3	EXTI2_3
7	EXTI4_15	EXTI4_15
8	TSC	UPCD1/UPCD2USB(1)
9	DMA_CH1	DMA_CH1
10	DMA_CH2_3 DMA2_CH1_2	DMA_CH2_3
11	DMA_CH4_5_6_7 DMA2_CH3_4_5	DMA_CH4_5_6_7DMAMUX/DMA2_CH1-5(1)
12	ADC/COMP	ADC/COMP
13	TIM1_BRK_UP_TRG_COM	TIM1_BRK_UP_TRG_COM
14	TIM1_CC	TIM1_CC
15	TIM2	TIM2
16	TIM3	TIM3/TIM4(1)
17	TIM6/DAC	TIM6_DAC/LPTIM1
18	TIM7	TIM7/LPTIM2
19	TIM14	TIM14
20	TIM15	TIM15
21	TIM16	TIM16/FDCAN_IT0(1)
22	TIM17	TIM17/FDCAN_IT1(1)
23	I2C1	I2C1
24	I2C2	I2C2/I2C3(1)
25	SPI1	SPI1
26	SPI2	SPI2/SPI3(1)
27	USART1	USART1
28	USART2	USART2/LPUART2(1)
29	USART3/USART4/USART5/USART6/ USART7/USART8	USART3/USART4/LPUART1
30	CEC/CAN	CEC
31	USB	AES/RNG

1. *Only available on the STM32G0Bx and STM32G0Cx*

5.7 EXTI source selection (EXTI lines)

Table 9. EXTI lines for STM32F0 and STM32G0 Series

EXTI line	STM32F0	STM32G0
0-15	GPIOs	
16	PVD output	
17	RTC Alarm event	COMP1 output
18	USB wakeup event	COMP2 output
19	RTC Tamper and TimeStamp events	RTC
20	RTC Wakeup event (1)	COMP3 output(2)
21	COMP1 output	TAMP
22	COMP2 output	I2C2 wakeup(2)
23	I2C1 wakeup	
24	Reserved	USART3 wakeup(2)
25	USART1 wakeup	
26	USART2 wakeup (1)	USART2 wakeup
27	CEC wakeup	
28	USART3 wakeup (3)	LPUART1 wakeup
29	Reserved	LPTIM1
30	Reserved	LPTIM2
31	V_{DDIO2} supply comparator output (4)	LSE_CSS
32	NA	UCPD1 wakeup
33	NA	UCPD2 wakeup
34	NA	V_{DDIO2} monitoring configurable
35	NA	LPUART1 wakeup

1. *Available only on STM32F07x and STM32F09x devices.*
2. *Only available on the STM32G0Bx and STM32G0Cx*
3. *Available only on STM32F09x devices.*
4. *Available only on STM32F04x, STM32F07x and STM32F09x devices.*

5.8 DMA

There is only one DMA peripheral in the MCUs of the STM32F0 Series, there are two DMA related peripherals in those of the STM32G0 Series, as the DMA peripheral is complemented with DMAMUX (request multiplexer). To offer more flexibility it is possible, with DMAMUX, to map any hardware request to any DMA channel.

Table 10. **DMA peripheral**

DMA	STM32F03x, STM32F04x and STM32F05x	STM32F09x	STM32G0 Series (1)	STM32G0B/Cx
Instances	1	2	1	2
Independent channels	Up to 7	12	7	12
Controller	The requests is simply logically OR-ed. Up to 12 requests for each channel.	Dedicated DMAx channel. Selection register.	DMAMUX: each channel can be triggered by any of either up to 57 peripheral request or 4 generated requests.	DMAMUX: each channel can be triggered by any of either 73 peripheral request or 4 generated requests.

1. *Except 512k devices*

5.9 GPIO interface

The STM32G0 GPIOs are not mapped on the AHB bus as on STM32F0, but directly accessed by the Cortex M0+ dedicated I/O port, which provides single-cycle access to peripherals.

The single-cycle I/O port is memory mapped and from the programming point of view there's no difference between STM32F0 and STM32G0.

On STM32G0 there is the possibility to replace RESET functionality by a standard GPIO. A specific pin (PF2) replaces NRST if configured by appropriate value in options bytes.

Another feature, called internal reset holder, makes it possible to keep driving out an internal reset source until the GPIO reaches its low level threshold VIL. When internal reset is generated it is possible to drive bigger capacitances on pad by extending the length of the reset pulse coming from internal sources.

Table 11. **GPIO peripheral speed**

Feature	STM32F0	STM32G0
Speeds	2 MHz 10 MHz 50 MHz	3 MHz 15 MHz 60 MHz 80 MHz
Pull-up/down	-	Configured for Standby and Shutdown

5.10 RTC and TAMP

The original RTC peripheral in STM32F0 devices is split into two peripherals in STM32G0 devices. As a consequence, the registers are split into two sections, and the memory map has been reworked.

Table 12. **RTC/Tamper for the F0 and G0 Series**

Peripheral	Feature	STM32F0	STM32G0
RTC	Number of alarms	1	2
	Number of output	1	2
Tamper	Number of events	Up to 3	Up to 3 external + 4 internal

5.11 USART

Addition of the buffer is the most notable difference. Synchronous mode on STM32G0 series now supports slave mode. Also STM32G0x series introduces an option of LPUART peripheral.

Table 13. **USART peripheral**

Feature	STM32F0	STM32G0
RX/TX FIFO	-	2x 8B

5.12 I2C

There are no significant differences between the two Series.

5.13 CEC

There are no significant differences between the two Series.

5.14 FLASH

STM32G0Bx and STM32G0Cx are dual bank with RWW capability. Dual bank can be disabled in OB.

Feature		STM32F0	STM32G0	
Page size		• 1KByte (STM32F03x, STM32F04x and STM32F05x) • 2KBytes (STM32F07x and STM32F09x	2KByte	
ECC		No	Yes (64 bits plus 8 ECC bits)	
Security		• Read protection activated by option (RDP) • Two write protection areas selected by option (WRP)	• Read protection activated by option (RDP) • Two write protection areas selected by option (WRP) • Two proprietary code read protection area selected by option (PCROP) • Securable memory area • BOOT_LOCK forcing boot from main Flash memory	
Maximum HCLK frequency	Number of wait states	-	**In V_{CORE} Range 1**	**In V_{CORE} Range 2**
	0WS	≤ 24 MHz	≤ 24 MHz	≤ 8 MHz
	1WS	≤ 48 MHz	≤ 48 MHz	≤ 16 MHz
	2WS	-	≤ 64 MHz	-

5.15 Timers

Table 14. Timers on STM32G0 microcontrollers

Type	Timer	Counter		Prescaler factor	DMA request generation	Capture/ Compare channels	Complementary outputs
		Resolution	Type				
Advanced control	TIM1(1)	16-bit	Up, down, up/ down	Integer from 1 to 65536	Yes	4 (6 internal)	3
General purpose	TIM2	32-bit				4	-
	TIM3	16-bit				4	-
	TIM4					4	-
	TIM14		Up		No	1	-
	TIM15(1)				Yes	2	1
	TIM16					1	1
	TIM17					1	1
Basic	TIM6					1	-
	TIM7					1	-
LP timer	LPTIM1			2^n, where n = 0 to 7	No	-	-
	LPTIM2					-	-

1. *Up to 128 MHz.*

TIM1 and TIM15 timers are clocked at a frequency up to 128 MHz, to bring additional resolution, below 10 ns. In this case the frequency must not exceed 128 MHz, derived from the same clock source, and the ratio between PCLK and TIM1 and TIM15 clocks must be an integer.

The break input is bidirectional to accept external fault events and/or signal the internal fault events outside the MCU.

This feature makes it possible to have:

- a global break information available for external MCUs or gate drivers shut down inputs, with a single-pin
- an internal comparator and multiple external open drain comparators outputs OR-ed together and triggering a break event, when multiple internal and external break inputs must be merged
- all internal fault sources (system, comparator) are merged into a single signal
- a specific disarming logic prevents lock-up while being safe (no disarming possible while the fault is present or while the PWM is enabled).

Concerning the interconnection, new TIMx AF mappings have been added, and new PWM modes as well:

- asymmetric center-aligned PWM
- combined PWM mode
- combined 3-phase mode.

5.16 SRAM

Table 15. SRAM density, STM32F0 vs. STM32G0

Maximum Flash memory density	STM32F0	STM32G0
32 Kbytes	STM32F03x: 4 Kbytes STM32F04x: 6 Kbytes	-
64 Kbytes	STM32F05x: 8 Kbytes	STM32G03x/04x: 8 Kbytes STM32G05x/06x: • 16 Kbytes (parity enabled) • 18 Kbytes (parity disabled)
128 Kbytes	STM32F07x: 16 Kbytes	STM32G07x/08x: • 36 Kbytes (parity disabled) • 32 Kbytes (parity enabled)
256 Kbytes	STM32F09x: 32 Kbytes	STM32G0Bx/0Cx: • 128Kbytes (parity enabled) • 144Kbytes (parity disabled)
512 Kbytes	-	

5.17 ADC

Table 16. ADC characteristics, STM32F0 vs. STM32G0

Feature	STM32F0	STM32G0
Built-in hardware oversampler	Not available	Yes, providing 16-bit resolution
External trigger	TIM1_TRGO TIM1_CC4 TIM2_TRGO TIM3_TRGO TIM15_TRGO	TIM1_TRGO2 TIM1_CC4 TIM2_TRGO TIM3_TRGO TIM4_TRGO TIM15_TRGO TIM6_TRGO EXTI line 11
Supply voltage	2.4 to 3.6 V	1.62 to 3.6 V
Clock frequency	Up to 14 MHz	Up to 35 MHz
Sampling rate (12-bit resolution)	1.0 Msps	2.5 Msps

5.18 DAC

The sample and hold (S&H) feature to maintain DAC output voltage when the MCU is in low power modes such as Stop 1 mode is available on STM32G0 products.

5.19 COMP

STM32G0 comparators implement new features:

- possibility to have blanking to mask spurious over-current during turn-on, or zero-crossing events during turn-off
- the two comparators combined in a window comparator can provide just one output.

Table 17. Comparator characteristics, STM32F0 vs. STM32G0

Feature	STM32F0	STM32G0
Power modes	4	2
Registers	1	2

5.20 VREFBUF

This peripheral is available on STM32G0 Series, supports two voltages controlled with the VRS bit in the VREF_CSR register:

- V_{REFBUF_OUT1}≈2.05 V (requires V_{DDA}≥ 2.4 V)
- V_{REFBUF_OUT1}≈2.50 V (requires V_{DDA}≥ 2.8 V)

5.21 AES and RNG

These peripherals are available on the STM32G0 secure products, with the following features:

- AES key sizes: 128 bits, 256 bits
- AES operation modes: Decryption, Encryption, Key derivation
- AES chaining modes: ECB, CBC, CTR, GCM, GMAC, CCM

6 Firmware migration using the Cube library

This section describes how to migrate an application based on STM32Cube MCU package.

The STM32F0xx and STM32G0xx Cube packages have the same architecture and are CMSIS compliant; they use the same driver naming and the same APIs for all compatible peripherals.

Only a few peripheral drivers need to be updated to migrate the application from STM32F0 to STM32G0 Series.

6.1 Migration steps

To update the application code to run on STM32G0xx Library, follow the steps listed below:

1. Update the toolchain startup files
   a. Project files: device connections and Flash memory loader. These files are provided with the latest version of the toolchain that supports STM32G0xxx devices. For more information, user has to refer to the toolchain documentation.
   b. Linker configuration and vector table location files: templates of these files are developed following the CMSIS standard and are included in the Cube install package under the following directory: Drivers\CMSIS\Device\ST\STM32G0xx\Source\Templates.
2. Replace STM32G0xx Library source files to the application sources
   a. Replace the stm32f0x_conf.h file with stm32g0xx_conf.h
   b. Replace the existing stm32f0x_it.c/stm32f0x_it.h files with stm32g0xx_it.c/Stm32g0xx_it.h

As several IPs have evolved, it is recommended to check header files for new or more advanced features. For example newly added HDP feature is useful for secure boot implementations.

The basic peripheral control functions are mostly identical, however the init structures may differ and omitting some new parameters could result in unpredictable behavior.

Other features, specific to each family, are covered in “_ex” files and depend upon the implementation, hence they usually differ significantly and cannot be easily reused.

7 Conclusion

This application note is a useful complement to the datasheets and reference manuals.

It provides simple guidelines to migrate an application based on an STM32F0 device to the new STM32G0 Series microcontrollers.

Revision history

Table 18. **Document revision history**

Date	Version	Changes
04-Apr-2019	1	Initial release.
27-Jan-2022	2	Modified: • Table 4. Comparison of peripherals between the two STM32 Series • Table 7. RCC peripheral, STM32F0 vs. STM32G0 • Table 8. Interrupt vectors for STM32F0 and STM32G0 Series • Table 9. EXTI lines for STM32F0 and STM32G0 Series • Table 10. DMA peripheral • Table 15. SRAM density, STM32F0 vs. STM32G0

Contents

List of tables