Migrating between STM32F334/303 and STM32G431/G474/G491 MCUs

Introduction

For designers of STM32 microcontroller applications, the ability to easily replace one microcontroller type with another from the same product family is an important asset.

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size or increasing the number of I/Os. Cost reduction objectives may also be a reason to switch to smaller components and shrink the PCB area.

This application note analyses the steps required to migrate an existing design between STM32F303/F334 lines and STM32G431xx/G474xx/G491xx microcontrollers. All the most important information is grouped here. Three aspects need to be considered for the migration: the hardware, peripheral(s) and firmware.

This document lists the full set of features available for STM32F303/F334 lines and the equivalent features on STM32G431xx/G474xx/G491xx devices.

To fully benefit from this application note, the user should be familiar with the STM32 microcontroller documentation available on www.st.com with a particular focus on:

- STM32F3 reference manuals:
  - STM32F303xB/C/D/E, STM32F303x6/8, STM32F328x8, STM32F358xC, STM32F398xE advanced Arm®-based MCUs (RM0316)
  - STM32F334xx advance Arm®-based 32-bit MCUs (RM0364)
- STM32F3 datasheets:
  - STM32F303xB STM32F303xC datasheet
  - STM32F303xD STM32F303xE datasheet
  - STM32F303x6/x8 datasheet
- STM32G4xx reference manuals:
  - STM32G4xx advanced Arm®-based 32-bit MCUs (RM0440)
- STM32G431xx/G474xx/G491xx datasheets

Table 1. Applicable products

Type	Product lines and part numbers	
Microcontrollers	STM32F3xx	STM32F303 Lines STM32F334 Lines
	STM32G431xx	STM32G431C6, STM32G431C8, STM32G431CB, STM32G431K6, STM32G431K8, STM32G431KB, STM32G431M6, STM32G431M8, STM32G431MB, STM32G431R6, STM32G431R8, STM32G431RB, STM32G431V6, STM32G431V8, STM32G431VB
	STM32G474xx	STM32G474CB, STM32G474CC, STM32G474CE, STM32G474MB, STM32G474MC, STM32G474ME, STM32G474QB, STM32G474QC, STM32G474QE, STM32G474RB, STM32G474RC, STM32G474RE, STM32G474VB, STM32G474VC, STM32G474VE
	STM32G491xx	STM32G491CC, STM32G491CE, STM32G491KC, STM32G491KE, STM32G491MC, STM32G491ME, STM32G491RC, STM32G491RE, STM32G491VC, STM32G491VE

1 STM32G431xx/G474xx/G491xx overview

The STM32G431xx/G474xx/G491xx are based on the high-performance Arm® Cortex® -M4 32-bit, up to 170 MHz and include a larger set of peripherals with advanced features compared to the STM32F303 lines ones, such as:

- Advanced encryption hardware accelerator (AES)
- Serial audio interface (SAI)
- Low-power UART (LPUART)
- Low-power timer (LPTIM)
- Voltage reference buffer (VREFBUF)
- Quad-SPI interface (QUADSPI)
- Clock recovery system (CRS) for USB
- SRAM1 size is different on the various STM32G431xx/G474xx/G491xx devices:
  - 16 Kbytes for STM32G431xx
  - 80 Kbytes for STM32G474xx
  - 80 Kbytes for STM32G491xx
- Additional SRAM2 with data preservation in Standby mode:
  - 6 Kbytes for STM32G431xx
  - 16 Kbytes for STM32G474xx
  - 16 Kbytes for STM32G491xx
- CCM SRAM :
  - 10 Kbytes for STM32G431xx
  - 32 Kbytes for STM32G474xx
  - 16 Kbytes for STM32G491xx
- 8-bit ECC on FLASH memory
- Dual bank boot (only on STM32G474xx)

This migration guide is only covering the migration from STM32F303/F334 lines to STM32G431xx/G474xx/G491xx devices. As a consequence the new features present on STM32G431xx/G474xx/G491xx but not already present on STM32F303 lines are not covered (refer to the STM32G431xx/G474xx/G491xx devices reference manuals and datasheets for an exhaustive overview).

This document applies to STM32F334/303 lines and STM32G431xx/G474xx/G491xx Arm®-based devices.

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2 Hardware migration

2.1 Package availability

The STM32F303/334 line and the STM32G431xx/G474xx/G491xx devices have a wide selection of package. STM32F303/334 lines offer spreads from 32 to 144 pins packages and STM32G431xx/G474xx/G491xx offer spreads from 32 to 128 pin packages.

Table 2 lists the available packages in the STM32G431xx/G474xx/G491xx.

Table 2. Package availability on STM32G431xx/G474xx/G491xx devices

Package(1)	STM32G431xx	STM32G474xx	STM32G491xx	Size (mm x mm)
UFQFPN32	X	-	-	(5x5)
LQFP32	X	-	X	(7x7)
UFQFPN48	X	X	X	(7x7)
LQFP48	X	X	X	(7x7)
UFBGA64	X	-	X	(5x5)
LQFP64	X	X	X	(10x10)
WLCSP64	-	-	X	(3.56 x 3.52 pitch 0.4 mm)
LQFP80	X	X	X	(12X12)
LQFP100	X	X	X	(14x14)
LQFP128	-	X	-	(14x14)
WLCSP49	X	-	-	(3.277x3.109 pitch 0.4 mm)
WLCSP81	-	X	-	(4.4084x3.7594 pitch 0.4 mm)
TFBGA100	-	X	-	(8x8 pitch 0.8 mm)

1. *x = Supported package.*

Table 3 lists the available packages in the STM32F303/334 lines.

Table 3. Package availability on STM32F303/334 lines

Package(1)	STM32F303/334 lines		
	STM32F303xB/C	STM32F303xD/E	STM32F303x6/8 STM32F334xx
UFQFPN32	-	-	-
WLCSP49	-	-	x
WLCSP100	X	X	-
LQFP32	-	-	X
LQFP48	X	-	X
LQFP64	X	X	X
LQFP80	-	-	-
LQFP100	X	X	-
LQFP144	-	X	-
UFBGA100	-	X	-

1. *X = supported package.*

For a detailed package availability and package selection, refer to the STM32F303/334 lines and to the STM32G431xx/G474xx/G491xx microcontroller's documentation available on www.st.com.

Both families share a high level of pin compatibility. Most of the peripherals share the same pins. The transition between the two families is easy since only a few pins are impacted.

Table 4 compare the pinout between STM32F303/334 lines and STM32G431xx/G474xx/G491xx for 48, 64 and 100 pin packages.

Table 4. STM32F303/334 lines and STM32G431xx/G474xx/G491xx pinout differences (QFP)

STM32F303/334 lines				STM32G431xx/G474xx/G491xx			
LQFP48	LQFP64	LQFP100	Pinout	LQFP48	LQFP64	LQFP100	Pinout
7	7	14	NRST	7	7	14	PG10-NRST
8	12	20	VSSA/VREF-	19	27	35	VSSA
9	13	22	VDDA(1)/VREF+	21	29	37	VDDA
-	-	21	VREF+	20	28	36	VREF+
10	14	23	PA0	8	12	20	PA0
11	15	24	PA1	9	13	21	PA1
12	16	25	PA2	10	14	22	PA2
13	17	26	PA3	11	17	25	PA3
14	20	29	PA4	12	18	26	PA4
15	21	30	PA5	13	19	27	PA5
16	22	31	PA6	14	20	28	PA6
17	23	32	PA7	15	21	29	PA7
18	26	35	PB0	16	24	32	PB0
19	27	36	PB1	17	25	33	PB1
20	28	37	PB2	18	26	34	PB2
21	29	47	PB10	22	30	47	PB10
22	30	48	PB11	25	33	50	PB11
25	33	51	PB12	26	34	51	PB12
26	34	52	PB13	27	35	52	PB13
27	35	53	PB14	28	36	53	PB14
28	36	54	PB15	29	37	54	PB15
29	41	67	PA8	30	42	69	PA8
30	42	68	PA9	31	43	70	PA9
31	43	69	PA10	32	44	71	PA10
32	44	70	PA11	33	45	72	PA11
33	45	71	PA12	34	46	73	PA12
34	46	72	PA13	37	49	76	PA13
37	49	76	PA14	38	50	77	PA14
38	50	77	PA15	39	51	78	PA15
39	55	89	PB3	40	56	90	PB3
40	56	90	PB4	41	57	91	PB4
41	57	91	PB5	42	58	92	PB5
42	58	92	PB6	43	59	93	PB6
43	59	93	PB7	44	60	94	PB7

STM32F303/334 lines				STM32G431xx/G474xx/G491xx			
LQFP48	LQFP64	LQFP100	Pinout	LQFP48	LQFP64	LQFP100	Pinout
45	61	95	PB8	45	61	95	PB8-BOOT0
46	62	96	PB9	46	62	96	PB9
44	-	94	BOOT0	-	-	-	-
-	24	33	PC4	-	22	30	PC4
-	25	34	PC5	-	23	31	PC5
-	37	63	PC6	-	38	65	PC6
-	38	64	PC7	-	-	-	-
-	39	65	PC8	-	-	-	-
-	40	66	PC9	-	-	-	-
-	51	78	PC10	-	52	79	PC10
-	52	79	PC11	-	53	80	PC11
-	53	80	PC12	-	54	81	PC12
-	54	83	PD2	-	55	84	PD2
-	-	27	PF4	-	-	-	PF4
-	-	38	PE7	-	-	38	PE7
-	-	39	PE8	-	-	39	PE8
-	-	40	PE9	-	-	40	PE9
-	-	81	PD0	-	-	82	PD0
-	-	82	PD1	-	-	83	PD1
-	-	84	PD3	-	-	85	PD3
-	-	85	PD4	-	-	86	PD4
-	-	86	PD5	-	-	87	PD5
-	-	87	PD6	-	-	88	PD6
-	-	88	PD7	-	-	89	PD7
-	-	97	PE0	-	-	97	PE0
-	-	98	PE1	-	-	98	PE1

1. *For LQFP100 the VDDA pin is separated from VREF+*

3 Boot mode selection

The STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices can select the boot modes between three options: boot from main Flash memory, boot from SRAM or boot from system memory. However, the way to select the boot mode differs between the products.

In STM32F303/334 lines, the boot mode is selected with the pin BOOT0 and the option bit nBOOT1 located in the user option bytes as shown in Table 5.

In STM32G431xx/G474xx/G491xx, the boot is selected with nBOOT1 option bit and pin BOOT0 or nBOOT0 option bit depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register as shown in Table 6.

Table 5. Boot modes for STM32F303/334 lines

Boot mode selection(1)		Boot mode	Aliasing
BOOT1(2)	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

1. *X = Equivalent to 0 or 1.*
2. *The BOOT1 value is the opposite of the nBOOT1 option bit.*

Table 6. Boot modes for STM32G431xx/G474xx/G491xx devices

UBE	nBOOT1 FLASH_OPTR[23]	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PB8	nSWBOOT0 FLASH_OPTR[26]	Boot Memory Space Alias
1	X	X	X	X	Main Flash memory
0	X	X	0	1	Main Flash memory is selected as boot area
0	X	1	X	0	Main Flash memory is selected as boot area
0	0	X	1	1	Embedded SRAM1 is selected as boot area
0	0	0	X	0	Embedded SRAM1 is selected as boot area
0	1	X	1	1	System memory is selected as boot area
0	1	0	X	0	System memory is selected as boot area

3.1 Embedded bootloader

The embedded bootloader is located in the system memory and programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

Table 7. Bootloader interface

Peripheral	Pin	STM32F303 line			STM32G431xx/ 474xx/491xx
		C/B	D/E	6/8	
DFU	USB_DM (PA11) USB_DP (PA12)	x	x		x
USART1	USART1_TX (PA9) USART1_RX (PA10)	x	x	x	x
USART2	USART2_TX (PD5) USART2_RX (PD6)	x	-	-	-
	USART2_TX (PA2) USART2_RX (PA3)	-	x	x	x
USART3	USART3_TX (PC10) USART3_RX (PC11)	-	-	-	x
I2C2	SCL (PC4) SDA (PA8)	-	-	-	x
I2C3	SCL (PC8) SDA (PC9)	-	-	-	x
SPI1	SPI1 (PA4/PA5/PA6/PA7)	-	-	-	x
SPI2	SPI2 (PB12/PB13/PB14/PB15)	-	-	-	x

For more details on the bootloader, refer to STM32 microcontroller system memory boot mode application note (AN2606).

For smaller packages, verify the pin and peripheral availability.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals that can be classified in three groups:

- The first group is for the peripherals that are common to all products. Those peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second group is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third group is for peripherals which have been considerably modified from one product to another (new architecture, new features...). For this last group of peripherals, the migration will require new developments at application level.

Table 8 gives a general overview of this classification. The “software compatibility” mentioned in Table 8 refers to the register description for “low level” drivers.

The STM32Cube hardware abstraction layer (HAL) is compatible with STM32F303/F334 lines and STM32G431xx/G474xx/G491xx.

Table 8. STM32 peripheral compatibility analysis STM32F303/F334 lines compared to STM32G431xx/G474xx/G491xx

Peripheral		Nb inst. In STM32				Compatibility with STM32G431xx/G474xx/G491xx		
		STM32F303/F334 lines(1)	STM32G431	STM32G474	STM32G491	Software	Pinout	Comments
SPI		4	3	4	3	Full	Partial	Some alternate function are not mapped on the same GPIO for SPI2/SPI3
I2S (half duplex)		2	2	2	2			
WWDG		1	1	1	1	Full	NA	-
IWDG		1	1	1	1			-
DBGMCU		1	1	1	1			-
CRC		1	1	1	1			-
EXTI		1	1	1	1	Partial	Full	-
USB FS		1	1	1	1	Partial	Partial	-
DMA		2	2	2	2	Partial	NA	
TIMERs	Basic	2	2	2	2	Full	Partial	• Some pins are not mapped on the same GPIO • Internal connection may differ
	General purpuse	6	6	7	6			
	Advanced	3	2	3	3			
	low-power	0	1	1	1			
	HRTIM	1	0	1	0			
PWR		1	1	1	1	Partial	NA	-
RCC		1	1	1	1	Partial	NA	-
USART UART LPUART		3 2 0	3 1(2) 1	3 2(2) 1	3 2(2) 1	Full (NA for LPUART)	Full (NA for LPUART)	-
I2C		3	3	4	3	Full	Partial	• Additional features
ADC		4	2	5	2	Partial	Partial	• Additional features • Some ADC channels mapped on different GPIOs
RTC		1	1	1	1	Partial	Full	Additional features
FLASH		1	1	1	1			
GPIO		Up to 115 IOs	Up to 86 IOs	Up to 107 IOs	Up to 86 IOs	Full	Full	
SYSCFG		1	1	1	1	Partial	NA	-
CAN		1 x BxCAN	1 x FDCAN	3 x FDCANs	2 x FDCAN			
DAC		3	2	4	2	Partial	Partial	Additional features
FMC		1	0	1	0	Full	Full	
COMP		7	4	7	4	None	Partial	Some pins mapped on different GPIO
OPAMP		4	3	6	4	None	Partial	Some pins mapped on different GPIOs

1. *The maximum number of peripherals instances is provided considering all F303/F334 products. For example we have 4 SPIs only on the STM32F303xD/E, HRTIM only on the STM32F334*
2. *The UART peripheral is not available in STM32G474Cx,STM32G491Kx, STM32G491Cx, STM32G431Kx and STM32G431Cx*

4.2 Memory mapping

The peripheral address mapping has been changed in STM32G431xx/G474xx/G491xx compared to STM32F303/334 lines.

Table 9 provides the peripheral address mapping correspondence between STM32F303/334 lines and STM32G431xx/G474xx/G491xx.

Table 9. Peripheral address mapping differences

Peripheral	STM32F303/F334 lines		STM32G431xx/G474xx/G491xx	
	Bus	Base Address	Bus	Base Address
QUADSPI	-	-	-	0xA000 1400 – 0xAFFF FFFF
FSMC control Registers	AHB4	0xA000 0400 – 0xA000 0FFF	-	0xA000 0000 – 0xA000 03FF
RNG	-	-	AHB2	0x5006 0800 – 0x5006 0BFF
Tiny AES	-	-	AHB2	0x5006 0000 – 0x5006 03FF
DAC4	-	-	AHB2	0x5000 1400 – 0x5000 17FF
DAC3	-	-	AHB2	0x5000 1000 – 0x5000 13FF
DAC2	-	0x4000 9800 – 0x4000 9BFF	AHB2	0x5000 0C00 – 0x5000 0FFF
DAC1	-	0x4000 7400 – 0x4000 77FF	AHB2	0x5000 0800 – 0x5000 0BFF
TSC	AHB1	0x4002 4000 – 0x4002 43FF	-	-
FMAC	-	-	AHB1	0x4002 1400 – 0x4002 1FFF
Cordic	-	-	AHB1	0x4002 0C00 – 0x4002 0FFF
DMAMUX	-	-	AHB1	0x4002 0800 – 0x4002 0BFF
DMA2	AHB1	0x4002 0400 – 0x4002 07FF	AHB1	0x4002 0400 – 0x4002 07FF
DMA1	AHB1	0x4002 0000 – 0x4002 03FF	AHB1	0x4002 0000 – 0x4002 03FF
HRTIM	APB2	0x4001 7400 - 0x4001 77FF	APB2	0x4001 6800 – 0x4001 77FF
SAI1	-	-	APB2	0x4001 5400 – 0x4001 57FF
FDCANs Message RAM	-	-	APB1	0x4000 A400 – 0x4000 AFFD
UCPD	-	-	APB1	0x4000 A000 – 0x4000 A3FF
LPUART1	-	-	APB1	0x4000 8000 – 0x4000 83FF
LPTIM1	-	-	APB1	0x4000 7C00 – 0x4000 7FFF
FDCAN3	-	-	APB1	0x4000 6C00 – 0x4000 6FFF
FDCAN2	-	-	APB1	0x4000 6800 – 0x4000 6BFF
FDCAN1/CAN1	APB1	0x4000 6400 – 0x4000 67FF	APB1	0x4000 6400 – 0x4000 67FF
I2S2ext	APB1	0x4000 3400 – 0x4000 37FF	-	-
TAMP	-	-	APB1	0x4000 2400 – 0x4000 27FF
CRS	-	-	APB1	0x4000 2000 – 0x4000 23FF
TIM5	-	-	APB1	0x4000 0C00 - 0x4000 0FFF

Table 10. SRAM differences in STM32F303 line and STM32G431xx/G474xx/G491xx

-	STM32F303x6/8	STM32F303xB/C	STM32F303xD/E	STM32G431xx	STM32G474xx	STM32G491xx
SRAM1	12K	40K	64K	16K	80K	80K
SRAM2(1)	N.A.	N.A.	N.A.	6K	16K	16K
CCM SRAM	4K	8K	16K	10K	32K	16K

1. *SRAM2 content can be preserved (RRS bit set in PWR_CR3 register) in standby mode.*

4.3 Direct memory access controller (DMA)

The STM32F303/334 devices implement a “general purpose” DMA similar to the STM32G431xx/G474xx/G491xx devices. Table 11 shows the main differences.

For STM32G431xx/G474xx/G491xx, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routine function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

Table 11. DMA differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices

DMA	STM32F303/334 lines	STM32G474xx/G491xx	STM32G431xx
Architecture	• 2 DMA controllers (F303xB/C/D/E) • 1 DMA controller (F303x6/8, F334)	• 2 DMA controllers	• 2 DMA controllers
Channels	• 12 channels (F3303xB/C/D/E) • 7 channels (F303x6/8) • 8 requests per channel	• 16 channels (G474xx/G491xx) • The DMA controller is connected to DMA requests through the DMAMUX peripheral • DMAMUX channels 0 to 7 are connected to DMA1 channels 0 to 7 • DMAMUX channels 8 to 15 are connected to DMA2 channels 0 to 7	• 12 channels (G431x) • The DMA controller is connected to DMA requests through the DMAMUX peripheral • DMAMUX channels 0 to 5 are connected to DMA1 channels 0 to 5 • DMAMUX channels 6 to 11 are connected to DMA2 channels 0 to 5

4.4 Interrupts

Table 12 presents the interrupt vectors in STM32F303 line compared to STM32G431xx/G474xx/G491xx devices.

Table 12. Interrupt vector differences between STM32F303 line and STM32G431xx/G474xx/G491xx devices

Position	STM32F303 line	STM32G431xx/G474xx/G491xx
2	TAMP_STAMP	RTC_TAMP_STAMP / CSS_LSE
19	USB_HP/CAN1_TX	USB_HP
20	USB_LP/CAN1_RX0	USB_LP
21	CAN1_RX1	FDCAN1_INTR1_IT
22	CAN1_SCE	FDCAN1_INTR0_IT
26	TIM1_TRG_COM / TIM17	TIM1_TRG_COM / TIM17 TIM1_DIR/TIM1_IDX
43	TIM8_BRK	TIM8_BRK/TIM8_TERR/TIM8_IERR
45	TIM8_TRG_COM	TIM8_TRG_COM/TIM8_DIR/TIM8_IDX
49	NA	LPTIM1
50		TIM5
62	NA	ADC5
63		UCPD GLOBAL INTERRUPT
72	I2C3_EV on F303xD/3 HRTIM_TIME_IRQN on F334	HRTIM_TIME_IRQN
73	I2C3_ER on F303xD/E HRTIM_TIME_IRQN in F334	HRTIM_TIMB_FLT_IRQN
74	USB_HP	HRTIM_TIMF_IRQN
75	USB_LP	CRS
76	USB_Wakeup_RMP	SAI
77	TIM20BRK	TIM20_BRK/TIM20_TERR/TIM20_IERR
79	TIM20_TRG_COM	TIM20_TRG_COM/TIM20_DIR/TIM20_IDX
82	NA	I2C4_EV
83		I2C4_ER
85	NA	AES
86		FDCAN2_INTR0
87		FDCAN2_INTR1
88		FDCAN3_INTR0
89		FDCAN3_INTR1
90		RNG
91		LPUART
92		I2C3_EV
93		I2C3_ER
94		DMAMUX_OVR
95		QUADSPI
96		DMA1_CH8
97		DMA2_CH6
98		DMA2_CH7
99		DMA2_CH8
100		CORDIC
101		FMAC

4.5 Reset and clock control (RCC)

The main differences related to the RCC between STM32G431xx/G474xx/G491xx devices and STM32F303/334 lines are presented in Table 13.

Table 13. RCC differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices

RCC	STM32F303/334 lines	STM32G431xx/G474xx/G491xx
HSI	8 MHz RC factory and user trimmed	16 MHz RC factory and user trimmed
LSI	Around 40KHz (between 30 KHz and 50 KHz)	• 32 KHz RC • Lower consumption, higher accuracy (refer to product datasheet)
HSE	4 to 32 MHz	4 to 48 MHz
LSE	• 32.768 KHz • Configurable drive/consumption • Available in backup domain (VBAT)	
HSI48	NA	• 48 MHz RC • Can drive USB FULL Speed and RNG
PLL	• Internal PLL can be used to multiply HSI or HSE output clock frequency • The PLL sources are HSI and HSE	• Internal PLL can be used to multiply HSI16 or HSE output clock frequency • The PLL sources are HSI16 and HSE • The PLL multiplication/division factors are different from STM32F3 line
System clock source	HSI, HSE or PLL	HSI16, HSE or PLL
System clock frequency	• Up to 72 MHz • 8 MHz after reset using HSI	• Up to 150 MHz • 16 MHz after reset using HSI16
AHB frequency	Up to 72 MHz	Up to 150 MHz
APB1 frequency	Up to 36 MHz	Up to 150 MHz
APB2 frequency	Up to 72 MHz	Up to 150 MHz
RTC clock source	LSI, LSE or HSE/32	LSI, LSE or HSE/32
Clock-out capability	• MCO pin (PA8): LSI, LSE, SYSCLK, HSI, PLLCLK/2	• MCO pin (PA8): LSI, LSE, SYSCLK, HSI16, HSI48, HSE, PLLCLK • LSCO pin (PA2): LSI, LSE. This output remains available in Stop (Stop 0 and Stop 1) and Standby modes.
CSS	• CSS on HSE (clock security system)	• CSS on HSE (clock security system) • CSS on LSE
Internal/external clock measurement	• with TIM16	• with TIM5/TIM15/TIM16/TIM17
Interrupt	• CSS (linked to NMI IRQ) • PLLRDY, HSERDY, HSIRDY, LSERDY, LSIRDY (linked to RCC global IRQ)	• CSS (linked to NMI IRQ) • LSECSS, LSIRDY, LSERDY, HSIRDY, HSERDY, PLLRDY (linked to RCC global IRQ)

In addition to the differences described in Table 13, the additional adaptation steps described in Section 4.5.1: Performance versus Vcore ranges, Section 4.5.2: Peripheral access configuration and Section 4.5.3: Peripheral clock configuration may be needed for the migration.

4.5.1 Performance versus Vcore ranges

In STM32G431xx/G474xx/G491xx devices, the maximum CPU clock frequency and number of Flash memory wait states depend on the selected voltage range V_{core}.

Table 14. STM32G431xx/G474xx/G491xx devices performance versus Vcore ranges

CPU performance	Power performance	Vcore Range	Typical value (V)	Max frequency (MHz)				
				4 WS	3 WS	2 WS	1 WS	0 WS
High	Medium	1 boost mode	1.28	170	136	102	68	34
		1 normal mode	1.2	150	120	90	60	30
Medium	High	2	1.0	-	-	26	24	12

Note: WS = wait state

On STM32F303 line, the maximum CPU clock frequency and the number of Flash memory wait states are linked by the below conditions:

- Zero wait state, if 0 < HCLK ≤ 24 MHz
- One wait state, if 24 MHz < HCLK ≤ 48 MHz
- Two wait states, if 48 MHz < HCLK ≤ 72 MHz.

4.5.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in STM32G431xx/G474xx/G491xx devices compared to STM32F303/334 lines, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from reset mode] (see Table 15).

Table 15. RCC registers used for peripheral access configuration

Bus	Register STM32F303 line	Register STM32G431xx/ G474xx/G491xx	Comments
AHB	RCC_AHBRSTR	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHBENR	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3)	Used to [enable/disable] the AHB peripheral clock
	NA	RCC_AHB1SMENR (AHB1) RCC_AHB2SMEUR (AHB2) RCC_AHB3SMEUR (AHB3)	Used to [enable/disable@ the AHB peripheral clock in sleep and stop modes
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2	Used to [enter/exit@ the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2	Used [enable/disable] the APB1 peripheral clock
	NA	RCC_APB1SMENR1 RCC_APB1SMEUR2	Used to [enable/disable] the APB1 peripheral clock in sleep and stop modes
APB2	RCC_APB2STR	Used to [enable/disable] the APB2 peripheral from reset	
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	NA	APB2	Used to [enable/disable] the APB2 peripheral clock in sleep and stop modes

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source independent from the system clock that is used to generate the clock required for their operation.

- USB:
  - In STM32F303 line: the USB 48 MHz clock is derived from the PLL VCO.
  - In STM32G431xx/G474xx/G491xx devices: the USB 48 MHz clock is derived from one of the following sources:
    - Main PLL (PLLQCLK)
    - HSI48 internal oscillator
- ADC:
  - In STM32F303 line: the ADCs asynchronous clock is derived from the PLL output. It can reach 72 MHz and can then be divided by 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128 or 256.
  - In STM32G431xx/G474xx/G491xx devices: the asynchronous ADCs clock can be derived from one of the two following sources:
    - System clock (SYSCLK)
    - Main PLL (PLLPCLK)

In STM32G431xx/G474xx/G491xx devices, the maximum ADC clock frequency is up to 60 MHz (refer to the ADC characteristics table in the product datasheet). Consequently , a prescaler must be used when the ADC clock source value is greater than the specified max ADC clock frequency.

The ADC clock source can be divided by 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128 or 256.

- DAC:
  - In STM32G431xx/G474xx/G491xx devices: in addition to the PCLK1 clock, LSI clock is used for the sampling and hold operation.

4.6 Power control (PWR)

In STM32G431xx/G474xx/G491xx devices, the PWR controller presents some differences when compared to STM32F303 line. These differences are summarized in Table 16.

Table 16. PWR differences between STM32F303 line and STM32G431xx/G474xx/G491xx devices

PWR	STM32F303 line	STM32G431xx/G474xx/G491xx
Power supplies	• VDD = 2.0 to 3.6V: external power supply for I/Os, Flash memory and internal regulator • It is provided externally through VDD pins	• VDD = 1.71 to 3.6V: external power supply for I/Os, Flash memory and internal regulator. • It is provided externally through VDD pins
	• VDD18= 1.65 to 1.95 V • VDD18 is the power supply for digital core, SRAM and Flash memory • VDD18 is internally generated through an internal voltage regulator	• Vcore = 1.0 to 1.28V • Vcore is the power supply for digital peripherals, SRAMs and Flash memory • It is generated by an internal voltage regulator • Two Vcore ranges can be selected by software depending on target frequency.
	VBAT = 1.65 to 3.6V: power supply for RTC, external clock, 32 KHz oscillator and backup registers (through power switch) when VDD is not present	VBAT = 1.55 to 3.6V: power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when VDD is not present
	VDD must always be kept lower than or equal to VDDA	
	• VSSA, VDDA STM32F303x6/8/B/C/D/E = 2.0 to 3.6V • External power supply for ADC, DAC, comparators, operational amplifiers, temperature sensor, PLL, HSI 8MHz oscillator, LSI 40KHz oscillator and reset block • VDDA must be in the 2.4 to3.6 V range when the OPAMP and DAC are used • It is forbidden to have VDD<VDD – 0.4V • An external Schottky diode must be placed between VDD and VDDA to guarantee that this condition is met	• VSSA, VDDA = – 1.62V (ADCs/COMPs) to 3.6V – 1.8V (DACs/OPAMPs) to 3.6V – 2.4V (VREFBUF) to 3.6V • VDDA is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators • The VDDA voltage level is independent from the VDD voltage
Battery backup domain	• RTC with backup registers (64 bytes on B/C, 20 bytes on 6/8) • LSE • PC13 to PC15 I/Os	• RTC with backup registers (128 bytes) • LSE • PC13 to PC15 I/Os
Power supply supervisor	• Integrated POR/PDR circuity • Programmable voltage detector (PVD)	
	• NA	• Brown-out reset (BOR) • BOR is always enabled, except in Shutdown mode
	• NA	• PVM

PWR	STM32F303 line	STM32G431xx/G474xx/G491xx
Low-power modes	• NA	• Low Power Run mode • System clock is limited to 2MHz • Consumption is reduced at lower frequency thanks to LP regulator usage •
	• Stop mode • (all clocks are stopped)	• Stop0, Stop1 mode • Some additional functional peripherals (see wakeup source)
	• Standby mode • (VDD18 domain powered off)	• Standby mode • (Vcore domain powered off) • Optional SRAM2 retention • Optional I/O pull-up or pull-down configuration
	• NA	• Shutdown mode • (Vcore domain powered off and power monitoring off)
Wake-up sources	• Sleep mode • Any peripheral interrupt/wakeup event	• Sleep mode • Any peripheral interrupt/wakeup event
	• Stop mode • Any EXTI line /interrupt • PVD, USB wakeup, RTC, COMPx I2Cx, U(S)ARTx	• Stop 0, Stop 1 mode • Any EXTI line/interrupt • BOR,PVD,PVM,COMP,RTC,USB,IWDG • U(S)ART,LPUART,I2C,LPTIM
	• Standby mode • NRST external reset • IWDG reset • 3 WKUP pins • RTC event	• Standby mode • 5WKUP pins rising or falling edge • RTC event • External reset in NRST pin • IWDG reset
	• NA	• Shutdown mode • 5 WKUP pins rising or falling edge • RTC event • External reset in NRST pin
Wake-up clocks	• Wake-up from Stop • HSI RC clock	• Wake-up from Stop • HSI16 16MHz allowing wakeup at high speed without waiting for PLL startup time
	• Wake-up from Standby • HSI RC clock	• Wake-up from Standby • HSI RC clock
	• NA	• Wake-up from Shutdown • HSI RC clock

4.7 Real-time clock (RTC)

STM32G431xx/G474xx/G491xx devices and STM32F303 line implement almost the same features on the RTC. Table 17 shows the few differences.

Table 17. SYSCFG differences between STM32F303 line and STM32G431xx/G474xx/G491xx devices

RTC	STM32F303 line	STM32G431xx/G474xx/G491xx
Features	Smooth calibration available	Smooth calibration available
	3 tamper pin (available in VBAT)	3 tamper pin (available in VBAT)
	• On STM32F303xB/C/D/E: 64 bytes backup registers • On STM32F303x6/8: 20 bytes backup registers	128 bytes backup registers

For more information, refer to the RTC section of STM32G4xx devices reference manual.

4.8 System configuration controller (SYSCFG)

The STM32G431xx/G474xx/G491xx devices implement additional features compared to the STM32F303 line.Table 18 shows the differences.

Table 18. SYSCFG differences between STM32F303 line and STM32G431xx/G474xx/G491xx devices

SYSCFG	STM32F303 line	STM32G431xx/G474xx/G491xx
Features	• Remapping memory areas • Managing the external input line connection to the GIOs • Setting CCM SRAM write protection and software erase • Enabling/disabling I2C Fast-mode Plus riving capability on some I/Os • ADC Triggers remapping • DAC Triggers remapping	• Remapping memory areas • Managing the external input line connection to the GPIOs • Managing robustness feature • Setting CCM SRAM write protection and software erase • Configuring FPU interrupts • Enabling/disabling I2C Fast-mode Plus driving capability on some I/Os and voltage booster fr I/Os analog switches
Configuration	-	• A few bits are different and EXTI configuration may differ (number of GPIO is different depending on product)

4.9 General-purpose I/O interface (GPIO)

The STM32G431xx/G474xx/G491xx devices GPIO peripheral embeds some identical features compared to the STM32F303/334 lines.

The GPIO code written for the STM32F303/334 devices may require minor adaptations for STM32G431xx/G474xx/G491xx devices. This is due to the mapping of particular functions on different GPIOs (refer to Section 2.1: Package availability for pin out differences, and to product datasheet for the detailed alternate function mapping differences).

At reset, the STM32F303/334 GPIOs are configured in input floating mode while the STM32G431xx/G474xx/G491xx devices GPIOs are configured in analog mode (to avoid consumption through the IO Schmitt trigger).

In the STM32G431xx/G474xx/G491xx, it becomes possible to enable/disable the pull down, so the combination PUPD = 10 is no more reserved. The pull up remains disabled by hardware.

For more information about the STM32G431xx/G474xx/G491xx devices GPIO programming and usage, refer to the “I/O pin multiplexer and mapping” section in the GPIO section of the STM32G431xx/G474xx/G491xx devices reference manuals and to the product datasheet for detailed description of the pinout and alternate function mapping.

4.10 Flash memory

Table 19 presents the differences between the Flash memory interfaces of STM32F303/334 compared to STM32G431xx/G474xx/G491xx devices.

For more information on programming, erasing and protection of STM32G431xx/G474xx/G491xx devices Flash memory, refer to the STM32G4xx reference manuals.

Table 19. FLASH differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices

Flash	STM32F303/334	STM32G431xx/G474xx/G491xx
Main/ Program memory	0x0800 0000 to (up to) 0x0807 FFFF	0x0800 0000 to 0x0807 FFFF
	• Up to 512 Kbytes • 1 bank • Up to 256 pages of 2 Kbytes • Programming granularity: 64-bit • Read granularity: 128-bit	**STM32G431xx** • 128 Kbytes • Single bank • Memory contains 64 pages of 2 Kbytes and each page: 8 rows of 256 bytes • Read width of 64-bits .
		STM32G474xx • 512 Kbytes • Split in 2 banks – When dual bank is enabled each bank: 128 pages of 2 Kbytes and each page: 8 rows of 256 bytes – When dual bank is disabled: memory block contains 128 pages of 4 Kbytes and each page: 8 rows of 512 bytes • Read width of 128 bits in single bank mode or read width of 64-bits in dual bank mode.
		STM32G491xx • 512 Kbytes • Single bank • Memory contains 256 pages of 2 Kbytes and each page: 8 rows of 256 bytes • Read width of 64-bits .
Features	NA	• Read while write (RWW) • Dual bank boot (Only on STM32G474xx)
Wait state	Up to 2 (depending on the frequency)	Up to 4 (depending on the frequency)
ART Accelerator	NA	• Instruction cache, data cache and pre-fetch buffer allowing linear performance in relation to frequency
One time programmable		1 Kbyte OTP bytes
Erase granularity	Page erase and mass erase	Page erase, bank erase and mass erase
Read protection (RDP)	• Level 0 no protection • RDP = 0xAA	• Level 0 no protection • RDP = 0xAA
	• Level 1 memory protection • RDP ≠ {0xAA, 0xCC}	• Level 1 memory protection • RDP ≠ {0xAA, 0xCC}
	Level 2 RDP = OxCC(1)	Level 2 RDP = OxCC(1)
Proprietary code readout protection (PCROP)	NA	YES

Flash	STM32F303/334	STM32G431xx/G474xx/G491xx
ECC	NA	• 8 bits for 64-bit double-word • Single error detection and correction • Double error detection
Securable memory area	NA	YES
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	SRAM_PE	SRAM_PE
	VDDA_MONITOR	NA
	RDP	RDP
	nRDP	NA
	USER	
	nUSER	
	NA	nRST_SHDW
	WDG_SW	IWDG_SW
	nBOOT1	nBOOT1
	NA	BOR_LEV[2:0]s
		IWDG_STOP, IWDG_STDBY
		WWDG_SW
		BFB2
		DBANK
		CCMSRAM_RST
		nSWBOOT0
		nBOOT0
		PG10_Mode
		IRH_EN

1. *Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1*

4.11 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32G431xx/G474xx/G491xx devices implement several new features on the U(S)ART when compared to the STM32F303/334. Table 20, Table 21 and Table 22 show the differences.

Table 20. U(S)ART differences between STM32F303/F334 and STM32G431xx/G474xx/G491xx devices

U(S)ART	STM32F303/334	STM32G431xx/G474xx/G491xx
Instances	• Up to 3 x USART • Up to 2 x UART	• 3 x USART • 2 x UART in G474xx/G491xx and 1 x UART in G431xx
Baud rate	Up to 9 Mbits/s	• Up to 18.75 Mbit/s

Table 21. **STM32F303/334 USART features**

USART modes/ features(1)	STM32F303xB/C			STM32F303xD/E			STM32F303x6/8 STM32F334	
	USART1/ USART2/ USART3	UART4	UART5	USART1/ USART2/ USART3	UART4	UART5	USART1	USART2/ USART3
Hardware flow control for modem	X	-	-	X	-	-	X	X
Continuous communication using DMA	X	X	-	X	X	-	X	X
Multiprocessor communication	X	X	X	X	X	X	X	X
Synchronous mode	X	-	-	X	-	-	X	X
Smartcard mode	X	-	-	X	-	-	X	-
Single-wire half-duplex communication	X	X	X	X	X	X	X	X
irDA SIR ENDEC block	X	X	X	X	X	X	X	-
LIN mode	X	X	X	X	X	X	X	-
Dual clock domain and wakeup from Stop mode	X	X	X	X	X	X	X	-
Receiver timeout interrupt	X	X	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	X	X	-
Auto baud rate detection	X	-	-	X	-	-	X	-
Driver Enable	X	-	-	X	-	-	X	X
USART data length	8 and 9 bits			7, 8 and 9 bits			7, 8 and 9 bits	

1. *X = Supported.*

Table 22. STM32G431xx/G474xx/G491xx USART/LPUART features

USART modes/features[1]	USART1/2/3	UART4/5[2]	LPUART
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode (Master/Slave)	X	-	-
Smartcard mode	X	-	-
Single-wire Half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual clock domain and wakeup from low-power mode	X	X	X
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto baud rate detection	X	X	-
Driver Enable	X	X	X
USART data length	7, 8 and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size	8		

1. *X = supported*
2. *UART5 is not available on the G431xx.*

4.12 Serial peripheral interface (SPI) / IC to IC sound (I2S)

Table 23 shows the differences.

Table 23. SPI differences between STM32F303 line and STM32G431xx/G474xx/G491xx devices

SPI	STM32F303 line	STM32G431xx/G474xx/G491xx
Instances	• x3 (STM32F303xB/C) • x4 (STM32F303xD/E) • x1 (STM32F303x6/8)	• x 4 on STM32G474xx • x 3 on STM32G431xx/G491xx
Features	• STM32F303xB/C = 3 x SPI + 2 x I2S (full duplex) • SM32F303xD/E = 4 x SPI + 2 x I2S (full duplex) • STM32F303x6/8 = 1 x SPI +0 x I2S	• STM32G474xx = 4 x SPI + 2 x I2S (half duplex) • STM32G431xx/G491xx = 3 x SPI + 2 x I2S (half duplex)
Speed	Up to 18 Mbit/s	Up to 41 Mbits/s

4.13 USB full speed (USB FS)

The main differences are listed in Table 24.

Table 24. USB differences between STM32F303 and STM32G431xx/G474xx/G491xx devices

USB FS	STM32F303	STM32G431xx/G474xx/G491xx
Features	• Universal serial bus revision 2.0 • STM32F404xD/E embed the USB with LPM support	• Universal serial bus revision 2.0 including link power management (LPM) support • CRS for USB clock
	• Configurable number of endpoints from 1 to 8 • Cyclic redundancy check (CRC) generation/checking, Non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing • Isochronous transfers support • Double-buffered bulk/isochronous endpoint support • USB Suspend/Resume operations • Frame locked clock pulse generation.	
	NA	• Attach detection protocol (ADP) • Battery charging detection (BCD) • USB connect/disconnect capability (controllable embedded pull-up resistor on USB_DP line)
Mapping	APB1	
Buffer memory	• STM32F303xB/C: 512 bytes of dedicated packet buffer memory SRAM • STM32F303xD/E: 1024 bytes of dedicated packet buffer memory SRAM. When the CAN peripheral clock is enabled in the RCC_APB1ENR register, only the first 768 Bytes are available to USB while the last 256 bytes are used by CAN	1024 bytes of dedicated packet buffer memory SRAM
Low-power modes	• USB suspend and resume • STM32F303xD/E: Link power management (LPM) support	• USB suspend and resume • Link power management (LPM) support

4.14 Analog-to-digital converters (ADC)

Table 25 shows the differences between the STM32F303/334 and STM32G431xx/G474xx/G491xx devices ADC peripherals.

Table 25. ADC differences between STM32F303/334 and STM32G431xx/G474xx/G491xx devices

ADC	STM32F303/334		STM32G431/G474/G491xx	
ADC Type	SAR structure		SAR structure	
Instances	• 4 instances (STM32F303xB/C/D/E) • 2 instances (STM32F303x6/8 and STM32F334)		• 5 instances in STM32G474xx • 3 instances in STM32G491xx • 2 instances in STM32G431xx	
Maximum sampling frequency	• 5.1 Msps (Fast channels) • 4.8 Msps (Slow channels		• 4 Msps	
Maximum ADC clock frequency	72 MHz		The maximum ADC clock frequency depends on the ADC configuration (single or multiple and single ended or differential). For more details, refer to the device datasheet.	
Number of channels	Up to 19 channels per ADC		• Up to 42 channels in STM32G474xx • Up to 36 channels in STM32G491xxx • Up to 18 channels in STM32G431xxx	
Resolution	12-bit		12-bit	
DMA	Yes		Yes	
External Trigger	External event for regular group: **ADC1/2** TIM1_CC1 TIM1_CC2 TIM1_CC3 TIM2_CC2 TIM3_TRGO TIM4_CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4	External event for injected group: **ADC1/2** TIM1_TRGO TIM1_CC4 TIM2_TRGO TIM2_CC1 TIM3_CC4 TIM4_TRGO EXTI line 15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO	External event for regular group: **ADC1/2** TIM1_CC1 TIM1_CC2 TIM1_CC3 TIM2_CC2 TIM3_TRGO TIM4_CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4 TIM20_TRGO TIM20_TRGO2 TIM20_CC1 TIM20_CC2 TIM20_CC3 HRTIM_ADCTRG1 HRTIM_ADCTRG3 HRTIM_ADCTRG5 HRTIM_ADCTRG6 HRTIM_ADCTRG7 HRTIM_ADCTRG8 HRTIM_ADCTRG9 HRTIM_ADCTRG10 LPTIMOUT TIM7_TRGO	External event for injected group: **ADC1/2** TIM1_TRGO TIM1_CC4 TIM2_TRGO TIM2_CC1 TIM3_CC4 TIM4_TRGO EXTI line 15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO TIM20_TRGO TIM20_TRGO2 TIM20_CC4 HRTIM_ADCTRG2 HRTIM_ADCTRG4 HRTIM_ADCTRG5 HRTIM_ADCTRG6 HRTIM_ADCTRG7 HRTIM_ADCTRG8 HRTIM_ADCTRG9 HRTIM_ADCTRG10 TIM16_CC1 LPTIMOUT TIM7_TRGO
External Trigger	External event for regular group: **ADC3/4**	External event for injected group: **ADC3/4**	External event for regular group: **ADC3/4/5**	External event for injected group: **ADC3/4/5**

ADC	STM32F303/334		STM32G431/G474/G491xx	
	TIM3_CC1 TIM2_CC3 TIM1_CC3 TIM8_CC1 TIM8_TRGO EXTI line 2 TIM4_CC1 TIM2_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM3_TRGO TIM4_TRGO TIM7_TRGO TIM15_TRGO TIM2_CC1	TIM1_TRGO TIM1_CC4 TIM4_CC3 TIM8_CC2 TIM8_CC4 TIM4_CC3 TIM4_CC4 TIM4_TRGO TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM1_CC3 TIM3_TRGO TIM2_TRGO TIM7_TRGO TIM15_TRGO	TIM3_CC1 TIM2_CC3 TIM1_CC3 TIM8_CC1 TIM3_TRGO EXTI line 2 TIM4_CC1 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM2_CC1 TIM20_TRGO TIM20_TRGO2 TIM20_CC1 HRTIM_ADCTRG2 HRTIM_ADCTRG4 HRTIM_ADCTRG1 HRTIM_ADCTRG3 HRTIM_ADCTRG5 HRTIM_ADCTRG6 HRTIM_ADCTRG7 HRTIM_ADCTRG8 HRTIM_ADCTRG9 HRTIM_ADCTRG10 LPTIMOUT TIM7_TRGO	TIM1_TRGO TIM1_CC4 TIM2_TRGO TIM8_CC2 TIM4_CC3 TIM4_TRGO TIM4_CC4 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM1_CC3 TIM3_TRGO EXTI line 3 TIM6_TRGO TIM15_TRGO TIM20_TRGO TIM20_TRGO2 TIM20_CC2 HRTIM_ADCTRG2 HRTIM_ADCTRG4 HRTIM_ADCTRG5 HRTIM_ADCTRG6 HRTIM_ADCTRG7 HRTIM_ADCTRG8 HRTIM_ADCTRG9 HRTIM_ADCTRG10 HRTIM_ADCTRG1 HRTIM_ADCTRG3 LPTIMOUT TIM7_TRGO
Supply requirement	2.0 V to 3.6 V		- 1.62 V to 3.6 V - Independent power supply (VDDA)	
Reference Voltage	• External • 2.0V ≤ VREF+ ≤ VDDA		Reference voltage for STM32G431xx/G474xx/G491xx (1.62 V to VDDA) or internal (2.048 V, 2.5 V or 2.9 V)	
Features	The STM32G431xx/G474xx/G491xx ADC has additional features comparing to the STM32F303/334 ADC such as: 16-bit oversampling, gain/offset compensation etc...		-	
Input range	VREF- ≤ VIN ≤ VREF+		VREF- ≤ VIN ≤ VREF+	

4.15 Digital-to-analog converter (DAC)

The STM32G431xx/G474xx/G491xx implements some additional features compared to the STM32F303/334 lines ones. Table 26 shows the differences.

Table 26. DAC differences between STM32F303/334 and STM32G431xx/G474xx/G491xx devices

DAC	STM32F303/334	STM32G431xx/G474xx/G491xx
Instances	• For STM32F303xB/C/D/E: – 2 x 12-bit DAC channels with output buffer • For STM32F303x/6/8 and STM32F334: – 3x12-bit DAC channels – Output buffer only on DAC1 ch1	• For STM32G474xx: – 7 DAC channels (3 external 1MSPS (with output buffer) and 4 internal 15MSPS (without output buffer)) • For STM32G431xx/G491xx: – 4 DAC channels (2 external 1MSPS with output buffer and 2 internal 15MSPS without output buffer) • Maximum two output channels per DAC
Resolution	12 bits	12 bits
Features	• Left or right data alignment in 12-bit mode • Noise-wave and triangular-wave generation (DAC1 only) • Dual DAC channel for independent or simultaneous conversions • DAC output connection to on chip peripherals	• Left or right data alignment in 12-bit mode • Noise-wave, triangular-wave generation and sawtooth • Dual DAC channel for independent or simultaneous conversions • DAC output connection to on chip peripherals • Sample and Hold mode for low power operation in Stop mode • Double data DMA capability to reduce the bus activity
DMA	Yes	Yes
External Trigger	**DAC1** TIM6_TRGO TIM3_TRGO or TIM8_TRGO TIM7_TRGO TIM15_TRGO TIM2_TRGO TIM4_TRGO EXTI line9 SWTRIG **DAC2** TIM6_TRGO TIM3_TRGO TIM7_TRGO TIM15_TRGO TIM2_TRGO EXTI line9 SWTRIG	**DAC1/2/4** TIM8_TRGO TIM7_TRGO TIM15_TRGO TIM2_TRGO TIM4_TRGO EXTI10 TIM6_TRGO TIM3_TRGO HRTIM_step_trig_1 HRTIM_step_trig_2 HRTIM_step_trig_3 HRTIM_step_trig_4 HRTIM_step_trig_5 HRTIM_step_trig_6 SWTRIG **DAC3** TIM1_TRGO TIM7_TRGO TIM15_TRGO TIM2_TRGO TIM4_TRG EXTI10 TIM6_TRGO TIM3_TRGO HRTIM_rst_trig_1 HRTIM_rst_trig_2

DAC	STM32F303/334	STM32G431xx/G474xx/G491xx
		HRTIM_rst_trig_3 HRTIM_rst_trig_4 HRTIM_rst_trig_5 HRTIM_rst_trig_6 SWTRIG
Supply requirement	2.4 V to 3.6 V	- 1.71 V to 3.6 V - Independent power supply (VDDA)
Reference Voltage	External 2.4 V ≤ VREF+ ≤VDDA	External (1.71 V to VDDA) or internal (2.048 V, 2.5 V or 2.9 V)

4.16 Comparator (COMP)

Table 27 shows the differences between the COMP interface of STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices.

Table 27. COMP differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices

COMP	STM32F303/334	STM32G431xx/G474xx/G491xx
Instances	• COMP1/2/3/4/5/6/7 on STM32F303xB/C/D/E • COMP2, COMP4, COMP6 on STM32F303x6/8 and STM32F334	• COMP1/2/3/4/5/6/7 on STM32G474xx • COMP1/2/3/4 on STM32G431xx/G491xx
Input	• COMP1/2/3/4/5/6/7: – Inverting: – 7(DAC1_CH1, DAC1_CH2, DAC2_CH1, Vrefint, ¾ Vrefint, ½ Vrefint, ¼ Vrefint) • COMP1:Non Inverting: 2(PA1, PA0) • COMP2: Non inverting: 3(PA3,PA7,PA2) • COMP3: Non inverting: 4(PB12, PD15, PB14, PD14) • COMP4: Non Inverting : 4(PB0, PE7,PB2,PE8) • COMP5: Non inverting: 4 (PB10, PD13,PB13,PD12) • COMP6: Non inverting 4 (PB11, PD11, PB15, PD10) • COMP7: Non inverting: 3(PC1, PA0, PC0)	• COMP1/2/3/4/5/6/7: inverting: (Vrefint, ¾ Vrefint, ½ Vrefint, ¼ Vrefint) • COMP1/3:Inverting (DAC3_CH1,DAC1_CH1) • COMP2/4:Inverting (DAC1_CH1, DAC3_CH2) • COMP5/7:Inverting (DAC4_CH1,DAC1_CH2) • COMP6:Inverting DAC4_CH2,DAC2_CH1) • COMP1:Non Inverting (PA1,PB1) • COMP2:Non inverting (PA3,PA7) • COMP3: Non inverting (PC1, PA0) • COMP4: Non inverting (PB0,PE7) • COMP5:Non inverting (PB13, PD12) • COMP6: Non inverting (PB11, PD11) • COMP7:Non inverting (PB14, PD14)
Output	• Output connection to GPIOs, Timers, HRTIM, wakeup	• Output connection to GPIOs, Timers, HRTIM, wakeup
Propagation delay	25 ns	16.7 ns
Features	Window comparator (only on STM32F303xB/C): COMP1/2, COMP3/4 and COMP5/6 • Output with blanking source • Programmable hysteresis only on STM32F303xB/C Programmable speed/consumption (only on STM32F303xB/C)	• Output with blanking source • Programmable hysteresis
Supply requirement	2.0V to 3.6 V	1.62 V to 3.6 V
Input range	VREF-≤ VIN ≤ VREF+	

4.17 Operational amplifier (OPAMP)

STM32G431xx/G474xx/G491xx devices implement some enhanced OPAMPs compared to STM32F303/334 devices. Table 28 shows the differences.

Table 28. OPAMP differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices

OPAMP	STM32F303/334	STM32G431xx/G474xx/G491xx
Instances	• Up to four	• 6 (STM32G474xx) • 4 (STM32G491xx) • 3 (STM32G431xx)
Features	• Rail-to-rail input and output voltage range • Low input bias current • Low input offset voltage • Low power mode • Fast wakeup time •	
	Programmable gain amplifier (PGA) are 2,4,8 and 16.	Programmable gain amplifier (PGA) are: 2, 4, 8, 16, 32, 64, -1, -3, -7, -15, -31, -63
	• Gain bandwidth of 8 MHz	• Gain bandwidth of 13 MHz
Timer controlled Multiplexer mode	• The switch is triggered by TIM1_CC6 signal only	• The switch is triggered by TIM1_CC6 or TIM8_CC6 or TIM20_CC6 signal
Configuration	-	• Register mapping is not the same • Refer to STM32G4xx reference manuals for details

4.18 GPTimer (General purpose timer)

The STM32G431xx/G474xx/G491xx devices implement several new features on the GPTimer when compared to STM32F303/334 devices. Table 29 shows the differences.

Table 29. GPTimer differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices

GPTimer	STM32F303/334	STM32G431xx/G474xx/G491xx
Instance	• STM32F303xD/E: TIM1/TIM8,TIM20, TIM2, TIM3, TIM4, TIM15, TIM16, TIM17, TIM6, TIM7 • STM32F303xB/xC: TIM1,TIM8,TIM2,TIM3,TIM15/16/17,TIM6,TIM7 • STM32F303x6/8: TIM1,TIM2,TIM3, TIM15/16/17, TIM6, TIM7	• STM32G474xx: TIM1,TIM8, TIM20,TIM2, TIM5, TIM3, TIM4, TIM15/16/17, TIM6, TIM7 • STM32G431xx: TIM1, TIM8, TIM2, TIM3, TIM4, TIM15/16/17, TIM6, TIM7 • STM32G491xx: TIM1, TIM2, TIM3, TIM4, TIM6, TIM7, TIM8, TIM15/16/17, TIM20,
Features	• Input capture • Output compare • PWM generation • One pulse mode • Break input • Complementary outputs • Encoder and Hall-sensor	
	NA	• Combined gated + reset mode • New encoding modes • Encoder index • Transition error • Encoder clock output • Asymmetric dead time • Dithering • Pulse on compare • Direction change interrupt • Direction output
Configuration	-	• Register mapping is not the same • Refer to STM32G4xx reference manuals for details

4.19 HRTIM (High-resolution timer)

Table 30 shows the differences between the HRTIM of STM32F334 line and STM32G474xx devices.

Table 30. HRTIM differences between STM32F334 line and STM32G474xx devices

HRTIM	STM32F334	STM32G474xx
Instance	HRTIM1	
Features	• 6 timers: 1 master + 5 slaves • 10 high-resolution outputs • 5 fault inputs for protection purposes • Digital kernel clocked at 144 MHz • 217 ps resolution • High-resolution deadtime insertion (down to 868 ps) • 7 interrupt vectors each one with up to 14 sources • 6 DMA requests with 14 sources.	• 7 timers: 1 master + 6 slaves • 12 high-resolution outputs • 6 fault inputs for protection purposes • Digital kernel clocked at 170 MHz • 184 ps resolution • High-resolution deadtime insertion (down to 735 ps) • 8 interrupt vectors, each one with up to 14 sources • 7 DMA requests with up 14 sources.
Configuration	-	• Register mapping is not the same • Refer to STM32G4xx reference manuals for details

Revision history

Table 31. **Document revision history**

Date	Version	Changes
01-Apr-2019	1	Initial release.
28-Apr-2020	2	Changed confidentiality level from ST Restricted to Public.
08-Jul-2020	3	Updated: • Table 14. STM32G431xx/G474xx/G491xx devices performance versus Vcore ranges , Table 11. DMA differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices, Table 19. FLASH differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices, Table 25. ADC differences between STM32F303/334 and STM32G431xx/G474xx/G491xx devices, Table 26. DAC differences between STM32F303/334 and STM32G431xx/G474xx/G491xx devices, Table 27. COMP differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices, Table 28. OPAMP differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices • Section 4.5.3: Peripheral clock configuration
08-Sep-2021	4	Replace in whole document: STM32G474xx/G431xx by STM32G431xx/G474xx /G491xx Updated: • Section 1: STM32G431xx/G474xx/G491xx overview, Section 4.5.3: Peripheral clock configuration • Table 2. Package availability on STM32G431xx/G474xx/G491xx devices, Table 8. STM32 peripheral compatibility analysis STM32F303/F334 lines compared to STM32G431xx/G474xx/G491xx, Table 9. Peripheral address mapping differences, Table 10. SRAM differences in STM32F303 line and STM32G431xx/G474xx/G491xx, Table 11. DMA differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices , Table 14. STM32G431xx/G474xx/G491xx devices performance versus Vcore ranges , Table 19. FLASH differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices, Table 20. U(S)ART differences between STM32F303/F334 and STM32G431xx/G474xx/G491xx devices, Table 23. SPI differences between STM32F303 line and STM32G431xx/G474xx/G491xx devices, Table 25. ADC differences between STM32F303/334 and STM32G431xx/G474xx/G491xx devices, Table 26. DAC differences between STM32F303/334 and STM32G431xx/G474xx/G491xx devices, Table 27. COMP differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices, Table 28. OPAMP differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices, Table 29. GPTimer differences between STM32F303/334 lines and STM32G431xx/G474xx/G491xx devices
06-Feb-2026	5	Updated document title.

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