Criteria for configuring L9945 diagnostic parameters in automotive switching applications

Introduction

The aim of this application note is to provide the criteria for configuring L9945 diagnostic parameters in automotive switching applications. The present analysis can be exploited to obtain a robust fault detection in different scenarios.

Independently of the application, this document aims at providing a set of information, equations and criteria useful to choose the correct values for the diagnostic filter times and currents, thus avoiding false detection and/or failure miss. This paper also covers the advanced diagnostic features implemented on this IC, along with their impact on application robustness. The L9945, an 8-channel configurable HS/LS pre-driver, is considered as the reference device to be used in several applications (P&H, H-Bridge, HS/LS). The ST STD105N10F7AG NMOS and ST STD10PF06T4 PMOS transistors are taken as an example of driver used in power applications.

1 Diagnostic summary

1.1 How to enable and read diagnostics

Diagnostics can be enabled/disabled by programming the **ENABLE_DIAGNOSTIC** bit via COMMAND 0, as shown in Figure 1. Diagnostic report for all channels is readable via SPI, after having issued the **0x9AAA0001** frame on MOSI line (SDI). The diagnostic status of each channel is encoded in 3 bits (**diag_xx[2-0]**), as shown in Table 1.

Table 1. Diagnostic codes

Channel Status	diag_xx[2-0]	Priority
OC pin failure (see note below)	000	1
OC failure	001	2
STG/STB failure	10	3
OL failure	11	4
No failure	100	5
No OC failure	101	6
No OL/STG/STB failure	110	7
No diagnostic done	111	8

Note: The code OC pin failure, corresponding to the code "000" is available only for channels operating in Peak & Hold. This code is unused in other configurations.

Figure 2 shows how diagnostic codes are partitioned in RESPONSE 9 frame. For an immediate fault detection, the MSB of the diagnostic code can be evaluated. An MSB equal to zero indicates that a failure occurred.

Figure 1. COMMAND 0 frame

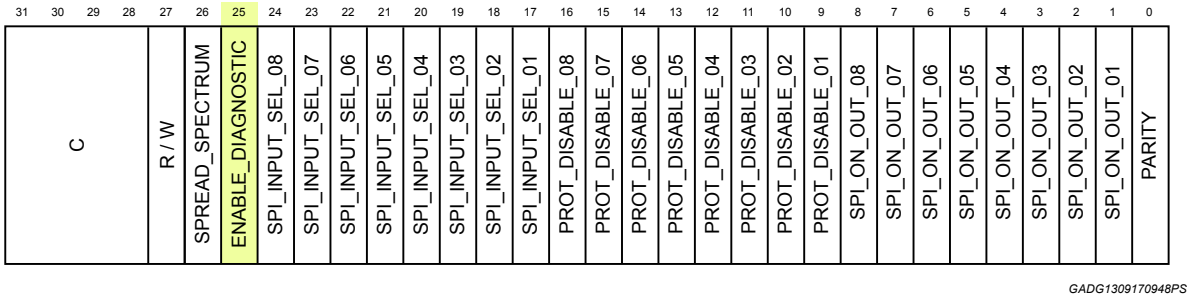

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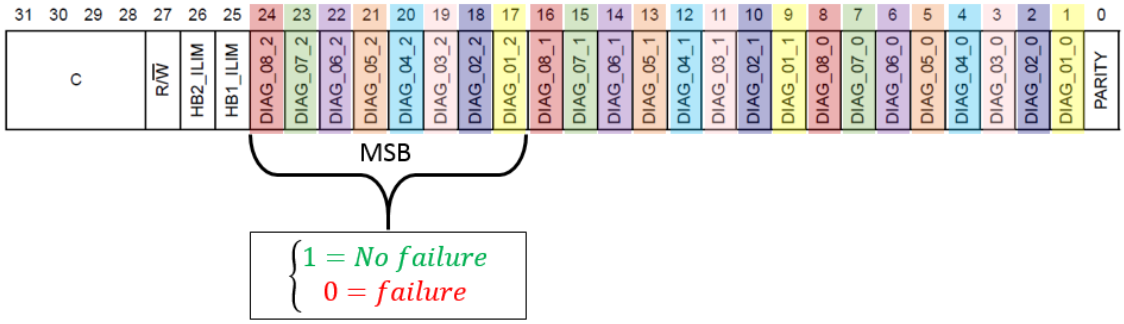
Figure 2. **RESPONSE 9 frame**



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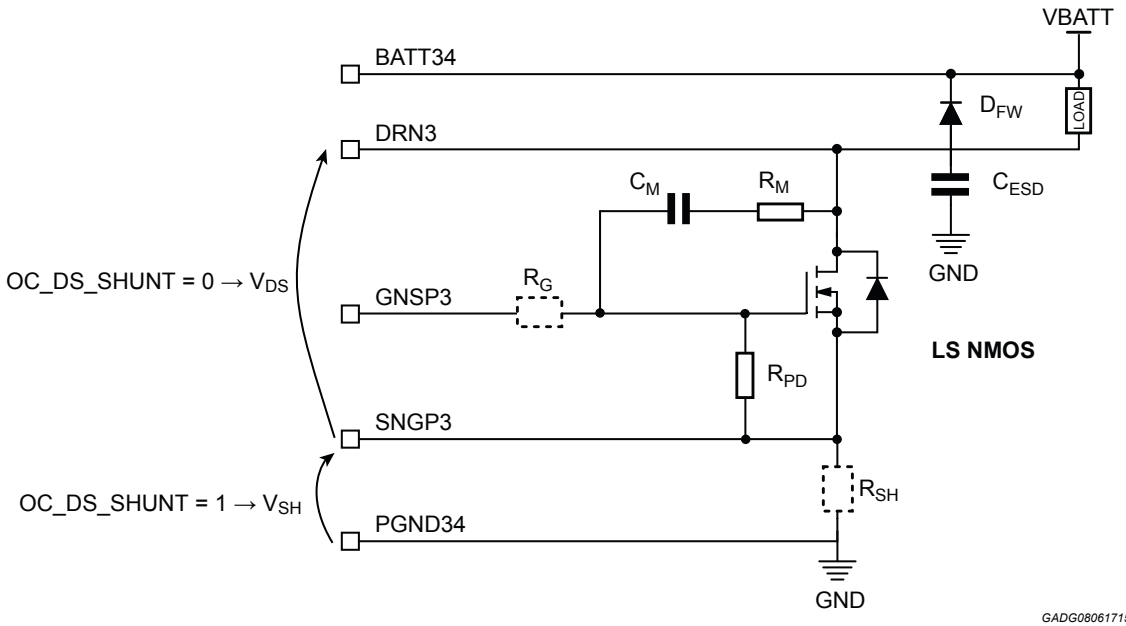
1.2 ON state diagnostics

L9945 protects the external FET against overcurrent (OC) during the ON phase. Sensing is performed measuring the voltage drop on an external element and comparing it to the programmed threshold. Refer to Table 4 for OC threshold selection. The external element can be either a shunt resistor or the FET itself: selection can be done by programming the **OC_DS_SHUNT** bit in the COMMANDx frame (x = channel index), as shown in the figure here below.

Figure 3. **OC detection method selection (example on a LS NMOS)**



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The following diagnostic codes can be set while in ON state:

- The diagnostic code corresponding to normal operation is **"No OC failure" (101)**
- The **"No failure" (100)** code will be reported only once, after an OFF->ON transition, assuming that "No OL/STG/STB failure" latch was set while in OFF state and “No OC failure” is detected
- The **"OC failure" (001)** or **"OC pin failure" (000)** codes will be reported in case of overcurrent detection

Three filter times are involved in ON diagnostics:

- t_{BLANK_OC} (programmable via SPI, see Table 2): this timer is started when the output is commanded ON, that is upon NONx 1→0 transition detection. In case t_{BLANK_OC} expires (no OC event stopped the counter), the **“No OC failure”** code is latched. The value for t_{BLANK_OC} can be selected independently of each channel by programming the **T_BLANK_OC_xx[2-0]** field in the COMMANDx frame (x = index of the channel).

- t_{FIL_ON} (fixed value, see Table 3): this is a deglitch filter to avoid false OC detection. It suppresses spikes on the OC comparator output due to the noise when the current is close to the programmed OC threshold. If the OC comparator output is high for a time interval longer than t_{FIL_ON}, the t_{OC} filter timer is started
- t_{OC} (fixed value, see Table 3): this is a filter time for OC detection. An OC event (previously deglitched by t_{FIL_ON}) lasting more than t_{OC} causes the related output to be immediately switched OFF in order to protect the external FET

1.2.1 ON state diagnostics involved parameters

Table 2. No overcurrent filter time: available values

T_BLANK_OC_xx[2-0]	Min.	Typ.	Max.	Unit
000	10	11.1	12.2	µs
001	14	15.6	17.1	µs
010	18	20	22	µs
011	28	31.1	34.2	µs
100	39	42.2	46.5	µs
101	48	53.3	58.7	µs
110	88	97.8	107.6	µs
111	128	142.2	156.5	µs

Table 3. Fixed filter times for OC detection

Parameter	Min.	Max.	Unit
t_{OC}	2	3	µs
t_{FIL_ON}	0.6	1	µs

Table 4. OC threshold selection

OC_config_xx[5-0]	Min.	Max.	Min.	Max.	Unit
	LS		HS		
0	53	67	53	69	mV
1	68	82	68	85	mV
2	83	97	83	101	mV
3	97	113	99	117	mV
4	113	128	113	133	mV
5	128	143	129	150	mV
6	142	158	144	166	mV
7	157	173	159	182	mV
8	172	188	172	198	mV
9	186	204	189	214	mV
10	201	220	204	231	mV
11	216	235	219	247	mV

OC_config_xx[5-0]	Min.	Max.	Min.	Max.	Unit
	LS		HS		
12	231	250	234	263	mV
13	246	266	248	279	mV
14	261	281	264	295	mV
15	275	296	278	311	mV
16	290	311	290	326	mV
17	305	327	305	341	mV
18	320	343	320	356	mV
19	334	358	338	375	mV
20	349	374	351	391	mV
21	364	389	367	407	mV
22	379	405	382	423	mV
23	393	420	397	439	mV
24	408	436	412	455	mV
25	423	451	427	471	mV
26	438	467	442	488	mV
27	453	482	456	504	mV
28	467	498	472	520	mV
29	482	513	486	536	mV
30	497	529	501	552	mV
31	512	544	515	568	mV
32	526	559	525	579	mV
33	541	575	545	595	mV
34	556	590	560	612	mV
35	570	606	575	628	mV
36	585	621	590	644	mV
37	600	637	604	660	mV
38	614	653	619	676	mV
39	629	668	634	693	mV
40	644	684	649	708	mV
41	658	699	663	724	mV
42	673	715	679	740	mV
43	688	730	693	756	mV
44	702	746	708	772	mV
45	717	761	723	788	mV
46	732	777	738	804	mV
47	746	792	753	821	mV
48	761	808	767	836	mV
49	776	823	782	852	mV
50	791	839	797	868	mV

OC_config_xx[5-0]	Min.	Max.	Min.	Max.	Unit
	LS		HS		
51	806	854	812	885	mV
52	820	870	827	900	mV
53	835	885	842	916	mV
54	849	900	856	933	mV
55	864	916	871	949	mV
56	878	931	886	964	mV
57	893	947	900	981	mV
58	908	962	916	997	mV
59	922	977	930	1013	mV
60	937	992	946	1029	mV
61	951	1008	960	1045	mV
62	967	1023	975	1061	mV
63	982	1038	987	1078	mV

Table 5. Gate turn on current I_{ON}: constant configuration options

GCC_config_xx	Nominal	Min.	Max.	Unit
NMOS				
01	20	19.6	32.4	mA
10	5	4	8.6	mA
11	1	1.1	1.88	mA
PMOS				
01	20	16.8	27.4	mA
10	5	3.8	7.4	mA
11	1	0.75	1.9	mA

1.3 OFF state diagnostics

L9945 detects open load (OL), short to ground (STG) on LS, and short to battery (STB) on HS during the OFF phase. Refer to Table 6 for the fault detection definition. The following diagnostic codes can be set while in OFF state:

- The diagnostic code corresponding to normal operation is **"No OL/STG/STB failure" (110)**
- The **"No failure" (100)** code will be reported only once, after an ON->OFF transition, assuming that "No OC failure" latch was set while in ON state and “No OL/STG/STB failure” is detected
- The **"OL failure" (011)** or **"STG/STB failure" (010)** codes will be reported respectively in case of open load and short to ground/battery failures

Two filter times are involved in OFF diagnostics (refer to Figure 4):

- t_{DIAG} (programmable via SPI, see Table 7): this timer is started when the output is commanded OFF, that is upon NONx → 1 transition detection. When t_{DIAG} expires, the voltage Vout on the pin connected to the load is compared to the fault thresholds VOL and VLVT (see Table 8) in order to determine the output status. If no failure is detected, the **"No OL/STG/STB failure"** code is latched. The value for t_{DIAG} can be selected independently on each channel by programming the **TDIAG_CONFIG_xx[1-0]** field in the COMMANDx frame (x = index of the channel)
- t_{FIL_OFF} (fixed value, see Table 8): this is a deglitch filter to avoid false OL/STB/STG detection. It suppresses spikes on the OL/STB/STG comparators outputs due to the noise when V_{out} is close to the V_{OL}/V_{LVT}

thresholds. If a V_{LVT} or V_{OL} comparator flags a failure for a time interval longer than t_{FIL_OFF}, the t_{DIAG} timer is reset and restarted.

Figure 4. Filter times for OFF state diagnostics: (left) STG detection on LS; (right) STB detection on HS

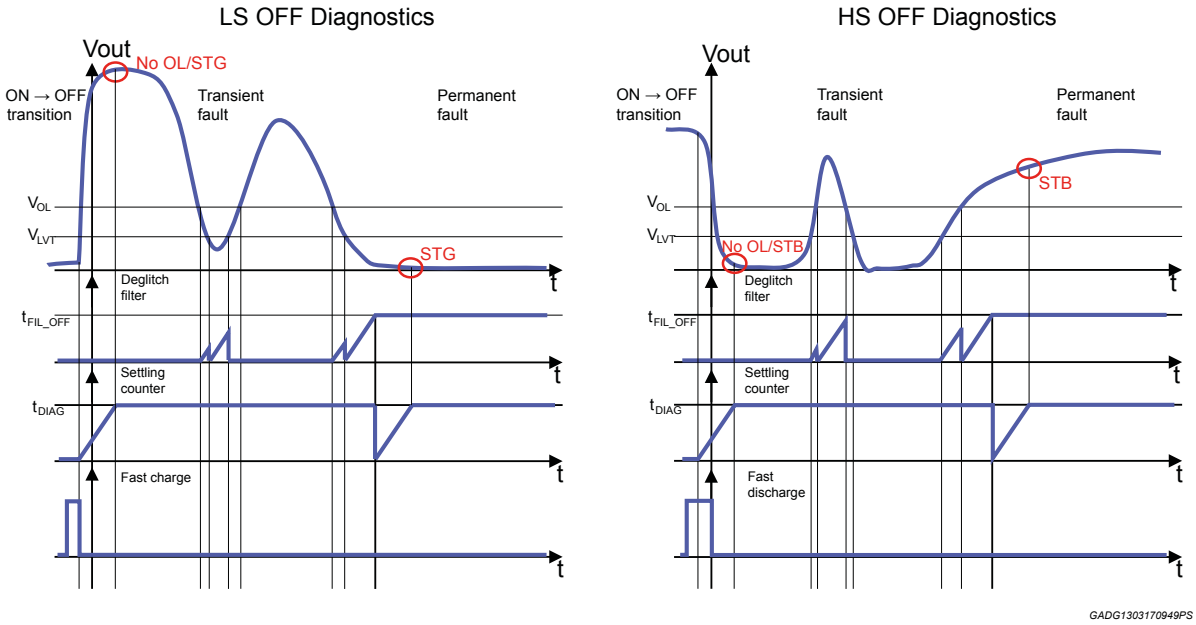


Table 6. Fault detection definition for OFF state diagnostics

FET Side	Condition	Diagnostic code
HS	$V_{out} < V_{LVT}$	"No OL/STG/STB failure" (110) or "No failure" (100)
	$V_{LVT} < V_{out} < V_{OL}$	"OL failure" (011)
	$V_{out} > V_{OL}$	"STG/STB failure" (010)
LS	$V_{out} < V_{LVT}$	"STG/STB failure" (010)
	$V_{LVT} < V_{out} < V_{OL}$	"OL failure" (011)
	$V_{out} > V_{OL}$	"No OL/STG/STB failure" (110) or "No failure" (100)

Note: V_{out} corresponds to DRNx pin for LS NMOS and HS PMOS configurations, while corresponds to SNGPx pin for HS NMOS configuration.

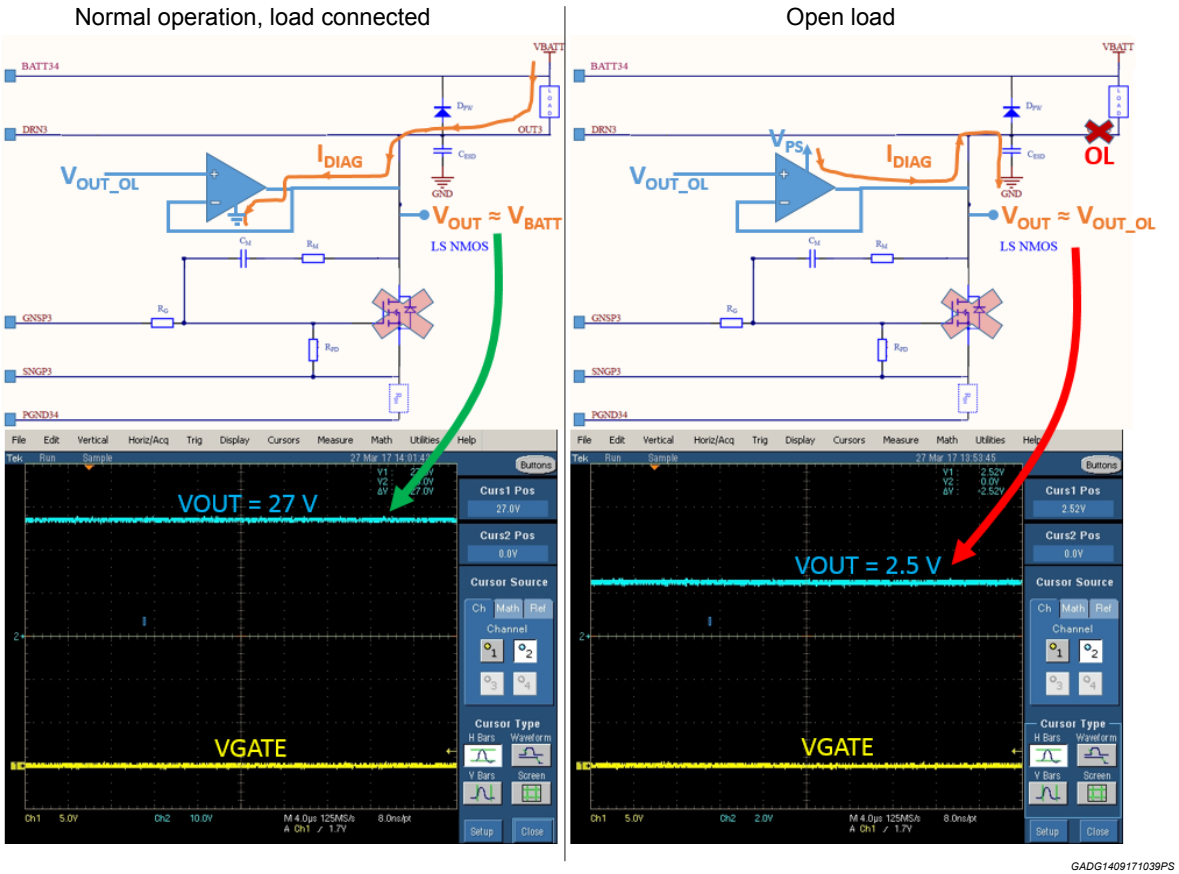
Each channel features an internal regulator with limited current capability that tries regulating the output node voltage V_{out} around V_{OUT_OL}, which falls in the [V_{LVT} ; V_{OL}] range. During normal operation, while in OFF state, the effect of the regulator current on the load is negligible due to its limited value. However, in case of open load failure, Vout will be effectively brought to V_{OUT_OL}, thus allowing OL failure detection. Refer to Figure 5 for an example.

Regulator current capability I_{DIAG} can be programmed via **diag_i_config_xx** bit in the COMMANDx frame (x = channel index), as shown in Table 9.

A higher current capability allows compensating the leakage of external devices (FET, recirculation diodes, etc.) The current limitation feature allows distinguishing between OL and STB/STG faults:

- In case of open load, the regulator is able to drive V_{out} around V_{OUT_OL} and the OL fault is flagged
- In case of STB/STG fault, due to the limited current capability, the regulator has no effect on V_{out}. Therefore, output node voltage stays below V_{LVT} (STG on LS) or above V_{OL} (STB on HS)

Figure 5. Example of OL detection on LS NMOS



In order to reliably detect a fault, the V_{out} voltage must be stable before the settling time t_{DIAG} expires:

- In case of STB/STG faults, high current capability of battery and ground supplies guarantees fast V_{out} settling.
- In case of open load, V_{out} must be brought in the [V_{LVT} ; V_{OL}] range before t_{DIAG} expires in order to guarantee fault detection. L9945 implements internal fast charge/discharge currents in order to allow the settling of V_{out} in a time suitable for detection:
  - When HS transistor is switched OFF, a fast discharge current I_{FAST_DIS} rapidly decreases V_{out} down to V_{OL} to help the OL regulator detect an eventual open load fault (see Figure 4). I_{FAST_DIS} is enabled in case:
    - The HS channel has been just switched OFF
    - The settling time t_{DIAG} is still running
    - V_{out} is below V_{LVT}
  - When LS transistor is switched OFF, a fast charge current I_{FAST_CHG} rapidly increases V_{out} up to V_{LVT} to help the OL regulator detect an eventual open load fault (see Figure 4). I_{FAST_DIS} is enabled in case:
    - The LS channel has been just switched OFF
    - The settling time t_{DIAG} is still running
    - V_{out} is above V_{OL}

Value of fast charge/discharge current depends on FET side and type, as shown in Table 11.

1.3.1 OFF state diagnostics involved parameters

Table 7. OFF state diagnostic filter time: available values

TDIAG_CONFIG_xx[1-0]	Min.	Typ.	Max.	Unit
Available for all configurations				
00	23	25.6	28.2	µs
01	55	61.2	67.4	µs
10	95	105.6	116.2	µs
11	135	150	165	µs
Available only for H-Bridge when HBx_TDIAG_EXT_CONFIG = 0				
00	10	11.2	12.4	µs
01	26	28.9	31.8	µs
10	36	40	44	µs
11	46	51.2	56.4	µs

Table 8. Fixed parameters for OFF state diagnostics

Parameter	Min.	Max.	Unit
t_{FIL_OFF}	0.3	0.5	µs
V_{OL}	2.8	3.4	V
V_{LVT}	1.9	2.3	V

Table 9. V_{out} regulator current capability I_{DIAG}

diag_i_config_xx	Min.	Max.	Unit
0	60	100	µA
1	0.6	1	mA

Table 10. Vout voltage in case of Open Load failure

VOUT_OL	Min.	Typ.	Max.	Unit
V_{out} voltage in case of Open Load	2.25	2.5	2.75	V

Table 11. Fast charge/discharge current generator electrical characteristics

Symbol	Parameter	Min.	Max.	Unit
I_{FAST_CHG}	V_{out} node fast charge current for LS NMOS	2.4	3.8	mA
$I_{FAST\_DIS\_P}$	V_{out} node fast discharge current for HS PMOS	8	13	mA
$I_{FAST\_DIS\_N}$	V_{out} node fast discharge current for HS NMOS	9	15	mA

Table 12. Gate turn off current I_{OFF}: constant configuration options

GCC_config_xx	Nominal	Min.	Max.	Unit
NMOS				
01	20	16.8	27.4	mA
10	5	3.8	7.4	mA
11	1	0.75	1.9	mA
PMOS				
01	20	19.6	32.4	mA
10	5	4	8.6	mA
11	1	0.55	1.85	mA

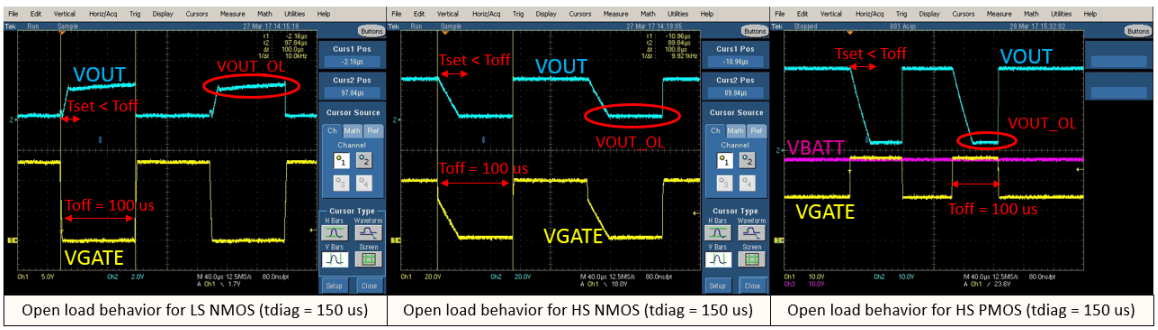
2 How to select the right filter time for OFF state diagnostics (t_{DIAG})

Two key aspects must be accounted for a robust fault detection while in OFF state. Considering a PWM signal controlling a generic output channel, the following points must be verified:

- The t_{DIAG} filter must be smaller than the PWM OFF time t_{OFF}. In fact, if the channel is switched ON before t_{DIAG} has expired, the OFF diagnostics are not performed at all. The diagnostic latches will hold the last value determined from ON state diagnostics. Refer to Figure 6 as an example of missed OL failure. In the example, the output node is stable at V_{OUT_OL} before t_{OFF} expires. Hence, OL fault could be correctly detected if a proper t_{DIAG} had been selected. However, since $t_{DIAG} > t_{OFF}$ had been intentionally programmed, the diagnostic code reported for the channel under analysis was **“No OC failure” (101)**, that is the last valid diagnostic code referred to the ON state.
  - As a consequence, a corner value for PWM t_{OFF} is represented by the smallest programmable t_{DIAG}, corresponding to 23 µs (consider a 20% additional margin for a robust behavior). A control signal with a t_{OFF} below this threshold may be correctly processed by L9945, but OFF diagnostics are not guaranteed and the external microcontroller must take care of catching eventual OL/STG/STB faults.
- The t_{DIAG} filter must be higher than the V_{out} settling time t_{SET_OFF}. If this constraint is not verified, wrong diagnostics will be reported. Referring to Figure 6, if the constraint related to settling time is not fulfilled, the sampled V_{out} might be lower than V_{LVT} in case of LS NMOS, leading to a false STG detection. In case of HS NMOS/PMOS, programming a $t_{DIAG} < t_{SET\_OFF}$ means sampling a V_{out} greater than V_{OL}, leading to a false STB detection.
  - As a consequence, t_{SET_OFF} evaluation represents a critical aspect for a correct t_{DIAG} selection. The t_{SET_OFF} is strongly dependent on the failure type and the chosen external components.
  - In case of STG/STB failures, transition on the V_{out} is almost immediate, due to the high current capability of the battery and ground supplies. Hence, failure will be detected independently on the chosen t_{DIAG} value (provided that $t_{DIAG} < t_{OFF}$).
  - In case of OL, t_{SET_OFF} depends on many application related parameters, thus representing the real boundary for the t_{DIAG} range evaluation.
    - As shown in Figure 6, settling time is significantly lower for LS NMOS configuration, due to the smaller voltage swing of the output node.
    - For a LS NMOS, in case of open load, V_{out} must be charged from GND to V_{OUT_OL}, thus implying a small output transition.
    - For a HS NMOS/PMOS, in case of open load, V_{out} must be discharged from V_{BATT} down to V_{OUT_OL}, thus implying a much wider output transition. This explains why the fast discharge currents are considerably higher than the fast charge one, as shown in Table 11.

The next figure shows an example of missed OL failure when the programmed t_{DIAG} is greater than the PWM t_{OFF}: OL on LS NMOS configuration (left); OL on HS NMOS configuration (center); OL on HS PMOS configuration (right).

Figure 6. Example of missed OL failure



Open load behavior for LS NMOS (tdiag = 150 us) | Open load behavior for HS NMOS (tdiag = 150 us) | Open load behavior for HS PMOS (tdiag = 150 us)

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Summarizing the first part of our analysis, the criterion to ensure robust OFF state diagnostics is described by the following equation:

Eq: General criterion for choosing the correct filter time for OFF state diagnostics

$$t_{SET\_OFF_{max}} < t_{DIAGmin} < t_{OFFmin} \quad (1)$$

Where:

- t_{OFFmin} depends on the PWM control signal and its minimum value must be considered
- t_{SET_OFFmax} is the output settling time in case of open load failure (worst case for settling time) and its maximum value must be considered
- $t_{DIAGmin}$ is the OFF state diagnostic filter whose minimum corner is still greater than the worst output settling time (see Table 7)

Because t_{OFF} is a PWM related parameter, it is supposed to vary along with the duty-cycle. Hence, a key point in order to allow smaller values for t_{OFF} without compromising diagnostics is to minimize the output settling time t_{SET_OFF}. In fact, the smaller the t_{SET_OFF}, the lower the t_{DIAG} and the wider the t_{OFF} range, as stated by Eq. (1).

2.1 Evaluation of the output settling time (t_{SET_OFF})

As discussed in Section 2 How to select the right filter time for OFF state diagnostics (tDIAG), the output settling time evaluation plays a key role in the t_{DIAG} selection. It is also clear that t_{SET_OFF} evaluation strongly depends on FET side. Before elaborating the analysis more in detail for each case, a common criterion for settling time estimation can be summarized by the following equation:

Eq: Output settling time estimation for ON to OFF transition: general criterion

$$\begin{cases} t_{SET\_OFF} = t_{FET\_OFF} + t_{CHARGE} & for\ LS \\ t_{SET\_OFF} = t_{FET\_OFF} + t_{DISCHARGE} & for\ HS \end{cases} \quad (2)$$

In Eq. (2), contributions are the following:

- t_{FET_OFF} is the time needed to turn OFF the external FET. In fact, there is a delay between the NONx 0 to 1 transition and the time instant t_{FET_OFF} when the transistor can be considered OFF. Voltage on the output node will be stable to the ON state value until the external FET is turned OFF. Such a delay is due to several contributions:
  - Internal Digital paths: asynchronous digital input synchronization stages and propagation through the disable paths
  - Internal Analog paths: switching time of the output current generators in the pre-driver stage
  - External paths: switching time of the external FET used as power driver

  The sum of internal digital and analog paths represents a negligible aliquot of the final t_{FET_OFF}, due to the high clock frequency (10 MHz typical) and the small capacitance of the internal analog nodes (in the fF/pF order of magnitude). Hence, t_{FET_OFF} can be reasonably approximated with the external path delay, whose entity depends on several application related parameters that will be analyzed in detail case by case.
- t_{CHARGE} is the time needed in a LS configuration to charge the output node from GND up to VOUT_OL. This time depends on the following parameters:
  - Fast charge current I_{FAST_CHG} (refer to Table 11): this current generator works in parallel to the OL regulator diagnostic current I_{DIAG} and it is considerably higher in respect to the latter in order to allow fast V_{out} settling time. Such a generator is activated once the external FET reaches the ON threshold voltage V_{GS_TH} and it's turned OFF when V_{out} reaches the [V_{LVT} ; V_{OL}] range.
  - OL regulator diagnostic current I_{DIAG} (refer to Table 9): the OL regulator is enabled upon digital input NONx 0 to 1 transition and stays ON for the whole PWM OFF time (t_{OFF})
  - Output node capacitance C_{OUT}: usually an ESD capacitor is mounted on the DRNx output pin in order to prevent L9945 and FET damage due to injected charge spikes. Such a component limits the output transition speed

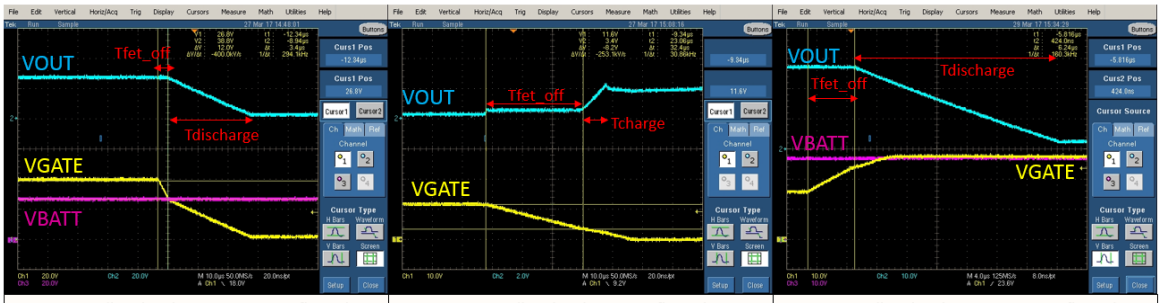
Note: The actual bound for OL detection is represented by the lower bound of the [V_{LVT}; V_{OL}] range. However, a more conservative approach is recommended and therefore V_{OUT_OL} is considered when evaluating the output swing.

- $t_{DISCHARGE}$ is the time needed in a HS configuration to discharge the output node from VBATT down to V_{OUT_OL}. This time depends on the following parameters:
  - Fast discharge current $I_{FAST\_DIS\_N}$/$I_{FAST\_DIS\_P}$ (refer to Table 11): this current generator works in parallel to the OL regulator diagnostic current I_{DIAG} and it is considerably higher in respect to the latter in order to allow fast Vout settling time. Such a generator is activated once the external FET reaches the ON threshold voltage V_{GS_TH} and it's turned OFF when Vout reaches the [V_{LVT}; V_{OL}] range.
  - OL regulator diagnostic current I_{DIAG} (refer to Table 9): the OL regulator is enabled upon digital input NONx 0 to 1 transition and stays ON for the whole PWM OFF time (t_{OFF})
  - Output node capacitance C_{OUT}: usually an ESD capacitor is mounted on the SNGPx/DRNx output pin in order to prevent L9945 and FET damage due to injected charge spikes. Such a component limits the output transition speed

Note: The actual bound for OL detection is represented by the upper bound of the [V_{LVT}; V_{OL}] range. However, a more conservative approach is recommended and therefore V_{OUT_OL} is considered when evaluating the output swing.

The figure below can be considered as a graphical reference for t_{FET_OFF}, t_{CHARGE} and $t_{DISCHARGE}$ individuation during the output transient.

Figure 7. Graphic example of t_{FET_OFF}, t_{CHARGE} and $t_{DISCHARGE}$



Output settling time in a HS NMOS configuration
I GATE = 20 mA

Output settling time in a LS configuration
I GATE = 1 mA

Output settling time in a HS PMOS configuration
I GATE = 1 mA

In general, LS configuration allows much faster settling times in respect to the HS one. This is due to the reduced output swing for the former configuration. In the example shown in Figure 7, a LS configuration with a gate discharge current equal to 1 mA features almost the same settling time of a HS configuration with a gate discharge current programmed to 20 mA. More details about settling time evaluation will be provided in the following paragraphs.

2.1.1 Output settling time for a LS NMOS configuration

The turn OFF phase of a LS NMOS can be divided into **two sub-intervals**, as shown in Figure 7 and Figure 8:

First sub-interval

In the initial phase, both Miller and C_{GS} capacitors are discharged through a constant current I_{OFF}. While V_{GS} is greater than the ON threshold V_{GS_TH}, the drain voltage is almost equal to GND, because the transistor is still turned ON, and the IDIAG won't charge the ESD capacitor on the output. During such an interval, the t_{FET_OFF} mentioned in Eq. (2) can be evaluated considering that C_M and C_{GS} are in parallel.

Eq: t_{FET_OFF} estimation for a LS NMOS configuration

$$I_{OFF} = (C_{GS} + C_M)\frac{\Delta V_{GS}}{\Delta t} \Rightarrow t_{FET\_OFF} = (C_{GS} + C_M)\frac{V_{GS\_ON} - V_{GS\_TH}}{I_{OFF}} \quad (3)$$

Where:

I_{OFF} is the programmed constant gate discharge current, that can be chosen among the values listed in Table 12 (only constant current options are considered);

V_{GS_ON} is the ON gate-to-source voltage, whose range is [10 - 14] V for L9945;

V_{GS_TH} is the external FET ON threshold voltage, whose range is [2.5 - 4.5] V for STD105N10F7AG.

Second sub-interval

Once t_{FET_OFF} has expired, the transistor is turned OFF and I_{FAST_CHG} is activated. Hence, the output node is charged with a total current equal to the sum of I_{DIAG} and I_{FAST_CHG}. Charging phase lasts until V_{out} reaches V_{OUT_OL}. The t_{CHARGE} mentioned in Eq. (2) can be evaluated considering the linear charge of the output ESD capacitor.

Eq: Estimation of t_{CHARGE} in a LS NMOS configuration.

$$I_{DIAG} + I_{FAST\_CHG} = C_{ESD}\frac{\Delta V_{out}}{\Delta t} \Rightarrow t_{CHARGE} = C_{ESD}\frac{V_{OUT\_OL}}{I_{DIAG} + I_{FAST\_CHG}} \quad (4)$$

Where:

I_{DIAG} is the programmed OL regulator current capability (refer to Table 9);

I_{FAST_CHG} is the fast charge current (refer to Table 11);

V_{OUT_OL} is the target voltage for the OL regulator, whose range is [2.25 – 2.75] V for L9945;

C_{ESD} is the external ESD capacitor mounted on the DRNx pin.

Figure 8. LS turn OFF transition

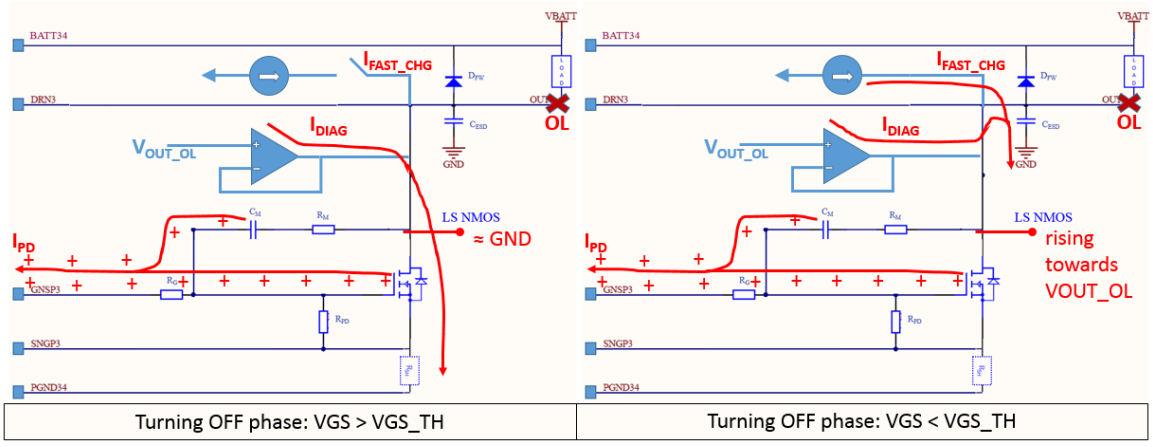


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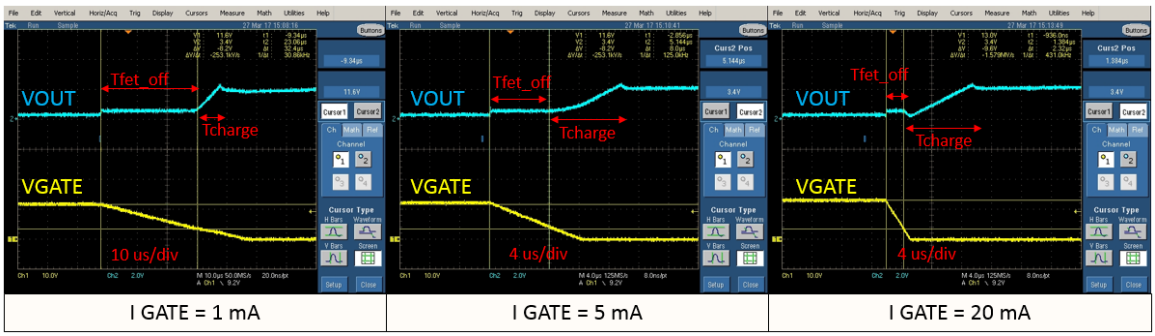
Figure 9. LS output settling time when different gate discharge currents are programmed



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The above figure shows how output settling time varies according to the programmed gate discharge current. Actually, the I_{OFF} acts only on t_{FET_OFF}, while t_{CHARGE} depends on I_{DIAG} and I_{FAST_CHG}. Hence, t_{SET_OFF} is extremely variable among different applications/settings. The final criterion to evaluate the output settling time is described by the following equation:

Eq: Final formula for t_{SET_OFF} estimation in a LS NMOS configuration.

$$t_{SET} = (C_{GS} + C_M)\frac{V_{GS\_ON} - V_{GS\_TH}}{I_{OFF}} + C_{ESD}\frac{V_{OUT\_OL}}{I_{DIAG} + I_{FAST\_CHG}} \quad (5)$$

Because t_{SET_OFF} represents the lower bound in Eq. (1), then its maximum corner must be considered in order to operate a robust choice for t_{DIAG}.

Eq: Corner case for the output settling time estimation in a LS NMOS configuration.

$$t_{SET\_OFF_{max}} = (C_{GSmax} + C_{Mmax})\frac{V_{GS\_ONmax} - V_{GS\_THmin}}{I_{OFFmin}} + C_{ESDmax}\frac{V_{OUT\_OLmax}}{I_{DIAGmin} + I_{FAST\_CHGmin}} \quad (6)$$

Eventually, $t_{SET\_OFF\_MAX}$ might be multiplied by a tolerance margin (1 + TM%) in order to be even more conservative. However, it is not recommend since it might represent an unrealistic constraint. It makes sense using the TM% when evaluating settling time using Eq. (5) and assuming typical values for all involved parameters.

Having evaluated $t_{SET\_OFF\_MAX}$, Eq. (1) states that the safest choice for t_{DIAG} is the nominal value from Table 7, whose minimum corner is still greater than $t_{SET\_OFF\_MAX}$.

Since a very conservative approach has been used when estimating $t_{SET\_OFF\_MAX}$, borderline cases where $t_{SET\_OFF\_MAX}$ is greater than t_{DIAG_min} by a really small amount, might still lead to choose the lower bound for t_{DIAG_min}. In fact, referring to Eq. (6), nine uncorrelated parameters assuming their worst case value is definitely unlikely to occur.

Differently from HS configuration, choosing different values for OL regulator current capability I_{DIAG} can lead to significant variations of $t_{SET\_OFF\_MAX}$. In fact, in Eq. (6) I_{DIAG_MIN} must be compared to $I_{FAST\_CHG\_MIN}$ whose value is only 2.4 mA, due to the reduced output swing. Hence, switching I_{DIAG_MIN} from 60 µA to 600 µA through **diag_i_config_xx** bit might have a visible impact on $t_{SET\_OFF\_MAX}$.

Regarding I_{OFF_MIN}, switching between 1 mA, 5 mA and 20 mA options through the **GCC_CONFIG_xx** bit will have a huge impact on t_{SET_MAX}.

All these elaborations can be verified using the Section 7 L9945 Diagnostic Filter Times calculator.

2.1.2 Output settling time for a HS NMOS configuration

The L9945 IC uses an internal charge pump to efficiently bias HS NMOS transistors and to obtain the same VGS as in LS configuration.

The turn OFF phase of a HS NMOS can be divided into **two sub-intervals**, as shown in Figure 7 and Figure 10:

First sub-interval

In the initial phase, both Miller and C_{GS} capacitors are discharged through a constant current I_{OFF}. While V_{GS} is greater than the ON threshold V_{GS_TH}, the source voltage is almost equal to VBATT, because the transistor is still turned ON, and the I_{DIAG} won't discharge the ESD capacitor on the output. During such an interval, the t_{FET_OFF} mentioned in Eq. (2) can be evaluated considering that C_M and C_{GS} are in parallel.

Eq: t_{FET_OFF} estimation for a HS NMOS configuration.

$$I_{OFF} = \left(C_{GS} + C_M\right)\frac{\Delta V_{GS}}{\Delta t} \Rightarrow t_{FET\_OFF} = \left(C_{GS} + C_M\right)\frac{V_{GS\_ON} - V_{GS\_TH}}{I_{OFF}} \quad (7)$$

Where:

I_{OFF} is the programmed constant gate discharge current, that can be chosen among the values listed in Table 12 (only constant current options are considered);

V_{GS_ON} is the ON gate-to-source voltage, whose range is [10 - 14] V for L9945;

V_{GS_TH} is the external FET ON threshold voltage, whose range is [2.5 - 4.5] V for STD105N10F7AG.

Second sub-interval

Once t_{FET_OFF} has expired, the transistor is turned OFF and $I_{FAST\_DIS\_N}$ is activated. Hence, the output node is discharged with a total current equal to the sum of I_{DIAG} and $I_{FAST\_DIS\_N}$. Discharging phase lasts until V_{out}

reaches V_{OUT_OL}. The $t_{DISCHARGE}$ mentioned in Eq. (2) can be evaluated considering the linear discharge of the output ESD capacitor.

Eq: Estimation of $t_{DISCHARGE}$ in a HS NMOS configuration.

$$I_{DIAG} + I_{FAST\_DIS\_N} = C_{ESD}\frac{\Delta V_{out}}{\Delta t} \Rightarrow t_{DISCHARGE} = C_{ESD}\frac{V_{BATT} - V_{OUT\_OL}}{I_{DIAG} + I_{FAST\_DIS\_N}} \quad (8)$$

Where:

I_{DIAG} is the programmed OL regulator current capability (refer to Table 9);

$I_{FAST\_DIS\_N}$ is the fast discharge current for HS NMOS configuration (refer to Table 11);

V_{OUT_OL} is the target voltage for the OL regulator, whose range is [2.25 – 2.75] V for L9945;

C_{ESD} is the external ESD capacitor mounted on the SNGPx pin;

V_{BATT} is the battery supply voltage.

Figure 10. HS NMOS turn OFF transition

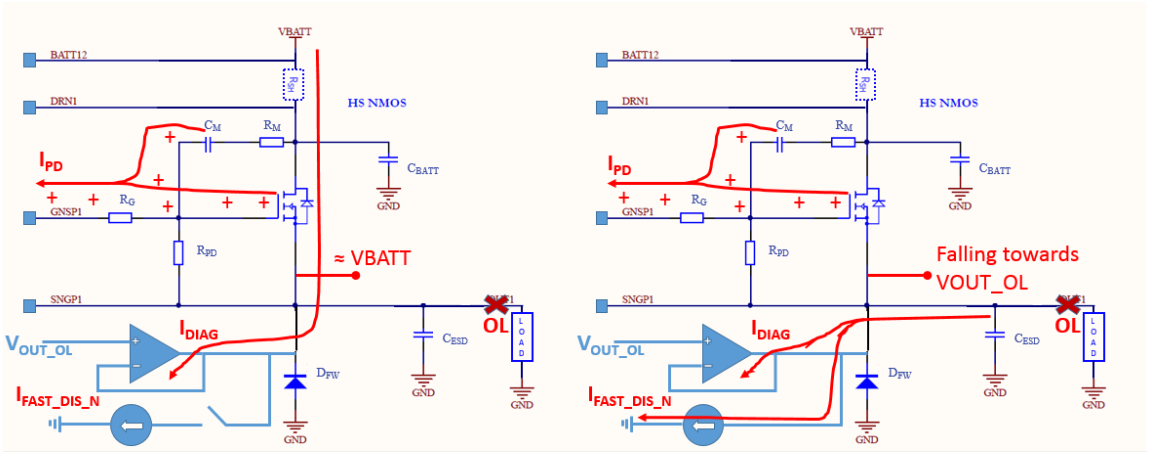

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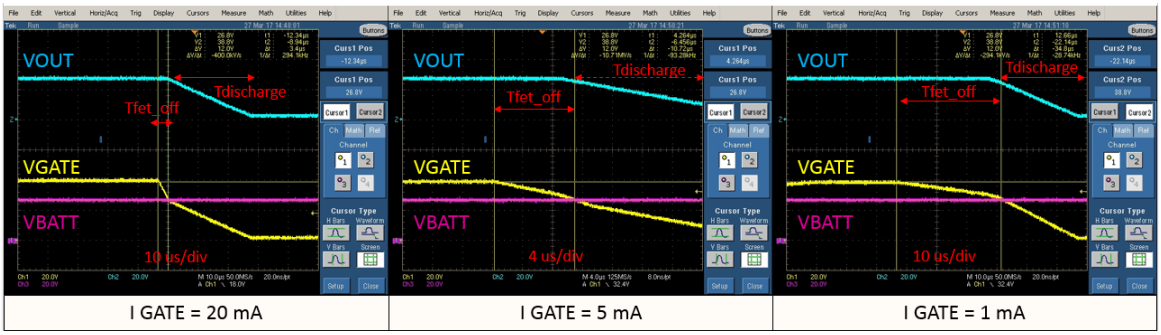
Figure 11. HS output settling time when different gate discharge currents are programmed



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The above figure shows how output settling time varies according to the programmed gate discharge current. Actually, the I_{OFF} acts only on t_{FET_OFF}, while $t_{DISCHARGE}$ depends on I_{DIAG} and $I_{FAST\_DIS\_N}$. Hence, t_{SET_OFF} is extremely variable among different applications/settings. The final criterion to evaluate the output settling time is described by the following equation:

Eq: Final formula for tSET_OFF estimation in a HS NMOS configuration.

$$t_{SET\_OFF} = (C_{GS} + C_M)\frac{V_{GS\_ON} - V_{GS\_TH}}{I_{OFF}} + C_{ESD}\frac{V_{BATT} - V_{OUT\_OL}}{I_{DIAG} + I_{FAST\_DIS\_N}} \quad (9)$$

Because t_{SET_OFF} represents the lower bound in Eq. (1), then its maximum corner must be considered in order to operate a robust choice for t_{DIAG}.

Eq: Corner case for the output settling time estimation in a HS NMOS configuration.

$$t_{SET\_OFFmax} = (C_{GSmax} + C_{Mmax})\frac{V_{GS\_ONmax} - V_{GS\_THmin}}{I_{OFFmin}} + C_{ESDmax}\frac{V_{BATT} - V_{OUT\_OLmin}}{I_{DIAGmin} + I_{FAST\_DIS\_Nmin}} \quad (10)$$

Eventually, $t_{SET\_OFF\_MAX}$ might be multiplied by a tolerance margin (1 + TM%) in order to be even more conservative. However, ST doesn't recommend it since it might represent an unrealistic constraint. It makes sense using the TM% when evaluating settling time using Eq. (9) and assuming typical values for all involved parameters.

It is worth noticing how the settling time in a HS configuration depends on the battery supply voltage. Hence, there is a huge difference between CV and PV applications: in the former, settling times are much higher due to the fact that VBATT is twice the one in the latter.

Having evaluated $t_{SET\_OFF\_MAX}$, Eq. (1) states that the safest choice for t_{DIAG} is the nominal value from Table 7, whose minimum corner is still greater than $t_{SET\_OFF\_MAX}$.

Since a very conservative approach has been used when estimating $t_{SET\_OFF\_MAX}$, borderline cases where $t_{SET\_OFF\_MAX}$ is greater than t_{DIAG}_min by a really small amount, might still lead to choose the lower bound for t_{DIAG}_min. In fact, referring to Eq. (10), nine uncorrelated parameters assuming their worst case value is definitely unlikely to occur.

Differently from LS configuration, choosing different values for OL regulator current capability I_{DIAG} doesn't lead to significant variations of $t_{SET\_OFF\_MAX}$. In fact, in Eq. (10) I_{DIAG_MIN} must be compared to $I_{FAST\_DIS\_N\_MIN}$ whose value is much higher (9 mA), due to the wider output swing. Hence, switching I_{DIAG_MIN} from 60 µA to 600 µA through **diag_i_config_xx** bit might not have a visible impact on $t_{SET\_OFF\_MAX}$.

Regarding I_{OFF_MIN}, switching between 1 mA, 5 mA and 20 mA options through the **GCC_CONFIG_xx** bit will have a huge impact on $t_{SET\_OFF\_MAX}$.

All these elaborations can be verified using the Section 7 L9945 Diagnostic Filter Times calculator.

2.1.3 Output settling time for a HS PMOS configuration

The turn OFF phase of a HS PMOS can be divided into **two sub-intervals**, as shown in Figure 7 and Figure 12:

First sub-interval

In the initial phase, both Miller and CGS capacitors are charged through a constant current I_{PU}. While V_{SG} is greater than the ON threshold V_{SG_TH}, the drain voltage is almost equal to VBATT, because the transistor is still turned ON, and the I_{DIAG} won't discharge the ESD capacitor on the output. During such an interval, the t_{FET_OFF} mentioned in Eq. (2) can be evaluated considering that CM and CGS are in parallel.

Eq: t_{FET_OFF} estimation for a HS PMOS configuration.

$$I_{OFF} = (C_{GS} + C_M)\frac{\Delta V_{SG}}{\Delta t} \quad \Rightarrow \quad t_{FET\_OFF} = (C_{GS} + C_M)\frac{V_{SG\_ON} - V_{SG\_TH}}{I_{OFF}} \quad (11)$$

Where:

I_{OFF} is the programmed constant gate charge current, that can be chosen among the values listed in Table 12 (only constant current options are considered);

V_{SG_ON} is the ON source-to-gate voltage, whose range is [10 - 14] V for L9945;

V_{SG_TH} is the external FET ON threshold voltage, whose range is [2 - 4] V for STD10PF06T4.

Second sub-interval

Once t_{FET_OFF} has expired, the transistor is turned OFF and $I_{FAST\_DIS\_P}$ is activated. Hence, the output node is discharged with a total current equal to the sum of I_{DIAG} and $I_{FAST\_DIS\_P}$. Discharging phase lasts until V_{out} reaches V_{OUT_OL}. The $t_{DISCHARGE}$ mentioned in Eq. (2) can be evaluated considering the linear discharge of the output ESD capacitor.

Eq: Estimation of $t_{DISCHARGE}$ in a HS PMOS configuration.

$$I_{DIAG} + I_{FAST\_DIS\_P} = C_{ESD}\frac{\Delta V_{out}}{\Delta t} \Rightarrow t_{DISCHARGE} = C_{ESD}\frac{V_{BATT} - V_{OUT\_OL}}{I_{DIAG} + I_{FAST\_DIS\_P}} \quad (12)$$

Where:

I_{DIAG} is the programmed OL regulator current capability (refer to Table 9);

$I_{FAST\_DIS\_P}$ is the fast discharge current (refer to Table 11);

V_{OUT_OL} is the target voltage for the OL regulator, whose range is [2.25 – 2.75] V for L9945;

C_{ESD} is the external ESD capacitor mounted on the DRNx pin.

Figure 12. HS PMOS turn OFF transition

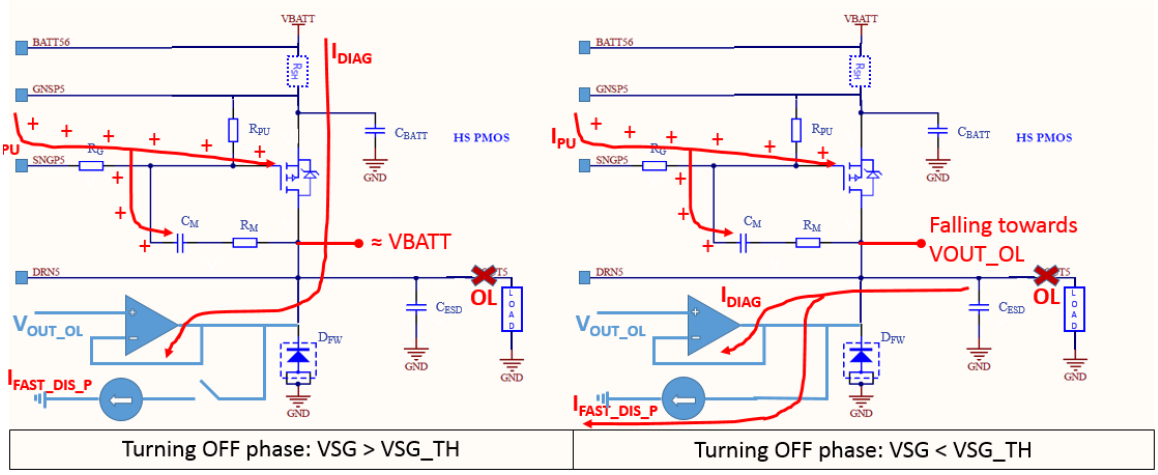

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Figure 13. HS PMOS output settling time when different gate charge currents are programmed

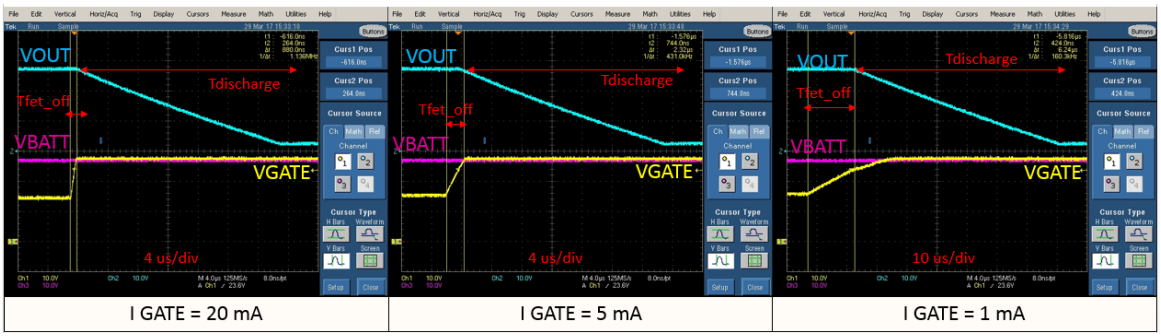


image13.png

The above figure shows how output settling time varies according to the programmed gate charge current. Actually, the I_{OFF} acts only on t_{FET_OFF}, while $t_{DISCHARGE}$ depends on I_{DIAG} and $I_{FAST\_DIS\_P}$. Hence, t_{SET_OFF} is extremely variable among different applications/settings. The final criterion to evaluate the output settling time is described by the following equation:

Eq: Final formula for t_{SET} estimation in a HS PMOS configuration.

$$t_{SET\_OFF} = (C_{GS} + C_M)\frac{V_{SG\_ON} - V_{SG\_TH}}{I_{OFF}} + C_{ESD}\frac{V_{BATT} - V_{OUT\_OL}}{I_{DIAG} + I_{FAST\_DIS\_P}} \quad (13)$$

Because t_{SET_OFF} represents the lower bound in Eq. (1), then its maximum corner must be considered in order to operate a robust choice for t_{DIAG}.

Eq: Corner case for the output settling time estimation in a HS PMOS configuration.

$$t_{SET\_OFF_{max}} = (C_{GSmax} + C_{Mmax})\frac{V_{SG\_ON_{max}} - V_{SG\_TH_{min}}}{I_{OFF_{min}}} + C_{ESDmax}\frac{V_{BATT} - V_{OUT\_OL_{min}}}{I_{DIAG_{min}} + I_{FAST\_DIS\_P_{min}}} \quad (14)$$

Eventually, $t_{SET\_OFF\_MAX}$ might be multiplied by a tolerance margin (1 + TM%) in order to be even more conservative. However, ST doesn't recommend it since it might represent an unrealistic constraint. It makes sense using the TM% when evaluating settling time using Eq. (13) and assuming typical values for all involved parameters.

It is worth noticing how the settling time in a HS configuration depends on the battery supply voltage. Hence, there is a huge difference between CV and PV applications: in the former, settling times are much higher due to the fact that VBATT is twice the one in the latter.

Having evaluated $t_{SET\_OFF\_MAX}$, Eq. (1) states that the safest choice for t_{DIAG} is the nominal value from Table 7, whose minimum corner is still greater than $t_{SET\_OFF\_MAX}$.

Since a very conservative approach has been used when estimating $t_{SET\_OFF\_MAX}$, borderline cases where $t_{SET\_OFF\_MAX}$ is greater than t_{DIAG}_min by a really small amount, might still lead to choose the lower bound for t_{DIAG}_min. In fact, referring to Eq. (14), nine uncorrelated parameters assuming their worst case value is definitely unlikely to occur.

Differently from LS configuration, choosing different values for OL regulator current capability I_{DIAG} doesn't lead to significant variations of $t_{SET\_OFF\_MAX}$. In fact, in Eq. (14) I_{DIAG_MIN} must be compared to $I_{FAST\_DIS\_P\_MIN}$ whose value is much higher (8 mA), due to the wider output swing. Hence, switching I_{DIAG_MIN} from 60 µA to 600 µA through **diag_i_config_xx** bit might not have a visible impact on $t_{SET\_OFF\_MAX}$.

Regarding I_{OFF_MIN}, switching between 1 mA, 5 mA and 20 mA options through the **GCC_CONFIG_xx** bit will have a huge impact on $t_{SET\_OFF\_MAX}$.

All these elaborations can be verified using the Section 7 L9945 Diagnostic Filter Times calculator.

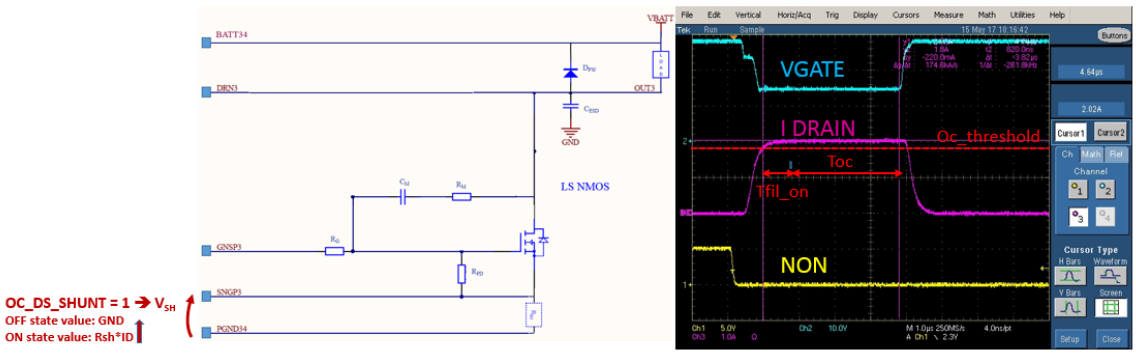
3 How to select the right filter time for ON state diagnostics (t_{BLANK_OC})

Two key aspects must be accounted for a robust fault detection while in ON state. Considering a PWM signal controlling a generic output channel, the following points must be verified:

- The t_{BLANK_OC} filter must be smaller than the PWM ON time t_{ON}. In fact, if channel is switched OFF before t_{BLANK_OC} has expired, the ON diagnostics are not performed at all. The diagnostic latches will hold the last value determined from OFF state diagnostics. Refer to Figure 16 as an example of missed OC failure. In the example, DSM is used as OC detection method. The external FET VDS is consistently above the OC threshold during the ON time, but the output is switched OFF before t_{BLANK_OC} expires. As a consequence, **"No OL/STG/STB" (110)** is reported instead of the expected "OC failure" (001). The diagnostic code reported refers in fact to the last valid entry latched during OFF state.

  As a consequence, a corner value for PWM t_{ON} is represented by the smallest programmable t_{BLANK_OC}, corresponding to 11 µs (consider a 20% additional margin for a robust behavior). A control signal with a t_{ON} below this threshold may be correctly processed by L9945, but ON diagnostics are not guaranteed and the external microcontroller must take care of catching eventual OC faults
- The t_{BLANK_OC} filter must be higher than the V_{sense} settling time t_{SET_ON}. If this constraint is not verified, wrong diagnostics will be reported. V_{sense} depends on the OC detection strategy chosen by programming the **OC_DS_SHUNT_xx** bit. A huge difference occurs between DSM and Rshunt methods (refer to Figure 14 and Figure 15. OC sensing using DSM method):
  - In case R_{shunt} method is selected, the Vsense behavior during the OFF to ON transition corresponds to an ascending transient. Hence, in case output current crosses the OC threshold with a positive slope, an actual OC event is really likely to be ongoing. In this case, t_{BLANK_OC} is almost meaningless from a diagnostics point of view. The OC detection will be mainly based on t_{FIL_ON} and t_{OC} parameters (see Table 3). The former is a deglitch filter to avoid small overshoots on the shunt resistor due to inductive effects, while the latter represents the actual OC blanking time. Summarizing, an OC event lasting t_{FIL_ON}+t_{OC} will be detected and the output switched OFF: the programmed t_{BLANK_OC} will have no effect on the OC reaction time, but it only causes the assertion of the "No OC failure" latch once it expires. Only in case Peak & Hold configuration is selected and the OC event occurs while t_{BLANK_OC} is still running, an **"OC pin failure" (000)** will be reported instead of simple "OC failure" (001). However, reaction time won't be affected.

Figure 14. OC sensing using Rshunt method



Pins used to measure Vsense **Example of transient**

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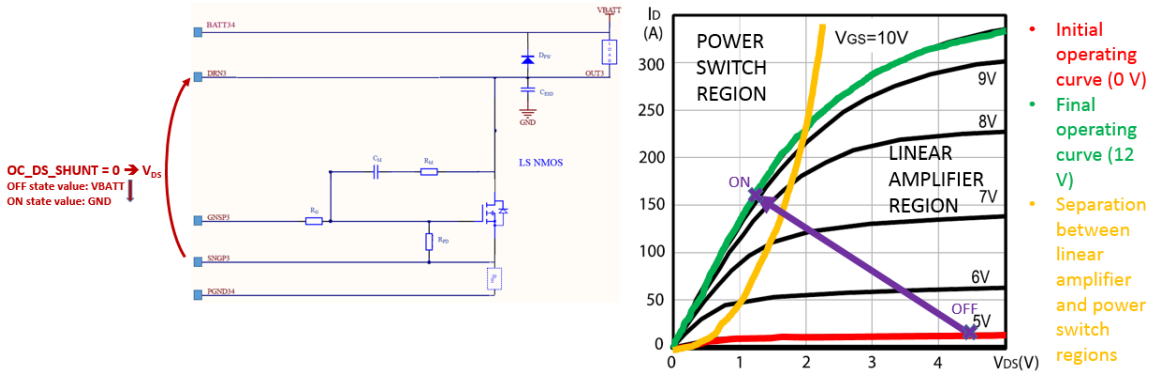
  - In case DSM method is selected, the V_{sense} behavior during the OFF to ON transition corresponds to a descending transient, whose slope depends on the programmed gate charge/discharge current (GCC_CONFIG_xx). Hence, in case t_{BLANK_OC} is smaller than the Vsense settling time, a false OC detection will occur. Referring to Figure 16, the sampled VDS is still higher than the OC threshold when t_{BLANK_OC} expires, resulting in a wrong OC detection that causes the output to be immediately shut OFF. In order to ensure maximum FET protection against critical OC events during blanking time, an OC threshold crossing with a positive slope will stop the t_{BLANK_OC} and engage the t_{OC} filter.

Figure 15. OC sensing using DSM method



Pins used to measure Vsense

Example of transient in DSM

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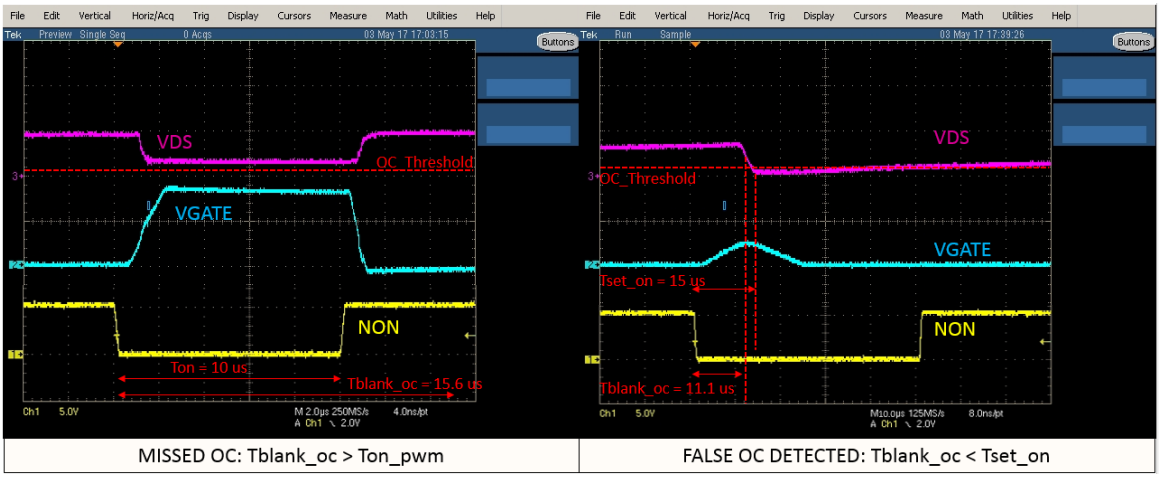
- As a consequence, t_{SET_ON} evaluation represents a critical aspect for a correct t_{BLANK_OC} selection. The t_{SET_ON} is strongly dependent on the programmed gate charge current and the chosen external components.

Figure 16. Example of wrong ON state diagnostics



MISSED OC: Tblank_oc > Ton_pwm

FALSE OC DETECTED: Tblank_oc < Tset_on

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The figure above shows:

- left side: the programmed t_{BLANK_ON} is greater than the PWM t_{ON}, resulting in a missed OC detection;
- right side: the programmed t_{BLANK_ON} is smaller than the output settling time, resulting in a false OC detection.

Summarizing the first part of our analysis, the criterion to ensure robust ON state diagnostics is described by the following equation:

Eq: General criterion for choosing the correct filter time for ON state diagnostics

$$t_{SET\_ONmax} < t_{BLANK\_OCmin} < t_{ONmin} \quad (15)$$

Where:

- t_{ONmin} depends on the PWM control signal and its minimum value must be considered
- t_{SET_ONmax} is the output settling time in case DSM method is selected for OC detection (worst case for settling time) and its maximum value must be considered
- t_{BLANK_OCmin} is the ON state diagnostic filter whose minimum corner is still greater than the worst output settling time (see Table 2)

Because t_{ON} is a PWM related parameter, it is supposed to vary along with the duty-cycle. Hence, a key point in order to allow smaller values for t_{ON} without compromising diagnostics is to minimize the output settling time t_{SET_ON}. In fact, the smaller the t_{SET_ON}, the lower the t_{BLANK_OC} and the wider the t_{ON} range, as stated by Eq. (15).

3.1 Evaluation of the output settling time (t_{SET_ON})

As discussed in Section 3 How to select the right filter time for ON state diagnostics (tBLANK_OC), the output settling time evaluation plays a key role in the t_{BLANK_OC} selection when DSM is used. Unlike the ON to OFF transition, where the t_{SET_OFF} varies according to FET side and type, the OFF to ON transition features the same VDS transient in all three different configurations, as shown in Figure 17. A common criterion for settling time estimation can be summarized by the following equation:

Eq: Output settling time estimation for OFF to ON transition: general criterion

$$t_{SET\_ON} = t_{FET\_ON} + t_{VDS\_STABLE} \quad (16)$$

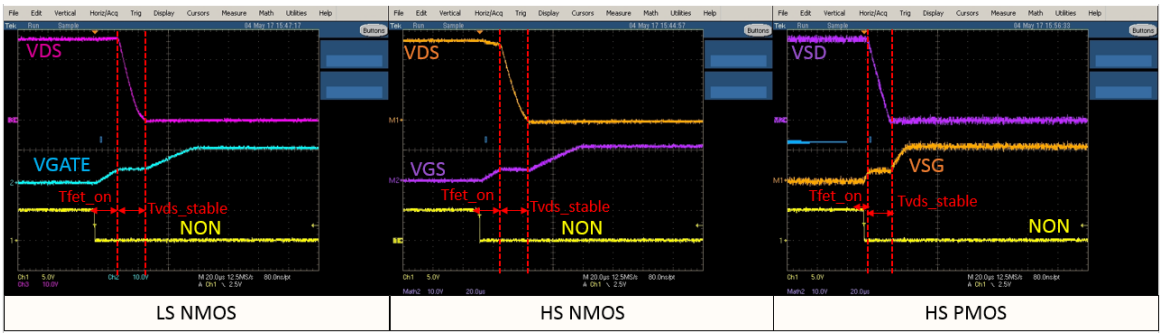
In Eq. (16), contributions are the following:

- t_{FET_ON} is the time needed to turn ON the external FET. In fact, there is a delay between the NONx 1 to 0 transition and the time instant t_{FET_ON} when the transistor can be considered ON. The FET VDS will be stable to the OFF state value until the external FET is turned ON. Such a delay is due to several contributions:
  - Internal Digital paths: asynchronous digital input synchronization stages and propagation through the disable paths
  - Internal Analog paths: switching time of the output current generators in the pre-driver stage
  - External paths: switching time of the external FET used as power driver

  The sum of internal digital and analog paths represents a negligible aliquot of the final t_{FET_ON}, due to the high clock frequency (10 MHz typical) and the small capacitance of the internal analog nodes (in the fF/pF order of magnitude). Hence, t_{FET_ON} can be reasonably approximated with the external path delay, whose entity depends on the following parameters:
  - Programmed gate charge current
  - External FET gate capacitance
- t_{VDS_STABLE} is the time needed for the VDS to switch from the OFF state value (usually VBATT) to the final value, which is usually very close to 0 V, since the external POWER MOS features a very low on-resistance. This time depends on the following parameters:
  - Programmed gate charge current
  - Miller capacitance (usually only the external discrete component is considered, while the FET internal C_{GD} is neglected because much smaller)

The figure below can be considered as a graphical reference for t_{FET_ON}, and t_{VDS_STABLE} individuation during the output transient. Observing the plots, it is evident that the external FET can be considered ON when the VGS plateau begins. The VDS will then be discharged.

Figure 17. VDS transients during the OFF to ON switch



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3.1.1 Output settling time for all configurations

Figure 18 and Figure 19 describe in detail the OFF to ON transition. They can be used to understand how the t_{FET_ON} and t_{VDS_STABLE} time intervals can be estimated.

Figure 18. VGS transient during transistor OFF to ON switching

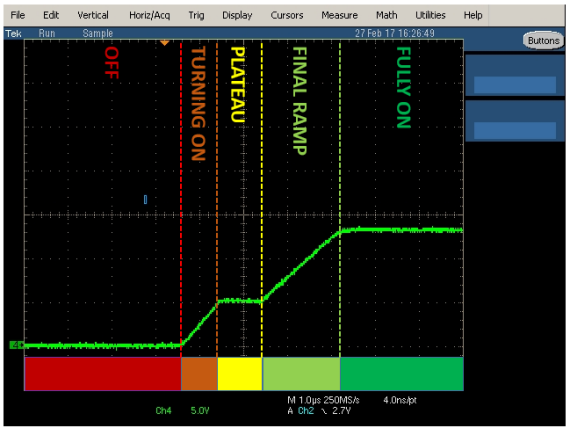

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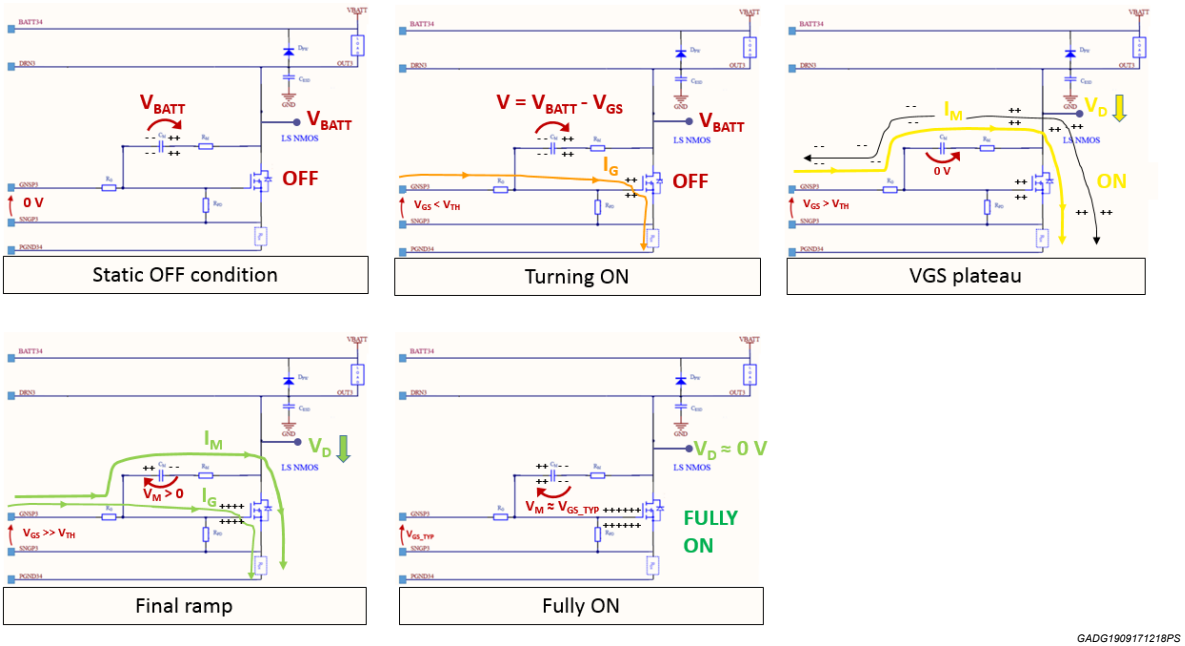
Figure 19. Step by step description of the OFF to ON transition



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The turn ON phase of an NMOS can be divided into two sub-intervals:

- In the initial phase, the C_{GS} capacitor is charged through a constant current I_{ON}. While V_{GS} is lower than the ON threshold V_{GS_TH}, the drain voltage is still constant and equal to VBATT (OFF state value), because the transistor is still OFF. During such an interval, the t_{FET_ON} mentioned in Eq. (16) can be evaluated considering the linear charge of the C_{GS}:

  Eq: t_{FET_ON} estimation for an NMOS configuration

$$I_{ON} = C_{GS}\frac{\Delta V_{GS}}{\Delta t} \Rightarrow t_{FET\_ON} = C_{GS}\frac{V_{GS\_TH}}{I_{ON}} \quad (17)$$

Where:

– I_{ON} is the programmed constant gate charge current, that can be chosen among the values listed in Table 5 (only constant current options are considered)

– V_{GS_TH} is the external FET ON threshold voltage, whose range is [2.5 - 4.5] V for STD105N10F7AG

- Once t_{FET_ON} has expired, the transistor is turned ON and the VGS plateau occurs. During such a phase, the charge current flows only through the external Miller capacitance CM mounted between drain and gate. The VDS undergoes a linear discharge with a constant current equal to I_{ON}. At the end of the transient, VDS will be close to 0 V, due to the very small on-resistance of the POWER MOS. The t_{VDS_STABLE} mentioned in Eq. (16) can be evaluated as follows:

Eq: Estimation of t_{VDS_STABLE} in an NMOS configuration.

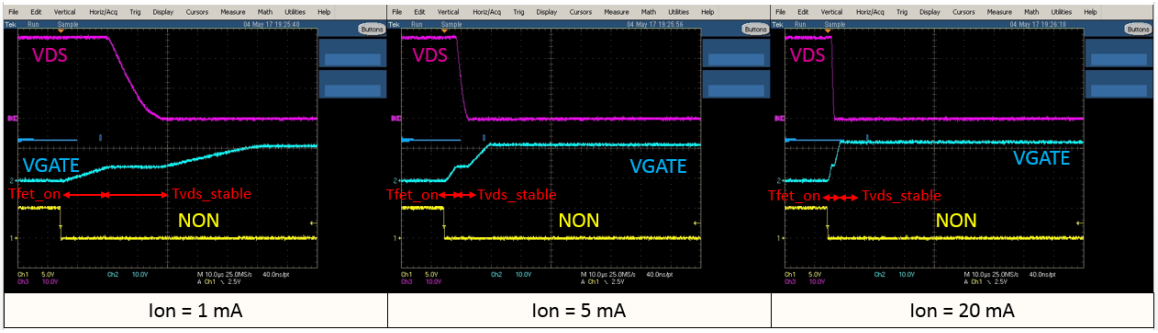
$$\begin{cases} \left.\frac{dV_{DS}}{dt}\right|_{V_{GS}plateau} = \left.\frac{d(V_{GS}+V_{DG})}{dt}\right|_{V_{GS}plateau} = \frac{dV_{DG}}{dt} \\ I_{ON} = C_M\frac{\Delta V_{DS}}{\Delta t} \Rightarrow t_{VDS\_STABLE} = C_M\frac{V_{BATT}}{I_{ON}} \end{cases} \quad (18)$$

Where:

– I_{ON} is the programmed constant gate charge current, that can be chosen among the values listed in Table 5 (only constant current options are considered)

– V_{BATT} is the battery supply voltage

Figure 20. Output settling time when different gate charge currents are programmed



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The above figure shows how output settling time varies according to the programmed gate discharge current. The I_{ON} acts on both t_{FET_ON}, and t_{VDS_STABLE}. Hence, t_{SET_ON} is extremely variable among different applications/ settings. The final criterion to evaluate the output settling time is described by the following equation:

Eq: Final formula for t_{SET_ON} estimation:

$$t_{SET\_ON} = \frac{1}{I_{ON}}\left(C_{GS}V_{GS\_TH} + C_M V_{BATT}\right) \quad (19)$$

Because t_{SET_ON} represents the lower bound in Eq. (15), then its maximum corner must be considered in order to operate a robust choice for t_{BLANK_OC}.

Eq: Corner case for the output settling time estimation

$$t_{SET\_ONmax} = \frac{1}{I_{ONmin}}\left(C_{GSmax}V_{GS\_THmax} + C_{Mmax}V_{BATTmax}\right) \quad (20)$$

Note: All the calculations made for NMOS are also valid in case of PMOS, provided that V_{SD} and V_{SG} are considered.

Eventually, $t_{SET\_ON\_MAX}$ might be multiplied by a tolerance margin (1 + TM%) in order to be even more conservative. However, ST doesn't recommend it since it might represent an unrealistic constraint. It makes sense using the TM% when evaluating settling time using Eq. (19) and assuming typical values for all involved parameters.

Having evaluated $t_{SET\_ON\_MAX}$, Eq. (15) states that the safest choice for t_{BLANK_OC} is the nominal value from Table 2, whose minimum corner is still greater than $t_{SET\_ON\_MAX}$.

Since a very conservative approach has been used when estimating $t_{SET\_ON\_MAX}$, borderline cases where $t_{SET\_ON\_MAX}$ is greater than $t_{BLANK\_OC\_min}$ by a really small amount, might still lead to choose the lower bound for $t_{BLANK\_OC\_min}$. In fact, referring to Eq. (20), five uncorrelated parameters assuming their worst case value is definitely unlikely to occur.

It is worth noticing how the settling time depends on the battery supply voltage. Hence, there is a huge difference between CV and PV applications: in the former, settling times are much higher due to the fact that VBATT is twice the one in the latter.

Regarding ION_MIN, switching between 1 mA, 5 mA and 20 mA options through the **GCC_CONFIG_xx** bit will have a huge impact on $t_{SET\_ON\_MAX}$.

All these elaborations can be verified using the Section 7 L9945 Diagnostic Filter Times calculator.

4 Understanding Open Load Detection

As discussed in OFF state diagnostics, each output channel features an independent voltage regulator with a limited current capability I_{DIAG}, programmable via SPI bit **DIAG_I_CONFIG_XX**. Such a regulator is active during the channel OFF state and performs OL detection, which occurs when the output node V_{out} is regulated around V_{OUT_OL}.

4.1 Tracking thresholds

Both OL and STG/STB detections are based on the output voltage V_{out} sensing. In particular, Table 6 defines the conditions that lead to fault detection while in OFF state. In order to avoid thresholds overlapping each other, causing wrong diagnostics (OL detected instead of STG/STB and vice versa), a tracking design technique has been adopted.

The table below shows a comparison between the fault thresholds (V_{OL} and V_{LVT}) and the open load regulator output target. The former has been designed in tracking, so that they both spread in the same direction according to the process tolerance. In other words, when V_{OL} shows its maximum corner, V_{LVT} is also equal to its upper bound (and vice versa).

Table 13. Comparison between fault thresholds and Open Load regulator output target

Parameter	Min.	Max.	Unit
VOL	2.8	3.4	V
VOUT_OL	2.25	2.75	V
VLVT	1.9	2.3	V

The V_{OUT_OL} is designed according to the following formula:

Eq:

$$t_{SET\_ON} = \frac{1}{I_{ON}}\left(C_{GS}V_{GS\_TH} + C_M V_{BATT}\right) \quad (21)$$

Hence, the fact that V_{OL} and V_{LVT} follow each other guarantees V_{OUT_OL} being always positioned in the middle of the [V_{OL}; V_{LVT}] range. For instance, the case where V_{LVT} = 2.3 V and V_{OUT_OL} = 2.25 V is impossible.

4.2 Minimum Load Resistance (R_{L_OPEN}) for Open Load Detection

In order for a load to be considered “Open”, its resistance must be higher than a threshold value R_{L_OPEN}. Such a value depends on FET side and selected OL regulator current capability I_{DIAG}. The latter has been designed in order to guarantee a good trade-off between having fast output settling time (see Section 2 How to select the right filter time for OFF state diagnostics (tDIAG)) and keeping an acceptable V_{out} ripple in case of open load.

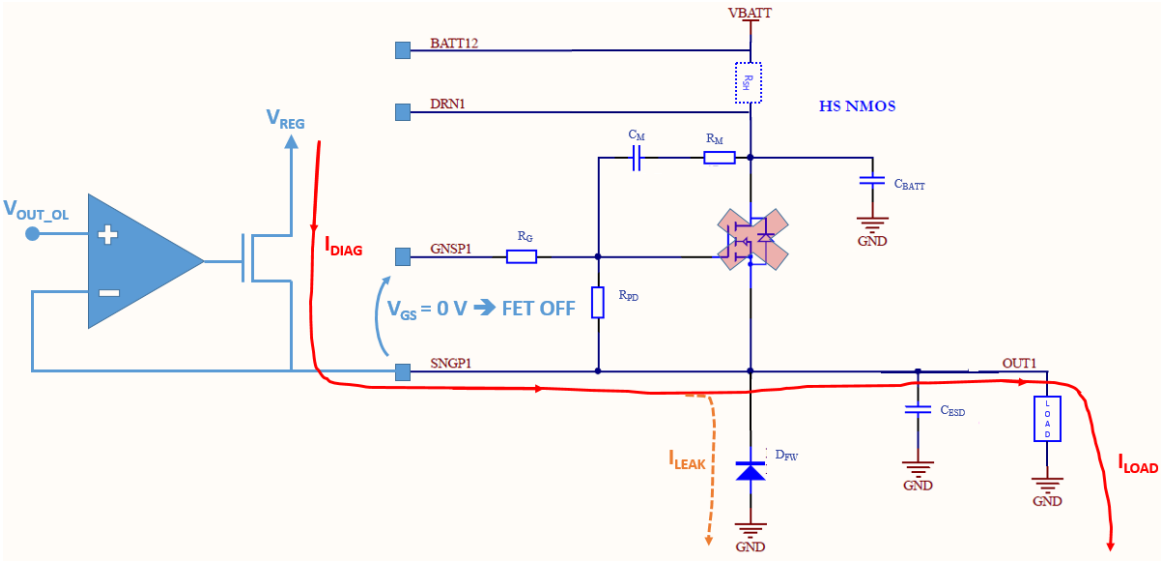
Moreover, an I_{DIAG} too high may alter the load behavior causing unwanted actuations while in the OFF state. Refer to Table 9 for the available I_{DIAG} values.

The open load detection occurs when V_{out} is in the [V_{LVT}; V_{OL}] range. Detailed description of the fault conditions is available in Table 6.

4.2.1 R_{L_OPEN} evaluation for HS configuration

In a High-Side configuration, I_{DIAG} flows through the load following the path described in the figure below. Apart from a small leakage aliquot due to external components, it can be stated that $I_{DIAG} \approx I_{LOAD}$. In case this is not verified, the stronger I_{DIAG} must be programmed to compensate for I_{LEAK}.

Figure 21. Open Load diagnostic current flowing through the RLOAD in HS configuration



The Vout in steady state can be calculated according to the following equation.

Eq:

$$V_{out} = R_{LOAD}{}^{*}I_{DIAG} \tag{22}$$

Referring to Table 6, the turning point between OL and No OL is represented by the condition $V_{out} = V_{LVT}$:

Eq:

$$V_{out} = V_{LVT} \Rightarrow R_{L\_OPEN} = \frac{V_{LVT}}{I_{DIAG}} \tag{23}$$

Values of load resistance smaller than R_{L_OPEN} will cause No OL detection, because the OL regulator current capability is not sufficient to bring the output voltage above the V_{LVT} threshold by increasing the drop on RL. On the other hand, values of load resistance greater than R_{L_OPEN} will cause OL detection, because the OL regulator is able to control the current in the [0 ; IDIAG] range in order to force $V_{out} = V_{OUT\_OL}$.

Taking in account the process spread (refer to Table 8 and Table 9), the following corners can be evaluated for R_{L_OPEN}:

Eq:

$$\begin{cases} R_{L\_OPENmin} = \frac{V_{LVTmin}}{I_{DIAGmax}} \\ R_{L\_OPENmax} = \frac{V_{LVTmax}}{I_{DIAGmin}} \end{cases} \tag{24}$$

Corners will change according to the programmed OL regulator current capability IDIAG. They're summarized in the following table:

Table 14. Minimum load resistance for open load detection RL_OPEN: corner cases

Parameter	Weak I_{DIAG} (100 µA)	Strong I_{DIAG} (1 mA)	Unit
$R_{L\_OPEN\_MIN}$	19	1.9	kΩ
$R_{L\_OPEN\_MAX}$	38.3	3.83	kΩ

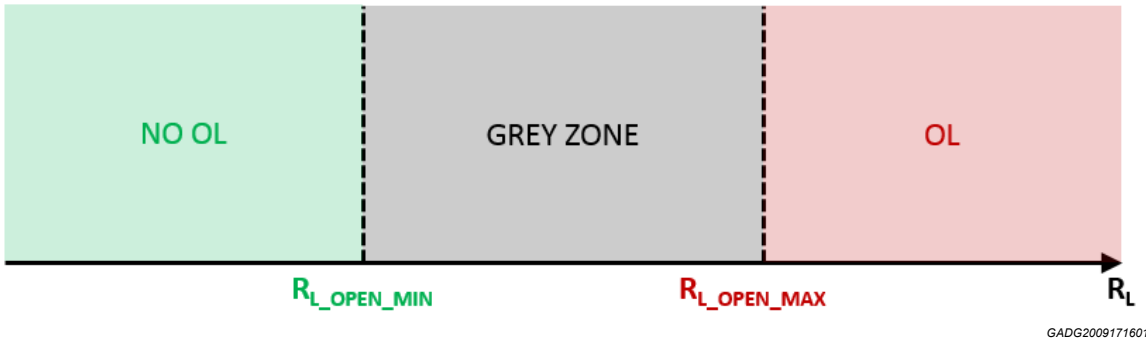
Concluding the analysis for the HS configuration:

- Values of $R_{LOAD} < R_{L\_OPEN\_MIN}$ will never flag OL
- Values of $R_{LOAD} > R_{L\_OPEN\_MAX}$ will certainly flag OL

The [$R_{L\_OPEN\_MIN}$; $R_{L\_OPEN\_MAX}$] represents a grey zone for OL detection due to process spread

Note: The analysis applies to both NMOS and PMOS FET types.

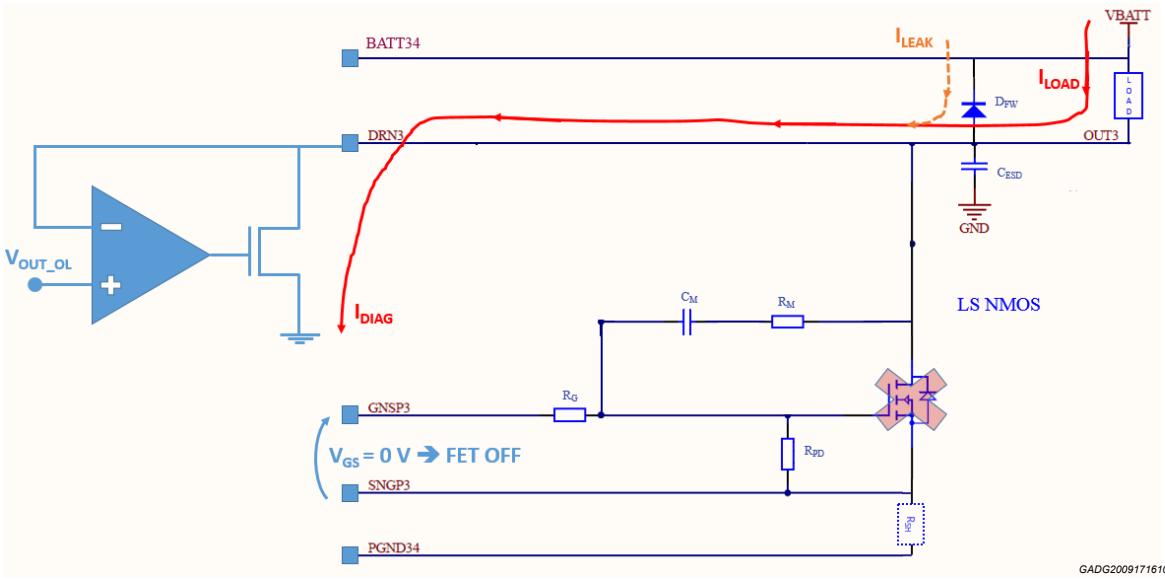
Figure 22. Summarizing critical values of load resistance for OL detection in HS configuration



4.2.2 R_{L_OPEN} evaluation for LS configuration

In a Low-Side configuration, I_{DIAG} flows through the load following the path described in the figure below. Apart from a small leakage aliquot due to external components, it can be stated that $I_{DIAG} \approx I_{LOAD}$. In case this is not verified, the stronger I_{DIAG} must be programmed to compensate for I_{LEAK}.

Figure 23. Open Load diagnostic current flowing through the RLOAD in LS configuration



The V_{out} in steady state can be calculated according to the following equation.

Eq:

$$V_{out} = V_{BATT} - R_{LOAD} * I_{DIAG} \quad (25)$$

Referring to Table 6, the turning point between OL and No OL is represented by the condition $V_{out} = V_{OL}$.

Eq:

$$V_{out} = V_{OL} \Rightarrow R_{L\_OPEN} = \frac{V_{BATT} - V_{OL}}{I_{DIAG}} \quad (26)$$

Values of load resistance smaller than R_{L_OPEN} will cause No OL detection, because the OL regulator current capability is not sufficient to bring the output voltage below the VOL threshold by increasing the drop on RL. On the other hand, values of load resistance greater than R_{L_OPEN} will cause OL detection, because the OL regulator is able to control the current in the [0 ; I_{DIAG}] range in order to force $V_{out} = V_{OUT\_OL}$.

Taking in account the process spread (refer to Table 8 and Table 9), the following corners can be evaluated for R_{L_OPEN}.

Eq:

$$\begin{cases} R_{L\_OPEN_{min}} = \dfrac{V_{BATT} - V_{OLmax}}{I_{DIAGmax}} \\ R_{L\_OPEN_{max}} = \dfrac{V_{BATT} - V_{OLmin}}{I_{DIAGmin}} \end{cases} \quad (27)$$

Differently from the HS configuration, the LS case introduces the dependency on the supply voltage. Corners will change according to the programmed OL regulator current capability I_{DIAG} and the V_{BATT}. Because V_{BATT} is not constant in a real scenario, the [$R_{L\_OPEN\_MIN}$; $R_{L\_OPEN\_MAX}$] is a dynamic range. Values for the most common applications are summarized in the following table:

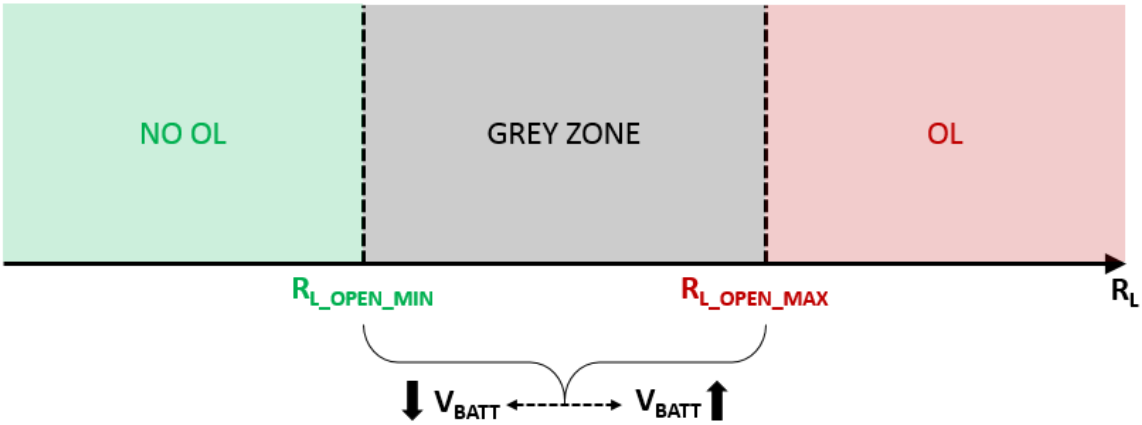
Table 15. Minimum load resistance for open load detection RL_OPEN: corner cases

Supply Voltage [V]	Parameter	Weak IDIAG (100 µA)	Strong IDIAG (1 mA)	Unit
Cranking (6 V)	$R_{L\_OPEN\_MIN}$	26	2.6	kΩ
	$R_{L\_OPEN\_MAX}$	53.3	5.3	kΩ
PV nominal (12 V)	$R_{L\_OPEN\_MIN}$	86	8.6	kΩ
	$R_{L\_OPEN\_MAX}$	153.3	15.3	kΩ
PV typical (14 V)	$R_{L\_OPEN\_MIN}$	106	10.6	kΩ
	$R_{L\_OPEN\_MAX}$	186.7	18.7	kΩ
PV max (18 V)	$R_{L\_OPEN\_MIN}$	146	14.6	kΩ
	$R_{L\_OPEN\_MAX}$	253.3	25.3	kΩ
CV nominal (24 V)	$R_{L\_OPEN\_MIN}$	206	20.6	kΩ
	$R_{L\_OPEN\_MAX}$	353.3	35.3	kΩ
CV typical (28 V)	$R_{L\_OPEN\_MIN}$	246	24.6	kΩ
	$R_{L\_OPEN\_MAX}$	420	42	kΩ
CV max (36 V)	$R_{L\_OPEN\_MIN}$	326	32.6	kΩ
	$R_{L\_OPEN\_MAX}$	553.3	55.3	kΩ
Load Dump (58 V)	$R_{L\_OPEN\_MIN}$	546	54.6	kΩ
	$R_{L\_OPEN\_MAX}$	920	92	kΩ

Concluding the analysis for the LS configuration:

- Values of $R_{LOAD} < R_{L\_OPEN\_MIN}$ will never flag OL
- Values of $R_{LOAD} > R_{L\_OPEN\_MAX}$ will certainly flag OL
- The [$R_{L\_OPEN\_MIN}$; $R_{L\_OPEN\_MAX}$] represents a grey zone for OL detection due to process spread. Moreover, such a range is dynamic and depends on the operating supply voltage

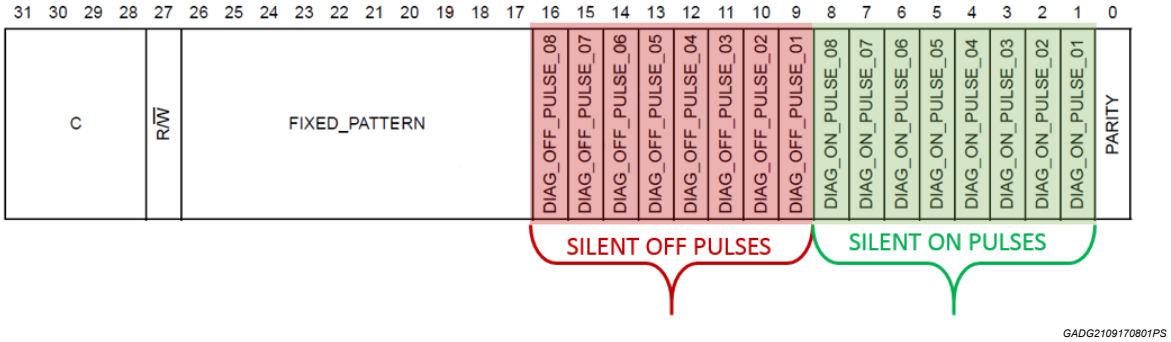
Figure 24. Summarizing critical values of load resistance for OL detection in LS configuration



5 Diagnostic pulses

Diagnostic pulses are intended to be used for static loads, that is, external FETs that are permanently ON or OFF. Because diagnostics depend on the output state, L9945 offers the possibility to temporarily switch the channel in order to perform diagnostic tests without disturbing the normal operation of the load. Diagnostic pulses can also be used when the PWM frequency and duty cycle don't allow to perform valid ON/OFF diagnostics. The microcontroller may decide to interrupt the switching activity once in a while with a diagnostic pulse in order to perform diagnostics. Both ON and OFF silent pulses can be sent through **COMMAND 9**.

Figure 25. Silent diagnostic pulses can be executed independently on each channel by sending COMMAND 9



In case both **DIAG_OFF_PULSE_xx** and **DIAG_ON_PULSE_xx** are set in the same command frame, the output reaction depends on current state:

- If the channel was being kept OFF, an ON pulse will be executed
- If the channel was being kept ON, an OFF pulse will be executed

Diagnostic pulses are not available for H-Bridge configuration. The IC will ignore any pulse request.

5.1 ON Pulses

ON pulses are meant to perform a “try and catch” operation on a channel that is being permanently kept OFF or turned ON for a very short time interval, not sufficient to perform ON state diagnostics. They can be used to temporarily switch ON the channel and verify that no overcurrent event occurs. Diagnostic FSM will always follow the priority codes listed in Table 1:

- In case **“No OL/STG/STB failure” (110)** was latched during OFF state, the channel will be turned ON and:
  - In case no overcurrent occurs, the **“No failure” (100)** code will be reported
  - In case of OC, the **“OC failure” (001)** code will be reported
- In case a failure was latched during OFF state (e.g. “OL failure” (011))
  - In case no overcurrent occurs, the failure code latched during the OFF state will be reported because it still has higher priority
  - In case of OC, the **“OC failure” (001)** code will overwrite the previous fault code because the new failure has higher priority

Note: In order to be sure of reading the actual ON state failure code, reset the FSM by reading the diagnostics through COMMAND 9 before executing the ON pulse.

The ON pulse duration is fixed and falls in the [80-120] µs range. It has been designed according to the trade-off between leaving the load operation unaltered and meeting the VDS settling time in case of DSM (as discussed in Section 3 How to select the right filter time for ON state diagnostics (tBLANK_OC)). When DSM is selected as OC detection strategy, overcurrent diagnostics are performed only if the blanking time is smaller than the ON pulse duration. Therefore, ON pulses will be effective only if used on channels whose blanking time has been set to t_{BLANK_OC} < 80 µs. In case this condition is not met, the diagnostic code reported will be the one latched during OFF state.

Note: OC events can be predicted while in OFF state by seeking for STB/STG failure. In case of such failures, switching the output ON will most likely result in an OC event.

5.2 OFF Pulses

OFF pulses are meant to perform a “try and catch” operation on a channel that is being permanently kept ON or turned OFF for a very short time interval, not sufficient to perform OFF state diagnostics. They can be used to temporarily switch OFF the channel and verify that no OL/STG/STB event occurs. Diagnostic FSM will always follow the priority codes listed in Table 1:

- In case **“No OC failure” (101)** was latched during ON state, the channel will be turned OFF and:
  - In case no OL/STG/STB occurs, the **“No failure” (100)** code will be reported
  - In case of OL/STG/STB, the corresponding fault code will be reported (e.g. “OL failure” (011))
- In case **“OC failure” (011)** was latched during ON state, its fault code will still be reported, independently of the OFF state diagnostics. This happens because OC events have a higher priority.

Note: In order to be sure of reading the actual OFF state failure code, reset the FSM by reading the diagnostics through COMMAND 9 before executing the OFF pulse.

The OFF pulse duration is fixed and falls in the [100-150] µs range. It has been designed according to the trade-off between leaving the load operation unaltered and meeting the V_{out} settling time (as discussed in Section 3 How to select the right filter time for ON state diagnostics (tBLANK_OC)). OFF state diagnostics are performed only if the t_{DIAG} is smaller than the OFF pulse duration. Therefore, OFF pulses will be effective only if used on channels whose t_{DIAG} < 100 µs. In case this condition is not met, the diagnostic code reported will be the one latched during ON state.

Note: STG/STB events can be predicted while in ON state because they’re responsible for overcurrent failures. In case OC is detected during ON state, switching the output OFF will most likely result in an STG/STB event. On the other hand, OL failure cannot be easily detected by L9945 while in ON state, because the output current drops down to zero, thus causing no overcurrent. Such a failure will be detected once the output is switched OFF.

6 Understanding the GCC Override function

When the normal operation of a channel requires programming a low I_{PU}/I_{PD} current, the output might require several tens of µs to be switched ON/OFF. However, such an interval can be too long in case of overcurrent, leading to excessive energy dissipation over the external FET and causing damage. L9945 protects the external FETs against overcurrent events by rapidly switching them OFF, overriding the programmed I_{PU}/I_{PD}. The override strategy can be programmed via the **GCC_OVERRIDE_CONFIG** bit in COMMAND 3. Behavior is described in the following table:

Table 16. I_{PU}/I_{PD} override function according to the GCC_OVERRIDE_CONFIG strategy

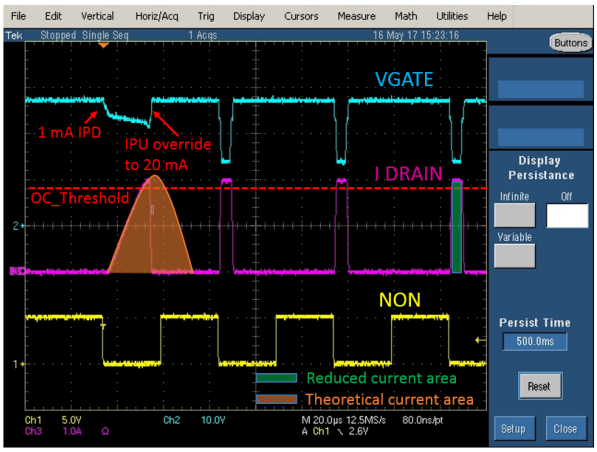
GCC_OVERRIDE_CONFIG	Nominal Current [mA]	Override Current [mA]
0	1	5
	5	20
	20	20
	Ext. lim.	Ext. lim.
1	1	20
	5	20
	20	20
	Ext. lim.	Ext. lim.

Note: The Ext. lim. option is not affected by the GCC_OVERRIDE_CONFIG bit.

6.1 GCC engagement and reset conditions

The figure below shows the benefits of the GCC override function applied to a HS PMOS. In the example, 1 mA I_{PD}/I_{PU} was programmed and GCC_OVERRIDE_CONFIG = '1'. As soon as the OC event is detected, the output is immediately switched OFF with a 20 mA IPU, overriding the original settings.

Figure 26. Effects of the GCC override function on a HS PMOS



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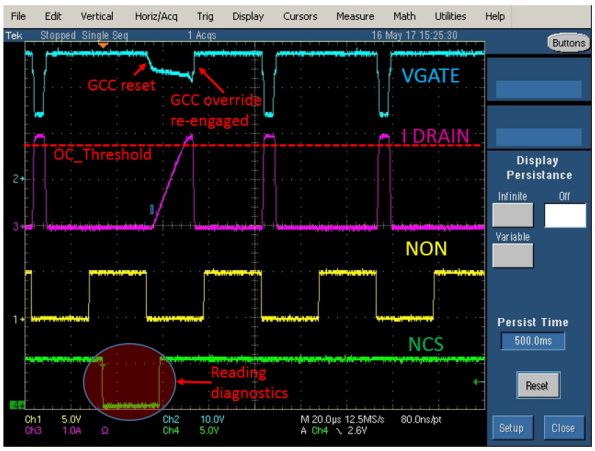
The GCC override is kept active until diagnostic latches are read, as shown in the figure below, where reading diagnostics causes a temporary reset of the override functionality, which is immediately re-engaged since overcurrent is persistent.

Figure 27. GCC override reset via diagnostics readout. Re-engagement with overcurrent event



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6.2 Energy dissipation reduction during OC events

In case the output re-engagement strategy requires diagnostics readout (PROT_CONFIG_XX = '1'), the external FET will be kept OFF after an OC event, regardless of its control signal. Therefore, high energy dissipation pulse occurs only once, during the first detection of the OC event.

On the other hand, if the output re-engagement strategy doesn't require diagnostics readout (PROT_CONFIG_XX = '0'), the output will keep following the PWM control signal, being periodically switched ON/OFF according to T_{PWM}. GCC override helps limiting the amount of energy periodically dissipated by the external FET by "chopping" the current area. Referring to Figure 26:

- the orange area is the theoretical current area that would have been obtained if a 1 mA current was used to switch the FET OFF
- the green area is the actual current area that is obtained by overriding the GCC settings and using a higher pull-up current to switch the FET OFF, thus chopping the current waveform

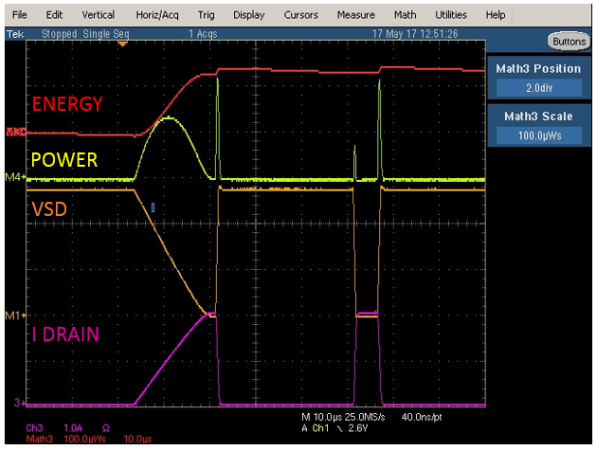
Figure 28 clearly shows the benefits of the GCC override activation in terms of energy dissipation. As it can be noticed, a huge energy dissipation occurs during the first transient, where OC event is detected and the GCC override activated. If the output continues switching according to the PWM control signal, following OC events will only add a small energy contribution due to the reduced output ON time.

Hence, GCC override setting contributes to limit the energy spikes and improves system robustness against OC failures.

ST recommends to program **GCC_OVERRIDE_CONFIG = '1'** in order to obtain the best robustness, forcing all currents to 20 mA in case of OC detection. In case a higher I_{PU}/I_{PD} current has already been implemented via external resistor, setting GCC_OVERRIDE_CONFIG = '1' won't affect this behavior, as shown in Table 16. In particular cases where the gate charge/discharge current cannot exceed certain limits, ST recommends to use the 1 mA option and to program **GCC_OVERRIDE_CONFIG = '0'**: by doing so, I_{PU}/I_{PD} current will be increased to 5 mA in case of OC detection.

Note: GCC override strategy is shared between all channels.

Figure 28. **Energy dissipation reduction through GCC override**



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7 L9945 Diagnostic Filter Times calculator

In order to summarize all the points explored in this paper, the **ST L9945 Charge Pump Stress Calculator** has been developed. Such a tool is a Microsoft Excel® workbook that applies all the equations formulated during our analysis in order to evaluate the best choice for both t_{DIAG} and t_{BLANK_OC} filter times.

The tool allows configuring each channel independently and helps understanding how the external components and the programmed gate charge/discharge current will impact on diagnostic filter times. A simple color code will highlight critical channels for which the diagnostics may not be guaranteed.

The analysis can be performed for different values of the power supply, including corner cases for cold cranking and load dump.

In the Excel workbook attached, two worksheets are available:

- The **Worst Case Scenario**, where the pessimistic approach described by Eq. (6), Eq. (10), Eq. (14), and Eq. (20) is pursued. ST recommends not to use any TM in this case.
- The **Typical Scenario**, where typical values are assumed for all the parameters involved. Such approach is described by Eq. (5), Eq. (9), Eq. (13), and Eq. (19). ST recommends using at least a 20% TM to add robustness.

Typically, the worst case scenario can be considered equivalent to a typical scenario with a 65% TM.

The tool is contained in a file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it.

Revision history

Table 17. **Document revision history**

Date	Version	Changes
20-Mar-2019	1	Initial release.

Contents

List of tables

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