
Guidelines for thermal management on STM32 MCUs and MPUs

Introduction

This document describes the thermal management guidelines for applications based on STM32 microcontrollers or microprocessors. These, like any silicon-based integrated circuits, have well-defined storage and operating temperature ranges. Only the STM32 operating temperature ranges defined in their product datasheets are considered. These are: the maximum operating temperature range, and the product operating temperature range. The maximum operating temperature range defines the threshold temperature beyond which there is a high probability of permanent damage to the device. The operating temperature range defines the threshold temperature beyond which the electrical parameters are not guaranteed to be within the specification.

The STM32 maximum specified operating range refers to the junction temperature, whereas the operating temperature range refers to the ambient temperature, and possibly also to the junction temperature.

Specifying the operating temperature ranges by reference to the ambient, or to the junction, temperature is common practice in the semiconductor industry. Depending on the device and its power consumption, semiconductor vendors use either of these for product operating-temperature range specification.



1 General information

This document applies to STM32 Arm®-based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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2 Thermal systems definitions and basic concepts

This section details basic definitions and concepts related to thermal systems, as applied to silicon-based integrated circuits (ICs).

2.1 Thermal systems definitions

Heat:

The amount of energy exchanged between two different bodies spontaneously under the effect of their different temperatures.

Temperature:

A comparative measurement of how hot or cold a body is. The temperature of a given body increases as it absorbs heat and decreases as it releases heat.

Temperature gradient:

Refer to the uneven temperature distribution over one body. The temperature gradient magnitude reflects the difference in temperature from one location to another inside a body.

Thermal resistance:

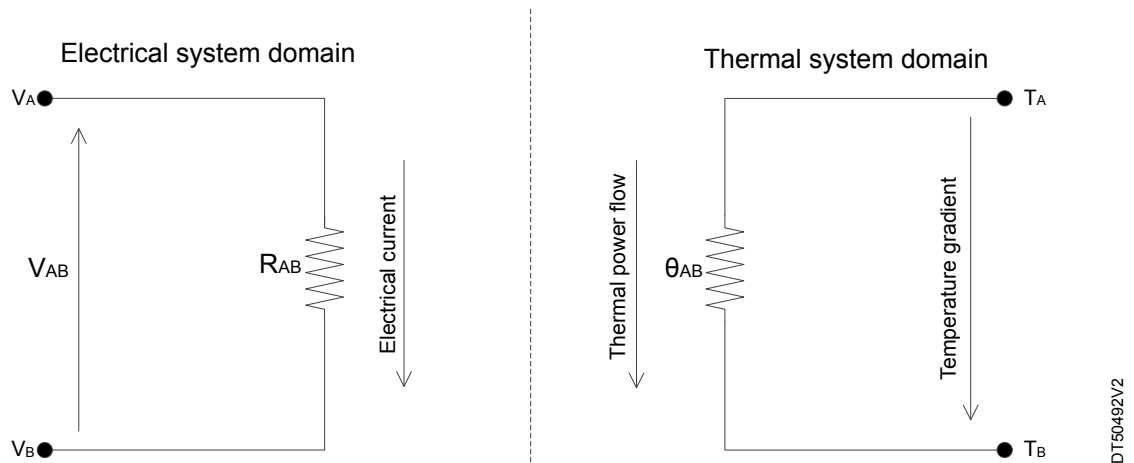
The property of a material to conduct a certain amount of heat under a certain temperature gradient.

2.2 Thermal system study

Thermal systems are designed with complex thermal models and advanced simulation software tools. These models and tools are used to obtain accurate results.

To resolve a thermal system with an acceptable accuracy and with limited computation effort, many simplifying hypotheses can be used (such as considering the thermal resistance to be temperature independent). Using these hypotheses, the study of thermal systems is analogous to the study of electrical systems, where the heat is equivalent to the electrical current, the temperature is equivalent to the voltage, and the thermal resistance is equivalent to the electrical resistance.

Figure 1. Analogy between electrical and thermal system domains

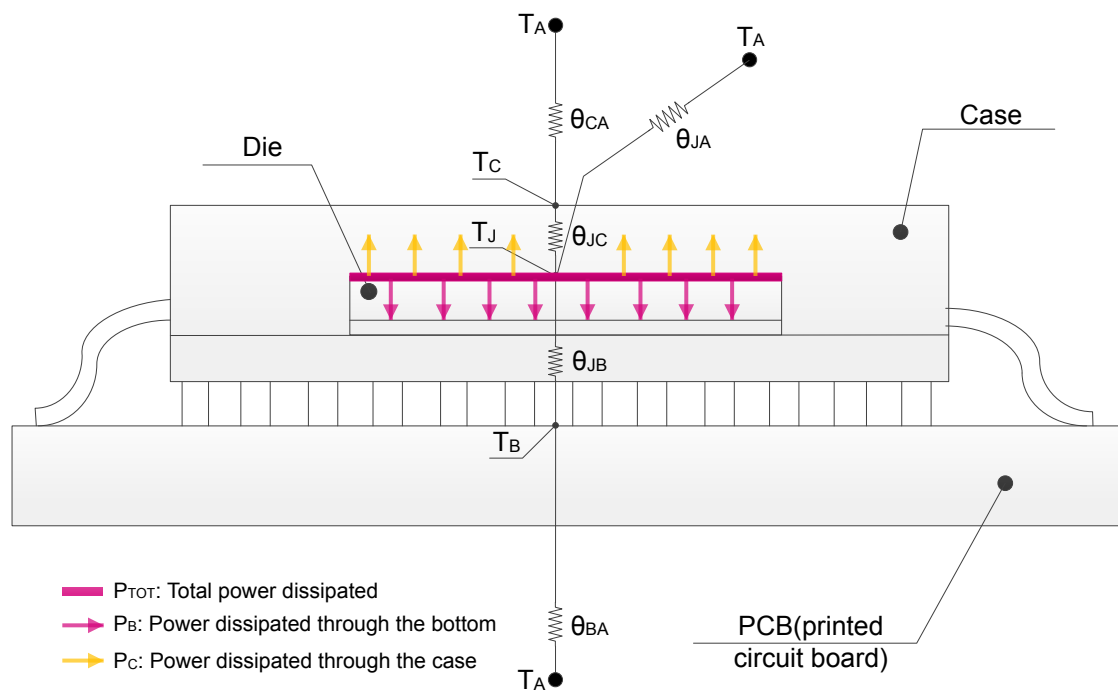


This model is widely accepted by the electronic industry. Most semiconductor vendors provide thermal resistance parameters of their packaged products based on this simplified model, in accordance with certain standardization bodies (like JEDEC EIA/JESD 51-X standards). Designers consider the provided thermal resistance parameters when dealing with heat dissipation in their application, or at least, at an earlier stage, when selecting the right package for a given product.

2.3 Thermal model of a chip carrier

A simplified thermal model for an LQFP-packaged STM32 product is provided in the figure below. All surface temperatures and thermal resistance (as defined by the JEDEC EIA/JESD 51-X standards) are depicted.

Figure 2. Thermal model of a chip carrier



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The definitions of thermal parameters mentioned in this figure are listed in the table below.

Table 1. Thermal parameters

Symbol	Description	Unit
T_J	Temperature of the die	°C
T_A	Temperature of surrounding air	
T_C	Temperature of the package top	
T_B	Temperature of the board near the device	
θ_{JC}	Thermal resistance between the die and the package	°C/W
θ_{JB}	Thermal resistance between the die and the PCB on which the IC is mounted	
θ_{JA}	Thermal resistance between the die and the air surrounding the die package	
P_B	Amount of power dissipated by the device through the board	W
P_C	Amount of power dissipated by the device through the package top	
P_{TOT}	The total power dissipated by the device ($P_{TOT} = P_B + P_C$)	

3 STM32 thermal parameters

This section explains the STM32 thermal parameters as specified by their respective datasheets.

3.1 Ambient temperature

In the electronic field, there is no consensus about a standard and unified definition of the ambient temperature. What is sure is that the ambient temperature is the temperature of the device surroundings, but there are many different ways to measure it. Measurement parameters such as the distance between the measurement point and the device, if the surrounding air is steady or not, the volume of the test environment, can severely impact later interpretation of the results.

JEDEC provides a standard definition for ambient temperature but that definition is limited to the JEDEC test environment used when determining package thermal characteristics.

Most of the time, the application operating conditions differ significantly from the JEDEC environment, making the JEDEC defined thermal resistance from junction-to-ambient temperature (Θ -JA) not practically usable for high-performance high-power-dissipation devices.

3.2 Junction temperature

The junction temperature is the widely used term to refer to the temperature of a die. Obviously, the die temperature is the most important temperature to consider for a device, as all its electrical parameters depend on this junction temperature. Indeed, the junction temperature is the one considered when qualifying the reliability of a device.

In theory, the die temperature is not uniformly distributed across the die. There is a temperature gradient across the die. In practice, the die temperature is generally considered to be uniformly distributed, and only a single temperature measurement is provided. This reduction of a temperature gradient into one temperature reading introduces a small uncertainty into subsequent assumptions and computations when the die dimensions are relatively small. This is the case for most STM32 devices.

3.3 Ambient temperature versus junction temperature

Both the ambient and the junction temperatures specify the thermal performance of STM32 devices.

For many STM32 devices, only the maximum ambient temperature is specified as their thermal performance limit. The junction temperature is also sometimes added.

The use of the ambient temperature for thermal performance assessment is much easier than using the junction temperature, as the die of a packaged device is not accessible. This makes the conventional temperature measurement methods unusable for measuring the die temperature.

Measuring the junction temperature requires more advanced measurement techniques. Most STM32 devices embed a junction temperature sensor, which serves as a primitive building block for thermal watchdog implementations. But at the design stage, this embedded temperature sensor cannot help in determining the thermal performance of the whole application. Instead, the junction temperature is estimated at the design stage. It is based on many parameters including the application power profile, the device thermal resistances, the surrounding temperature (board temperature and device case temperature). For accurate estimation of the junction temperature, modeling software tools are used when the final application has a complex thermal model and a complex power profile.

3.4 Case temperature

The case temperature is the temperature of the top of the package used as a chip carrier for the die. The JEDEC standards specify that the temperature sensor must be placed at the center of the package top, using 1 mm of conductive epoxy.

If the package case-to-ambient thermal resistance is much higher than the package junction-to-case thermal resistance (one order of magnitude at least), and as most devices dissipated power goes through the board, the junction temperature can be conflated with case temperature if some uncertainty is acceptable.

3.5 Board temperature

The board temperature, as defined by the JEDEC standards, is the PWB temperature measured near the center lead of the longest side of the device. The board temperature and the package junction-to-board thermal resistance are very critical parameters when assessing the device thermal performance.

Under steady air conditions, most of the heat generated by the device is dissipated through the board. The heat dissipated through the board can be 20 times higher than the heat dissipated through the package top. For instance, for a JEDEC high-conductivity test board and under steady air conditions, 95% of the device power dissipation passes through the board and only 5% is dissipated through the package top.

3.6 STM32 thermal parameters

Most of the STM32 datasheets give only Theta-JA thermal resistance, but some specify also Theta-JC and Theta-JB, defined in the table below.

Table 2. STM32 thermal resistances

Thermal metric	Symbol	Value	Main purpose
Theta-JA	θ_{JA}	$\frac{T_J - T_A}{P_{TOT}}$	Used to rank package performance in the JEDEC environment
Theta-JC	θ_{JC}	$\frac{T_J - T_C}{P_C}$	Used to rank package performance Used in simulations with a 2R model (2R = two resistances)
Theta-JB	θ_{JB}	$\frac{T_J - T_B}{P_B}$	Used to rank package performance Used in simulations with 2R model

These parameters are determined under the following specific conditions that differ from the final application conditions:

- Theta-JA: The JEDEC51-2 document *Integrated circuits thermal test method environmental conditions - natural convection (still air)* describes the thermal test method to define Theta-JA.
- Theta-JB: The JEDEC51 document *Integrated circuit thermal test method environmental conditions – junction-to-board* describes the thermal test method to define Theta-JB.
- Theta-JC: The MIL-STD-883E document *Test method standard microcircuits* describes the thermal test method to define Theta-JC.

These thermal resistances must be carefully defined in semiconductor packages and devices context.

The most important point about these values is that the total power dissipated by the device flows between the two following “points”:

- The junction
- Ambient or board temperature

There are no extraneous parallel thermal paths in the system allowing some of the heat to “leak” away. All the heat leaving the junction eventually arrives at or passes through the other point.

It is usually possible to know the total power dissipation of a device but it is far more difficult to know which fraction of the heat flows out through the case top, versus the part that flows through the leads, and versus the part that flows through the air gap under the package.

Theta-JC and Theta-JB are generally used as inputs for thermal simulation tools, which calculate which fraction of the heat flows out through the top and the bottom of the device.

4 Power dissipation and cooling methods

This section provides recommendations for efficient thermal analysis on STM32 applications, focusing on the following points:

- power dissipation and its variation with factors named PVTA (process, voltage, (junction) temperature, and activity)
- how to minimize the power consumption
- how to optimize the thermal dissipation

4.1 Power dissipation

There are two types of current consumed by the device:

- The static current: also called leakage current, depends on the process, voltage, and junction temperature but does not depend on the activity
- The dynamic current: depends on the process, voltage, and activity but does not depend on the junction temperature (at least in first approximation).

The static/leakage current grows exponentially with the junction temperature (while the dynamic current does not significantly change).

Therefore, the total current can be written as follows:

$$I_{Total}(P, V, T_j, activity) = I_{static}(P, V, T_j) + I_{Dynamic}(P, V, activity)$$

The dissipated power varies with PVTA conditions. It is calculated as the product of the voltage generated across the device and the (average) current consumed.

The junction temperature increase above the ambient temperature is calculated as a product of the dissipated power and the junction-to-room thermal resistance.

The junction temperature must be kept lower than the maximum target given by the following equation:

$$T_j = T_{room} + P_{diss} \times \Theta_{j_room} < T_{j_max}$$

Important: *In this simplified formula used only for didactic purpose, Θ_{j_room} is a complex coefficient that is not a device characteristic but a system one (device + other components + boards + casing).*

The following methods to keep the junction temperature below the ambient temperature are detailed in the next sections:

- Limiting P_{diss}
- Limiting Θ_{j_room} (cooling system, host board and casing design)

4.2 Minimizing power consumption (P_{diss})

To reduce the power consumption, the first action is to reduce the supply voltage. Some STM32 devices offer a multipower domain architecture that allows the different power domains to be set in low-power mode. The goal is to optimize the power efficiency (see the corresponding datasheets for more details).

The power consumption profile also varies with the application. Some applications are most of the time in idle mode, working on full or limited capacity only when an event occurs. Some others demand a regular workload.

For these various power profiles, the user programmer enables the low-power modes by software.

The most common available modes are listed below:

- Power gating: reduces power consumption by shutting off the current to a part of the circuit that is not in use.
- Clock gating: reduces dynamic power dissipation by shutting down clocks to a circuit or portion of the clock tree.
- Dynamic voltage scaling: power management technique where the voltage is increased or decreased, depending upon circumstances.
- Dynamic frequency scaling (also known as throttling when applied to a CPU): frequency automatically adjusted on-the-fly depending on the actual needs, to conserve power and reduce the amount of heat generated.

All these modes are available, for example, on STM32H7 and STM32MP1 series devices (see the reference manuals for more details).

4.3 Power dissipation variation with junction temperature

In this section, process, voltage, and activity factors are kept constant, and there is a focus on the effect of the junction temperature.

The static/leakage current grows exponentially with the junction temperature (while the dynamic current does not significantly change).

The power dissipation variation with junction temperature has the following main consequences:

- A cooling solution must be implemented to limit the junction temperature below 125 °C (maximum junction temperature).
- If the cooling system is not efficient enough, the device can go into thermal runaway that may be destructive.

When performing system-level thermal simulations in the design phase, it is fundamental to input junction temperature dependent power dissipation.

4.4 Risk of thermal runaway

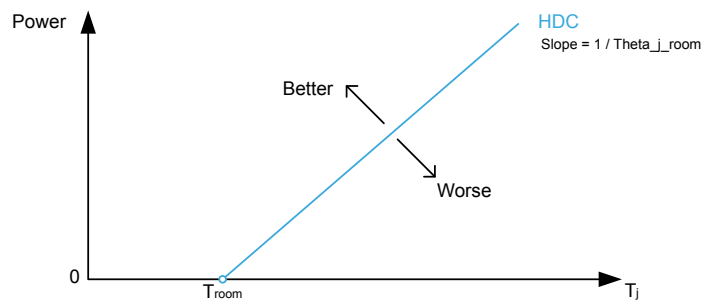
The junction-to-room temperature thermal resistance, Θ_{j_room} , characterizes the cooling system of a design.

This thermal resistance gives the capability to dissipate power in the design while limiting the junction temperature.

The following equation gives the heat dissipation capability (HDC):

$$HDC = (T_j - T_{room}) / (\Theta_{j_room})$$

Figure 3. HDC (heat dissipation capability)

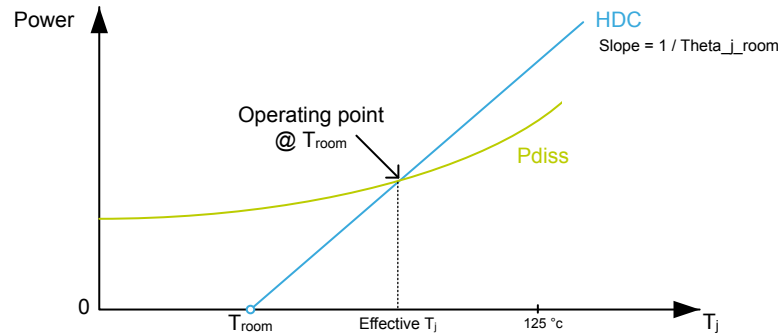


- Note:**
- *Better: design has more ability to dissipate heat*
 - *Worse: design has less ability to dissipate heat*

Case 1

The figure below shows the operating point at the intersection of the curve of the power that can be dissipated inside the design at a given T_J (HDC) and the curve of the power effectively dissipated inside the design (Pdiss).

Figure 4. HDC and junction-temperature-dependent dissipated power (case 1)

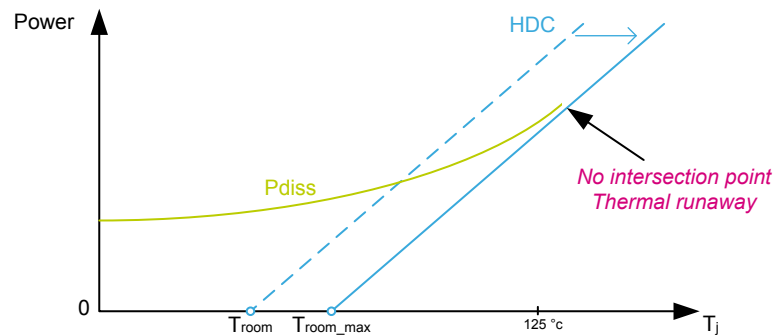


The cooling design is safe (no thermal runaway) if an intersection point exists for $T_{room} = T_{room_max}$, with a junction temperature $< 125\text{ °C}$.

Case 2

The figure below shows the effect of an increased room temperature (without changing any other factors).

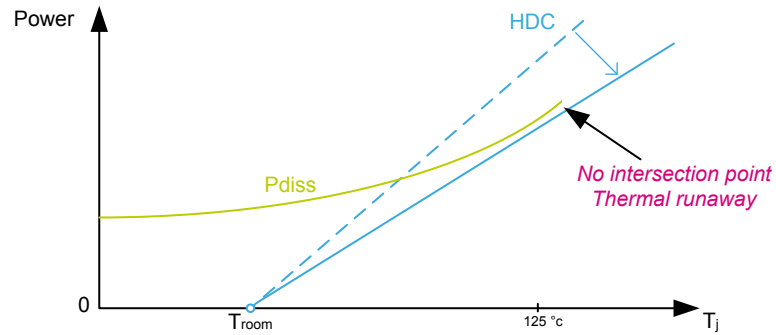
Figure 5. HDC and junction-temperature-dependent dissipated power (case 2)



Case 3

The figure below shows the effect of an increased junction-to-room thermal resistance (without changing any other factors).

Figure 6. HDC and junction-temperature-dependent dissipated power (case 3)

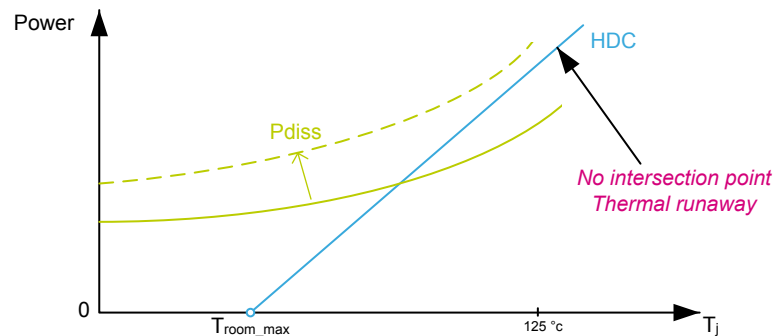


The two curves in case 2 and case 3 do not intersect. For this reason, no stable operating point is defined. This is a condition of thermal runaway.

Case 4

The figure below shows the effect of a decrease in power dissipation (without changing any other factors).

Figure 7. HDC and junction-temperature-dependent dissipated power (case 4)



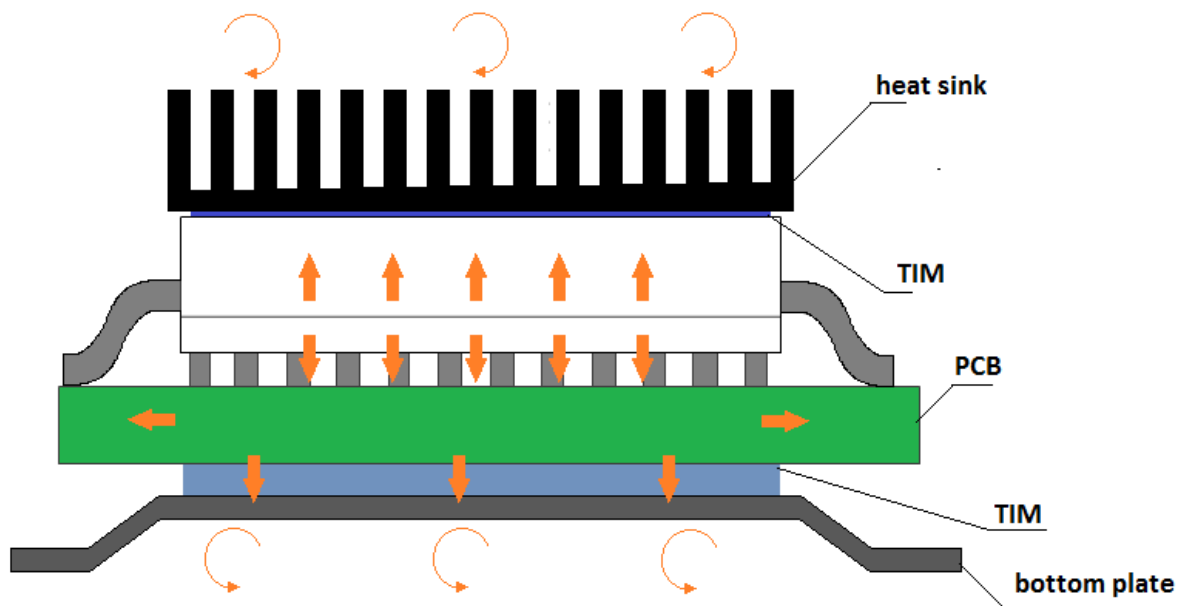
5 Cooling

5.1 Power dissipation paths

The power dissipated by the die is extracted along the two following main paths:

- top side: power dissipated from the top side, (by a heat sink through an optional TIM, thermal interface material)
- bottom side: power dissipated from the bottom side by the PCB, (by bottom metal plate through an optional TIM)

Figure 8. Power dissipation paths



5.2 Main cooling methods

The heat sink and the PCB dissipate the power to the surrounding environment by the convection and radiation methods.

5.2.1 Natural convection

The term 'natural convection' is used when no fan is used in the casing. This cooling method is a combination of natural convection and radiation that always work in parallel.

5.2.2 Forced convection

The term 'forced convection' is used when a fan is used in the casing.

5.2.3 Natural and forced convection comparison

The table below details the main comparison factors between the natural and forced convection.

Table 3. Natural and forced convection comparison

Comparison factors	Natural convection	Forced convection
Cooling efficiency	Low	Medium to high (depending on air speed)
Cost	Low (no fan)	Higher (cost of the fan)
Reliability	Higher (no moving parts)	Lower (mechanical part moving)
Acoustic noise	None	Small to medium (depending on air speed)
Possibility to control cooling efficiency based on needs	None	Yes, by varying fan voltage

5.3 Bottom cooling - host PCB design

To provide enough 'thermal vias', as the host PCB is a secondary heat sink for the device, it is important to use the recommended stack-up and to optimize the PCB layout beneath the package.

A significant power proportion is drawn from the package to ambient air through the host board by the paths detailed in the next sections (sorted by decreasing order of importance). The design rule implementation for ground and power connections is necessary for cooling and power distribution.

It is not possible to produce a set of rigid rules for layer construction within a PCB because each design has its own requirements.

5.3.1 Host PCB ground and power layout

The ground (GND) plane must have a low resistance (thermal and electrical) for all PCB areas. This improves signal quality and power dissipation. It also reduces EMI. The use of a ground layer and flooding of other layers with multiple vias maintain the resistance at a low level.

Placing as many thermal vias as possible on the ground and power planes just below the package, ensures that there is enough continuous copper between the adjacent vias for power distribution and thermal dissipation. A compromise must be found.

The possible thermal vias are listed below:

- ground vias: connecting GND to the unified GND plane (these are the most efficient thermal vias)
- power vias: connecting power to the power plane

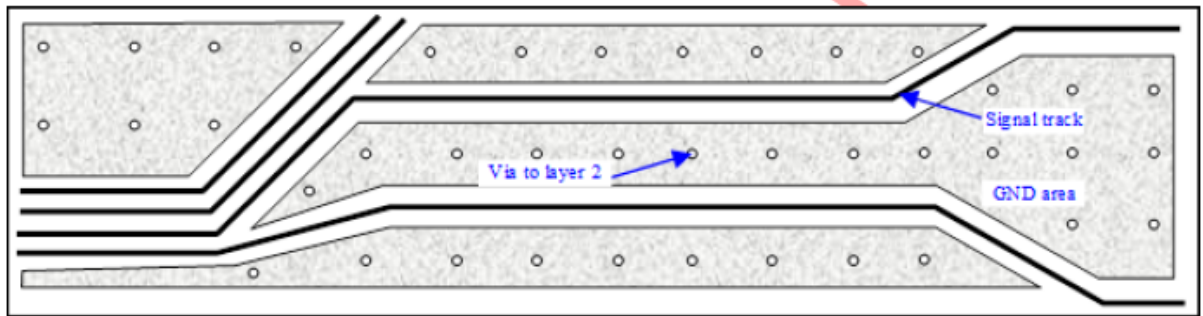
The thermal vias conduct heat from the device to the internal GND and power planes. These planes spread the heat inside the PCB that acts as a planar heat sink.

5.3.2 Additional GND areas on outer layers

On the outer layers, some GND areas can be added wherever functional tracks are absent. Connect these areas to GND by a network of vias wherever possible.

These GND areas help in heat spreading and dissipation along the board. The figure below shows the principle of additional GND areas and vias to the GND plane.

Figure 9. Principle of additional GND areas and vias to the GND plane



6 Thermal analysis examples

This section shows examples of thermal analysis performed on a discovery kit (STM32H747XI MCU), an evaluation board (STM32MP157), and an internal validation board (STM32MP135 MPU).

These analyses provide some answers to the following questions (at maximum ambient temperature 85 °C):

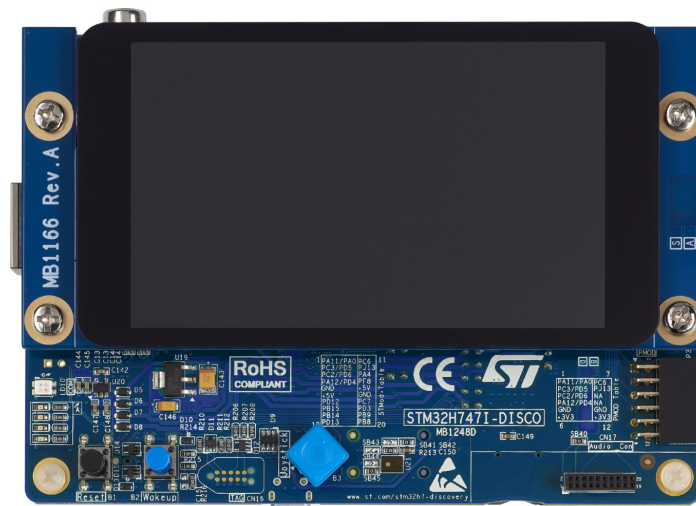
- How much does the power dissipation admit the leakage?
- Is $T_J < 125$ °C?
- Is there a risk of thermal runaway?

6.1 Discovery kit with STM32H747XI MCU

This thermal analysis has been done on a Discovery kit with an STM32H747XI device (STM32H747I-DISCO), without casing (see the figure below).

Figure 10. STM32H747I-DISCO

This picture is not contractual.



The test case is the following:

- Run mode (400 MHz) data processing running from the flash memory
- Cache ON
- All peripherals enabled

The temperature sensor connected to the ADC3 VINP [18] input channel, is used for T_J measurement.

The T_J measurements are read via the USART2 using the DMA transfer, without CPU interruption.

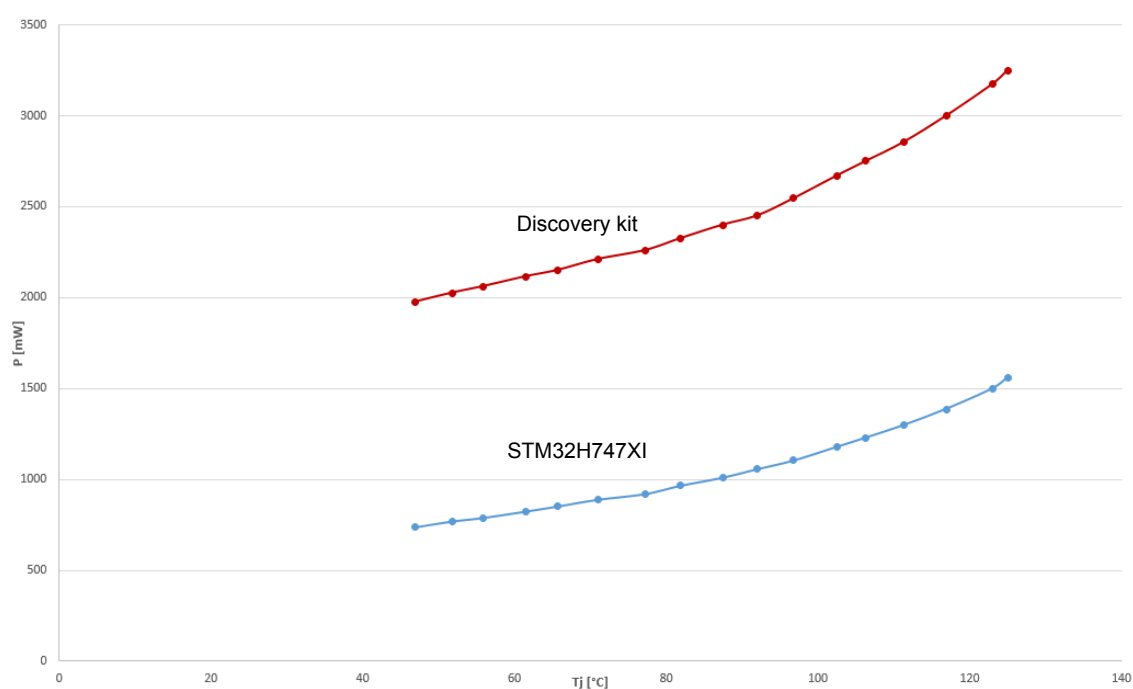
6.1.1 STM32H7 power dissipation

As stated in Section 3, the dissipated power varies with T_J . The power consumption in this example is measured for different T_J values (see the table and the figure below).

Table 4. STM32H747XI power dissipation versus T_J

T_J (°C)	STM32H747I-DISCO (supplied with 5 V)		STM32H747XI power dissipation (mW)
	Current consumption (A)	Power consumption (mW)	
46.9	0.395	1975	737
51.8	0.405	2025	769
55.8	0.412	2060	788
61.5	0.423	2115	824
65.7	0.430	2150	852
71	0.442	2210	888
77.3	0.452	2260	920
81.9	0.465	2325	965
87.5	0.480	2400	1010
92	0.490	2450	1056
96.8	0.509	2545	1104
102.5	0.534	2670	1179
106.3	0.550	2750	1229
111.3	0.571	2855	1298
116.9	0.600	3000	1387
123	0.635	3175	1499
125	0.650	3250	1559

Figure 11. Junction-temperature-dependent dissipated power for STM32H7



6.1.2 STM32H7 thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

The figures and table below detail the thermal measurements performed at $T_A = 25\text{ }^{\circ}\text{C}$.

Figure 12. STM32H747XI thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

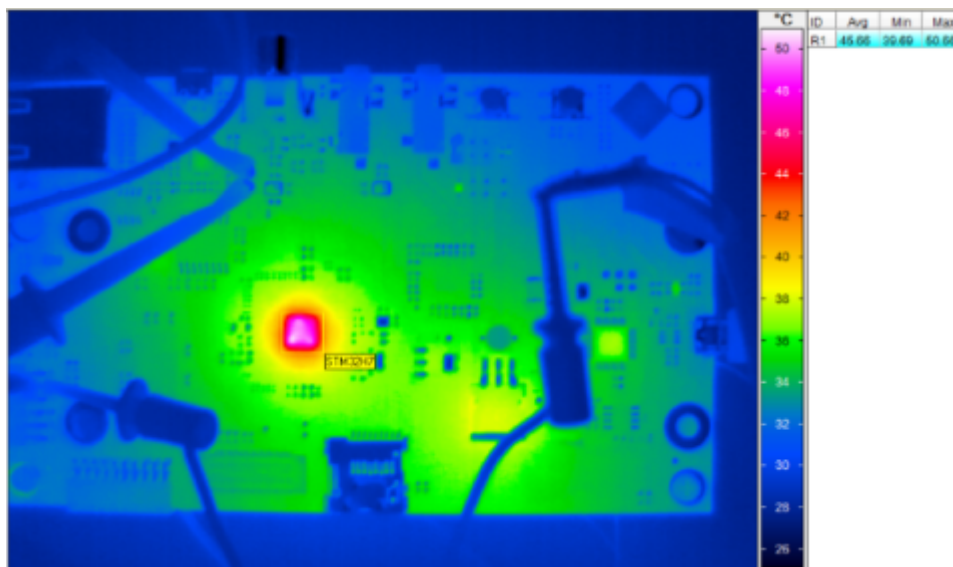
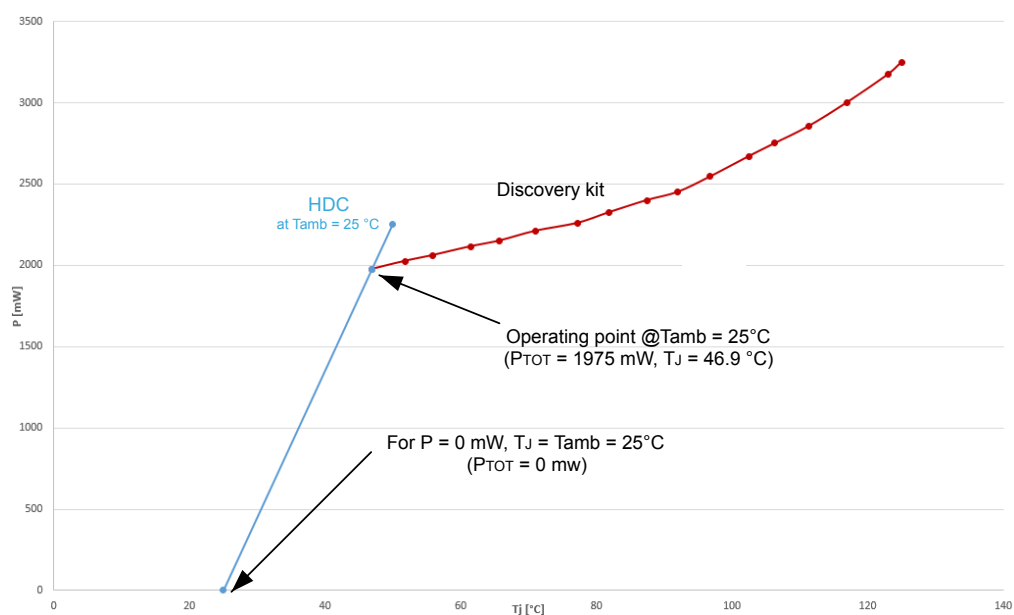


Table 5. STM32H7 thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

T_J ($^{\circ}\text{C}$)	Thermal camera module measurement ($^{\circ}\text{C}$)			STM32H7 power consumption (mW)	Total power consumption (mW)
	Avg	Min	Max		
46.9	45.5	39.7	50.6	737	1975

Figure 13. HDC at $25\text{ }^{\circ}\text{C}$ and junction-temperature-dependent dissipated power for STM32H7



Once the design HDC is defined (by measurement at 25 °C), and assuming that this HDC is constant at 25 °C and 85 °C, the operating point of the design at 85 °C is given by translating the HDC at 85 °C. See the figure and table below.

Figure 14. HDC at 85 °C and junction-temperature-dependent dissipated power for STM32H7

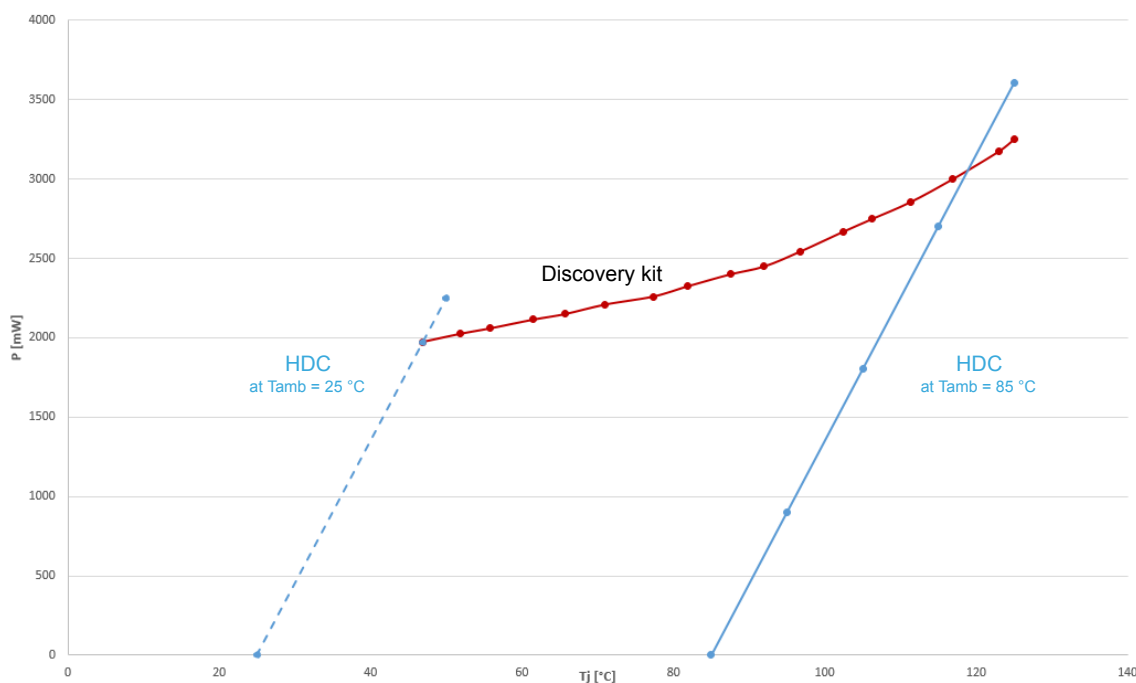


Table 6. Measurement interpolation at $T_A = 85\text{ °C}$ for STM32H7

Parameter	Value
T_J	119 °C
P_{TOT}	3050 mW

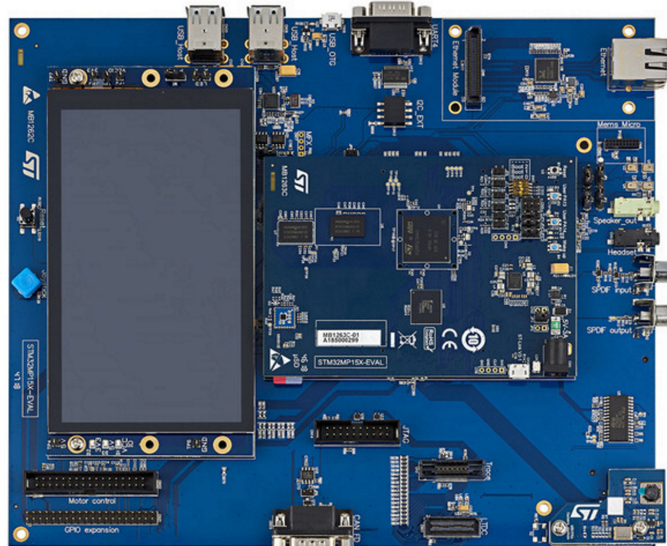
In conclusion, the STM32H7 device is safe, with no thermal runaway, and T_J remaining < 125 °C.

6.2 Evaluation board with STM32MP157 MPU

This thermal analysis has been done on an evaluation board with an STM32MP157 device, without casing (see the figure below).

Figure 15. STM32MP157x-EV1

This picture is not contractual.



While running commands, the script monitors the following:

- The CPU load with `mpstat`
- The board temperature via `/sys/class/hwmon/hwmon0/temp1_input`
- The memory used via the `free` command

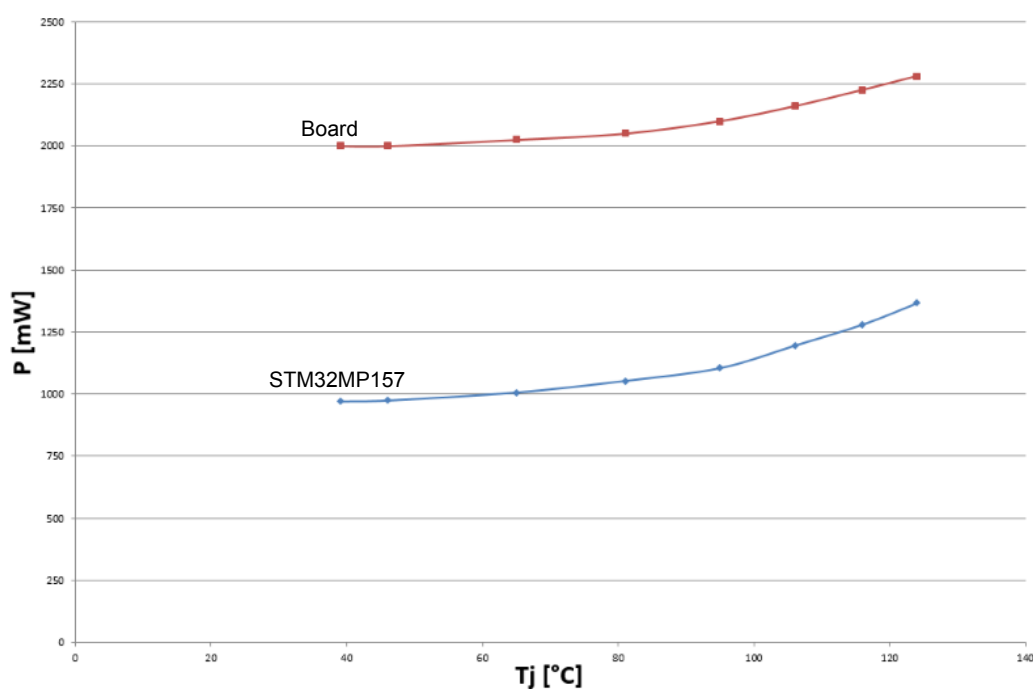
6.2.1 STM32MP157 power dissipation

As stated in Section 3, the dissipated power varies with T_J . The power consumption in this example is measured for different T_J values (see the table and the figure below).

Table 7. STM32MP157 power dissipation versus T_J

T_J (°C)	STM32MP157x-EV1 board (supplied with 5 V)		STM32MP157 power dissipation (mW)
	Current consumption (A)	Power consumption (mW)	
39	0.4	2000	970.2
46	0.4	2000	973.8
65	0.405	2025	1006.4
81	0.41	2050	1053.1
95	0.42	2100	1104.7
106	0.432	2160	1195.5
116	0.445	2225	1280.6
125	0.456	2280	1366.6

Figure 16. Junction-temperature-dependent dissipated power for STM32MP157



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6.2.2 STM32MP157 thermal measurements at $T_A = 25^\circ\text{C}$

The figures and table below detail the thermal measurements performed at $T_A = 25^\circ\text{C}$.

Figure 17. STM32MP157 thermal measurements at $T_A = 25^\circ\text{C}$

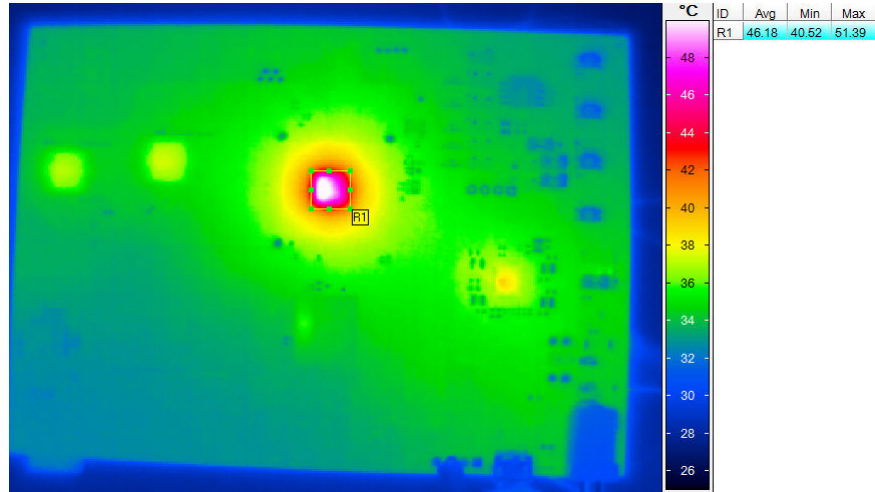
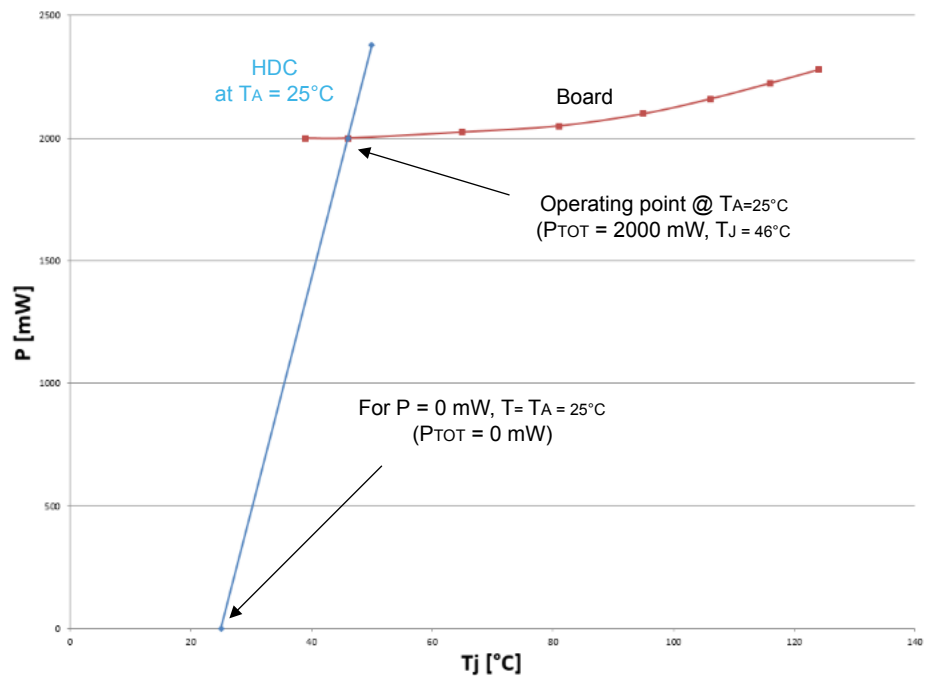


Table 8. STM32MP157 thermal measurements at $T_A = 25^\circ\text{C}$

T_J ($^\circ\text{C}$)	Thermal camera measurement ($^\circ\text{C}$)			STM32MP157 power consumption (mW)	Total power consumption (mW)
	Avg	Min	Max		
46	46.2	40.52	51.4	974	2000

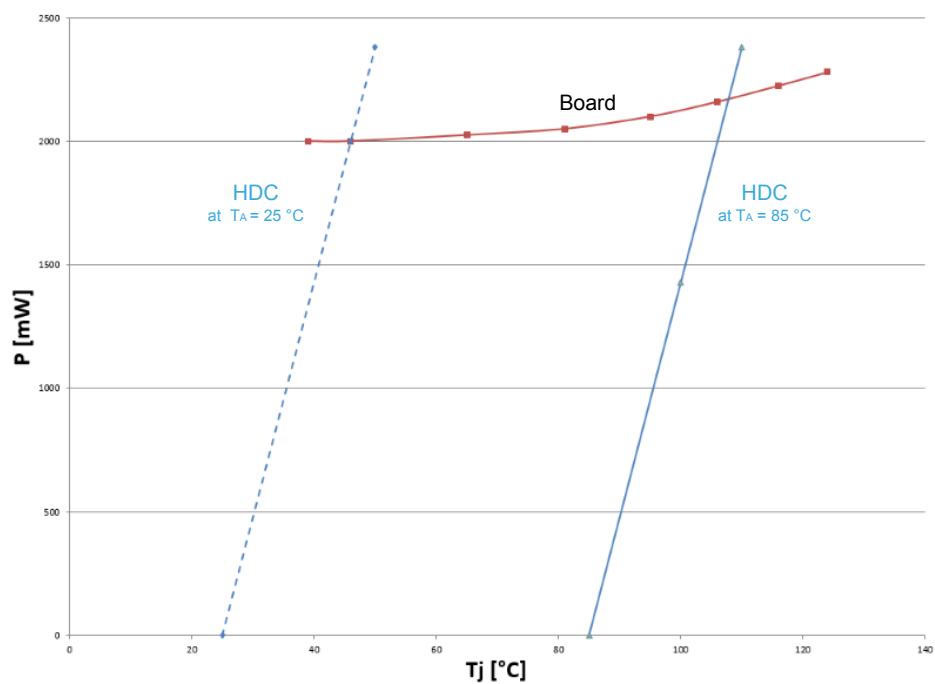
Figure 18. HDC at 25°C and junction-temperature-dependent dissipated power for STM32MP157



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Once the HDC of the design is defined (by measurement at 25 °C), and assuming that this HDC is constant at 25 °C and 85 °C, the operating point of the design at 85 °C is given by translating the HDC at 85 °C as shown in the figure and table below.

Figure 19. HDC at 85 °C and junction-temperature-dependent dissipated power for STM32MP157



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Table 9. Measurement interpolation at $T_A = 85\text{ °C}$ for STM32MP157

Parameter	Value
T_J	110 °C
P_{TOT}	2200 mW

In conclusion, the STM32MP157 device is safe, with no thermal runaway, and T_J remaining < 125 °C.

6.3 Internal validation board with STM32MP135 MPU

This thermal analysis has been done on an internal validation board with an STM32MP135 device without casing. This analysis is based on the use cases detailed in the table below. They correspond to CPU frequencies of 900 MHz and 1 GHz:

Table 10. Use cases for STM32MP135 MPU

Name	Description	CPU load	DDR load
cpuburn	-	100%	R = 3 Mbyte/s, W = 0 Mbyte/s, R&W = 4 Mbyte/s
dd	Idle (weston launcher, netdata) + dual eth + USB hard drive + dd on hard drive (ETH cables unplugged)		R = 129 Mbyte/s, W = 40 Mbyte/s, R&W = 169 Mbyte/s

6.3.1 STM32MP135 power dissipation

6.3.1.1 Use case about cpuburn

As stated in [Section 3](#), the dissipated power varies with T_J . The power consumption in this example is measured for different T_J values (see the following tables and figure).

Table 11. STM32MP135 power dissipation versus T_J at 900 MHz (cpuburn)

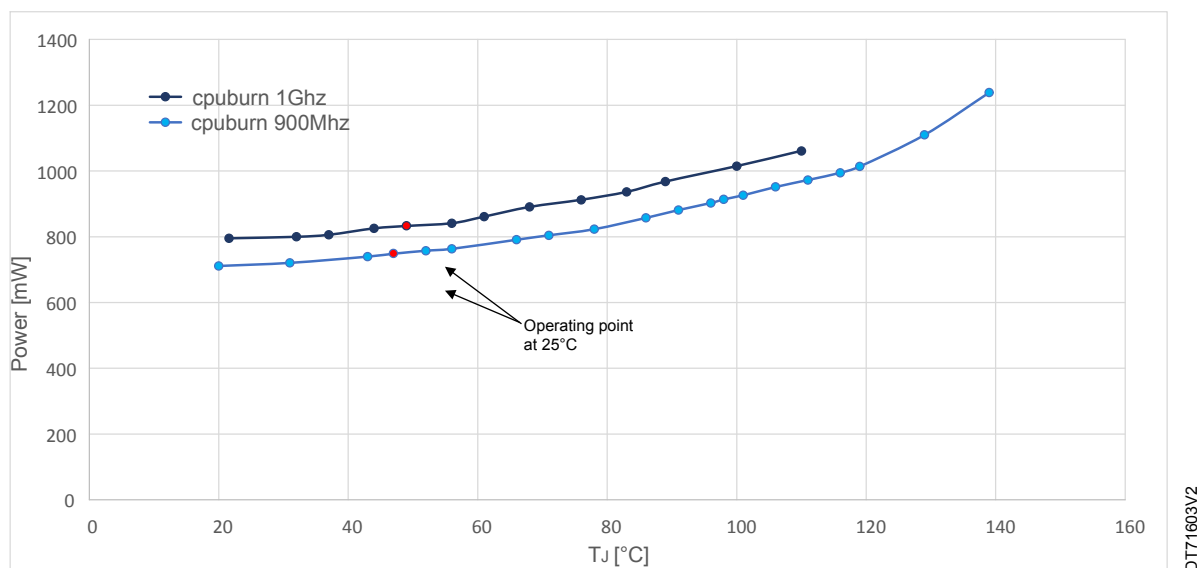
T_J (°C)	STM32MP135 power dissipation (mW) at 900 MHz
20.00	711.44
31.00	721.04
43.00	740.00
47.00	748.83
52.00	757.93
56.00	763.62
66.00	791.42
71.00	804.79
78.00	823.36
86.00	857.92
91.00	881.62
96.00	903.01
98.00	914.23
101.00	926.44
106.00	951.83
111.00	973.00
116.00	994.98
119.00	1014.19
129.00	1110.12
139.00	1238.89

Table 12. STM32MP135 power dissipation versus T_J at 1 GHz (cpuburn)

T_J (°C)	STM32MP135 power dissipation (mW) at 1 GHz
21.60	795.45
32.00	800.12
37.00	806.26
44.00	825.79
49.00	833.00
56.00	841.39
61.00	861.53
68.00	890.82
76.00	912.60
83.00	936.60
89.00	967.97
100.00	1014.80
110.00	1061.20

Table 13. STM32MP135 thermal measurements at $T_A = 25$ °C (cpuburn)

Parameter	900 MHz	1 GHz	Unit
T _J	47	49	[°C]
V _{CORE}	1.32	1.332	[V]
I _{CORE}	180	195	[mA]
P _{CORE}	237	260	[mW]
V _{DD}	3.33	3.321	[V]
I _{DD}	13	19	[mA]
P _{DD}	43	63	[mW]
V _{CPU}	1.415	1.414	[V]
I _{CPU}	306	331	[mA]
P _{CPU}	432	468	[mW]
V _{DDR2}	1.2	1.206	[V]
I _{DDR2}	30	35.5	[mA]
P _{DDR2}	36	43	[mW]
STM32MP135 power dissipation	748	834	[mW]
	+11%		

Figure 20. Junction temperature-dependent dissipated power for STM32MP135 (cpuburn)


DT71603V2

6.3.1.2 Use case about dd

As stated in [Section 3](#), the dissipated power varies with the T_J . The power consumption in this example is measured for different T_J values (see the following tables and figure).

Table 14. STM32MP135 power dissipation versus T_J at 900 MHz (dd)

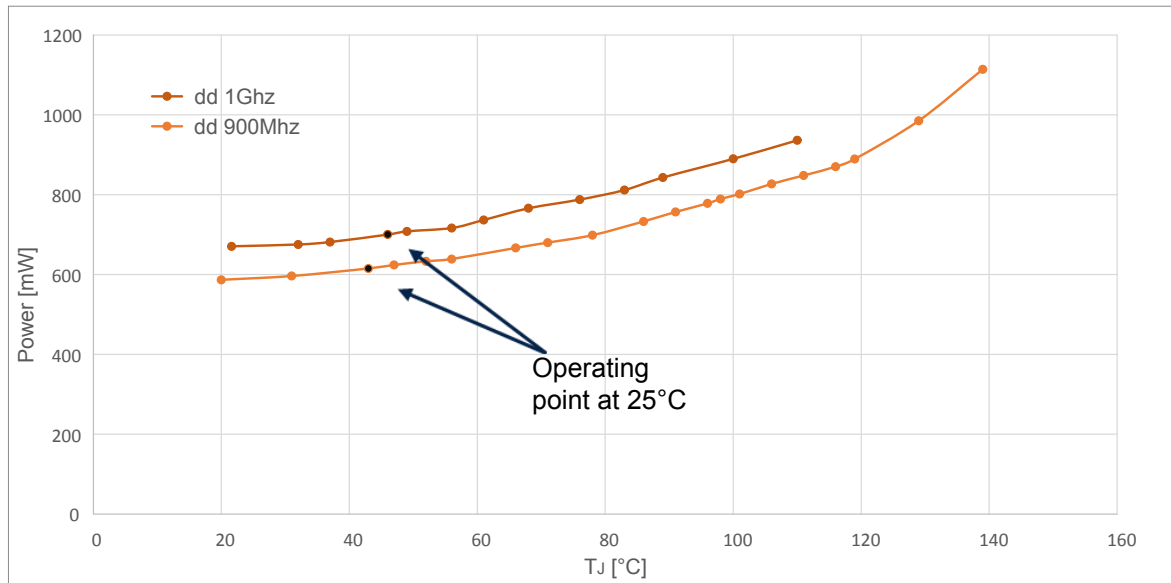
T_J (°C)	STM32MP135 power dissipation (mW) at 900 MHz
20	586.44
31	596.04
43	615.00
47	623.83
52	632.93
56	638.62
66	666.42
71	679.79
78	698.36
86	732.92
91	756.62
96	778.01
98	789.23
101	801.44
106	826.83
111	848.00
116	869.98
119	889.19
129	985.12

Table 15. STM32MP135 power dissipation versus T_J at 1 GHz (dd)

T_J (°C)	STM32MP135 power dissipation (mW) at 1 GHz
21.6	670.45
32	675.12
37	681.26
46	700
49	708.00
56	716.39
61	736.53
68	765.82
76	787.60
83	811.60
89	842.97
100	889.80
110	936.20

Table 16. STM32MP135 thermal measurements at $T_A = 25$ °C (dd)

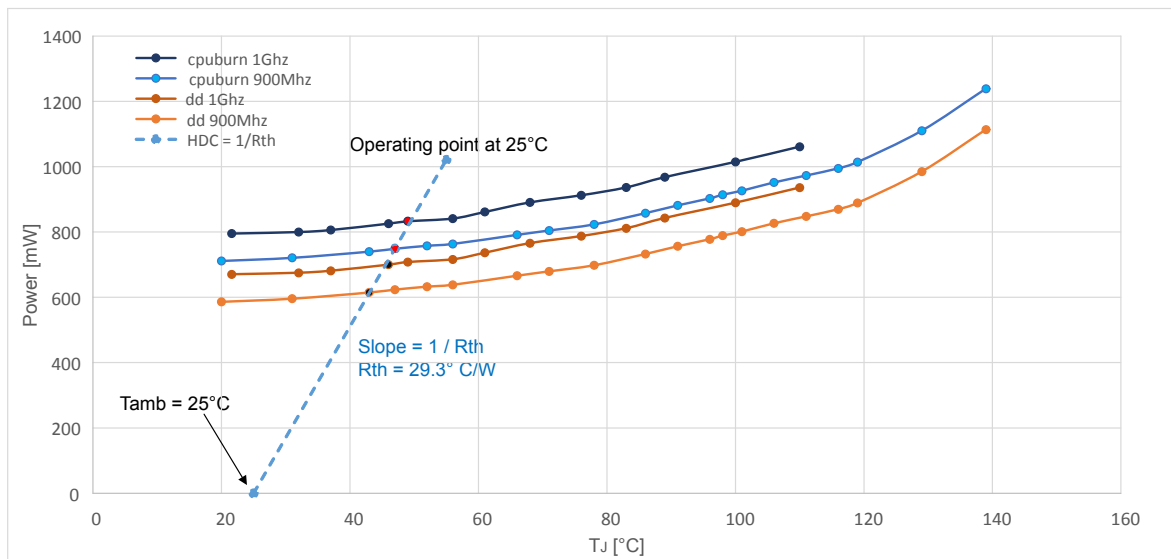
Parameter	900 MHz	1 GHz	Unit
T _J	43	46	[°C]
V _{CORE}	1.32	1.32	[V]
I _{CORE}	177	198	[mA]
P _{CORE}	233	261	[mW]
V _{DD}	3.33	3.33	[V]
I _{DD}	13	19	[mA]
P _{DD}	43	63	[mW]
V _{CPU}	1.415	1.398	[V]
I _{CPU}	173	199	[mA]
P _{CPU}	244	278	[mW]
V _{DDR2}	1.268	1.268	[V]
I _{DDR2}	75	77	[mA]
P _{DDR2}	95	97	[mW]
STM32MP135	615	700	[mW]
	+ 13%		

Figure 21. Junction temperature-dependent dissipated power for STM32MP135 (dd)


DT71604V2

6.3.2 HDC at 25 °C and junction temperature

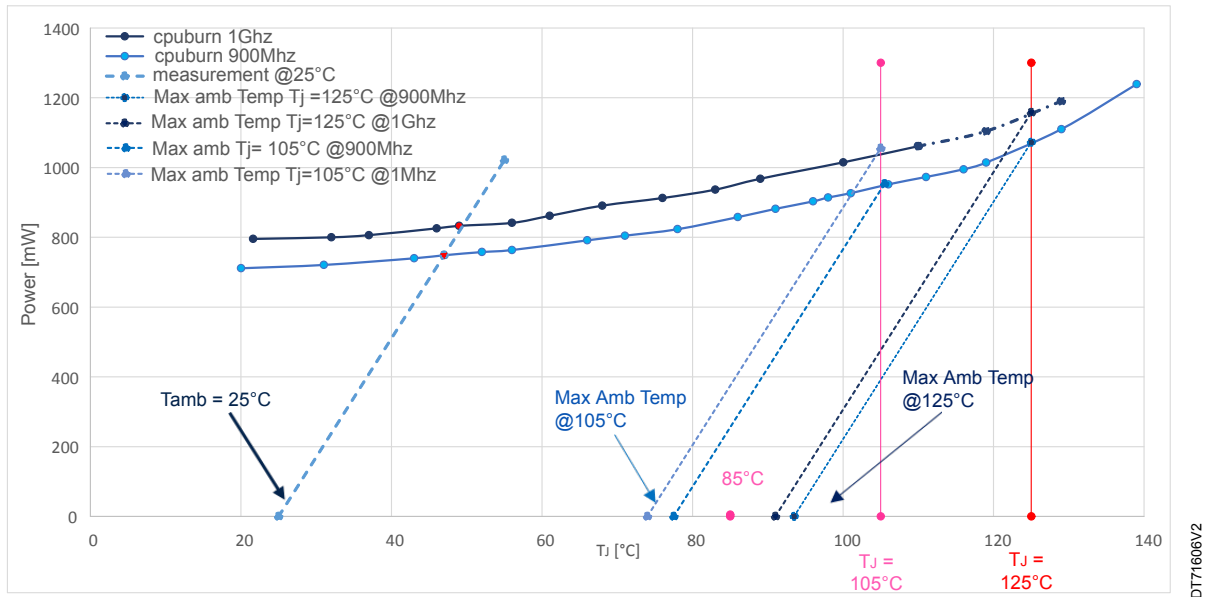
Once the design HDC is defined (by measurement at 25 °C), and assuming that this HDC is constant at 25 °C and 85 °C, the operating point of the design at 85 °C is given by translating the HDC at 85 °C as shown in the figure below.

Figure 22. MPU power dissipation


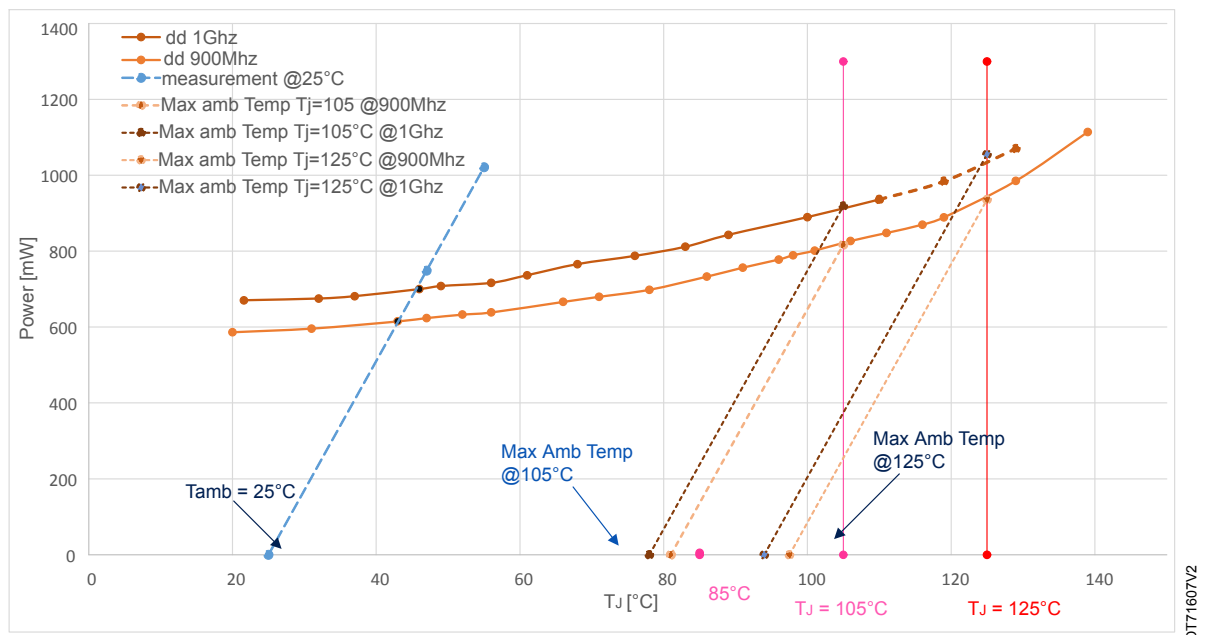
DT71605V2

6.3.3 Maximum ambient temperature (STM32MP135 MPU)

The maximum ambient temperature for the cpuburn and dd use cases are given in the figures below.

Figure 23. Maximum ambient temperature(Cpuburn)


DT71606V2

Figure 24. Maximum ambient temperature (dd)


DT71607V2

6.3.4

Conclusion

The measurement details given in the previous sections give:

- An 11% and 13% increase of the power consumption between 900 MHz and 1 GHz. These are respectively for the cpuburn and dd use cases.
- A 2 and 3 °C increase of T_J between 900 MHz and 1 GHz (for cpuburn and dd use case respectively)
- No risk of thermal runaway

Table 17 summarizes the maximum ambient temperature for various configurations.

Table 17. Maximum ambient temperature (STM32MP135 MPU)

Frequency	Maximum ambient temperature (°C)			
	T _J = 105 °C		T _J = 125 °C	
	cpuburn	dd	cpuburn	dd
900 MHz	77.5	81	93.5	97.5
1 GHz	74	78	91	94

6.4 Internal validation board with STM32MP257 MPU

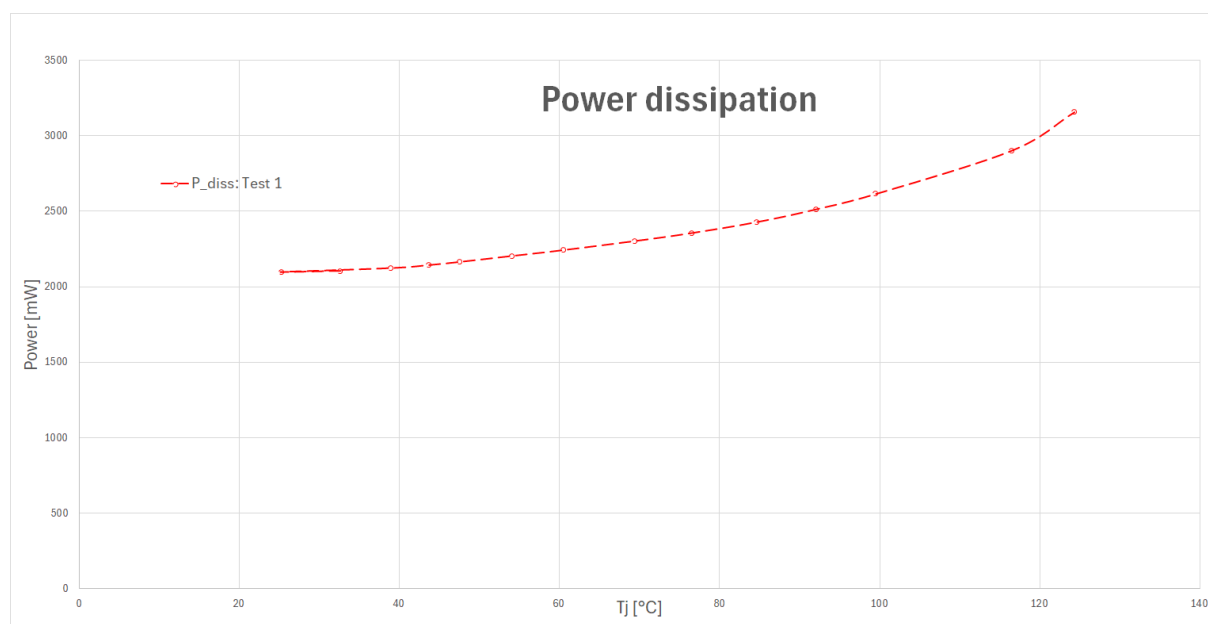
This thermal analysis has been done on an internal validation board with an STM32MP257 device without casing. The test case is the following:

- Glmark2-es2-drm
- Video decoder
- Endecoder
- Memtester1
- Memtester2

6.4.1 STM32MP257 power dissipation

As stated in Section 3, the dissipated power varies with T_J . In Figure 25, the power consumption is measured for different T_J values.

Figure 25. Junction temperature-dependent dissipated power for STM32MP257



6.4.2 STM32MP257 thermal measurements at $T_A = 25\text{ °C}$

The figures and table below detail the thermal measurements performed at $T_A = 25\text{ °C}$.

Figure 26. STM32MP257 thermal measurements at $T_A = 25\text{ °C}$

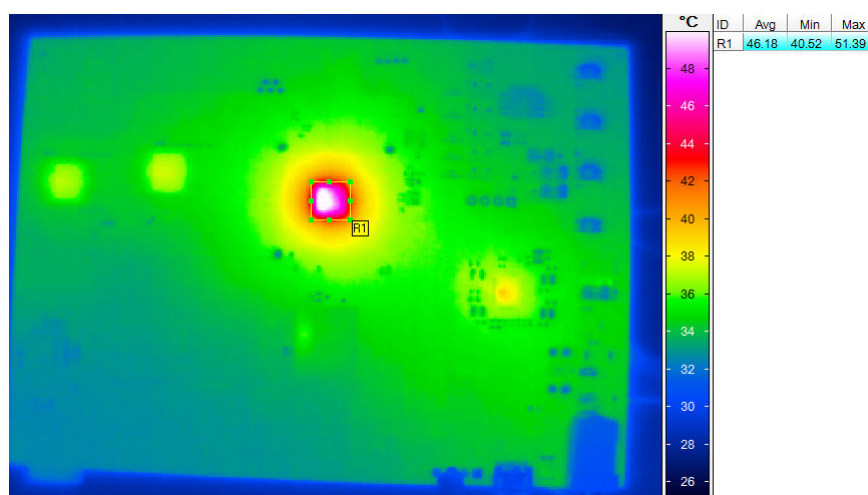
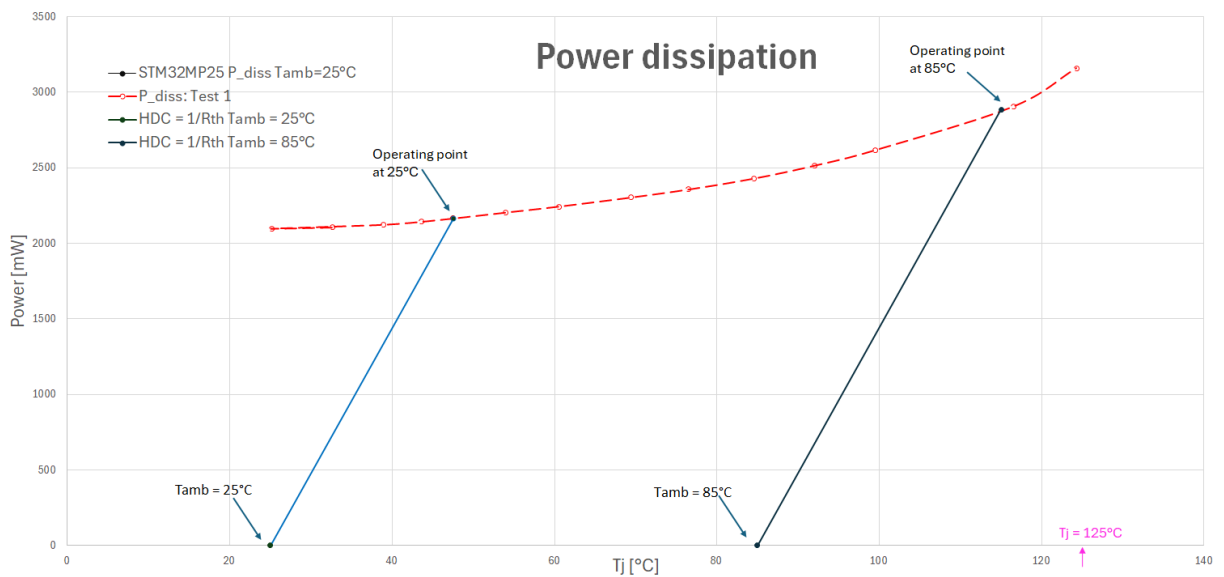


Table 18. STM32MP257 thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

T_J ($^{\circ}\text{C}$)	Thermal camera module measurement ($^{\circ}\text{C}$)			STM32MP257 power consumption (mW)
	Avg	Min	Max	
47.5 ⁽¹⁾	40.24	31.5	48.7	2164.77

1. Thermocouple measurement

Once the HDC of the design is defined (by measurement at $25\text{ }^{\circ}\text{C}$), and assuming that this HDC is constant at $25\text{ }^{\circ}\text{C}$ and $85\text{ }^{\circ}\text{C}$, the operating point of the design at $85\text{ }^{\circ}\text{C}$ is given by translating the HDC at $85\text{ }^{\circ}\text{C}$ as shown in Figure 27 and Table 19.

Figure 27. HDC at $85\text{ }^{\circ}\text{C}$ and junction temperature-dependent dissipated power for STM32MP257

Table 19. Measurement interpolation at $T_A = 85\text{ }^{\circ}\text{C}$ for STM32MP257

Parameter	Value
T_J	$115\text{ }^{\circ}\text{C}$
P_{TOT}	2886.5 mW

In conclusion, the STM32MP257 device is safe, with no thermal runaway, and T_J remaining $< 125\text{ }^{\circ}\text{C}$.

6.5 Discovery kit with STM32N657XOH3 MCU

This thermal analysis was done on a Discovery kit with an STM32N657XOH3 device without casing.

The test case is the following:

- Internal V_{DD_core}
- voshigh-trusted.bin configuration
- CPU frequency = 800 MHz
- NPU frequency = 1000 MHz
- NPU RAM frequency = 900 MHz

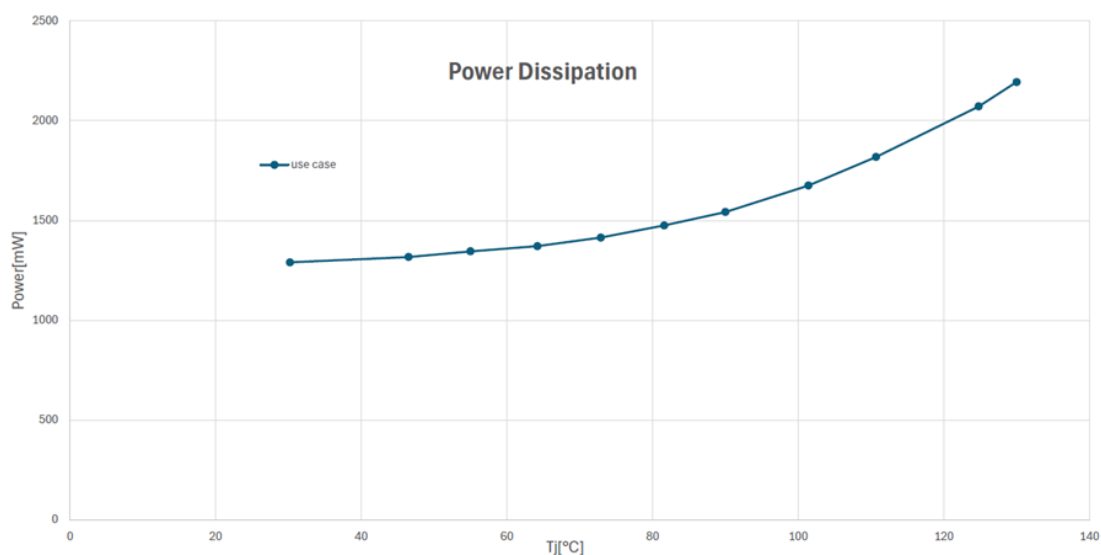
STM32N6 max load application firmware:

- Use DCMI and VENC in YUV2 (camera board MB1723C with OV5640 sensor)
- Use NPU inference
- Stream video on LTDC using GPUD2 accelerator

6.5.1 STM32N657 power dissipation

As stated in [Section 3](#), the dissipated power varies with T_J . The power consumption in this example is measured for different T_J values (as [Figure 28](#) below demonstrates).

Figure 28. Junction-temperature-dependent dissipated power for STM32N657



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6.5.2 STM32N657 thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

The figures and table below detail the thermal measurements performed at $T_A = 25\text{ }^{\circ}\text{C}$.

Figure 29. STM32N657 thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

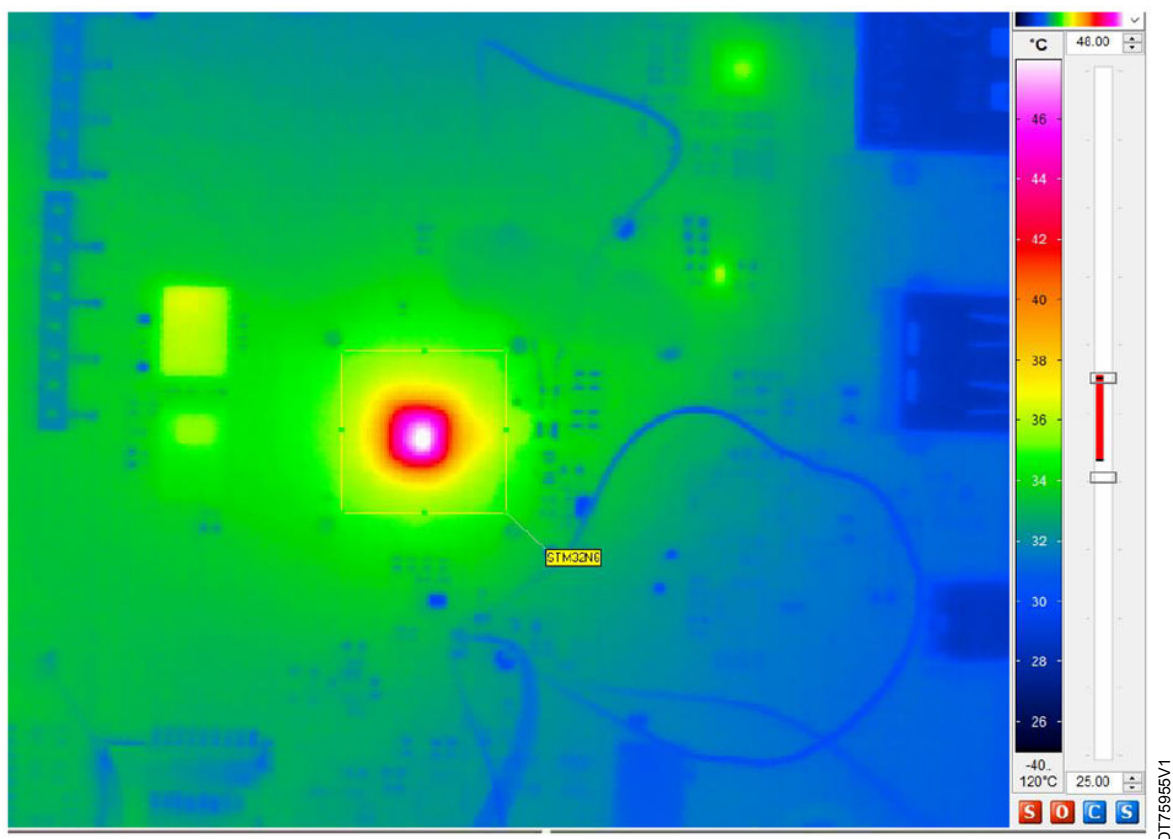
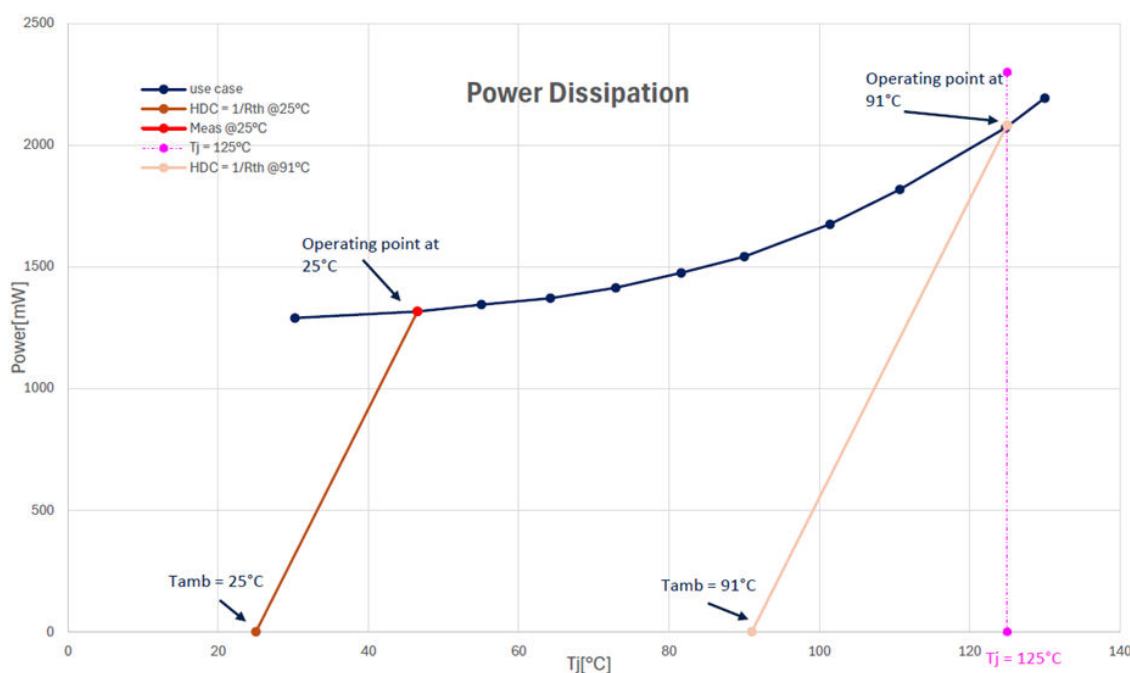


Table 20. STM32N657 thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

T_J ($^{\circ}\text{C}$)	Thermal camera module measurement ($^{\circ}\text{C}$) Max	STM32N657 power consumption (mW)
47 ⁽¹⁾	48.7	1318

1. Thermocouple measurement

Once the heat dissipation capability (HDC) of the design has been defined (by measurement at $25\text{ }^{\circ}\text{C}$), and assuming that this HDC is constant at $25\text{ }^{\circ}\text{C}$ and maximum ambient temperature, the operating point of the design at $T_J = 125\text{ }^{\circ}\text{C}$ is given by translating the HDC, as shown in the figure and table below.

Figure 30. HDC at $91\text{ }^{\circ}\text{C}$ and junction temperature-dependent dissipated power for STM32N657

Table 21. Measurement interpolation at maximum ambient temperature for STM32N657

Parameter	Value
T_J	$125\text{ }^{\circ}\text{C}$
P_{TOT}	2082 mW
Maximum ambient temperature	$91\text{ }^{\circ}\text{C}$

In conclusion, the STM32N657 device is safe, with no thermal runaway, and for $T_J = 125\text{ }^{\circ}\text{C}$, the maximum ambient temperature $T_A = 91\text{ }^{\circ}\text{C}$.

6.6 Internal validation board with STM32MP215F MPU

This thermal analysis was done on an internal validation board with an STM32MP215F device without casing.

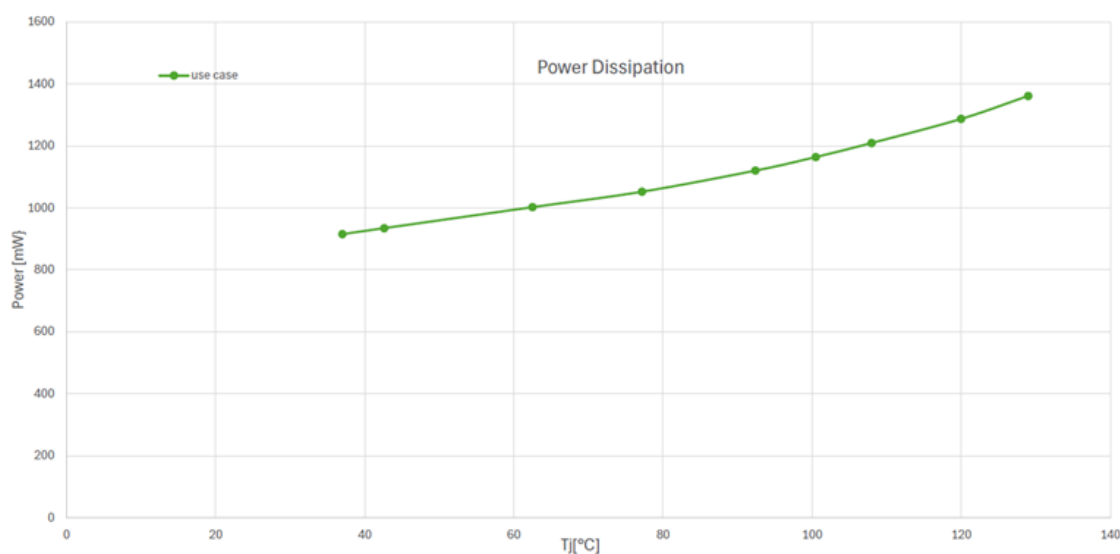
The test case is the following:

- Tests on hwrng
- Tests on DDR (memtester)
- Tests on DMA

6.6.1 STM32MP215F power dissipation

As stated in [Section 3](#), the dissipated power varies with T_J . The power consumption in this example is measured for different T_J values (as [Figure 31](#) below demonstrates).

Figure 31. Junction-temperature-dependent dissipated power for STM32MP215F



DT80404V1

6.6.2 STM32MP215F thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

This section explains the STM32 thermal parameters as specified by their respective datasheets. Figure and table below detail the thermal measurements performed at $T_A = 25\text{ }^{\circ}\text{C}$.

Figure 32. STM32MP215F thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

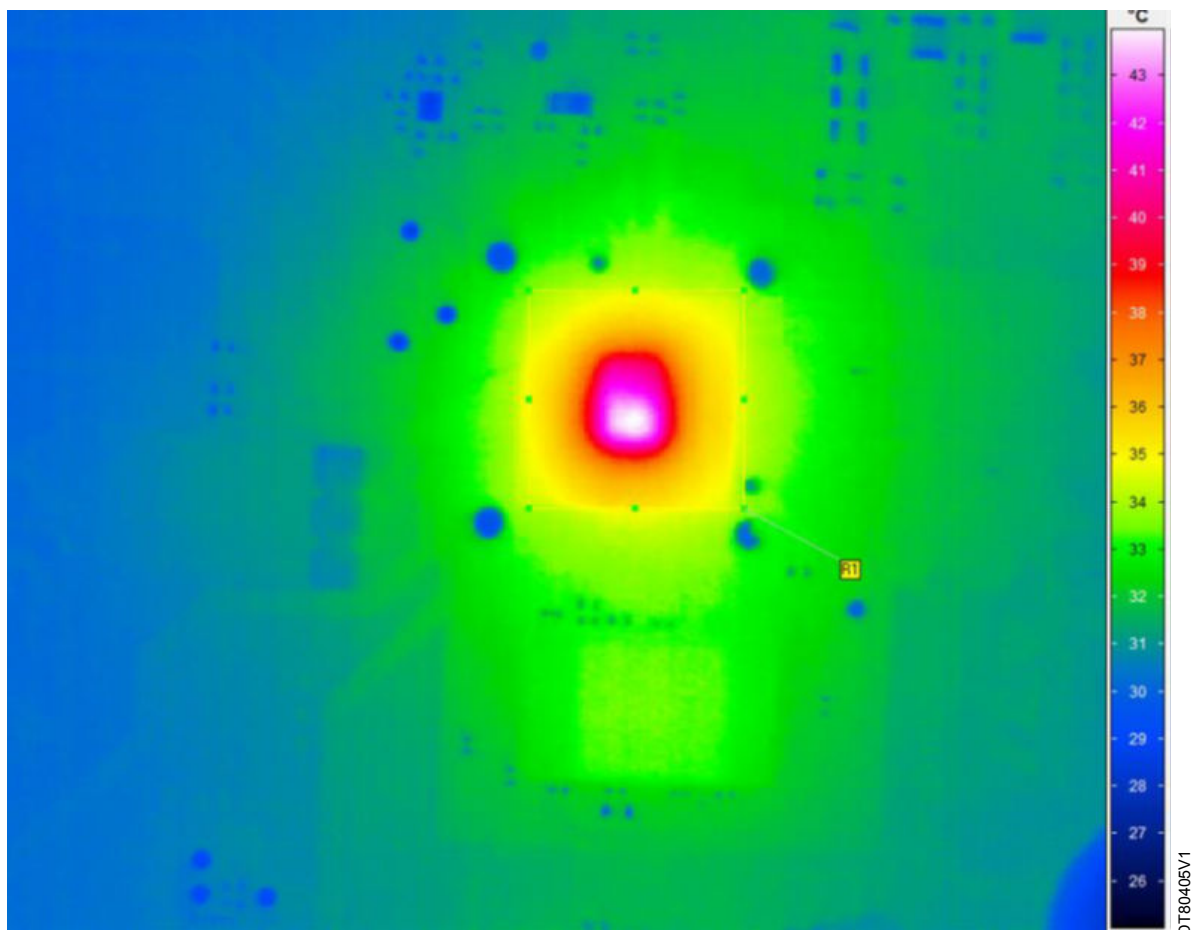


Table 22. STM32MP215F thermal measurements at $T_A = 25\text{ }^{\circ}\text{C}$

T_J ($^{\circ}\text{C}$)	IO		CPU		CORE		DDR		1V8		Power (mW)
43 ⁽¹⁾	V (V)	3.319	V (V)	0.935	V (V)	0.893	V (V)	1.239	V (V)	1.814	934.37
	I (mA)	40	I (mA)	160	I (mA)	315	I (mA)	226	I (mA)	50	

1. Thermocouple measurement

Figure and table hereafter detail the thermal measurements performed at maximum ambient temperature $T_A = 100\text{ }^{\circ}\text{C}$.

Figure 33. HDC at 100 °C and junction temperature-dependent dissipated power for STM32MP215F

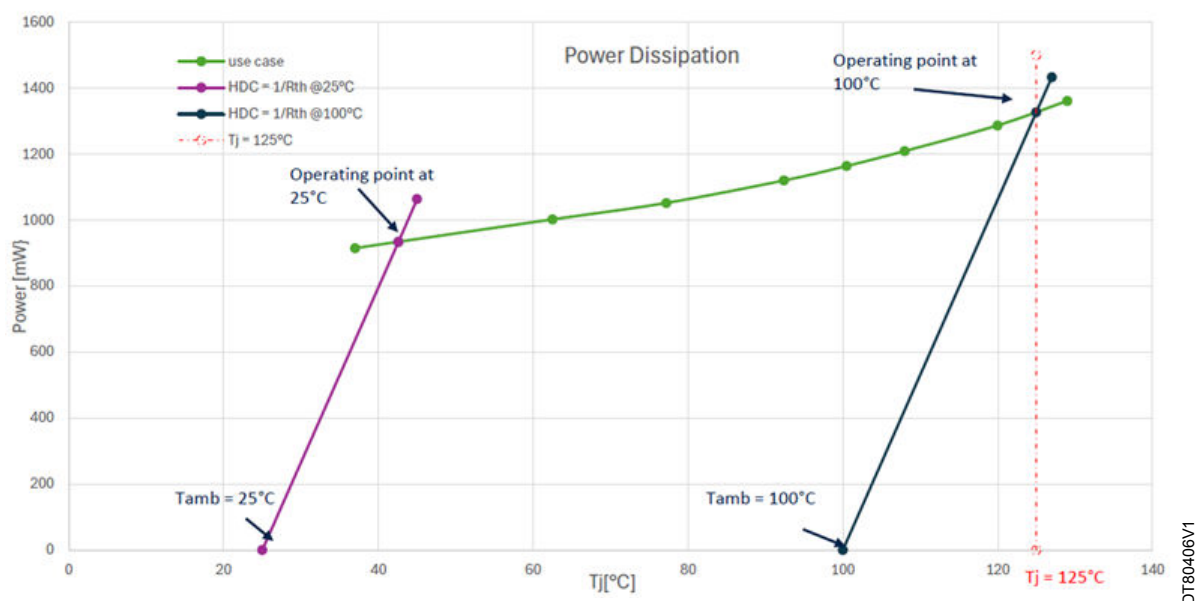


Table 23. Measurement interpolation at maximum ambient temperature for STM32MP215F

Parameter	Value
T_J	125 °C
P_{TOT}	1327 mW
Maximum ambient temperature	100 °C

In conclusion, the STM32MP215F device is safe, with no thermal runaway, and for $T_J = 125^\circ\text{C}$, the maximum ambient temperature $T_A = 100^\circ\text{C}$.

Revision history

Table 24. Document revision history

Date	Version	Changes
24-May-2018	1	Initial release.
4-Mar-2019	2	Updated: <ul style="list-style-type: none"> Title of the document Section 2.3 Thermal model of a chip carrier Section 3.3 Ambient temperature versus junction temperature Section 3.5 Board temperature Section 4 Power dissipation and cooling methods Added: <ul style="list-style-type: none"> Section 3.6 STM32 thermal parameters Section 6 Thermal analysis example
19-Apr-2019	3	Updated Section 3.6 STM32 thermal parameters. Added Section 6.2 Discovery kit with STM32H747XI MCU.
28-Feb-2023	4	Updated: <ul style="list-style-type: none"> Section orders between Section 6.1 and Section 6.2 Section 6.2 Evaluation board with STM32MP157 MPU Figure 3. HDC (heat dissipation capability) Added Section 6.3 Internal validation board with STM32MP135 MPU
11-Oct-2023	5	Updated: <ul style="list-style-type: none"> Document title Figure 20. Junction temperature-dependent dissipated power for STM32MP135 (cpuburn)
28-Jun-2024	6	Added Section 6.4: Internal validation board with STM32MP257 MPU
21-Nov-2024	7	Added Section 6.5: Discovery kit with STM32N657XOH3 MCU
19-Jan-2026	8	Updated document title Added Section 6.6: Internal validation board with STM32MP215F MPU

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