

**19 V - 90 W adapter based on the STCMB1,
combo TM PFC and HB LLC**

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Introduction

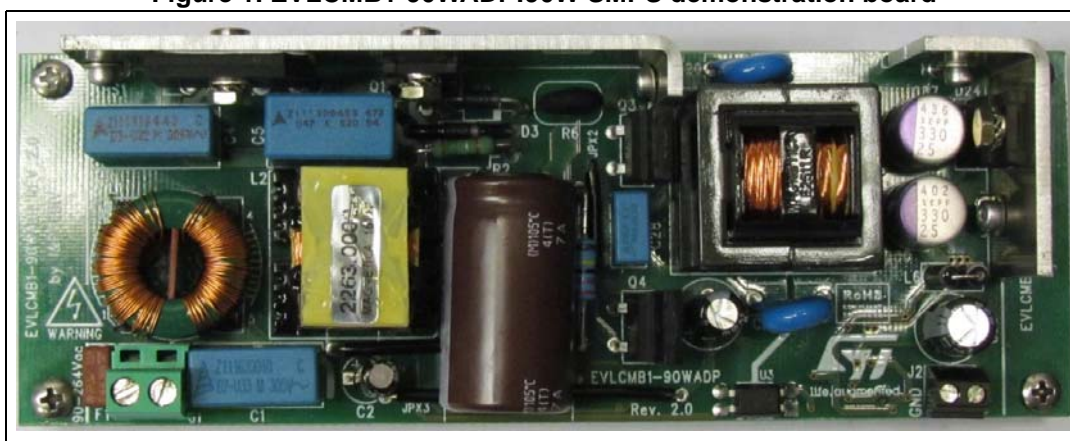
This application note describes the EVLCMB1-90WADP demonstration board, a 19 V - 90 W converter tailored for the typical specification of an AC/DC adapter for laptops and notebooks.

The architecture is based on a two-stage approach: a front-end transition mode PFC pre-regulator and a downstream LLC resonant half bridge converter.

The PFC and LLC controllers are both integrated in the STCMB1 combo integrated circuit that also integrates a high voltage start-up generator, an X-capacitor discharge circuit, the AC brownout/in function and a complete set of protections as detailed later on.

The PFC section of the STCMB1 uses a proprietary constant-on-time control methodology that does not require a sinusoidal input reference, thereby reducing the system cost and external component count. It also includes burst mode function that is independent on the LLC, cycle-by-cycle overcurrent protection on the whole input current, output overvoltage protection, latched feedback failure protection, boost inductor saturation and inrush current detection at both the start-up and after mains sags or missing cycles.

The LLC section of the STCMB1 is based on a proprietary time shift control method that improves dynamic behavior and input ripple rejection resulting in a cleaner output voltage. It includes the adaptive dead time function, burst mode function that masters on PFC, proprietary safe-start procedure, hard-switch protection, anti-capacitive protection, two-level cycle-by-cycle overcurrent protection with the automatic restart, DC brownout protection.

Figure 1. EVLCMB1-90WADP:90W SMPS demonstration board

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1 Main characteristics, adapter architecture and controller description

In this section, the main characteristics and the adapter architecture are summarized. Moreover, a brief description is given of the STCMB1, the controller on which the EVLCMB1-90WADP device is based. Main features of the EVLCMB1-90WADP are listed in [Table 1](#):

Table 1. Main features of EVLCMB1-90WADP

Parameter	Value
Input mains range	90 to 264 Vac - frequency 45 to 65 Hz
Output voltage	19 V at 4.75 A, continuous operation
Full load efficiency	> 90% at 115 Vac
Avg. efficiency (at 25, 50, 75, 100% of full load)	> 90% at 115 Vac
Efficiency (at 250 mW)	> 60% at 230 Vac
No load mains consumption	< 90 mW
Mains harmonics according to	EN61000-3-2 Class-D and JEITA-MITI Class-D
EMI	According to EN55022 Class-B
Safety	According to EN60950
Dimensions	52 x 130 mm, height = 27 mm
PCB	Double side, 70 μ m, FR-4, mixed PTH/SMT

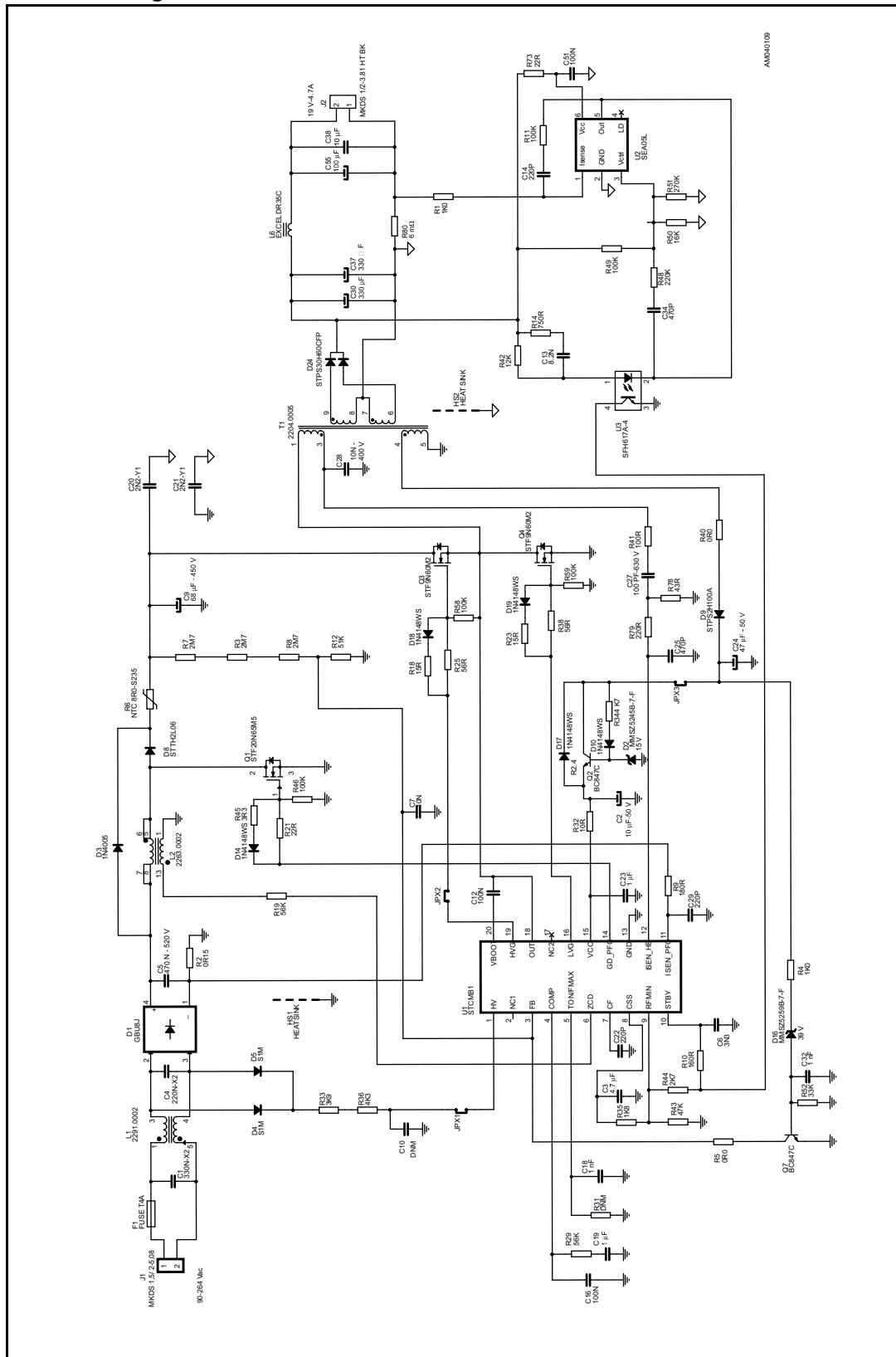
The EVLCMB1-90WADP is a two-stage adapter: a front-end transition mode PFC pre-regulator and a downstream LLC resonant half bridge converter, both controlled by the STCMB1 combo IC. The PFC section of the STCMB1 is a proprietary constant-on-time PFC controller operating in transition mode. The LLC section of the STCMB1 integrates all the functions necessary to operate the resonant converter with the 50% duty cycle and variable working frequency, based on a proprietary time shift control method. At the secondary side, asynchronous rectification is done by the center tap transformer and two diodes in the same package. The control loop is based on the SEA05L: the CV loop is active up to about 7 A then the CC loop starts to limit the output current while the output voltage decreases.

The STCMB1 device also integrates a comprehensive set of features that allows the design of a robust and safe SMPS, for both the final user and the supplied system, while keeping a reduced external component count. Such features are the high voltage start-up generator, X-capacitor discharge circuit, AC and DC brownout/in functions, cycle-by-cycle overcurrent protections on the whole boost inductor current and on the resonant tank current, the latched feedback failure protection, boost inductor saturation and inrush current detection.

In order to reach very low power consumption at the light loads, burst mode management functions are also embedded in the STCMB1. The PFC section can enter in the burst load driven by its feedback signal and independently on the LLC: this is especially useful when the adapter operates in the high mains range with the moderate output load. The system level burst mode is mastered by the LLC section when the output load becomes very low. In this case, the STCMB1 enters in an idle state driven by the decreasing feedback signal (from the secondary side to the primary side, through the optocoupler) below a threshold. As

the feedback signal rises again above the threshold plus a hysteresis, the STCMB1 exits the idle state and switching restarts. In this way, negative feedback is of course maintained, but the control changes from continuous to discrete. Last but not least, the system level burst mode includes a proprietary IP that allows minimizing the number of cycles in the burst packet and so minimizing the switching losses. Details about the burst mode management are given in [Section 5.3 on page 19](#) and [Section 5.4 on page 20](#) and in the datasheet of the STCMB1 device. The schematic of the EVLCMB1-90WADP is shown in [Figure 2](#).

Figure 2. EVLCMB1-90WADP demonstration board schematic



2 Efficiency measurements

2.1 Overall efficiency

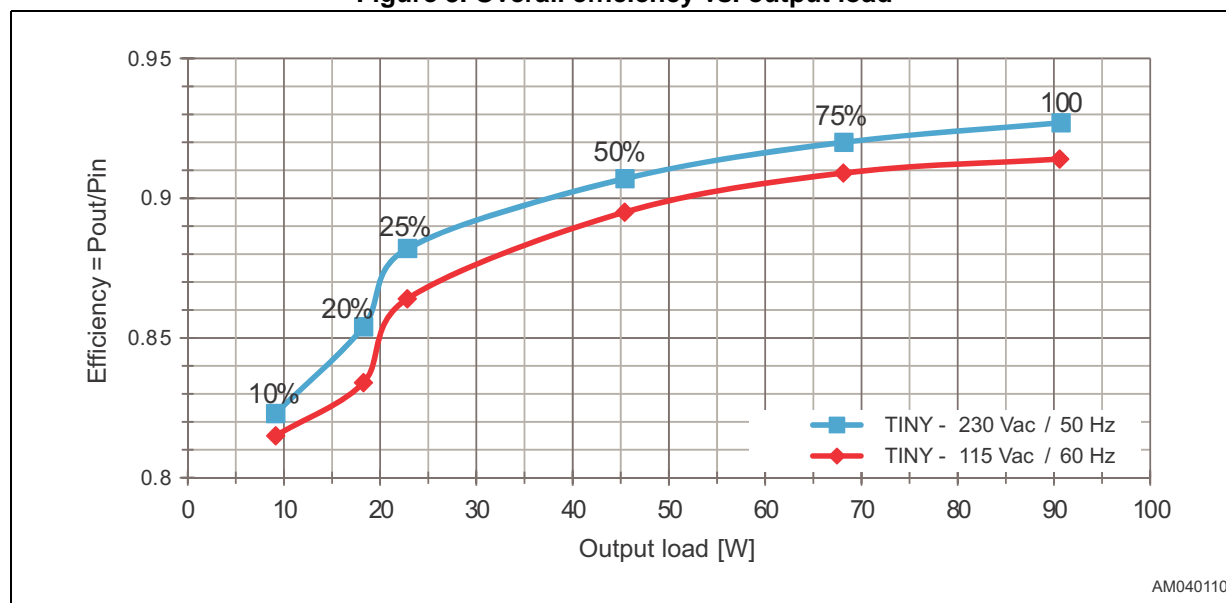
[Table 2](#) and [Figure 3](#) show the overall efficiency of the EVLCMB1-90WADP demonstration board, measured at the nominal mains voltages, after a warm up time of about 20 min. at each measurement point.

Conversely, consumption at the open load has been measured by energy integration over 6 min., after a short warm up time, always in the open load, and removing all probes from the board during the tests.

Table 2. Overall efficiency

Output load	230 Vac / 50 Hz					115 Vac / 60 Hz				
	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η (Pout/Pin)	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η (Pout/Pin)
Open load	19.04	-	-	0.085	-	19.04	-	-	0.075	-
10%	19.04	0.48	9.14	11.1	0.823	19.03	0.48	9.13	11.2	0.815
20%	19.03	0.96	18.27	21.4	0.854	19.02	0.96	18.26	21.9	0.834
25%	19.03	1.2	22.84	25.9	0.882	19.01	1.2	22.81	26.4	0.864
50%	19.01	2.39	45.43	50.1	0.907	18.99	2.39	45.39	50.7	0.895
75%	18.99	3.59	68.17	74.1	0.92	18.97	3.59	68.1	74.9	0.909
100%	18.98	4.78	90.72	97.9	0.927	18.95	4.78	90.58	99.1	0.914

Figure 3. Overall efficiency vs. output load



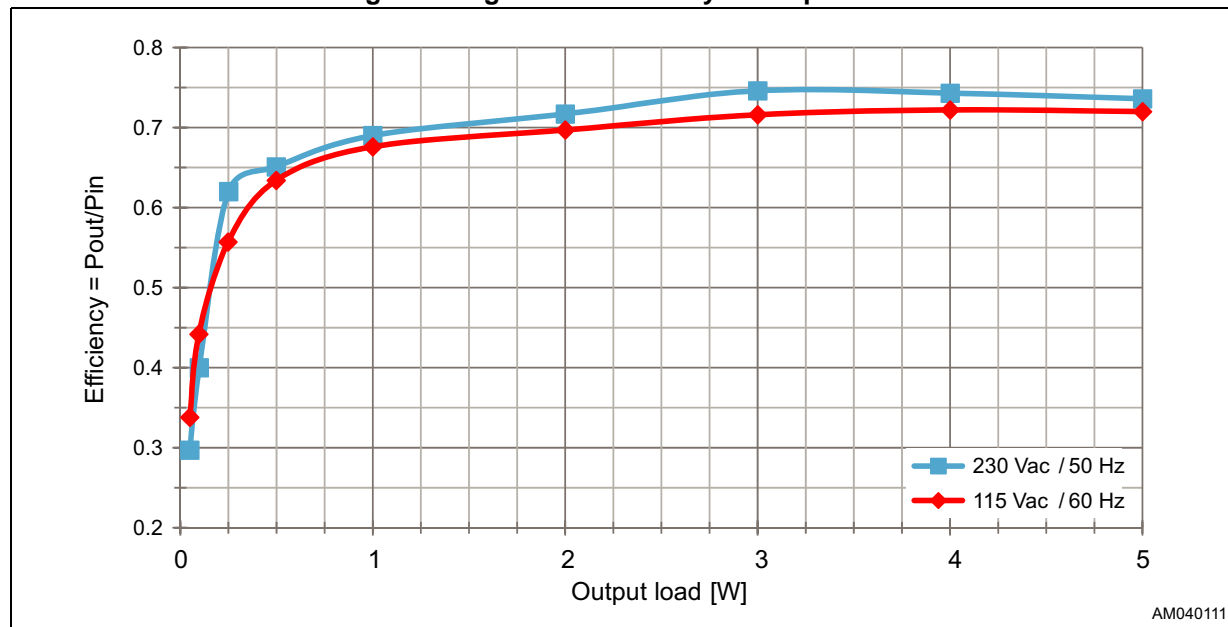
2.2 Efficiency at light load operation

Computer power supplies must now meet higher efficiency limits than in the past even at the light load because the maximum power consumption during the computer standby and off mode has decreased. Measurement results are reported in [Table 3](#) and [Figure 4](#).

Table 3. Light load efficiency

Load [W]	115 Vac / 60 Hz					230 Vac / 50 Hz				
	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η
0.05	19.05	0.003	0.049	0.145	0.338	19.05	0.003	0.049	0.165	0.297
0.10	19.05	0.005	0.096	0.217	0.442	19.05	0.005	0.098	0.245	0.4
0.25	19.05	0.013	0.248	0.445	0.557	19.05	0.013	0.251	0.405	0.62
0.50	19.05	0.026	0.498	0.785	0.634	19.05	0.026	0.498	0.765	0.651
1.0	19.05	0.052	1	1.48	0.676	19.05	0.052	1	1.45	0.69
2.0	19.05	0.105	2	2.87	0.697	19.05	0.105	2	2.79	0.717
3.0	19.05	0.157	3	4.19	0.716	19.05	0.157	3	4.02	0.746
4.0	19.04	0.210	4	5.54	0.722	19.04	0.210	4	5.38	0.743
5.0	19.04	0.263	5	6.94	0.72	19.04	0.263	5	6.79	0.736

Figure 4. Light load efficiency vs output load



The measurement procedure is described hereinafter:

Measurement procedure

1. The board under the test is supplied by an AC source and it is loaded by an active load set in the CP mode with VOUT sensing. The input power and voltage are measured by a power meter while the output power and voltage are read on the active load display.
2. At light loads, the input current is relatively small and the contribution of the current absorbed by the power meter could be not negligible. To overcome its impact, the current measurement circuit is toward the board under the test, while the voltage measurement circuit is toward the AC source.
3. Moreover, at light loads, the current drawn by the board under the test from the AC source is irregular and its measurement is typically unstable. To overcome this issue, the active energy consumption is measured, in mWh, by integration over 36 s and the corresponding input power is computed as energy by time. Because of the integration time, mW are simply $\text{mWh} \times 100$.
4. In order to control the proper operation of the adapter during the test, a high voltage oscilloscope probe is connected to the HB node. Each measurement point is kept for about 10 min., hence the values are taken. Loads have been applied increasing the output power from minimum to maximum. The output current is computed as the output power divided by the output voltage.

3 Eco-design requirement verification

From [Table 4](#) to [Table 6](#) the compliance of the regulation requirements for Eco-design of the EVLCMB1-90WADP is shown.

Table 4. ENERGY STAR® requirements for computers ver. 6.1

ENERGY STAR for computers ver. 6.1	Test results		Limits	Status
	230 Vac / 50 Hz	115 Vac / 60 Hz		
Efficiency at 20% load	85.4%	83.4%	> 82%	Pass
Efficiency at 50% load	90.7%	89.5%	> 85%	
Efficiency at 100% load	92.7%	91.4%	> 82%	
Power factor at 100% load	0.973	0.993	> 0.9	

Table 5. EuP Lot 6 Tier 2 requirements for household and office equipment

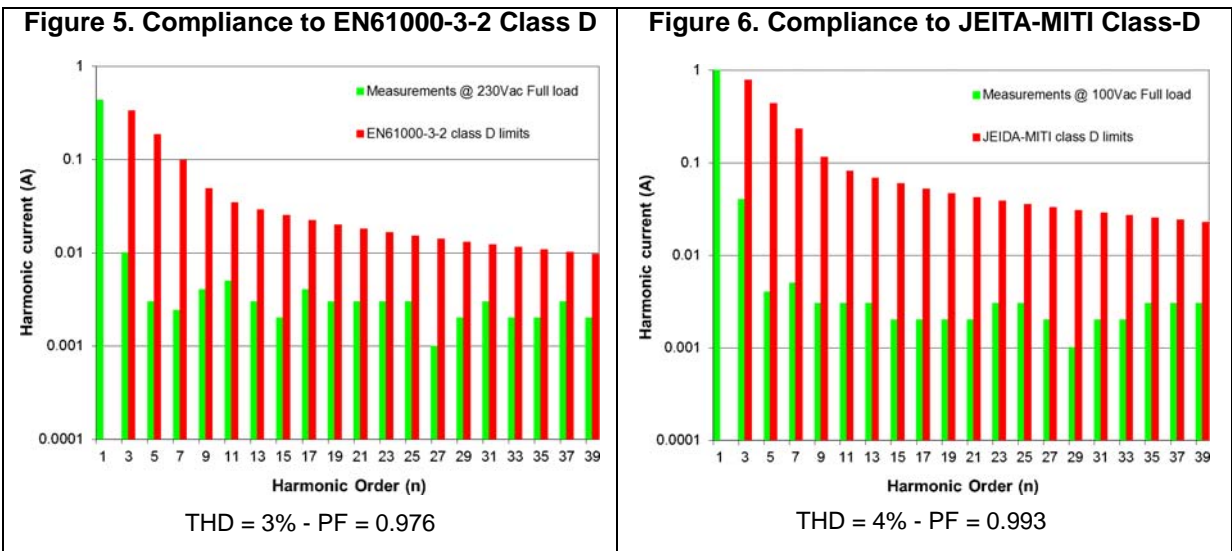
EuP Lot 6 Tier 2	Test results		Limits	Status
	230 Vac / 50 Hz	115 Vac / 60 Hz		
Avg. efficiency measured at 25, 50, 75, 100%	91%	90%	> 87%	Pass
Efficiency at 250 mW load	62%	55.7%	> 50%	
Efficiency at 100 mW load	40%	44.2%	> 33%	

Table 6. European CoC ver. 5 Tier 2 requirements for external power supplies

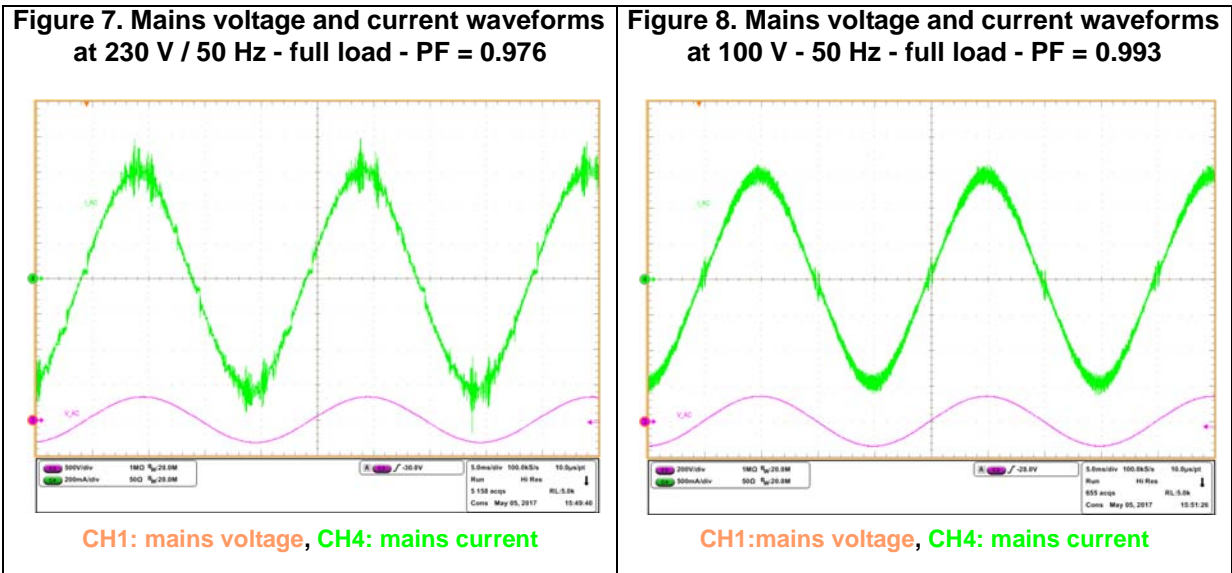
European CoC ver. 5 Tier-2 for ext. pow. sup.	Test results		Limits	Status
	230 Vac / 50 Hz	115 Vac / 60 Hz		
Avg. efficiency measured at 25, 50, 75, 100%	91%	90%	> 89%	Pass
Efficiency at 10% load	82.3%	81.5%	> 79%	
No load input power [W]	0.085	0.075	< 0.15 W	

4 Harmonic content measurement

The board has been tested in accordance with the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI Class-D, at the nominal input voltage mains. Results are reported in [Figure 5](#) and [Figure 6](#).



As an evidence of the way the PFC properly works, the input mains current is shown with the corresponding mains input voltage in [Figure 7](#) and [Figure 8](#).

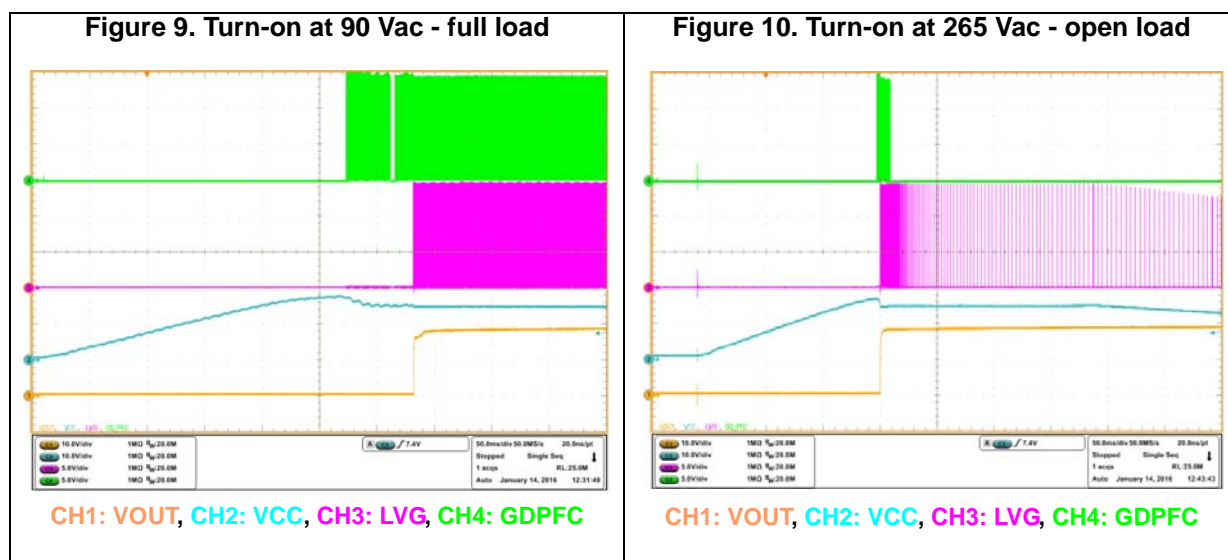


5 Functional check

5.1 PCB turn-on and LLC start-up

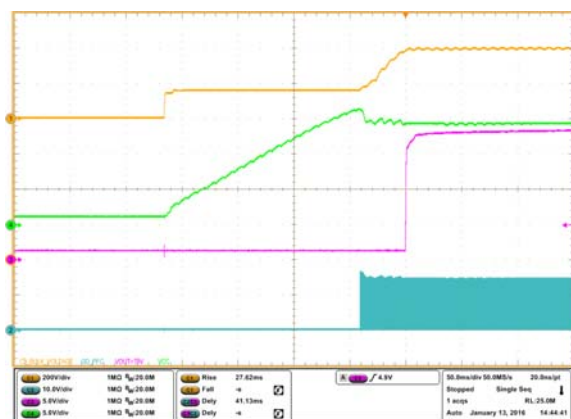
As the mains voltage, in the operating range, is applied to the EVLCMB1-90WADP, the high voltage start-up (HVSU) generator of the STCMB1 brings the VCC pin to the VCCon threshold at which the PFC starts working. The output voltage of the PFC (VPFC on C9) increases up to the enabling voltage of the LLC that is about 380 V (corresponding to the FB_E threshold on the FB pin). As the LLC starts switching, VOUT begins to increase and the self-supply circuitry based on the auxiliary winding of the LLC transformer takes over the HVSU generator.

Figure 9 and *Figure 10* show PFC and LLC driving signals with VOUT and VCC, when the EVLCMB1-90WADP is turned on at the limits of the input voltage range and with the full / open load.



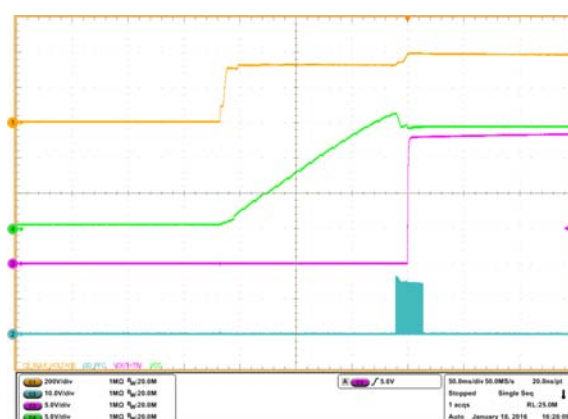
In a similar way, *Figure 11* and *Figure 12* show the PFC driving signal with VPFC and again VOUT and VCC, when the EVLCMB1-90WADP is turned on at nominal input voltages and with the full / open load.

Figure 11. Turn-on at 115 Vac - full load



CH1: VPFC, CH2: GDPFC, CH3: VOUT, CH4: VCC

Figure 12. Turn-on at 230 Vac - open load

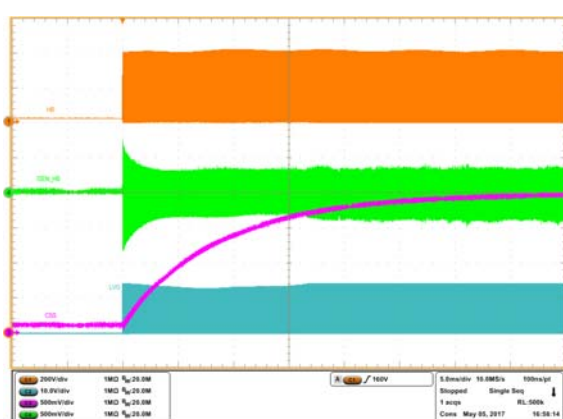


CH1: VPFC, CH2: GDPFC, CH3: VOUT, CH4: VCC

It is worth to highlight an important peculiarity of the resonant converter start-up that comes from the time shift control methodology implemented in the LLC section of the STCMB1 and that makes the implementation of a proprietary hard switching prevention function straightforward. In other words, on one side, a transition of the half bridge is allowed only when the resonant tank current has properly reversed; on the other side, in the time shift control, being the oscillator ramps synchronous with the zero crossings of the resonant tank current, a ramp in a half cycle starts only after the resonant tank current has reversed in that half cycle. So, the proprietary hard switch prevention method is naturally integrated in the time shift control. As a result, the duty cycle of the initial cycles is less than 50% until the DC voltage across the resonant capacitor reaches $VPFC/2$ which eliminates the typical initial $V \cdot s$ start-up imbalance and ensures soft switching.

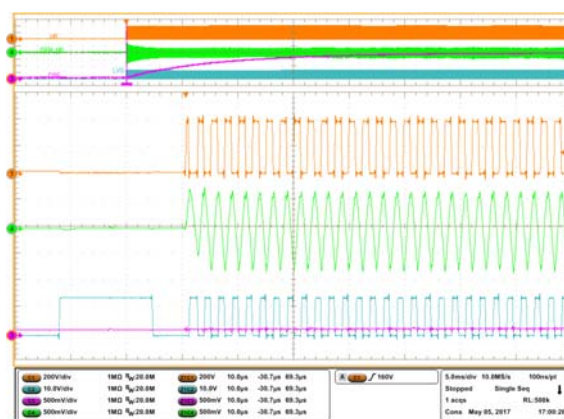
Furthermore, the traditional soft-start mechanism based on the frequency shift through the charge of a capacitor connected to the CSS pin, is implemented as well. A typical LLC start-up as driven by the STCMB1 is shown in [Figure 13](#) and [Figure 14](#).

Figure 13. LLC start-up at 115 Vac - full load



CH1: HB, CH2: LVG, CH3: CSS, CH4: ISEN_HB

Figure 14. Detail of first LLC cycles



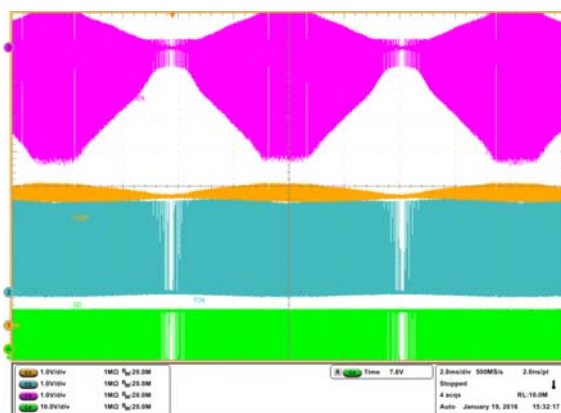
CH1: HB, CH2: LVG, CH3: CSS, CH4: ISEN_HB

5.2 Steady-state operation at heavy loads (PFC and LLC in continuous switching)

At heavy loads, both stages of the adapter work in continuous switching to deliver the required power from the mains to the load. Some waveforms relevant to the steady-state operation of the EVLCMB1-90WADP in continuous switching are shown from [Figure 15](#) to [Figure 18](#).

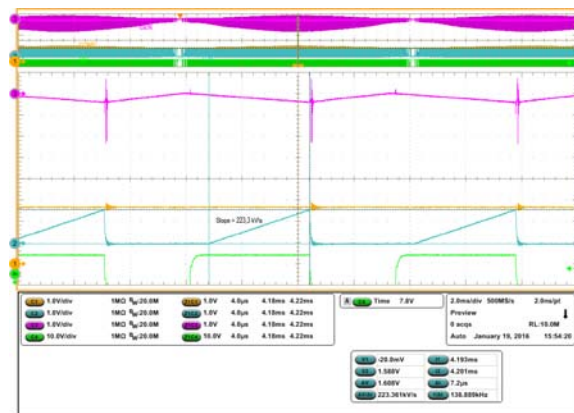
For the PFC stage, note that the whole input current is sensed through the resistor (R2) placed on the return path to the negative pin of the bridge rectifier and that the comparison between TON ramps and the COMP signal is exactly at COMP-1V. The charge current ITON is used to implement discrete voltage feed forward compensation: in the high mains range is about four times than in the low mains range.

Figure 15. PFC at 90 Vac - full load



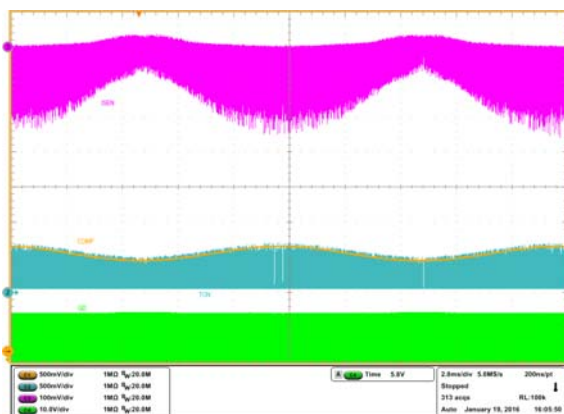
CH1: COMP, CH2: TON, CH3: ISEN_PFC, CH4: GDPFC

Figure 16. PFC at 115 Vac - full load (detail)



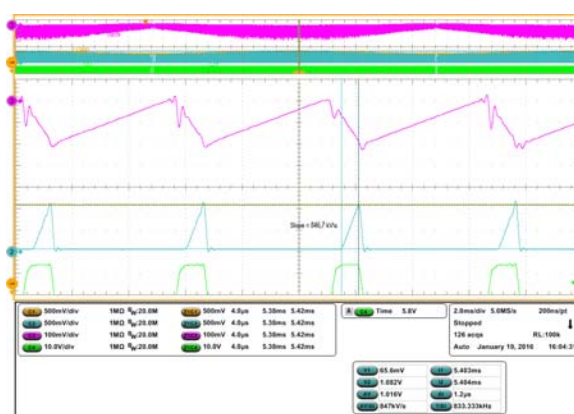
CH1: COMP, CH2: TON, CH3: ISEN_PFC, CH4: GDPFC

Figure 17. PFC at 265 Vac - full load



CH1: COMP, CH2: TON, CH3: ISEN_PFC, CH4: GDPFC

Figure 18. PFC at 230 Vac - full load (detail)



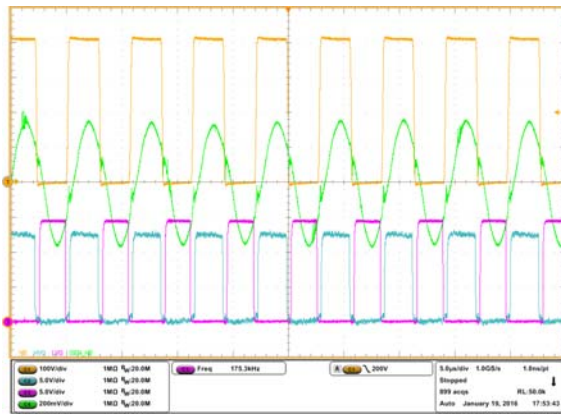
CH1: COMP, CH2: TON, CH3: ISEN_PFC, CH4: GDPFC

For the LLC stage, at the full load, the oscillator and driving signals and the half bridge node are shown with the resonant tank current as the voltage at the ISEN_HB pin. As visible, the switching frequency is about 170 kHz to have a good compromise among the magnetic components size and the converter efficiency.

In [Figure 21](#) and [Figure 22](#) we can see the rise and fall times of the half bridge node. We can note that they are quite similar, providing for similar dead times, thanks to the transformer good symmetry of construction of the secondary windings.

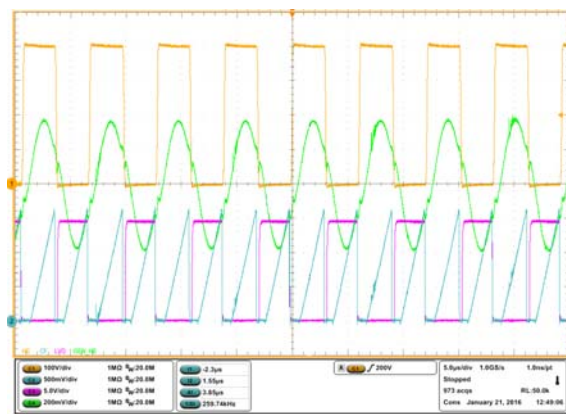
This last is an important point to check; actually good symmetry of the primary side waveforms assures the symmetry of the operation by the secondary windings, avoiding unexpected unbalance of the secondary currents conduction in each winding of the center tap during each half cycle.

Figure 19. LLC signals at full load



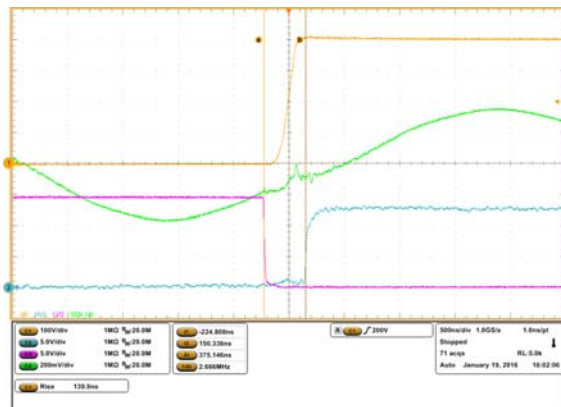
CH1: HB, CH2: HVG, CH3: LVG, CH4: ISEN_HB

Figure 20. LLC signals at full load (CF)



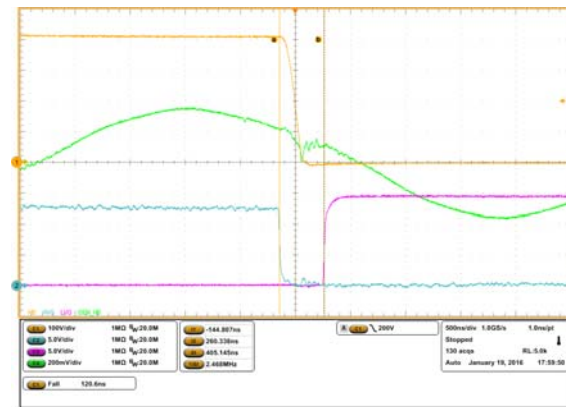
CH1: HB, CH2: CF, CH3: LVG, CH4: ISEN_HB

Figure 21. HB rising edge at full load



CH1: HB, CH2: HVG, CH3: LVG, CH4: ISEN_HB

Figure 22. HB falling edge at full load



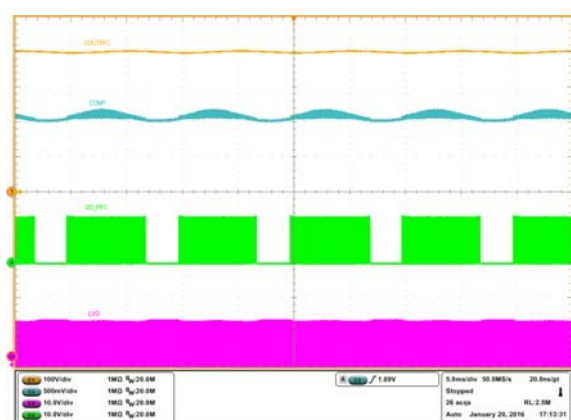
CH1: HB, CH2: HVG, CH3: LVG, CH4: ISEN_HB

5.3 Steady-state operation at moderate loads (PFC in burst mode, LLC in continuous switching)

When working at the moderate output loads, to prevent an unwanted rising of the PFC output voltage and the consequent activation off the PFC OVP, especially during the operation at the higher mains range, the PFC stage can work in its own burst mode, while the LLC stage is still working in continuous switching. The PFC gate driver is stopped as the COMP pin voltage falls across 1 V, while the LLC may proceed in its own operation in continuous switching. PFC switching restarts as COMP rises across 1 V; a small hysteresis (20 mV) is provided to avoid bouncing.

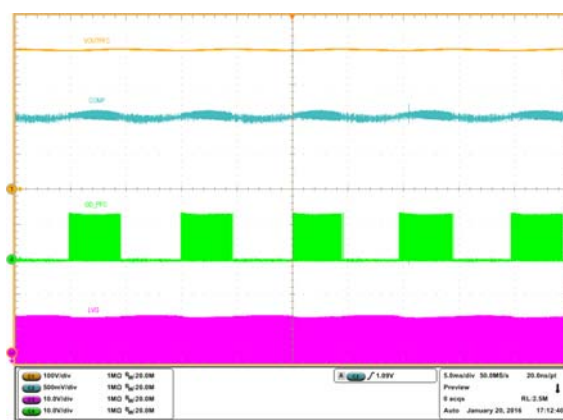
Some waveforms relevant to the steady-state operation of the EVLCMB1-90WADP in this condition are shown in [Figure 23](#) and [Figure 24](#).

Figure 23. PFC in burst mode, 230 Vac - 2 A



CH1: VPFC, CH2: COMP, CH3: LVG, CH4: GDPFC

Figure 24. PFC in burst mode, 230 Vac - 1 A



CH1: VPFC, CH2: COMP, CH3: LVG, CH4: GDPFC

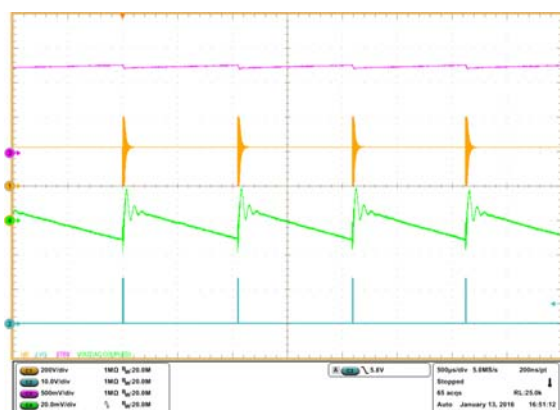
This operating mode (PFC in burst mode and LLC in continuous switching) can take place until the output load level is higher than the LLC burst mode set point (programmed by the RFmax resistor) or in case the burst mode by the LLC is inhibited by connecting the STBY pin to the RFmin pin. If the load decreases below the LLC burst mode set point the LLC begins working in the burst mode too and it takes over the burst mode of both converters that work synchronized, as described in [Section 5.4](#).

5.4 Steady-state operation at light loads (burst mode operation)

At light loads, the LLC stage works in the burst mode and it is the master on the PFC stage: when STBY falls across 1.25 V because of the light load, LLC switching is stopped as soon as the HVG pulse is completed; then, the control loop, through the error amplifier and the optocoupler, makes STBY increasing; LLC switching is restarted as STBY rises across 1.25 V plus its hysteresis (40 mV). Note that the first cycle after restarting is shortened to minimize the initial high current peak in the transformer.

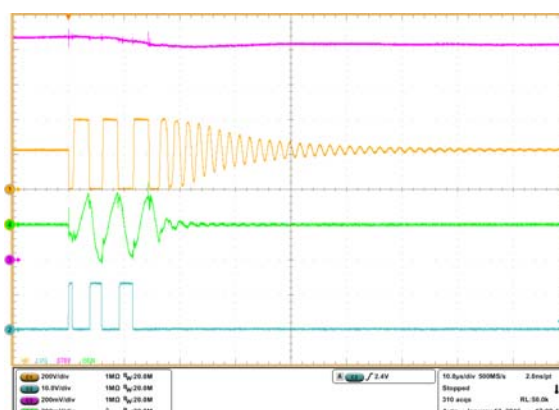
The detailed waveforms of the EVLCMB1-90WADP at light loads are shown in [Figure 25](#) and [Figure 26](#). During the burst mode operation, the VOUT variation is less than 40 mV.

Figure 25. Pout = 250 mW (90 Vac)



CH1: HB, CH2: LVG, CH3: STBY, CH4: VOUT (AC coupling)

Figure 26. Detail with ISEN_HB



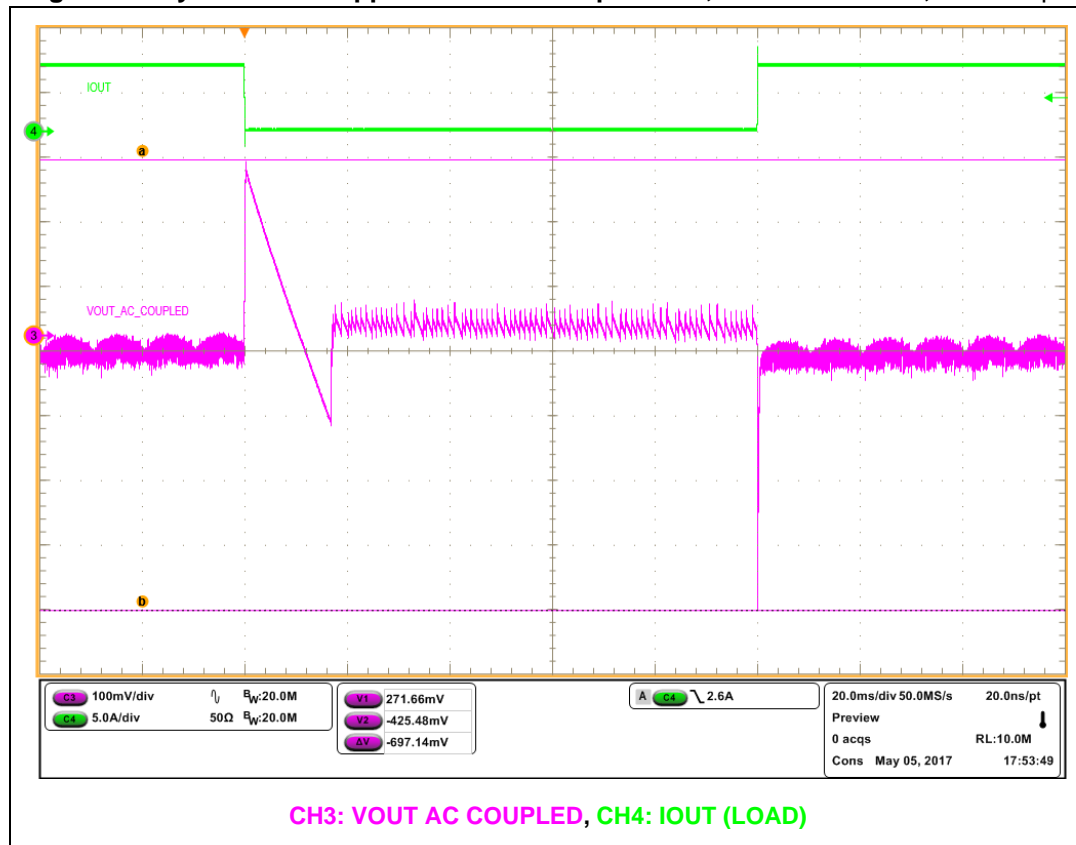
CH1: HB, CH2: LVG, CH3: STBY, CH4: ISEN_HB

5.5 Dynamic load and control loop response

Here, a dynamic load, full to open, has been applied to the EVLCMB1-90WADP: the output voltage variation is about -430 mV / +270 mV, at load step-up / down, respectively. The undershoot at load step-up can be reduced of about 100 mV by short-circuiting the output bead.

The loop response is qualitatively good: the output voltage deviation is limited to about 2%. The response is also clean and monotonic, without oscillations, indicating the appropriate margin phase of the regulation loop.

Figure 27. Dynamic load applied - full load / open load, 100 ms / 100 ms, 800 mA/μs



5.6 Overcurrent management

The EVLCMB1-90WADP is also equipped with the CC loop that takes control when the output load is about 150% of the full load. When the CC loop takes control, as the load is further increased, the output current is kept constant while VOUT falls down. The output load at which the control changes from CV to CC is set by a resistor (R80) at the secondary side that senses the whole return current.

From the controller viewpoint, in the STCMB1, overcurrent management is based on the resonant tank current sensing on the ISEN_HB pin and, for the proper operation, the instantaneous current has to be sensed: this means that the recommended RC filter nearby the ISEN_HB pin should have time constant limited to few hundreds nanoseconds, to avoid too much delay between the sensed signal on the R78 and the signal at the ISEN_HB pin.

When longer time constants are used, it is recommended to carefully verify the converter behavior close to the capacitive mode boundary and when the short-circuit is applied.

Two overcurrent thresholds can be triggered at the ISEN_HB pin: OCP1 (0.8 V) and OCP2 (1.5 V). The first level protection activates a frequency shift based mechanism and, in some cases, an internal overload protection based on digital counters. The second level protection is for the immediate stop of the converter.

5.6.1 Constant current (CC) loop

The EVLCMB1-90WADP is also equipped with the CC loop that takes control when the output load is about 150% of the full load. The output load at which the control changes from CV to CC is set by a resistor (R80) at the secondary side that senses the whole return current.

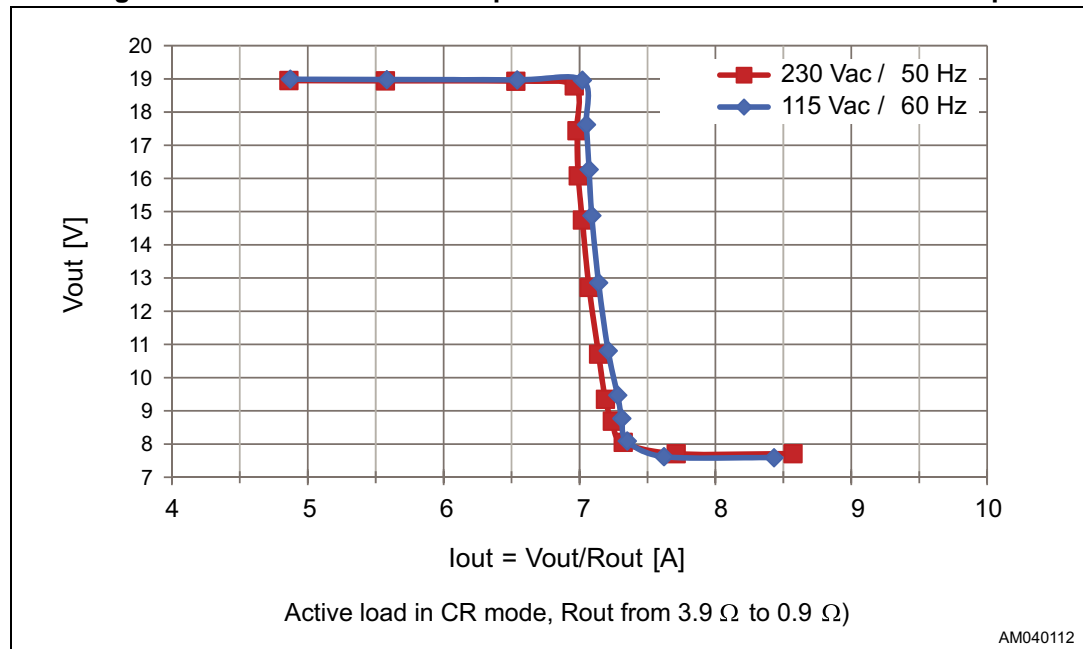
With $R_{80} = 6 \text{ m}\Omega$, a handshake between CV and CC loops begins at about 6.5 A and becomes effective at about 7.0 A. Note that, in order to properly test the CC loop, the active load has to be set in the CR mode rather than in the CC mode; this to avoid the conflict by the board CC loop and the active load constant current operation.

Once the CC loop is active, further reduction of R_{out} , results in V_{OUT} decreasing while the output current is kept constant. However, when V_{OUT} is about 7/8 V, the CC loop cannot regulate anymore since the error amplifier has used up its dynamic.

Also note that, during CC loop control, at low mains voltage ($\leq 115 \text{ Vac}$), the PFC can lose regulation due to the operation of current limiting (OCP of PFC). In this case, V_{PFC} can go down to 320 V ($> 280 \text{ V} = \text{DC brownout}$), but the overall behavior is as described above.

Figure 28 shows the typical I_{OUT} vs V_{OUT} diagram when the CC loop is active.

Figure 28. EVLCMB1-90WADP operation in constant current control loop



5.6.2 First level OCP

If the signal at the ISEN_HB pin exceeds 0.8 V (OCP1 threshold), then the soft-start capacitor CSS (C3) is discharged for 5 μ s and, as a consequence, the oscillator frequency quickly increases; correspondingly, the resonant peak current and therefore the signal at the ISEN_HB pin decreases. This mechanism limits the energy transfer to the output and occurs each time the OCP1 threshold is triggered.

Under the overload or output short-circuit condition, this overcurrent protection results in a peak primary current that periodically oscillates around the maximum value allowed by the sense resistor (R78) and is effective in limiting the primary-to-secondary energy flow in case of the overload or a “soft” output short-circuit.

However, this frequency shift based mechanism cannot last indefinitely because it could jeopardize the safety of the adapter. So, in order to prevent any damage, the operation during the overload, as described above, has limited duration; afterward, the adapter is forced to work intermittently (hiccup mode), which brings the average output current to values such that the thermal stress is within safe limits.

Internal overload protection is described in the datasheet of the STCMB1 device. Only note that the actual duration of the allowed overload depends on the occurrence of the OCP1 events, therefore on CSS, RSS and characteristics of the resonant circuit and the short-circuit impedance. Its value is usually few tens of milliseconds.

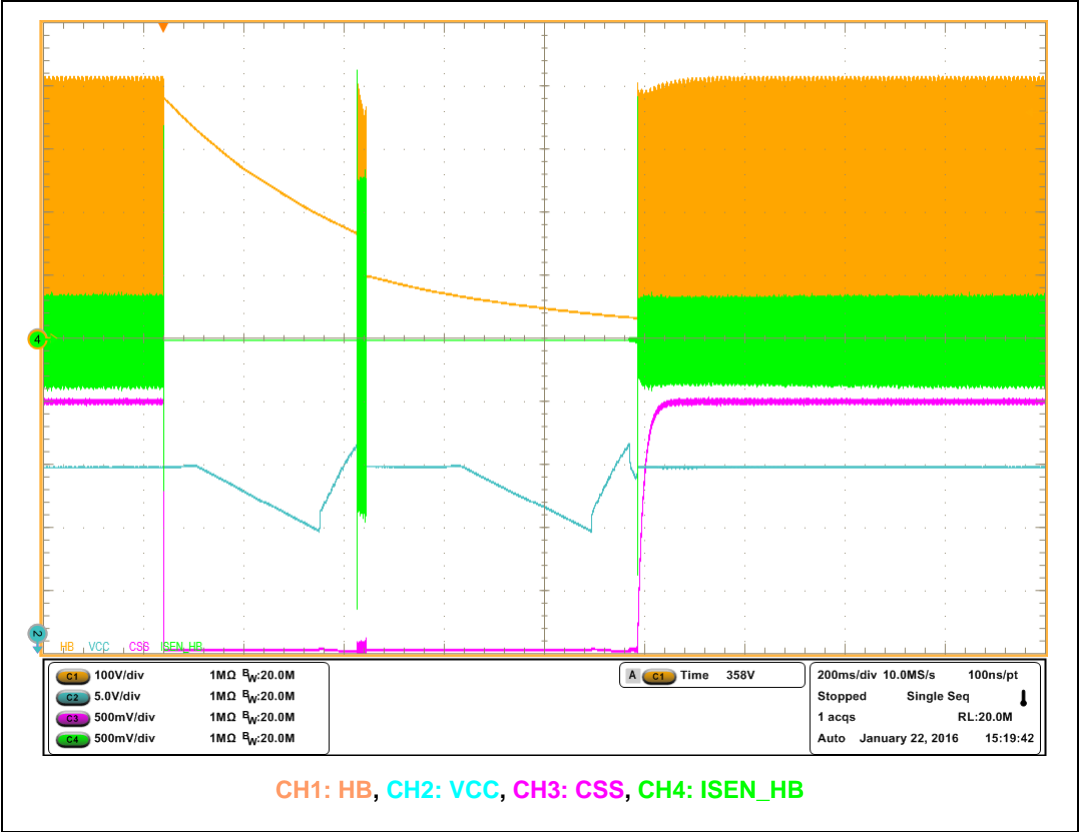
5.6.3 Second level OCP

In case of a particularly severe dead short-circuit the resonant tank current can rise very quickly to very high levels. In such cases it would be dangerous for the converters to wait the timing set up by the procedure described above, so the STCMB1 provides second level overcurrent protection.

If the signal at the ISEN_HB pin exceeds 1.5 V (OCP2 threshold), then the converter is immediately stopped, right after the ongoing half bridge cycle is completed, and CSS is completely discharged. Then, the adapter is forced to work intermittently (hiccup mode), following the dynamic of VCC driven by the HVSU generator. In order to avoid that the second level overcurrent protection is triggered during the start-up, because of any initial transient or spike, the protection is inhibited until the voltage on CSS is higher than 0.3 V.

In general, the behavior of the adapter when a short-circuit is applied does depend on the impedance of the short-circuit itself, but also on the reaction of the current loop control and on the dynamic of the voltage on the auxiliary winding of the LLC transformer that could trigger the rough feedback failure protection implemented by sensing such voltage. In general, a short-circuit kept at the output of the EVLCMB1-90WADP makes the adapter to work in the hiccup mode; however, in case of a severe hard short-circuit, the adapter can be turned off in the latch. In this case, it is necessary to disconnect and reconnect the mains to restart the adapter. [Figure 29](#) shows an example of the short-circuit applied and removed to the output of the EVLCMB1-90WADP.

Figure 29. Soft short-circuit applied and removed



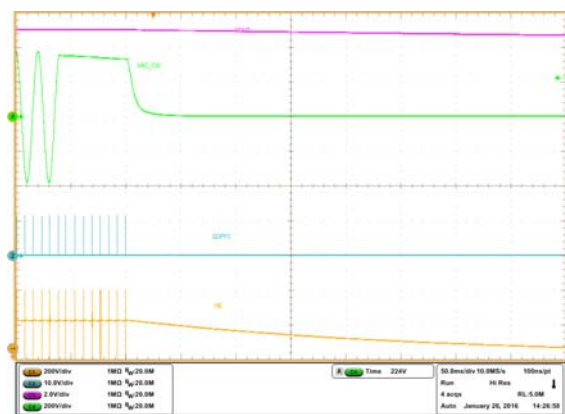
5.7 Adapter turn-off by mains disconnection - X-cap function

As the adapter is turned off by mains disconnection, the X-cap function plays the essential role of bringing the mains input of the adapter at a safe voltage level for the user, avoiding the use of the safety discharging resistors in parallel to the Cx filter capacitors that would dissipate a significant power during the light load operation, thus affecting the efficiency.

Waveforms from [Figure 30](#) to [Figure 33](#) show the operation of the X-cap function integrated in the STCMB1 device. Tests have been mainly done in the whole input voltage range and from the open load to the full load. However, the reported examples are at light loads and high mains because they are definitely the worst case conditions. In fact, at heavy loads, the X-cap discharge would be helped by the operation of the converter while at low mains, the Cx residual voltage to discharge would be lower.

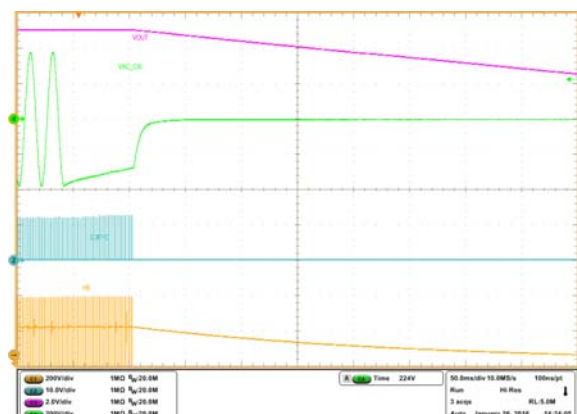
In all the cases, at mains disconnection the Cx are discharged within the safety limit in few hundreds milliseconds.

Figure 30. Vac removed at 265 Vac / no load



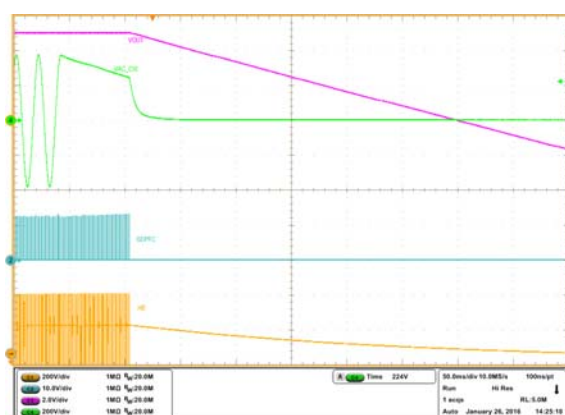
CH1: HB, CH2: GDPFC, CH3: VOUT, CH4: VAC (on C1)

Figure 31. Vac removed at 265 Vac / 100 mW



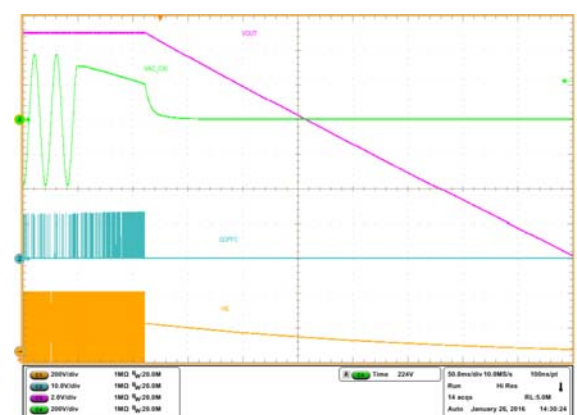
CH1: HB, CH2: GDPFC, CH3: VOUT, CH4: VAC (on C1)

Figure 32. Vac removed at 265 Vac / 250 mW



CH1: HB, CH2: GDPFC, CH3: VOUT, CH4: VAC (on C1)

Figure 33. Vac removed at 265 Vac / 500 mW



CH1: HB, CH2: GDPFC, CH3: VOUT, CH4: VAC (on C1)

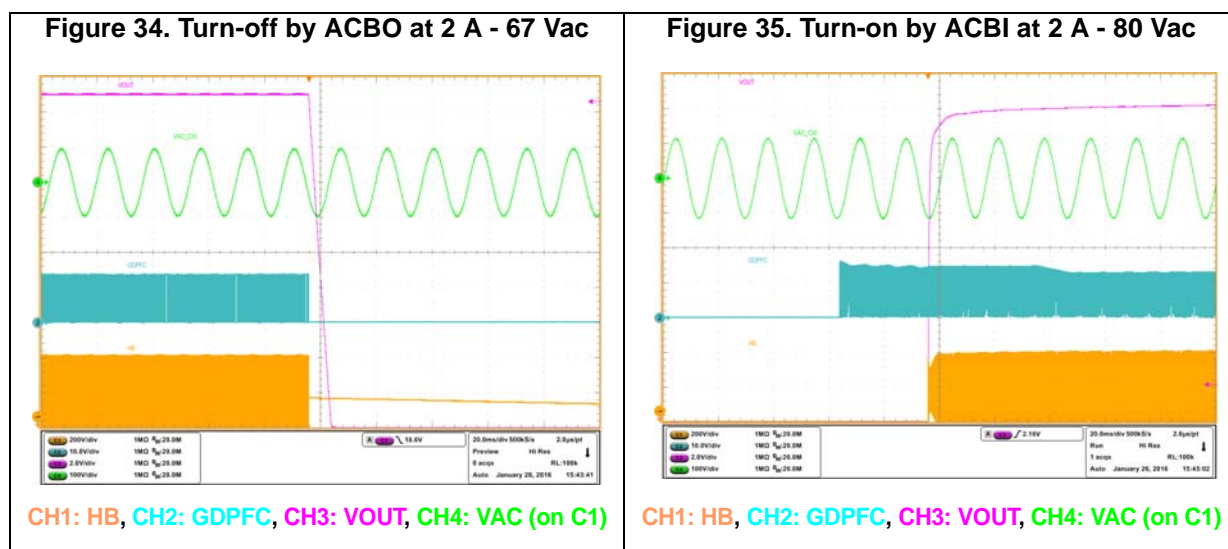
5.8 Adapter turn-off/on by ACBO/BI function

Here, the EVLCMB1-90WADP has been turned off/on by the AC brownout/in function respectively. The test is done by slowly reducing the mains voltage from 90 Vac to the adapter turn-off; then, the mains voltage has been slowly increased up to the adapter turn-on.

If the test is done at heavy loads, the ACBO action is mixed with the overcurrent protection of the PFC: its output power is consequently limited and so its output voltage is no more regulated at the nominal level. In this condition, if the PFC output voltage drops below the DCBO threshold, then it might be possible to observe bouncing of the output voltage because the DCBO turns off the LLC only when the ACBO is not yet reached. Afterward, because the PFC rapidly brings its output to the enabling threshold of the LLC (DCBI) causing a restarting attempts.

If the user wanted to avoid this behavior, then the PFC overcurrent protection limit and the boost inductor size should be designed at the minimum AC brownout voltage rather than at the AC minimum mains voltage. However, it is worth highlighting that this design criterion would result in a bigger size of the boost inductor size that should carry a larger mains current.

Figure 34 and *Figure 35* are for the test done at 2 A that is about the half load, for the EVLCMB1-90WADP: ACBO occurs at about 67 Vac, while ACBI occurs at about 80 Vac (mains voltage read on the AC source display).



5.9 Feedback failure disconnection (latch by FB pin)

Here, the EVLCMB1-90WADP has been shut down in latch by opening the PFC feedback divider, as pulling the FB pin down to ground: the adapter immediately stops and the latch is maintained by the VCC cycling between VCCoff and VCCon, driven by the HVSU generator.

Figure 36. Latch by FB at 90 Vac / full load

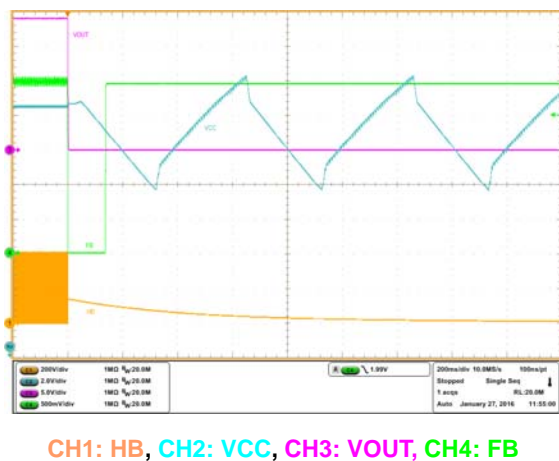
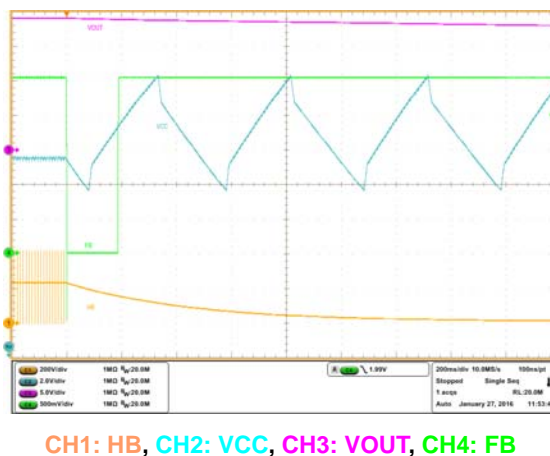


Figure 37. Latch by FB at 265 Vac / open load



5.10 Line transitions at full load

Here, the EVLCMB1-90WADP has been exposed to a full range line transition in both directions, i.e. from 265 Vac to 90 Vac and vice versa, while operating at the full load: in both cases, there is only a negligible variation on the output voltage.

Figure 38. Line transition: full load, 265 → 90 Vac

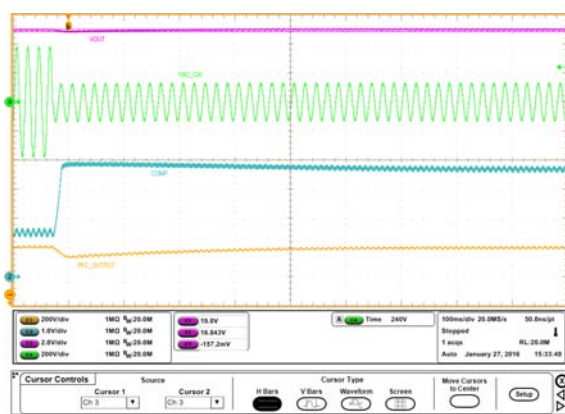
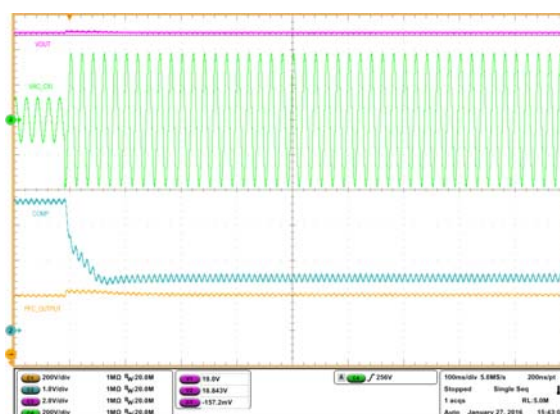
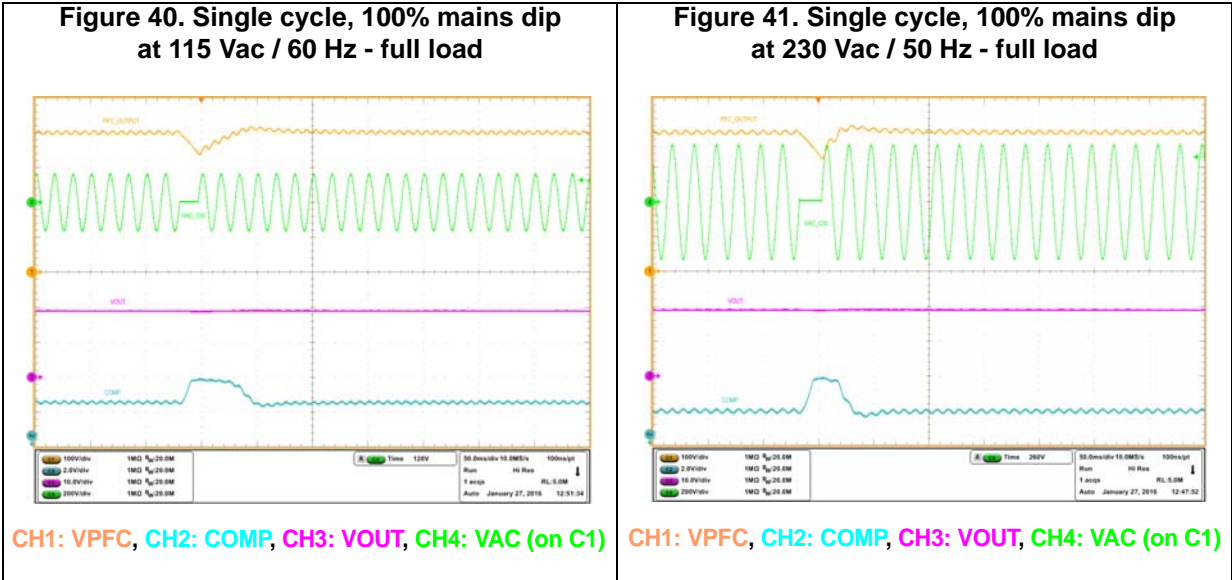


Figure 39. Line transition: full load, 90 → 265 Vac



5.11 Mains dips at full load

Here, the EVLCMB1-90WADP has been checked against a 0% mains dip (single line cycle, in accordance with IEC61000-4-11), at both nominal mains voltages while operating at the full load. The board behavior is correct: there are no output voltage drops, in both cases.



6 Thermal map

In order to check the design reliability, a thermal mapping by means of an IR camera has been done. [Figure 42](#) and [Figure 43](#) show the thermal maps of the top side of the EVLCMB1-90WADP device after about 2 h at the given conditions. Temperatures of the most relevant elements have been taken and highlighted in [Figure 42](#), [Figure 43](#), and in [Table 7](#). The room temperature during both measurements was around 25 °C.

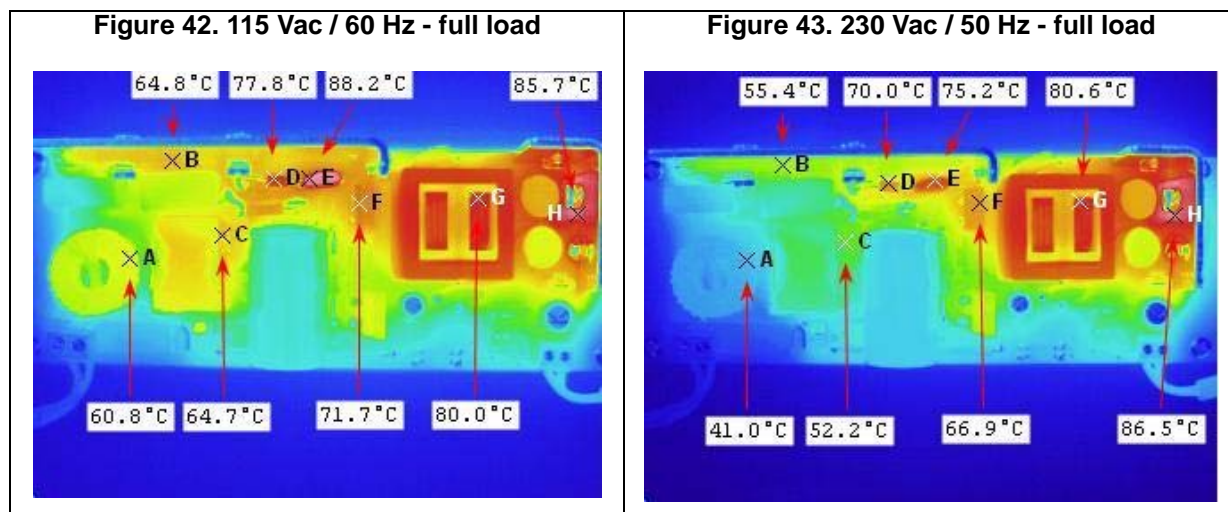
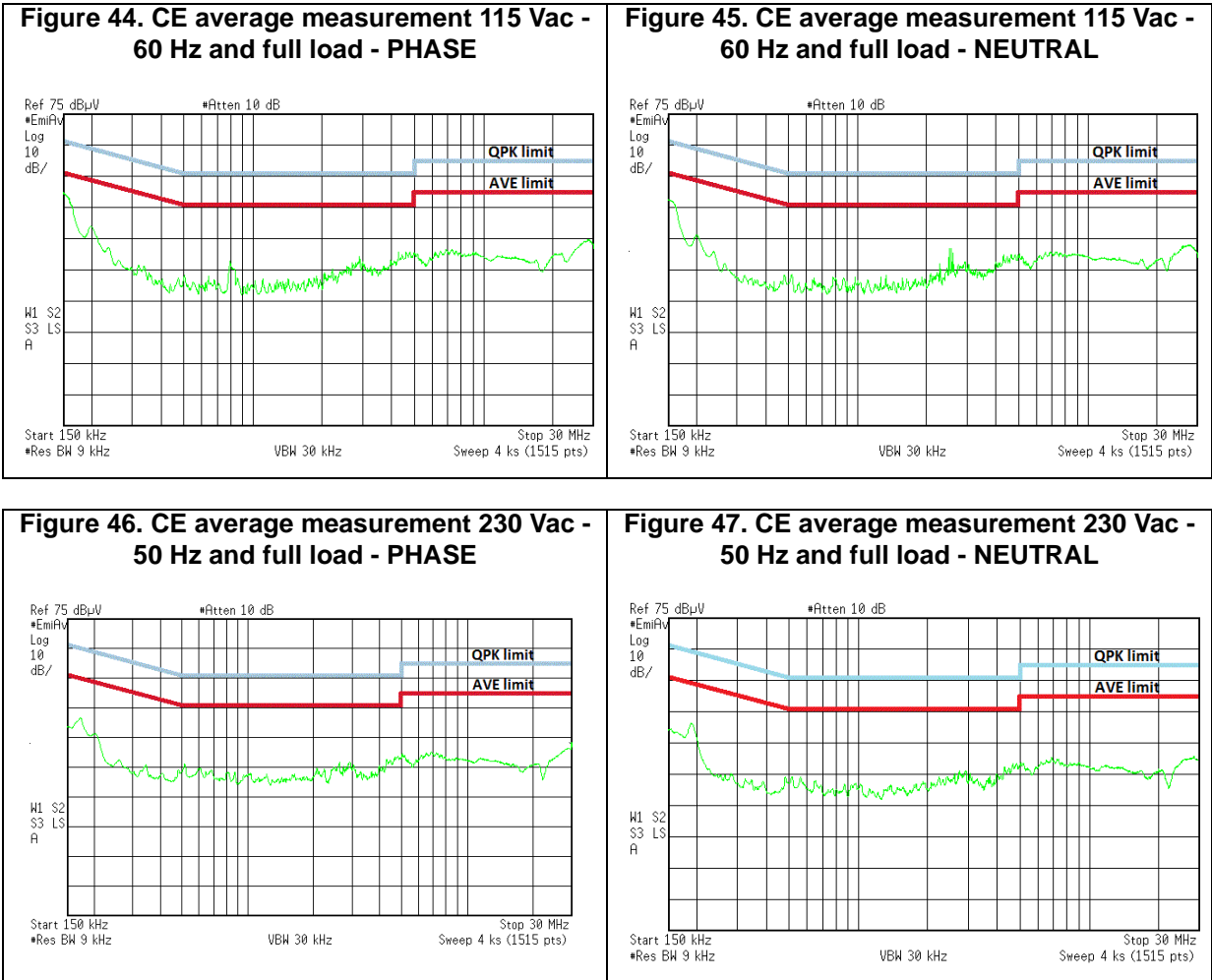


Table 7. Thermal map reference points

Point	Reference	Description	T [°C] at 115 Vac/60 Hz	T [°C] at 230 Vac/50 Hz
A	L1	Input common mode choke	60.8	41.0
B	D1	Bridge rectifier	64.8	55.4
C	L2	PFC inductor	64.7	52.2
D	D8	PFC boost diode	77.8	70.0
E	R6	NTC resistor	88.2	75.2
F	Q4	LLC low side MOSFET	71.7	66.9
G	T1	Secondary of LLC transformer	80.0	80.6
H	D24	Output rectifier	85.7	86.5

7 Conducted emission pre-compliance test

A pre-compliance test on conducted emission has been carried on. From [Figure 44](#) to [Figure 47](#) show the average measurement of the conducted emission at the full load and nominal mains voltages, for both conductors (PHASE and NEUTRAL), compared to the EN55022 Class B limits.



8 Bill of material

Table 8. EVLCMB1-90WADP BOM

Sch. ref.	Part no.	Case	Description	Supplier
C1	330N X2	9.0 x 18.0, p. 15 mm	X2 - film cap. - B32922C3334M	EPCOS
C2	10 μ F, 50 V	Dia. 5 x 11, p. 2 mm	Aluminum ELCAP - YXF SERIES - 105 °C	RUBYCON
C3	4.7 μ F	1206	25 V CERCAP - general purpose	AVX
C4	220 N X2	9.0 x 18.0, p. 15 mm	X2 - film cap. - B32922C3224K	EPCOS
C5	470 N 520 V	9.0 x 18.0, p. 15 mm	520 V - film cap. - B32672Z5474K	EPCOS
C6	3.3 N	0805	50 V CERCAP - general purpose	AVX
C7	10 N	0805	50 V CERCAP - general purpose	AVX
C9	68 μ F, 450 V	Dia. 18 x 32, p. 10 mm	450 V aluminum ELCAP - KXG series - 105 °C	UNITED CHEMICON
C12	100 N	1206	50 V CERCAP - general purpose	AVX
C13	8.2 nF	0805	50 V CERCAP - general purpose	AVX
C14	220 P	0805	50 V - 5% - C0G - CERCAP	AVX
C22	220 P	0805	50 V - 5% - C0G - CERCAP	AVX
C29	220 P	0805	50 V - 5% - C0G - CERCAP	AVX
C16	100 N	0805	50 V CERCAP - general purpose	AVX
C51	100 N	0805	50 V CERCAP - general purpose	AVX
C18	1.2 nF	0805	50 V CERCAP - general purpose	AVX
C19	1 μ F	0805	50 V CERCAP - X7R - 20%	TDK
C20	2.2 N, Y1	P. 10 mm	Y1 safety cap. CD12-E2GA222MYGSA	EPCOS
C21	2.2 N, Y1	P. 10 mm	Y1 safety cap. CD12-E2GA222MYGSA	EPCOS
C23	1 μ F	1206	50 V CERCAP - X7R - 20%	TDK
C24	47 μ F, 50 V	Dia. 6.3 x 11, p. 2.5 mm	Aluminum ELCAP - YXF series - 105 °C	RUBYCON
C25	470 P	0805	50 V - 5% - C0G - CERCAP	AVX
C27	100 PF 630 V	1206	630 V CERCAP - GRM31A7U2J101JW31D	MURATA
C28	10 N 400 V	5 x 10 p.7.5 mm	400 V - MKP film cap. - B32620A6103	EPCOS
C30	330 μ F	Dia. 10 x13, p. 5 mm	25 V OSCON ELCAP - SEPF series - 105 °C	SANYO
C37	330 μ F	Dia. 10 x13, p. 5 mm	25 V OSCON ELCAP - SEPF series - 105 °C	SANYO
C32	1 nF	0805	25 V CERCAP - general purpose	AVX
C34	470 pF	0805	50 V CERCAP - general purpose	AVX
C38	10 μ F	1206	50 V CERCAP - X5R - 20%	TDK
C55	100 μ F	Dia. 8 x 11.5, p. 3.5 mm	50 V aluminum ELCAP - ZLH series - 105 °C	RUBYCON
D1	GBU8J	STYLE GBU	Single phase bridge rectifier	VISHAY

Table 8. EVLCMB1-90WADP BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
D2	MMSZ5245B-7-F	SOD-123	Zener diode	DIODES
D3	1N4005	DO - 41	General purpose rectifier	VISHAY
D4	S1M	DO214AC	General purpose rectifier, SMT	FAIRCHILD
D5	S1M	DO214AC	General purpose rectifier, SMT	FAIRCHILD
D8	STTH2L06	DO-41	Ultrafast high voltage rectifier	ST
D9	STPS2H100A	SMA	Power Schottky diode	ST
D10	1N4148WS	SOD-323	High speed signal diode	VISHAY
D14	1N4148WS	SOD-323	High speed signal diode	VISHAY
D17	1N4148WS	SOD-323	High speed signal diode	VISHAY
D18	1N4148WS	SOD-323	High speed signal diode	VISHAY
D19	1N4148WS	SOD-323	High speed signal diode	VISHAY
D16	MMSZ5259B-7-F	SOD-123	Zener diode	DIODES
D24	STPS30H60CFP	TO-220FP	Dual power Schottky rectifier	ST
F1	Fuse T4A	8.5 x 4, p. 5.08 mm	FUSE 4 A - time lag - 3921400	LITTLEFUSE
HS1	Heatsink	DWG	Heatsink for D1, Q1	-
HS2	Heatsink	DWG	Heatsink for D24	-
JPX1	Shorted	-	Wire jumper	-
JPX2	Shorted	-	Wire jumper	-
JPX3	Shorted	-	Wire jumper	-
J1	MKDS 1.5/ 2-5.08	DWG	Screw conn., pitch 5 MM - 2 W.	PHOENIX CONTACT
J2	MKDS 1/2-3.81 HT BK	DWG	Screw conn., 3.81 MM, 2 W., black	PHOENIX CONTACT
L1	2291.0002	DWG	Common mode inductor 2 x 30 mH, 1 A	AQ MAGNETICA
L2	2263.0002	DWG	PFC inductor 520 μ H, 1.5 A, 90 W	AQ MAGNETICA
L6	EXCELD35C	DWG	Bead on wire 9 x 3.8, p. 5 mm	PANASONIC
Q1	STF20N65M5	TO-220FP	N-channel power MOSFET	ST
Q2	BC847C	SOT-23	NPN small signal BJT	VISHAY
Q7	BC847C	SOT-23	NPN small signal BJT	VISHAY
Q3	STF9N60M2	TO-220FP	N-channel power MOSFET	ST
Q4	STF9N60M2	TO-220FP	N-channel power MOSFET	ST
R1	1 k Ω	1206	SMD std. film. res. - 1/4 W - 1% - 100 ppm/ $^{\circ}$ C	VISHAY
R2	0.15 Ω	PTH	RSMF1TB - metal film res. - 1 W - 2% - 200 ppm/ $^{\circ}$ C	AKANEOHM

Table 8. EVLCMB1-90WADP BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
R3	2.7 MΩ	1206	SMD std. film. res. - 1/4 W - 1% - 100 ppm/°C	VISHAY
R8	2.7 M7Ω	1206	SMD std. film. res. - 1/4 W - 1% - 100 ppm/°C	VISHAY
R4	1 kΩ	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R5	0 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R9	180 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R6	8 Ω - S235	DWG	NTC resistor P/N B57235S0809M000	EPCOS
R7	2.7 MΩ	PTH	PTH std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R10	160 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R11	100 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R46	100 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R49	100 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R58	100 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R59	100 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R12	51 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R14	750 Ω	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R18	15 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R23	15 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R19	56 kΩ	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R21	22 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R73	22 RΩ	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R25	56 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200ppm/°C	VISHAY
R38	56 Ω	0805	SMD std. film. res.- 1/8W - 5% - 200 ppm/°C	VISHAY
R29	56 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R31	DNM	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R32	10 Ω	1206	SMD std. film. res. - 1/4 W - 5% - 200 ppm/°C	VISHAY
R33	3.9 kΩ	1206	SMD std. film. res. - 1/4 W - 5% - 200 ppm/°C	VISHAY
R34	4.7 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R35	1.8 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R36	4.3 kΩ	1206	SMD std. film. res.- 1/4 W - 5% - 200 ppm/°C	VISHAY
R40	0 Ω	1206	SMD std. film. res. - 1/4 W - 5% - 200 ppm/°C	VISHAY
R41	100 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R42	12 kΩ	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R43	47 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R44	2.7 kΩ	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY

Table 8. EVLCMB1-90WADP BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
R45	3.3 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R48	220 k Ω	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R50	16 k Ω	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R51	270 k Ω	0805	SMD std. film. res. - 1/8 W - 1% - 100 ppm/°C	VISHAY
R52	33 k Ω	0805	SMD std. film. res. - 1/8W - 1% - 100 ppm/°C	VISHAY
R78	43 Ω	0805	SMD std. film. res.- 1/8 W - 1% - 100 ppm/°C	VISHAY
R79	220 Ω	0805	SMD std. film. res. - 1/8 W - 5% - 200 ppm/°C	VISHAY
R80	6 m Ω	2512	SMD curr. sense res. TE conn. TLR - 2.5 W - 1% - 75 ppm/°C	TE CONN.
T1	2204.0005	DWG - E25	Res. transf. 100 W 600 μ H 170 kHz 19 V	AQ MAGNETICA
U1	STCMB1	SO20W	TM PFC and HB LLC res. combo contr.	ST
U2	SEA05L	SOT23-6L	ADV. CV/CC contr. with LED driver	ST
U3	SFH617A-4	DIP-4, 10.16 MM	Optocoupler	VISHAY

9 PFC coil specification

General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: vertical type, 6 + 8 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temperature: 60 °C
- Mains insulation: N.A.
- Unit finishing: varnished

Electrical characteristics

- Converter topology: transition mode boost
- Core type: PQ20/20-PC44 or equivalent
- Min. operating frequency: 50 kHz
- Typical operating frequency: 120 kHz
- Primary inductance: 520 $\mu\text{H} \pm 10\%$ at 1 kHz - 0.25 V^(a)
- Peak primary current: 3.2 Apk
- RMS primary current 1.1 A_{RMS}

Electrical diagram and winding characteristics

Figure 48. PFC coil electrical diagram

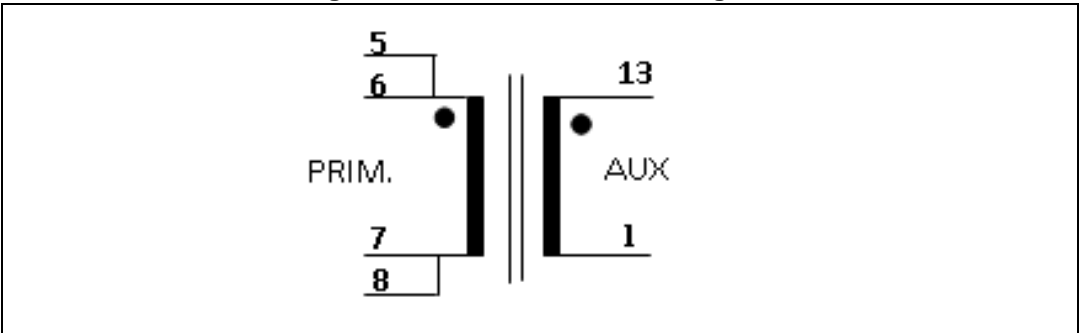


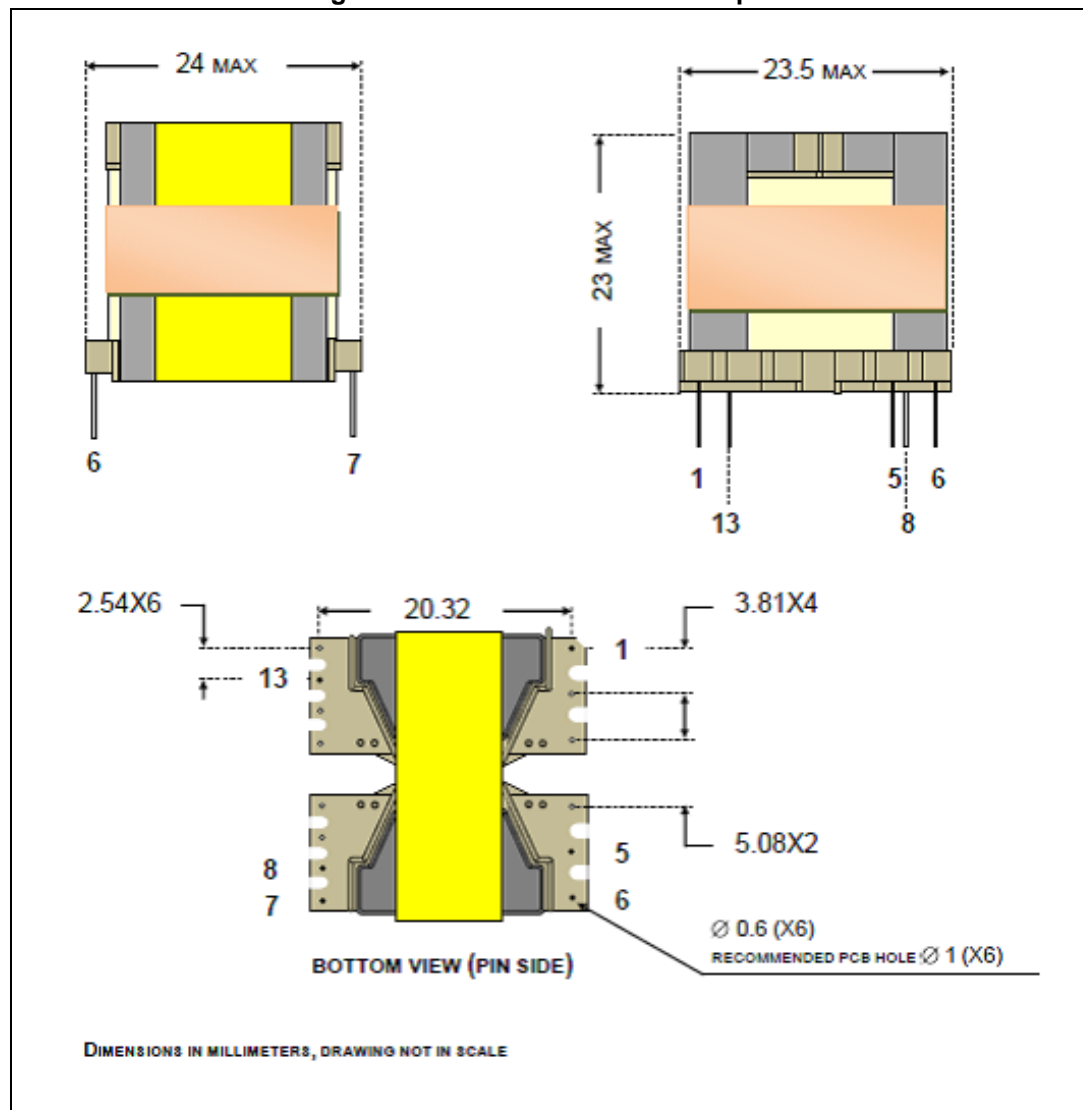
Table 9. PFC coil winding data

Pins	Windings	RMS current	Number of turns
5.6 - 7.8	PRIMARY	1.1 A _{RMS}	-
13 - 1	AUX	0.05 A _{RMS}	-

a. Measured between pins 5 and 7.

Mechanical aspect and pin numbering

- Maximum height from PCB: 23 mm
- Coil former type: vertical, 6 + 8 pins (pins 2, 3, 4, 9, 10, 11, 12, 14 are removed)
- Pin distance, pins from 1 to 6: 3.81 / 5.08 / 3.81 mm
- Pin distance, pins from 7 to 14: 2.54 / 5.08 / 2.54 mm
- Row distance: 20.32 mm
- External copper shield: not insulated, wound around the ferrite core and including the coil former. The height is 5 mm. Connected to the pin #1 by a soldered solid wire.

Figure 49. PFC coil mechanical aspect**Manufacturer**

- AQ MAGNETICA - Italy
- Inductor P/N: 2263.0002

10 LLC transformer specification

General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: horizontal type, 5 + 4 pins, two slots
- Max. temp. rise: 45 °C
- Max. operating ambient temperature: 60 °C
- Mains insulation: according to EN60065

Electrical characteristics

- Converter topology: resonant half-bridge
- Core type: E25/11 or equivalent
- Min. operating frequency: 65 kHz
- Typical operating frequency: 170 kHz
- Primary inductance: 600 $\mu\text{H} \pm 10\%$ at 1 kHz - 0.25 V^(b)
- Leakage inductance: 68 $\mu\text{H} \pm 10\%$ at 100 kHz - 0.25 V^(c)

Electrical diagram and winding characteristics

Figure 50. Transformer electrical diagram

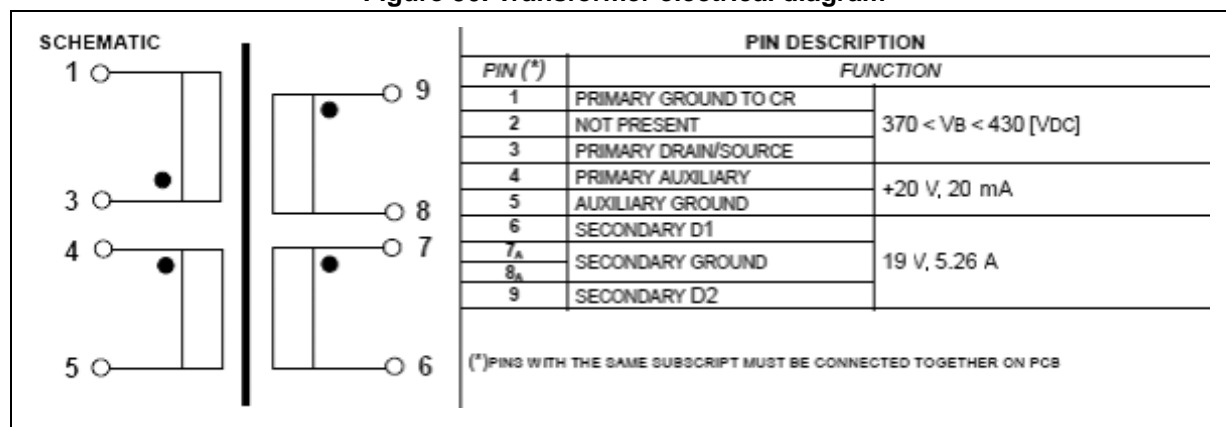


Table 10. Transformer winding data

Pins	Winding	RMS current	Number of turns
3 - 1	PRIMARY	0.35 A _{RMS}	-
7 - 6	SEC-D1	5.25 A _{RMS}	-
9 - 8	SEC-D2	5.25 A _{RMS}	-
4 - 5	AUX ⁽¹⁾	0.02 A _{RMS}	-

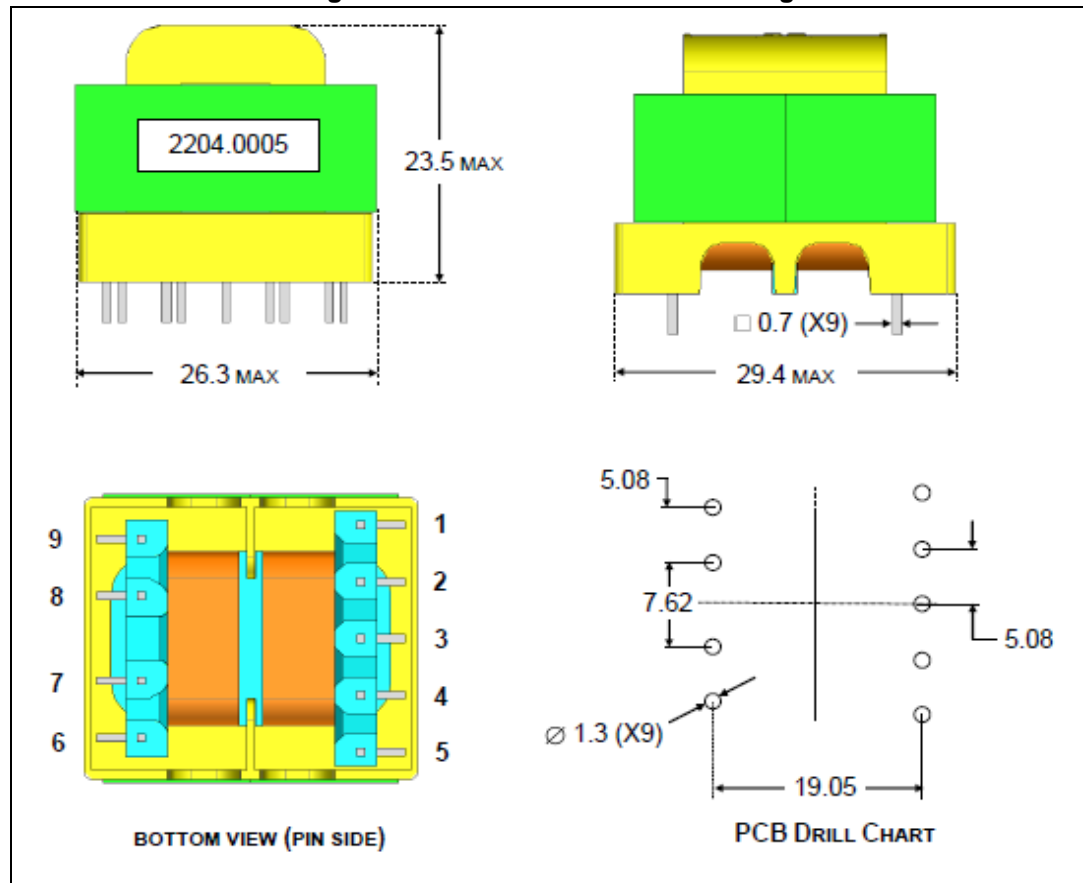
1. Aux winding is wound on the top of primary winding.

b. Measured between pins 1 and 3.

c. Measured between pins 1 and 3 with pins from 6 to 9 shorted.

Mechanical aspect and pin numbering

- Maximum height from PCB: 23.5 mm
- Pin distance, primary: 5.08 mm
- Pin distance, secondary: 5.08 / 7.62 / 5.08 mm
- Row distance: 19.05 mm

Figure 51. Transformer overall drawing**Manufacturer**

- AQ MAGNETICA - Italy
- Transformer P/N: 2204.0005

11 Revision history

Table 11. Document revision history

Date	Revision	Changes
23-May-2017	1	Initial release.
20-Jul-2017	2	Updated Figure 2: EVLCMB1-90WADP demonstration board schematic .

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