AN4867
Application note

L9960, L9960T automotive integrated H-bridges

Introduction

This is the Application Notes for L9960 (Single H-bridge) and L9960T (Twin H-bridge), the ASSP H-bridge solutions offered by STMicroelectronics.

It covers automotive applications such as electronic throttle control actuators (ETC) or exhaust gas recirculation control valves (EGR).

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1 Purpose

This document is intended as an Application Notes regarding the usage of the so called L9960, the ASSP H-bridge provided by ST, in a real scenario of application usage. The tests in this document described, are some of those that can help to point out the behavior of the new H-bridge under some particular conditions.

Functionality described by the specification must be guaranteed after tests have been applied to the device.

2 Glossary of terms

The following list reports the main terms and acronyms used in this document:

ASSP = *Application-Specific Standard Product*

BEMF = *Back Electromotive force*

DC = *Direct Current*

DT = *Duty Cycle*

ECU = *Electronic Control Unit*

EGR = *Exhaust Gas Recirculation*

EMI = *Electro Magnetic Interference*

ETC = *Electronic Throttle Control*

HSD = *High Side Driver*

LSD = *Low Side Driver*

OL = *Open Load*

OLDA = *Open Load Diagnostic Active*

OV = *Over Voltage*

PWM = *Pulse Width Modulation*

SOPC = *Switch-Off Path Check*

SPI = *Serial Peripheral Interface*

UV = *Under Voltage*

VVL = *Variable Valve Lift*.

3 General overview

Below the list of arguments treated along this document.

1. **Thermal considerations**
   - (a) Thermal dissipation
   - (b) Avoiding cross-conduction
2. **Driving the load**
   - (a) Usable DT in Normal / IN1 IN2 mode
3. **Current Freewheeling and protection**
   - (a) Current Limitation and Overcurrent detection
   - (b) LSD Freewheeling
   - (c) Current Limitation Freewheeling in IN1 IN2 mode
   - (d) HSD Freewheeling in IN1 IN2 mode
4. **SPI communication and registers**
   - (a) SPI communication
   - (b) Configuration registers
   - (c) TSW low current function
5. **Disabling the H-bridge**
   - (a) DIS, NDIS and SOPC
   - (b) Tristate procedure
6. **Diagnosis management**
   - (a) General diagnosis
   - (b) Open Load in active mode
   - (c) Diagnosis reset strategy
   - (d) LSD driver vs. H-bridge configuration

3.1 Thermal dissipation

This is a section regarding the theoretical calculus for Thermal Dissipation produced on integrated MOS due to the driving of a DC motor (rotating RL load).

We drive the bridge through IN1 and IN2 pins. IN1 acts as PWM input signal and IN2 as DIR input signal. In our case, we assume that the H-bridge is working in forward mode DIR=1.

Figure 1. How integrated MOS work in the H-bridge

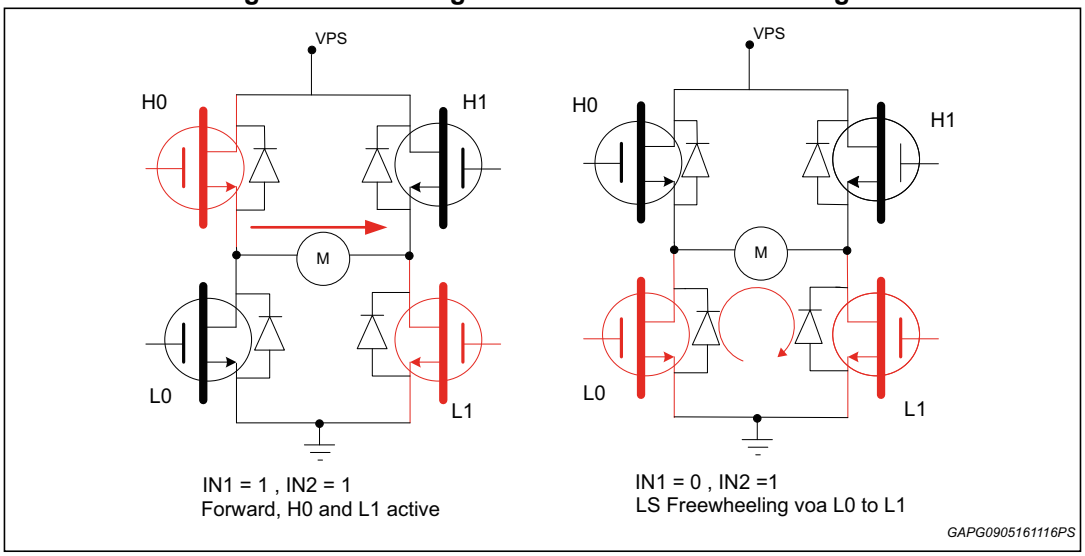
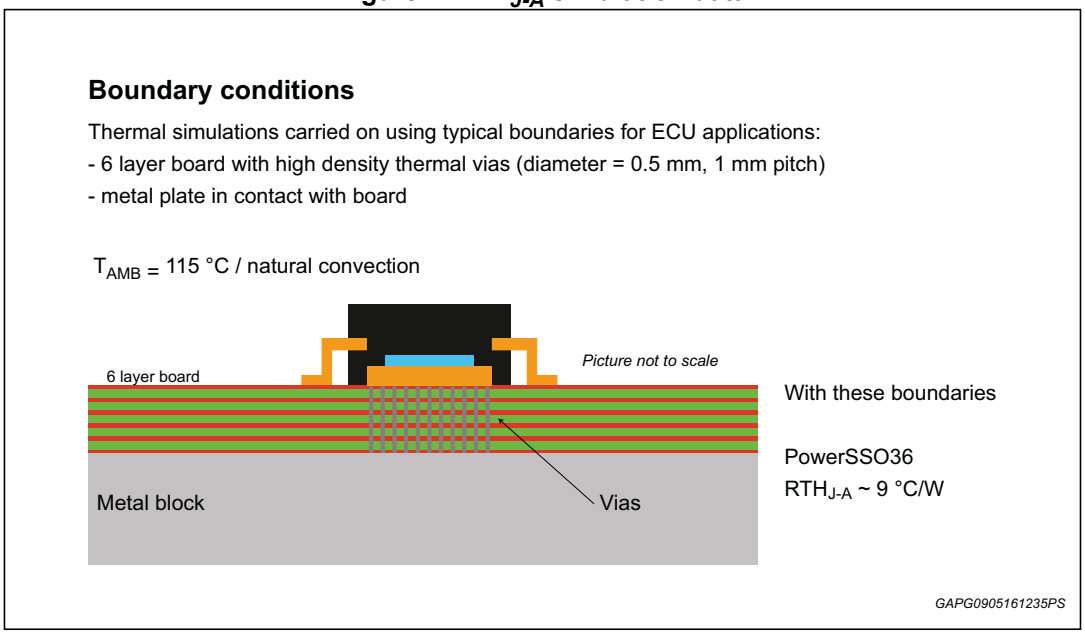


Figure 2. *RTH$_{J-A}$* simulation data



3.1.1 Average power dissipation: the theoretical model

The total average power P_{AV} per PWM cycle can be calculated by using the below set of *worst case* conditions:

Table 1. Power dissipation worst-case parameters

Parameter	Value	Units
DT	50%	-
α_{sw}	5.4%	-
f_{pwm}	2.0	kHz
I_{load}	2.0	A
V_{ps}	14.0	V
R_{dsonH0}=R_{dsonL1}	225.0	mΩ
$V\ SR\ slow$	2.0	V/µs
$ISR\ slow$	0.3	A/µs
T_{amb}	115.0	°C
R_{thja}	9.0	°C/W

We calculate the power dissipation $P_{AV\ single}$ due to a Single die contribution which works in the above table reported conditions. The parameter α_{sw} takes into account the switching time which must be subtracted to the nominal Duty Cycle (DT).

$$HSD_0 : \begin{cases} P_{static-on-H0} = R_{dsonH0} \cdot I_{load}^2 \cdot (DT - \alpha_{sw}) & (1) \\ where\ :\ \alpha_{sw} = \frac{\sum_{i=0}^{3} tsw_i}{T} & \\ P_{sw-H0} = (I_{load} \cdot V_{ps}) \cdot \left(\frac{V_{ps}}{VSR} + \frac{I_{load}}{ISR}\right) \cdot f_{pwm} & (2) \end{cases}$$

$$LSD_1 : P_{static-on-L1} = R_{dsonL1} \cdot I_{load}^2 \quad (3)$$

$$HSD_1 : P_{static-on-H1} = 0 \quad (i.e.\ always\ off) \quad (4)$$

$$LSD_0 : P_{static-on-L0} = R_{dsonL0} \cdot I_{load}^2 \cdot (1-DT) \quad (5)$$

Switching times tsw_i (i = 0, 1, 2, 3) are timings defined both in function of the maximum power peak on HSD_0 in a PWM cycle P_a, and the power dissipation in conduction P_b.

$$P_a = I_{load} \cdot V_{ps} \quad (6)$$

$$P_b = I_{load}^2 \cdot R_{dsonH0} \quad (7)$$

Based upon the foregoing partial contributions, for the Single option we have an average power consumption:

$$P_{AVsingle} = P_{sw} + P_{static} = (1) + (2) + (3) + (4) + (5) \quad (8)$$

In case we use the Twin option (both dies simultaneously working), we have to consider both die contributions:

$$P_{AVtwin} = 2 \bullet P_{AVsingle} \quad (9)$$

Junction temperature calculation for Twin option is defined as:

$$T_j = T_{amb} + (R_{thja} \bullet P_{AVtwin}) \quad (10)$$

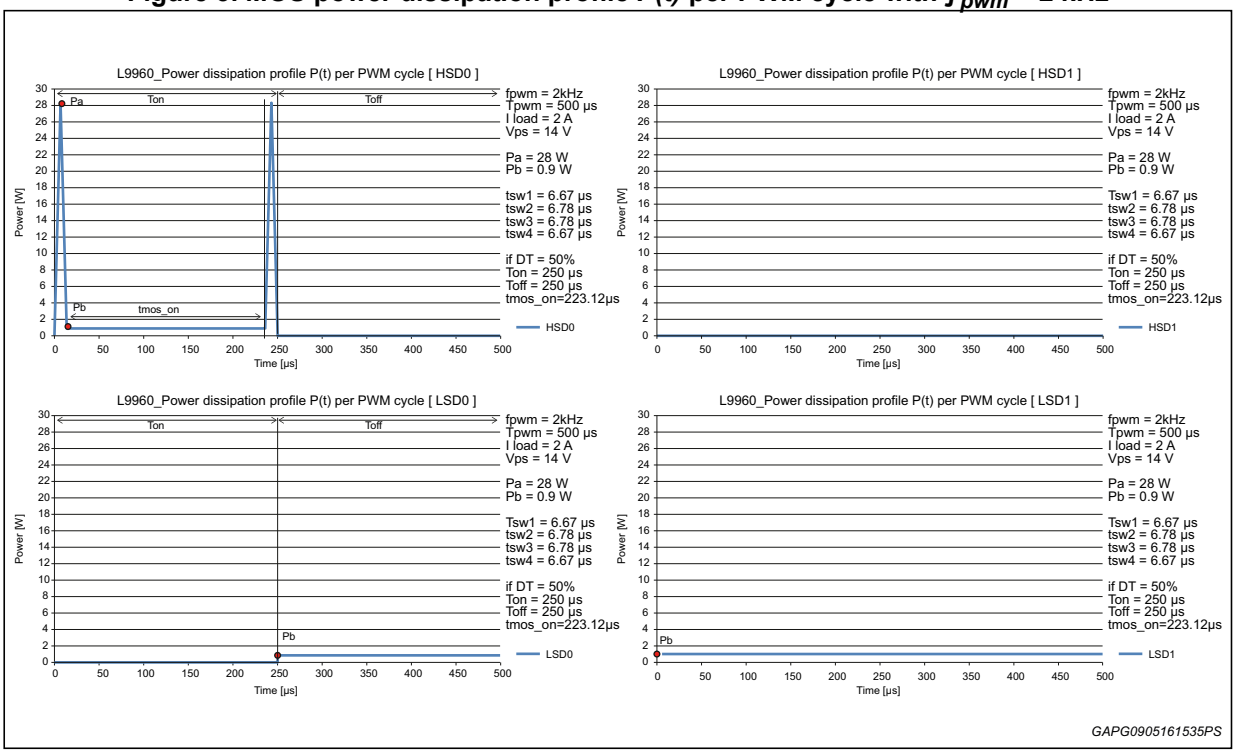
For our particular case:

- By applying (6) formula, we obtain the total average power consumption for the Single: $P_{AV\ single}$ = 2.52 W
- By applying (7) formula, we obtain the total average power consumption for the Twin: $P_{AV\ twin}$ = 5.03 W
- By applying (8) formula, we find the junction temperature in the steady state: T_j = 160.4 °C

Below, the resulting power profile *P(t)* for each one of the 4 MOS our H-bridge is made up.

By applying (6) and (7) formulas to our particular case, we obtain P_a = 28 W, P_b = 0.9 W.

Figure 3. MOS power dissipation profile *P(t)* per PWM cycle with f_{pwm} = 2 kHz



3.1.2 Average power dissipation: simulation data

We analyze the Twin die dissipation profile and the T_{jmax} reached by the device by following these steps:

1. First step will be to simulate the thermal map after n pulses when $n \rightarrow \infty$ (*steady state*).

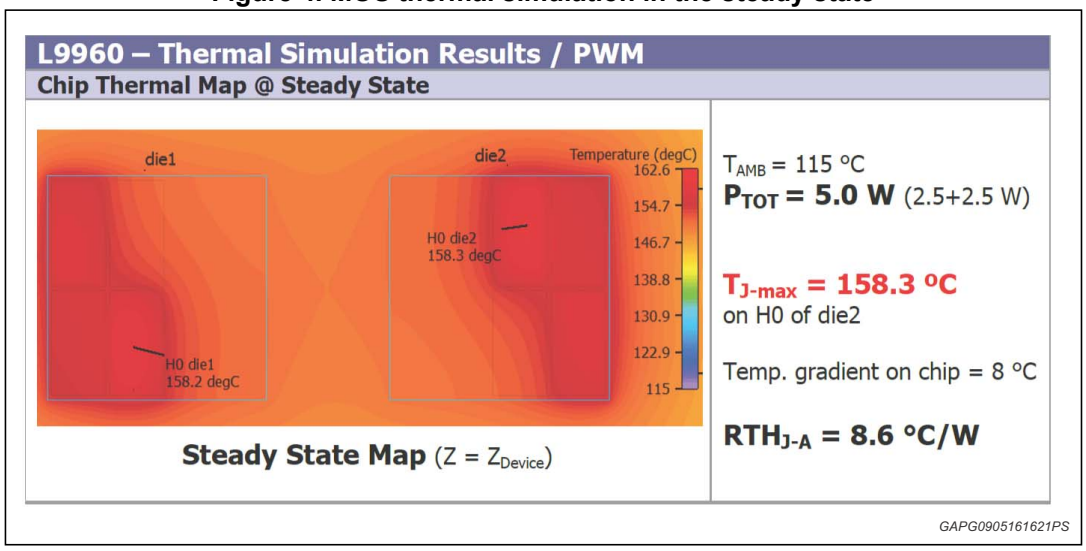
   We here use mean powers as previously calculated per each MOS in order to obtain thermal map.

   For practical reasons, we consider the situation after n = 8 pulses as a good approximation to the one reached at the *steady state*.

2. By using T_{jmax} value from the steady state as the initial conditions for the thermal simulation in a single PWM cycle, we find that the maximum temperature is T_{jmax} = 162.6 °C and the value is reached at t = 246 µs in the central area of the HSD_0 of die2.

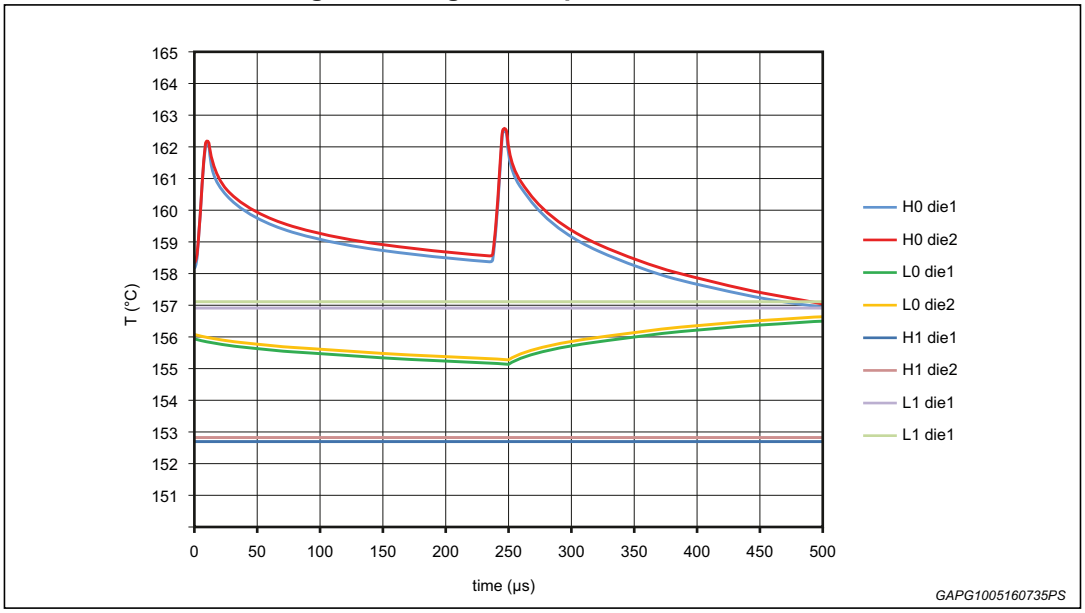
Here below, the thermal simulation at the *steady state*. Thermal gradient stands for the difference between **red** and **orange** plotted areas, which is hottest versus coldest areas on the die surface. This is intended to indicate that the temperature out of MOS power areas remains around T = 150 °C.

Figure 4. MOS thermal simulation in the steady state



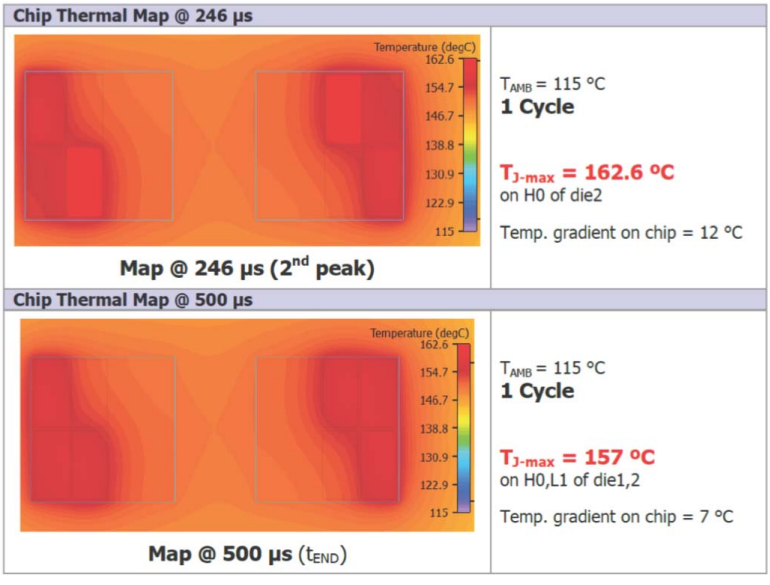
Below we can find the chart which represents the temperature profile T = T(t) for the 8 integrated MOS during a single PWM cycle.

Figure 5. Single PWM pulse thermal data



We simulate the single PWM period and observe that the peak at t = 246 µs corresponds to the maximum silicon temperature. At the end of the period, we can observe the maximum temperature T_{jmax} decreases to 157 °C, which is a result quite close to the one calculated for the steady state (T_{jmax} = 158.3 °C).

Figure 6. Thermal simulation at profile's second peak and at the end of PWM cycle



3.1.3 Maximum workable load current

We could here define the maximum load current I_{load} flowing in a single die at which we can work in case we use Twin option and have defined a maximum tolerated T_j threshold:

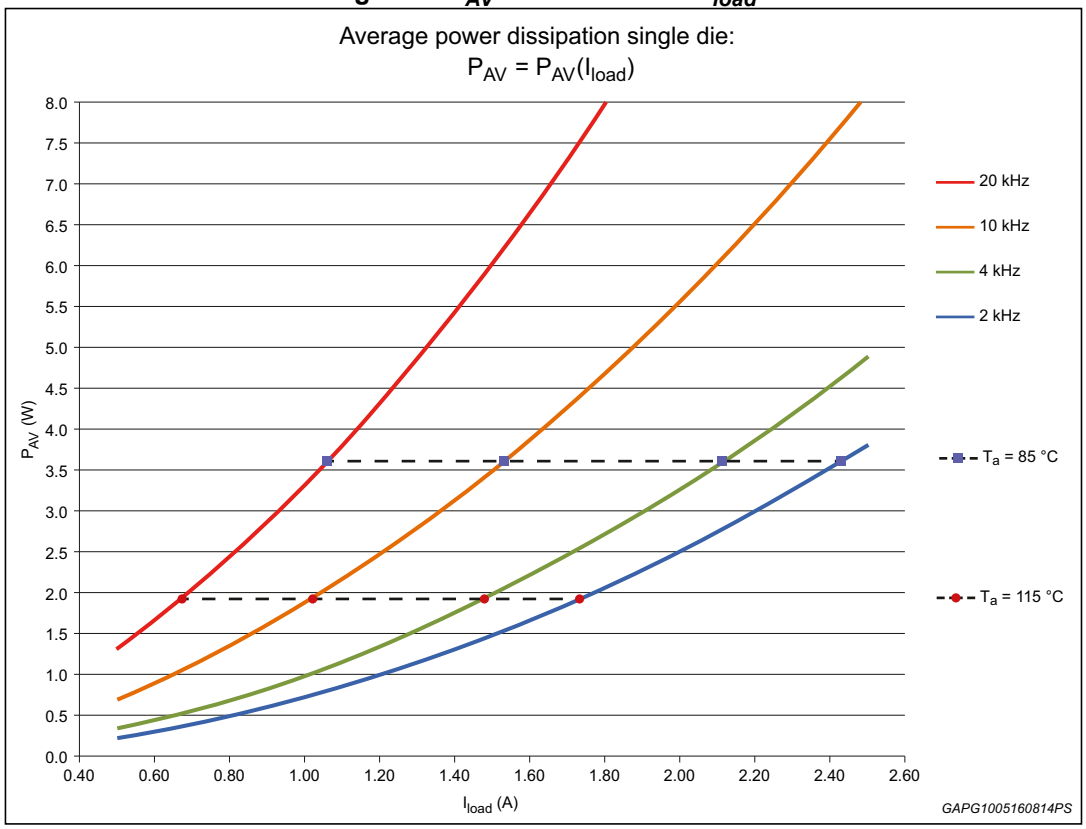
Table 2. Maximum workable load current

Parameter	Value	Units
V_{ps}	14.0	V
DT	50%	-
f_{pwm}	2.0, 4.0, 10.0, 20.0	kHz
R_{thja} (1)	9.0	°C/W
T_{jmax}	150.0	°C
T_{amb}	115.0, 85.0	°C

1. *Please, note that we deal with thermal resistance as a constant value in the range $R_{thja} \in [0.5, 2.5]$A , because in the first approximation R_{thja} does not depend on power dissipation, but only on boundary conditions (application board, system architecture).*

By plotting $P_{AV\ single}$ as a function of I_{load}, we can extract from the resulting chart the maximum value for the load current which assures us still working within the defined safe area: $T_j \leq T_{jmax}$ = 150.0 °C.

Figure 7. P_{AV} as a function of I_{load}



For example, by working at the following conditions: f_{pwm} = 2 kHz, DT = 50%, V_{ps} = 14 V T_{amb} = 115 °C, the load current matching the $P_{AV\ single}$ = 1.94 W is an I_{load} = 1.74 A (per each die of the Twin option). So, as we would expect, if we want to work within the safe area with the Twin option we can do it (see *Mission Profile section*) by using an I_{load} value in the range of [0.50, 1.74]A (per die). It is here important to note, that if we could work at a lower temperature, let us say T_{amb} = 85 °C, then the allowed range for load current would be broader. By only decreasing 20 °C the ambient temperature, we obtain an admissible value $I_{load} \in [0.50, 2.43]A$, which means working inside a range 1:6 times larger than the original. Minimizing the T_{amb} provides higher flexibility when developing applications in environments where the H-bridge has to be integrated by taking into account restrictive power dissipation constraints.

Mission Profile

During this thermal analysis we have used the below thermal mission profile:

Table 3. Mission profile thermal data

T_j (°C)	time (h)	percentage over lifetime
$T_j < 90$	1497	18.70 %
$90 < T_j < 100$	1818	22.72 %
$100 < T_j < 110$	2499	31.23 %
$110 < T_j < 120$	1211	15.14 %
$120 < T_j < 130$	748	9.35 %
$130 < T_j < 140$	139	1.73 %
$140 < T_j < 150$	11	0.14 %
$150 < T_j < 170$	80	1.00 %

Our case of study (T_j = 160.2 °C) falls in the one related to the bottom line of the table. Please, note that this must not be the usual working temperature, but it only refers to the temperature the device can withstand for a time 1% of the total lifetime of the device, which considering a **lifetime = 8000h**, makes a total amount of 80h working at the maximum range of allowed junction temperature. Above that, the device could become unusable and seriously damaged, so this limit must not be exceed.

*Note: The device switches directly to **Super Fast SR** in case at least one of this conditions is present: (T_j > OTwarn with TDSR=1 bit manually set), (ILIM_REG = 1 highlighting), (NOC = 0 highlighting), or (NOSR = 1 bit manually set).*

3.2 Avoiding cross-conduction

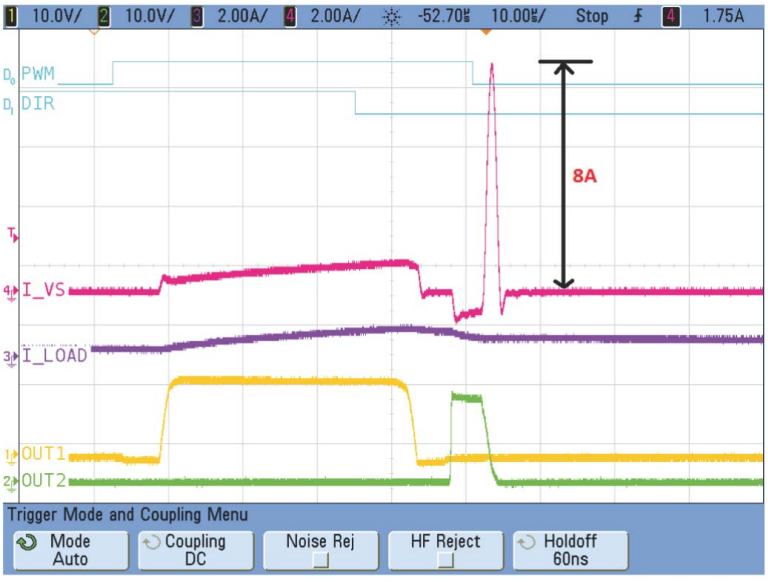
The issue of cross-conduction is avoided in L9960. However, because of the importance of it in power devices, and for clarification purposes, we have here added a brief description of the phenomenon.

Here below, we can find an example of a device in which the cross-conduction is present because the HSD and LSD (being both part of the same leg of the bridge) are switched-on at the same time. As it can be seen from the below image, the additional current does not flow through the load, but through the battery line. In order to avoid this unwanted phenomenon that can damage the device, a filter time T_{sw} has been implemented in L9960.

Description: IN1 pin was controlled with a PWM signal at 2 kHz and DT 20%, IN2 pin was controlled with a PWM signal at 2.4 kHz and DT 50% from external generator. As load was used a free running motor. On the VS line appeared current spikes 8 A which looks like shoot through current. The same behavior is observed when no load is connected. This result is valid for VSR, ISR = fast. For VSR = slow the current spikes are even higher around 11 A.

In the below oscilloscope image we have a delay between DIR, PWM signals of Δt = 16 µs. As a consequence of the cross-conduction we obtain a peak of amplitude I_0 = 8 A on V_{ps} line.

Figure 8. Cross-conduction due to PWM DIR switching



Considerations

When the duty cycle on IN1 pin was increased to 50% the power stage stopped working and reactivation was possible only by a “SW reset” + “request for HWSC/LBIST”.

3.3 Usable DT in Normal / IN1 IN2 mode

Because timings to turn-on and turn-off the integrated MOS impact on output driveability, we present here some data to take in mind when designing the Application. The period of the PWM input signal can be split up as:

$$T = T \bullet DT + T \bullet (1 - DT) = T_{on} + T_{off}$$

$DT = T_{don} / T \rightarrow DT_{min} = T_{donmax} / T$

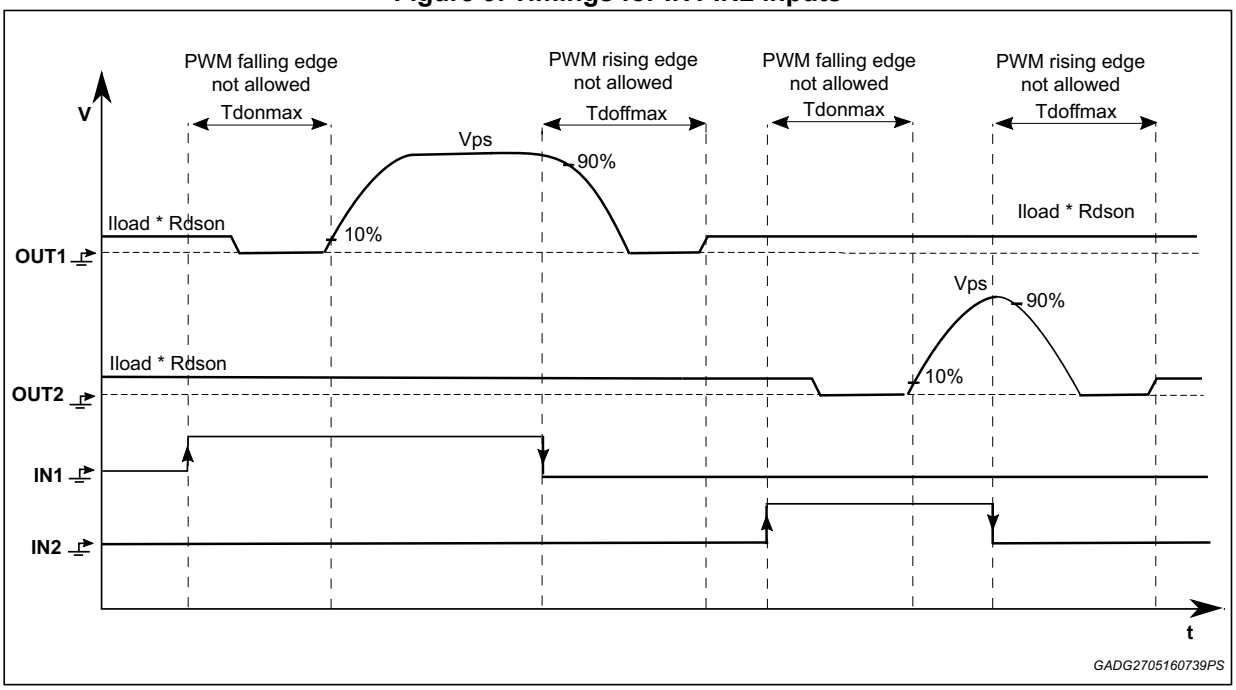
$(1 - DT) = T_{off} / T \rightarrow DT_{max} = (1 - T_{doffmax} / T)$

$T = 1/F_{pwm}$

T_{donmax} represents the maximum time elapsed from PWM input rising edge to the driven output reaches 10% of Vps by considering LSD switches OFF, T_{SW_sr} filter (delay between LSD OFF and HSD ON, 4.6 µs typ.), and finally output raises up to 10% of Vps.

$T_{doffmax}$ represents the maximum time elapsed from PWM falling edge until LSD is ON by considering that output decreases down to 90%, then the particular SR applied on output stage, the T_{SW} filter (delay between HSD OFF and LSD ON, 2.0 µs typ.), and finally LSD switches ON.

Figure 9. Timings for IN1 IN2 inputs



Above mentioned timings assure the device functionality and are applicable both for Normal and IN1 IN2 mode, they represent two core time windows that cannot be violated, otherwise the device procedures for switching ON/OFF could be interrupted causing consequent driveability issues. Therefore, the PWM falling edge signal cannot reach the device before T_{donmax} timing elapsed, and the PWM rising edge signal cannot reach the device before the $T_{doffmax}$ has elapsed. We can now construct the possible [DTmin, DTmax] to apply on PWM input signal which allow us driving the output stage in the proper way.

Some application data obtained at bench shows T_{don} and T_{doff} timings as from datasheet described depend on which load we are considering, which PWM frequency is been used, the battery voltage and even at which ambient temperature are we working:

- T_{don} is the time elapsed from rising edge on PWM signal to V_{out} reaching fully ON voltage;
- T_{doff} is the time elapsed from falling edge on PWM signal to V_{out} reaching fully OFF voltage

On a Freewheeling DC motor from E-Gas module with RL equivalent circuit R = 4.0 Ω L = 700 µH, we have that worst performances at room temperature in terms of delay timings are reached for Slow SR and highest possible frequency 20 kHz. Values at this condition are T_{don} = 9.5 µs, T_{doff} = 9.2 µs. In case NOSR mode is activated (Very Fast SR), the timings decrease down to T_{don} = 6.2 µs, T_{doff} = 4.0 µs.

On a resistive load of R = 2.0 Ω, we have that worst performances at room temperature in terms of delay timings are reached for Slow SR and the highest possible frequency 20 kHz. Values at this condition are T_{don} = 8.8 µs, T_{doff} = 9.0 µs. In case NOSR mode is activated (Very Fast SR), the timings decrease down to T_{don} = 6.2 µs, T_{doff} = 3.8 µs.

Some considerations should be done before choosing the Slew Rate: The highest SR (NOSR mode active) provides quickest timings and large operative range, but provides also the highest rate of electromagnetic emitted radiation. On the other hand Slow SR is the worst Slew Rate in terms of DT coverage, but due to MOS are driven slower, this option decreases the switching power dissipation lowering the emitted radiation.

Because T_{don} and T_{doff} timings give us the behaviour about how output voltage responds to the PWM signal, but lack in describing the full application scenario regarding total set of analog and digital timings the device needs to accomplish a particular action, we here give the data to take into account when designing the Application, which as already seen before, points at knowing the T_{donmax} and $T_{doffmax}$ timings that define the operative range [DT_{min}, DT_{max}] for a particular chosen PWM frequency and Slew Rate. In the next pages we use a resistive load of R = 6 Ω as reference load fixing a load current about 3 A.

All the following considerations are valid under the condition of TSW_low_current = 0.

From wafer-level testing data we know that large T_{don}, T_{doff} timings are associated with cold temperature (-40 °C) and for the maximum guaranteed battery voltage (28 V), the worst case for DT allowed range is reached taking below T_{donmax}, $T_{doffmax}$ values:

Figure 10. DT minimum and maximum on input PWM signal at 28 V table

Condition: resistive load R = 6 Ohm, Vps = 28V, T = - 40°C			
Parameter	**VSR=ISR=0**	**VSR=ISR=1**	**NOSR=1**
Tdonmax (µs)	11.5	10.5	7.0
Tdoffmax (µs)	25.0	19.0	11.0

		Condition: resistive load R = 6 Ohm, Vps = 28V, T = - 40°C					
		SLOW (VSR=ISR=0)		**FAST (VSR=ISR=1)**		**Very Fast (NOSR=1)**	
F_pwm (kHz)	**T_pwm (µs)**	**DTmin [%]**	**DTmax [%]**	**DTmin [%]**	**DTmax [%]**	**DTmin [%]**	**DTmax [%]**
1.0	1000.0	1.2	97.5	1.1	98.1	0.7	98.9
2.0	500.0	2.3	95.0	2.1	96.2	1.4	97.8
3.0	333.3	3.5	92.5	3.2	94.3	2.1	96.7
4.0	250.0	4.6	90.0	4.2	92.4	2.8	95.6
5.0	200.0	5.8	87.5	5.3	90.5	3.5	94.5
6.0	166.7	6.9	85.0	6.3	88.6	4.2	93.4
7.0	142.9	8.1	82.5	7.4	86.7	4.9	92.3
8.0	125.0	9.2	80.0	8.4	84.8	5.6	91.2
9.0	111.1	10.4	77.5	9.5	82.9	6.3	90.1
10.0	100.0	11.5	75.0	10.5	81.0	7.0	89.0
11.0	90.9	12.7	72.5	11.6	79.1	7.7	87.9
12.0	83.3	13.8	70.0	12.6	77.2	8.4	86.8
13.0	76.9	15.0	67.5	13.7	75.3	9.1	85.7
14.0	71.4	16.1	65.0	14.7	73.4	9.8	84.6
15.0	66.7	17.3	62.5	15.8	71.5	10.5	83.5
16.0	62.5	18.4	60.0	16.8	69.6	11.2	82.4
17.0	58.8	19.6	57.5	17.9	67.7	11.9	81.3
18.0	55.6	20.7	55.0	18.9	65.8	12.6	80.2
19.0	52.6	21.9	52.5	20.0	63.9	13.3	79.1
20.0	50.0	23.0	50.0	21.0	62.0	14.0	78.0

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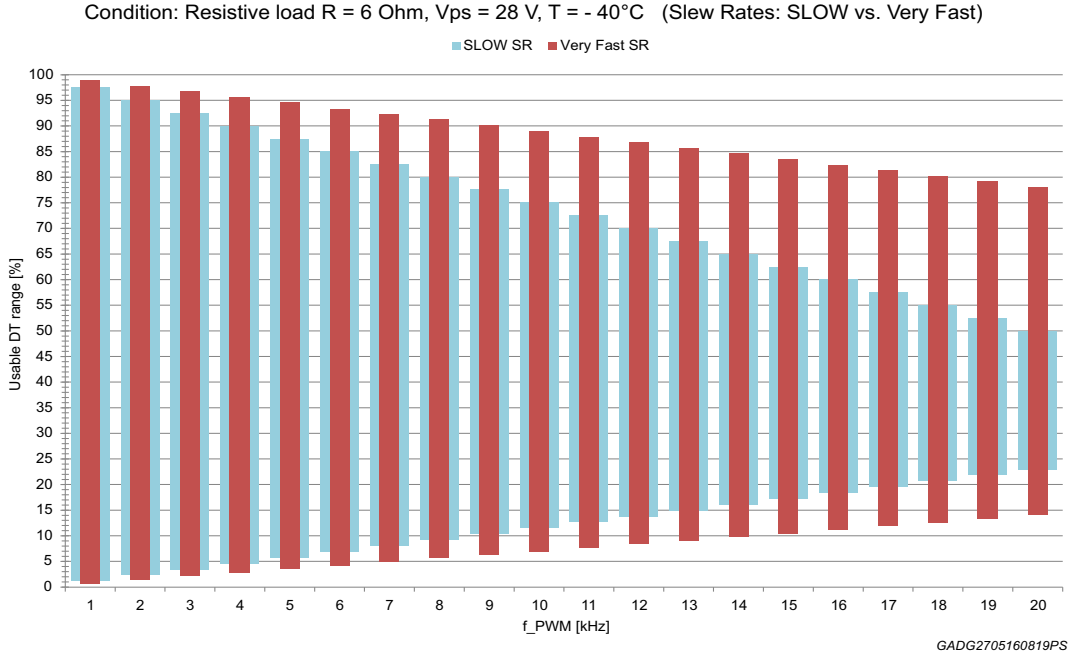
A graphical representation Slow vs. Very Fast up to f_pwm = 20 kHz can be seen below:

Figure 11. DT minimum and maximum on input PWM signal at 28 V diagram



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In order to provide a more realistic situation, below we show the values associated with a battery level set at Vps = 16 V considering load and temperature still being the same ones:

Figure 12. DT minimum and maximum on input PWM signal at 16 V table

Condition: resistive load R = 6 Ohm, Vps = 16V, T = - 40°C			
Parameter	**VSR=ISR=0**	**VSR=ISR=1**	**NOSR=1**
Tdonmax (µs)	11.0	10.0	7.0
Tdoffmax (µs)	21.0	17.0	10.0

		Condition: resistive load R = 6 Ohm, Vps = 16V, T = - 40°C					
		SLOW (VSR=ISR=0)		**FAST (VSR=ISR=1)**		**Very Fast (NOSR=1)**	
F_pwm (kHz)	**T_pwm (µs)**	**DTmin [%]**	**DTmax [%]**	**DTmin [%]**	**DTmax [%]**	**DTmin [%]**	**DTmax [%]**
1.0	1000.0	1.1	97.9	1.0	98.3	0.7	99.0
2.0	500.0	2.2	95.8	2.0	96.6	1.4	98.0
3.0	333.3	3.3	93.7	3.0	94.9	2.1	97.0
4.0	250.0	4.4	91.6	4.0	93.2	2.8	96.0
5.0	200.0	5.5	89.5	5.0	91.5	3.5	95.0
6.0	166.7	6.6	87.4	6.0	89.8	4.2	94.0
7.0	142.9	7.7	85.3	7.0	88.1	4.9	93.0
8.0	125.0	8.8	83.2	8.0	86.4	5.6	92.0
9.0	111.1	9.9	81.1	9.0	84.7	6.3	91.0
10.0	100.0	11.0	79.0	10.0	83.0	7.0	90.0
11.0	90.9	12.1	76.9	11.0	81.3	7.7	89.0
12.0	83.3	13.2	74.8	12.0	79.6	8.4	88.0
13.0	76.9	14.3	72.7	13.0	77.9	9.1	87.0
14.0	71.4	15.4	70.6	14.0	76.2	9.8	86.0
15.0	66.7	16.5	68.5	15.0	74.5	10.5	85.0
16.0	62.5	17.6	66.4	16.0	72.8	11.2	84.0
17.0	58.8	18.7	64.3	17.0	71.1	11.9	83.0
18.0	55.6	19.8	62.2	18.0	69.4	12.6	82.0
19.0	52.6	20.9	60.1	19.0	67.7	13.3	81.0
20.0	50.0	22.0	58.0	20.0	66.0	14.0	80.0

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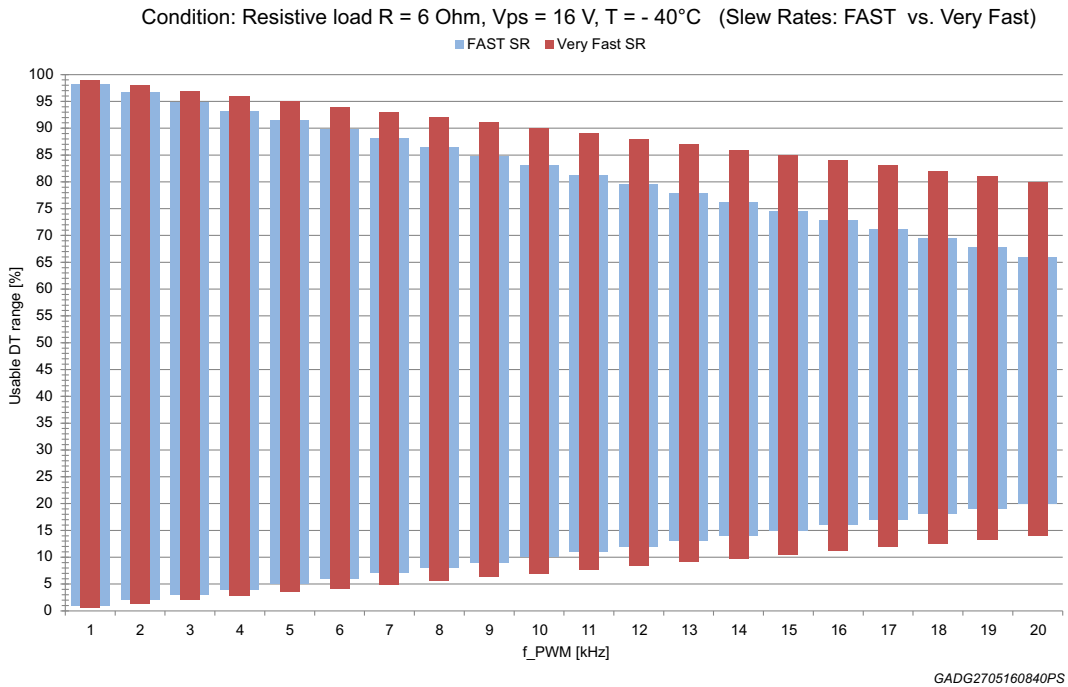
A graphical representation Fast vs. Very Fast for allowed frequencies can be seen below:

Figure 13. DT minimum and maximum on input PWM signal at 16 V diagram



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3.4 Current Limitation and Overcurrent detection

We start assuming PWM=”0” and current is not flowing through the load. At a certain moment, PWM=”1” command arrives. Due to a rising edge on PWM input signal, HSD turns ON, current starts to increase and the diagnosis programmable validation time Tdiag1 starts. After a delay timing (T_{on}), the driven output voltage will follow PWM level setting output to High.

As soon as current reaches ILIMH threshold (TlimH filter implemented) the device switches to NOSR mode, the internal SR control (very fast SR), and the ILIM_REG bit in ONDiagnosis will be set to "1". Tdiag2 timing starts and overcurrent control is now enabled.

The Tdiag2 timing is used to ensure short circuit detection: in case current reaches I_{oc} threshold (Toc filter implemented) before the end of Tdiag2, the device will set the relevant OVC diagnosis bits (OCH0, OCH1, OCL0, OCL1) according to the 4 MOS overcurrent data [(1)] and both outputs will be put in Tristate due to an "overcurrent" event that will have been detected on at least one MOS.

In case of NO OVC (no Ioc threshold reached) at the end of the Tdiag2 timing, the device takes the control, deactivates the VVL mode (if selected), and it enters CURRENT LIMITATION by switching OFF the HSD and forcing an active freewheeling phase on both LSD [(2)] that decreases current during a minimum time t_off_min; this timing is used to assure a minimum recirculation time, so it is not possible to switch ON the HSD regardless PWM="1" user command. (Because of PWM information is still being analyzed, a possible falling edge on PWM before the end of Tdiag2 timing will also trigger the t_off_min timing).

Current continue decreasing due to the LSD active recirculation down to ILIML threshold (with TlimL filter time implemented). ILIM_REG diagnosis bit is set to "0" as soon as current is below ILIML+hyst. After current is below ILIML threshold during at least TlimL AND t_off_min is elapsed, then we exit from CURRENT LIMITATION (still with NOSR active). Being out of Current Limitation, the PWM="1" input signal will be now accepted, so current will increase with NOSR active. The device will exit from NOSR coming back to the user-programmed parameters only if it sees both PWM="0" AND current below ILIML threshold.

1. Load in short circuit (bits NOC=1 Ion_th=1 in SPI diagnosis) is difficult to obtain because its highlighting really depends on application scenario: battery level, selected range of current limitation threshold. Most of the time, a "load in short circuit" will be shown just as one MOS in overcurrent (the one with the lower threshold will put in HiZ both outputs).
2. Current limitation is implemented in LSD only. Therefore the ILIMH threshold on LSD (Four possible selectable thresholds) is used as reference for defining the overcurrent threshold that will be used for:

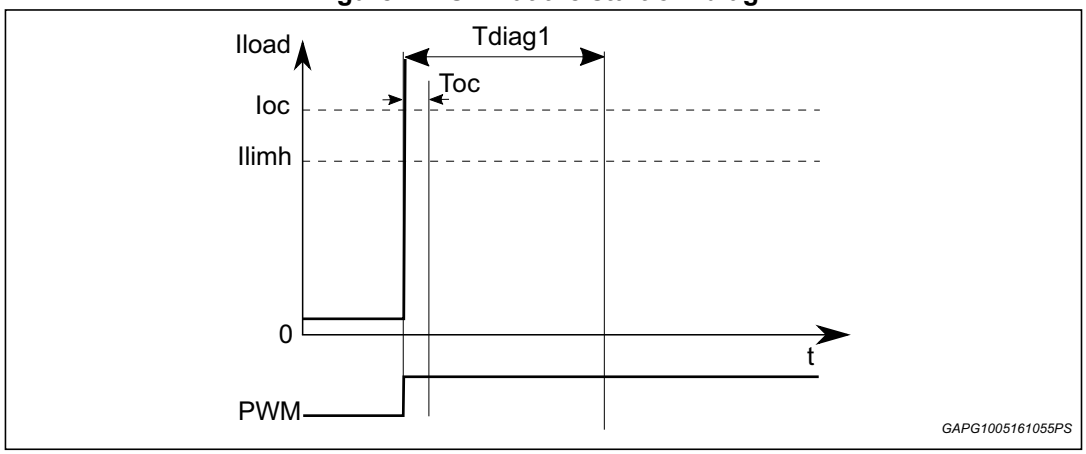
   Short-to-battery on LSD by: Ioc_ls = Itrack_ls + ILIMH

   Short-to ground on HSD by: Ioc_hs = Itrack_hs + ILIMH

Furthermore, apart from the previous explained "OVC in a Tdiag2 with Tdiag1 running", there are other ways to highlight an overcurrent event, that is setting NOC=0 Ion_th=0 in the OCxx[1:0] bits and to increment the OVC event counter. This is done in order to guarantee there is an overall protection against overcurrents preventing from device damages.

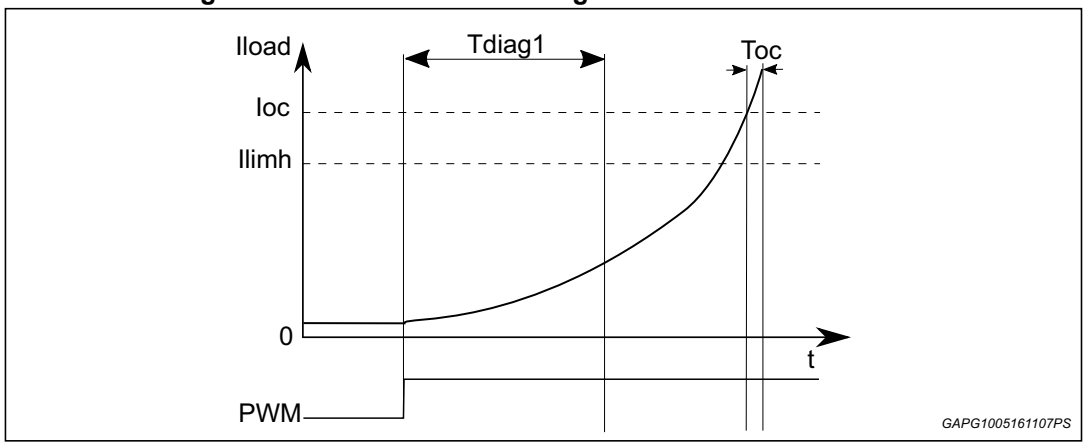
- The device starts the Tdiag1 timer and sees the Ioc threshold has been reached for Toc timing:

Figure 14. OVC at the start of Tdiag1



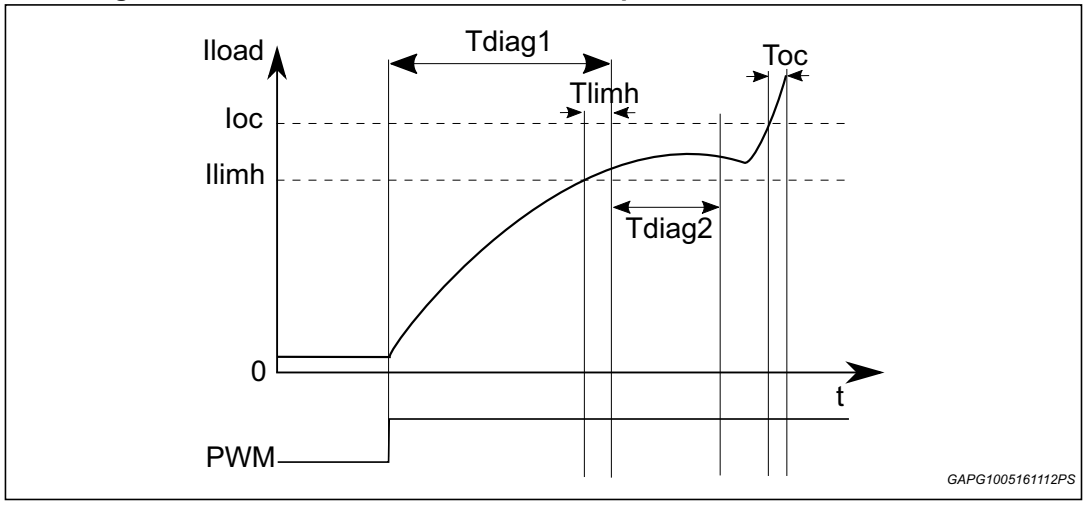
- The device reached neither Ilimh nor Ioc thresholds when Tdiag1 was running but reaches Ioc for at least Toc after Tdiag1 has elapsed:

Figure 15. OVC event after Tdiag1 and current below Ilimh



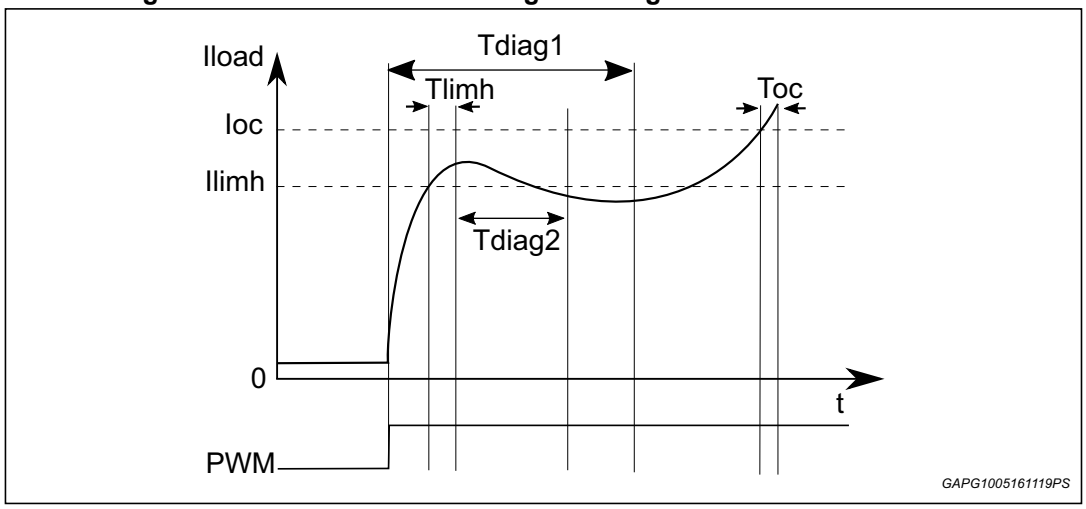
- The device reaches Ilimh threshold during Tdiag1; at the end of Tdiag1 + Tdiag2 current is above Ilimh threshold and grows up reaching Ioc for at least Toc:

Figure 16. OVC event after both timers elapsed with current above Ilimh



- The device initially reached Ilimh threshold, and being the current below Ilimh at the end of Tdiag1 the current grows up reaching Ioc for at least Toc:

Figure 17. OVC event while Tdiag1 running and current below Ilimh



3.5 LSD freewheeling

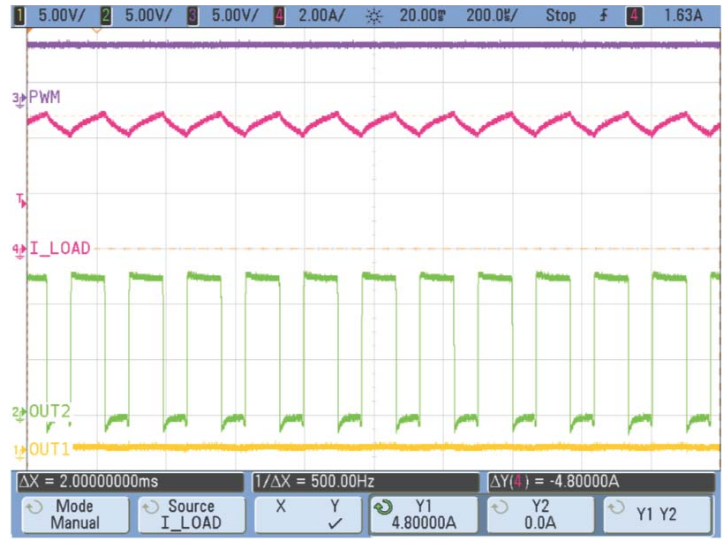
Normal mode by construction makes use of the LSD Freewheeling recirculation both in case of recirculating the current stored in the inductance when HSD switches off and when device is in Current Limitation. *IN1 IN2 mode* uses by construction LSD recirculation when device reaches Current Limitation, but the user can choose between LSD/HSD recirculation in case of recirculating current stored in the load after HSD is switched-off. (See *Section 3.7* for details).

Below an example of LSD recirculation with PWM=2 kHz, DT=40%, no current limitation.

Figure 18. LSD recirculation due to PWM fall edge

On the other hand, below an example with DT=100% and Current Limitation Active (Ilim_th = 4.7 A).

Figure 19. Current limitation LSD recirculation



3.6 Current limitation freewheeling in IN1 IN2 mode

How to enable in IN1 IN2 mode

In order to enable the IN1 IN2 mode, the device inputs IN1 IN2 must be set to LOW before the SPI request being sent.

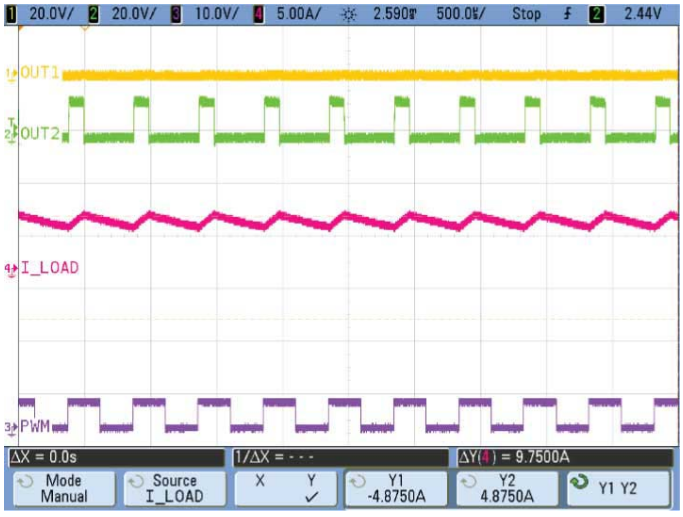
It is not recommended to have any of the two inputs IN1 or IN2 at high level, while changing via SPI the driving mode, in order to avoid unwanted behavior, due to eventually undefined states.The bit In1_in2_if latch in Configuration request 2 register set to "1" provides feedback the IC successfully entered IN1 IN2 mode.

In case of reaching the Current Limitation threshold while driving the device in its IN1 IN2 mode, after filtering time *Tdiag2* has been elapsed, the High Side recirculation will be automatically switched back to the active Freewheeling on Low Side transistors in NOSR mode (fastest slew rates used). During the switching process, the device is protected from suffering Shoot Through phenomena (*Vps* and GND shorted) thanks to the implementation of the T_{SW} dead-time.

LSD recirculation in IN1 IN2 mode

In the below image it can be seen as in IN1 IN2 mode with IN1=0 IN2=PWM (Reverse), even if DT=50%, after reaching load current the defined Current Limitation Threshold $Ilim_H$, the device takes the control and starts the LSD recirculation by itself (red line) in order to force decreasing the load current no matter the PWM input command (violet line) is High.

Figure 20. C_L = 4.7 A, PWM = 2 kHz, DT = 50%



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About recirculation and decay modes

In L9960 device, we will always use what is commonly called as *synchronous Slow Decay mode*. That assertion applies to each one of three possible driving modes of the bridge: normal, VVL, IN1 IN2.

- We refer to *synchronous mode* because the recirculation is implemented using the integrated MOS in a way that assures us a controlled, safer and more effective recirculation path during current decay thanks to a suitable switching of the MOS. This is different from using only internal or external recirculation diodes because the dissipating elements would not be driven, and hence the recirculation would be produced in an asynchronous way.
- By the other hand, the *Slow Decay mode* stands for the technique used during the recirculation which is intended to make use of a same-kind couple of integrated MOS; Low Sides (LSD0, LSD1) or High Sides (HSD0, HSD1). The term "Slow" is related to the time load current takes collapsing to zero during a decay. That is, for example, the case when driving a DC motor with the bridge being set in *forward normal mode*. We keep the LSD1 ON, HSD0 is switched OFF and LSD0 is switched ON. A specific dead-time T_{SW} is implemented between HSD0 and LSD0 transistors switching to avoid *cross-conduction*. As dead-time elapsed, it is produced a synchronized dissipation (resistive) path for the current stored in the inductance. This closed loop allows current to flow between LSD0 and LSD1 until all the energy stored in the inductance has been dissipated. It is well known that the opposite voltage (V_{BEMF}) on DC motor terminals because of abrupt load current variations ultimately lead to higher rotor rotation. The idea is to maintain both motor terminals as shorted as possible by keeping active recirculation on both LSD in order to maintain a constant flux during the decay. Because of Faraday-Lenz Law ($V_L = -\dot{\phi} = -L \cdot \dot{I}_{load}$), larger current recirculation times will produce smooth magnetic flux variations which will induce a relative lower Back EMF compared to Fast Decay. We call this phenomenon "braking the DC motor" or "the collapse of the Back EMF".
  Please, note that the usage of the LSD in the recirculation strategy is just a convention. We could also have chosen the couple of HSD instead of LSD in order to perform the Slow Decay recirculation.

Fast Decay is another recirculation technique which consist in switching ON the HSD1 after switching OFF the LSD1 (dead-time implemented). In this case we would recirculate via HSD1 through the battery V_{ps} in a shorter time than in the case of Slow Decay mode.

This is because the induced Back EMF would be greater than V_{ps} ($V_{BEMF} = 2 \cdot V_{be} + V_{ps}$), but being this situation not possible, the time to decay to zero raises quickly. Load current will disappear fast and the STOP of the motor's rotor would come about in longer times, which is not desired because this behavior avoid determining the position of the rotor precisely. This is the reason the DC motor drivers implement Slow Decay strategy instead of Fast Decay.

3.7 HSD Freewheeling in IN1 IN2 mode

Having enabled the IN1 IN2 mode via SPI, the HSD Freewheeling mode can be chosen in order to make use of the internal High Side MOS body diodes for recirculating load current, in contrast to what is done for the same purpose in Normal mode with LSD body diodes.

During the device driving, IN2=0 IN1=1 (Forward) or IN2=1 IN1=0 (Reverse), HSD Freewheeling is performed by setting IN2=IN1="1".

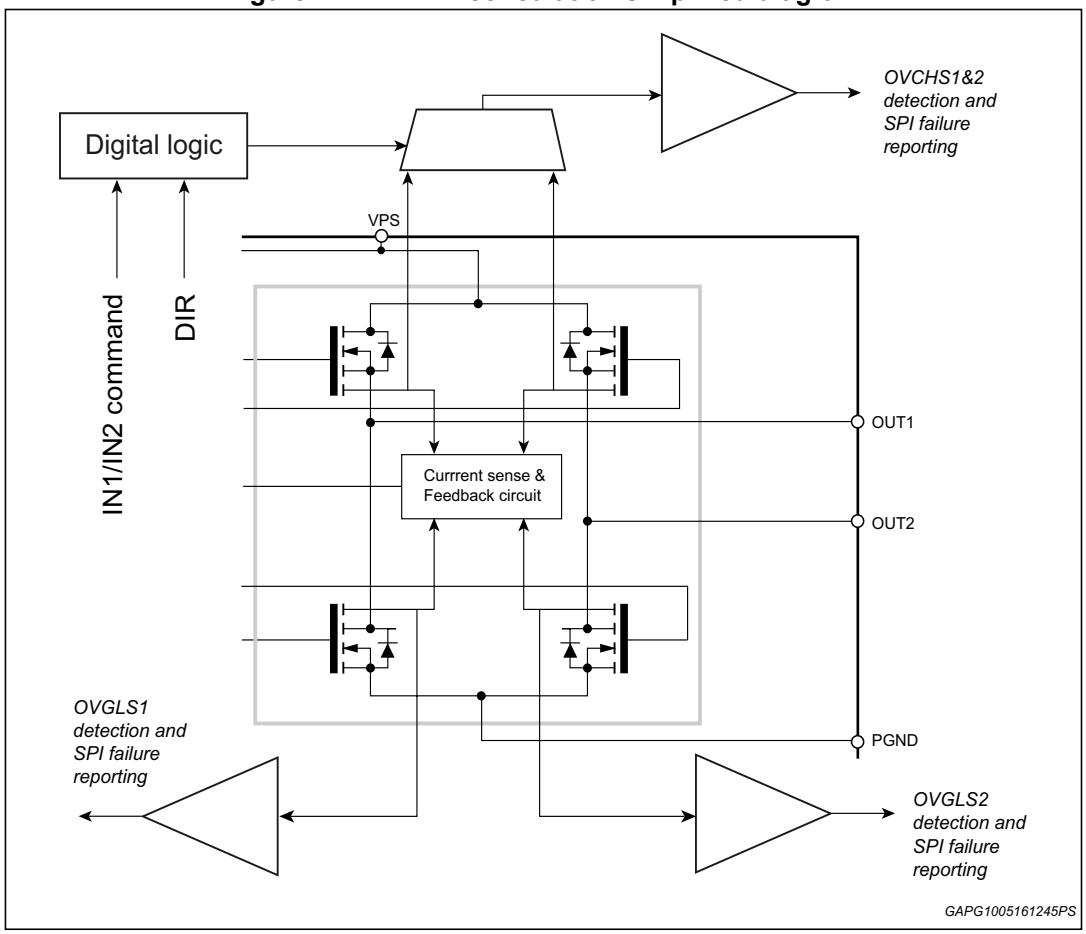
A unique HS driver comparator is present on HS driver stage to detect OVC depending on IN1/IN2 mode command and DIR command. In the active Recirculation phase on LS stage there is a dedicated OVC Comparator for both LS power. The presence of a single comparator does not allow the monitor and detection of SCG failure on both outputs.

Due to a partial coverage against Short-to-Ground event, HSD Freewheeling is strongly discouraged.

It's advised against selecting active phase recirculation on HS drivers when the IN1/IN2 mode is active due to unsafe protection against SCG for both outputs. If the driving preferred mode is IN1/IN2 mode, it's advised to recirculate actively on LS drivers only.

PWM/DIR mode is not affected by the issue, as the recirculation is set to LS drivers by default and independent and dedicated comparators are present.

Figure 21. IN1 IN2 recirculation simplified diagram

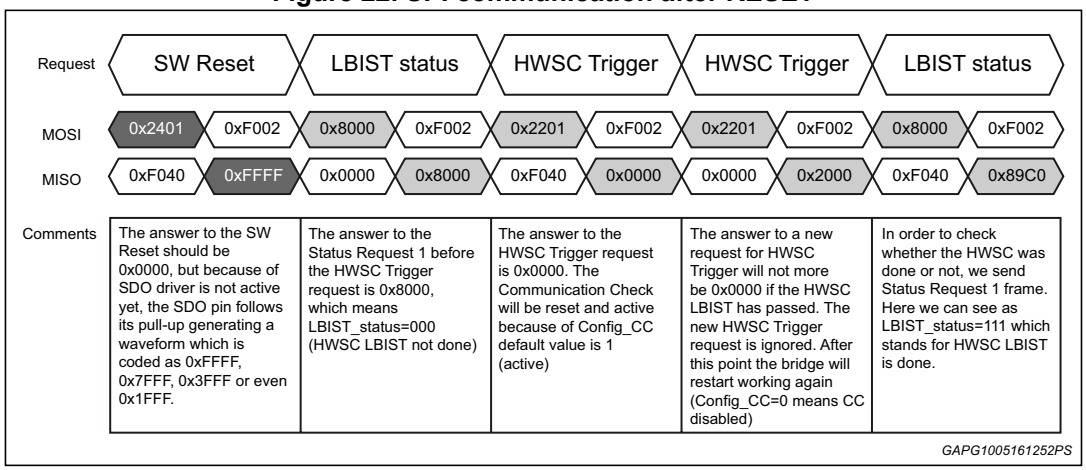


3.8 SPI communication

This section is intended to describe what a user should expect from a SPI communication between ucontroller and L9960.

We here remember that SPI protocol used in L9960 is called *out-of-frame*, that is, a command sent by the microcontroller during transfer n is answered during transfer *n+1*. Here below, an example of SPI communication in case the refresh period T_{spi} is higher than the Communication Check Time (typ. value T_{cc} = 66 ms). In this case we have used a T_{spi} = 100 ms.

Figure 22. SPI communication after RESET



Important thing to note from the above example is that we use SW Reset as RESET condition with NO Communication Check (0x2401), and even if the CC is disabled, the CC will be enabled due to the HWSC Trigger.

The $T_{spi} > T_{cc}$ will cause a CC error that prevents the bridge from start working again after successful HWSC checked and passed (LBIST_status=111) at the next PWM rising edge.

With the intention of receiving the answer to a desired command, a dummy frame is used, which in our case is the #15b "Silicon version request" (0xF002) [3].

Communication check

In order to avoid the CC error and the second "restart trigger" frame after every RESET condition, we suggest to use a dummy frame like "Silicon version request" (0xF002) to be sent with a refresh period of $T_{dummy} < T_{cc}$ *(e.g.* T_{dummy} *= 40 ms)*.

3. The SPI answer to "Silicon version request" (0xF002) in AC silicon revision is 0xF040.

3.9 Configuration registers

This section has been added in order to explain some behaviors either in case of fault on SPI communication that flips one bit or the accidental set of the single-value and dedicated *device configuration register bits*.

Let's take a closest look at each $Configuration_k$ 16-bit SPI frame: [4],[5]

Word ID #3, Configuration 1:

D[1] bit in the SPI frame must be set to "1".

In case this bit accidentally changes its value, the behaviour on Output will be a PWM ON time (T'_{ON}) about ΔT_{ON} = 5 µs longer than the expected PWM ON time (T_{ON}), what depending on thePWMfrequency used could have appreciable effects (e.g. +5% @10kHz).

Word ID #4, Configuration 2:

D[1] bit in the SPI frame must be set to "0".

In case this bit accidentally changes its value, the behaviour observed will be a slope in the Thermal current limitation adjustment, that is $Ilim_H$ current threshold will dynamically decrease with temperature using a different slope by ending in any case at the OT_{sd} threshold as in datasheet described.

Word ID #5, Configuration 3:

D[5]..D[1] shall be set to '0_0000'.

POR value for this bitfield is '0_0000', however any alteration does not introduce a different behaviour because the whole SPI frame will be discarded. A new 16-bit frame containing the desired configuration together with D[5]..D[1]='0_0000' shall be sent if a configuration different from default one is desired.

Word ID #6, Configuration 4:

D[8]..D[0] bits status have no effect on device behaviour.

Even though, after any RESET condition this bitfield is set at its POR value '0_0111_1101', it is not processed by the logic as whatever other configuration.

The bitfield status is mirrored in bitfield R[9]..R[1] in answer frame # 7d.

4. Because we are here dealing with the abnormal setting of configuration bits, the proper value as in datasheet described shall be newly set.
5. The undesired change in other configuration bits different from the below ones falls into the functionality domain and the behaviour can be found in datasheet.

3.10 TSW low current function

The *TSW_low_current* function introduces a strong dependence on external conditions and influences the treatment of internal signals, in particular it activates the dynamic Freewheeling phase based on feedback coming from the current flowing through the load *i_on_out*.

Because of a very low currents the *i_on_out* status becomes highly sensitive to current oscillations and the lack of a *non-zero current* signal prevents the device from starting the active Freewheeling phase (which is something within the bounds of possibility), the function's usage cannot be generalized for all applications and loads and therefore it must be disabled by setting TSW_low_current="0" in the SPI command #3 (*Configuration1*).

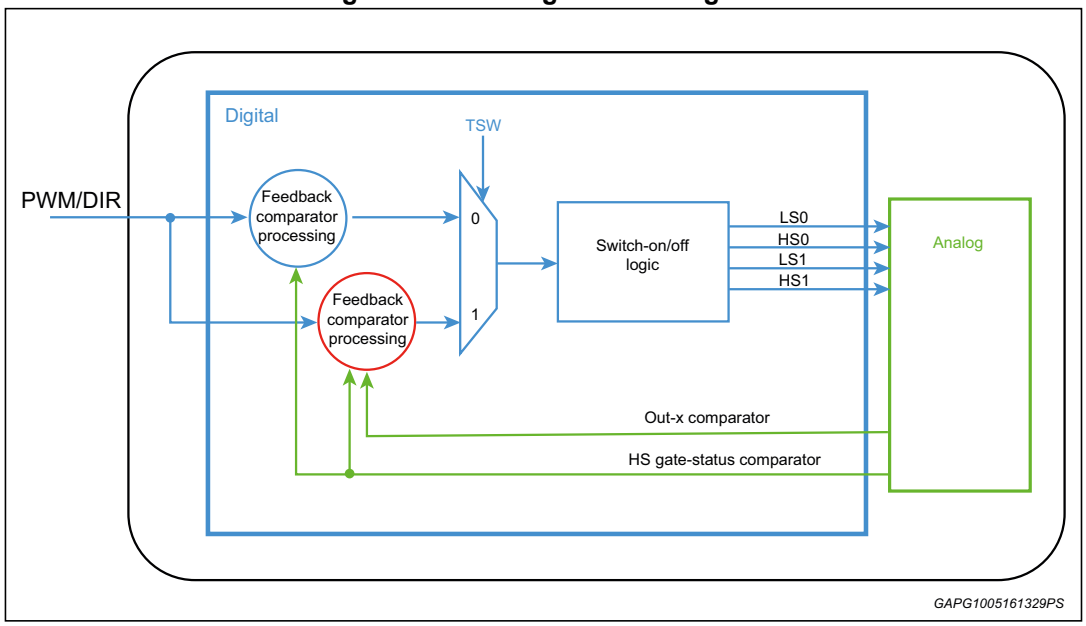
Function disabled, TSW_low_current="0" (value to be explicitly set)

Logic has a fixed time (2.2 µs) between HS gate status and LS switch-ON which is independent from external load conditions. Please, keep in mind that after any RESET condition such as Power on Reset, Software Reset, or at the end of the LBIST, whole SPI register map will be reset to its POR value which in case of TSW low current function means "function enabled" making necessary to newly set TSW_low_current="0". A violation can bring to an unexpected lock condition just because active Freewheeling phase will not actually start.

Function enabled, TSW_low_current="1" (POR value)

The TSW low current feature was developed and debugged in specific scenario (i.e. DIR change when PWM=0). Logic expects a specific sequence of analog comparators. The sequence of comparators activation can be different from the expected one considered at the beginning based on external condition: battery value, type of motor, PWM duty cycle, frequency, etc. Nevertheless, if the customer decides to use this feature, the customer should know that the feature has to be carefully analyzed in order to avoid the known and quite possible locking condition above described.

Figure 23. TSW logic block diagram



3.11 DIS, NDIS and SOPC

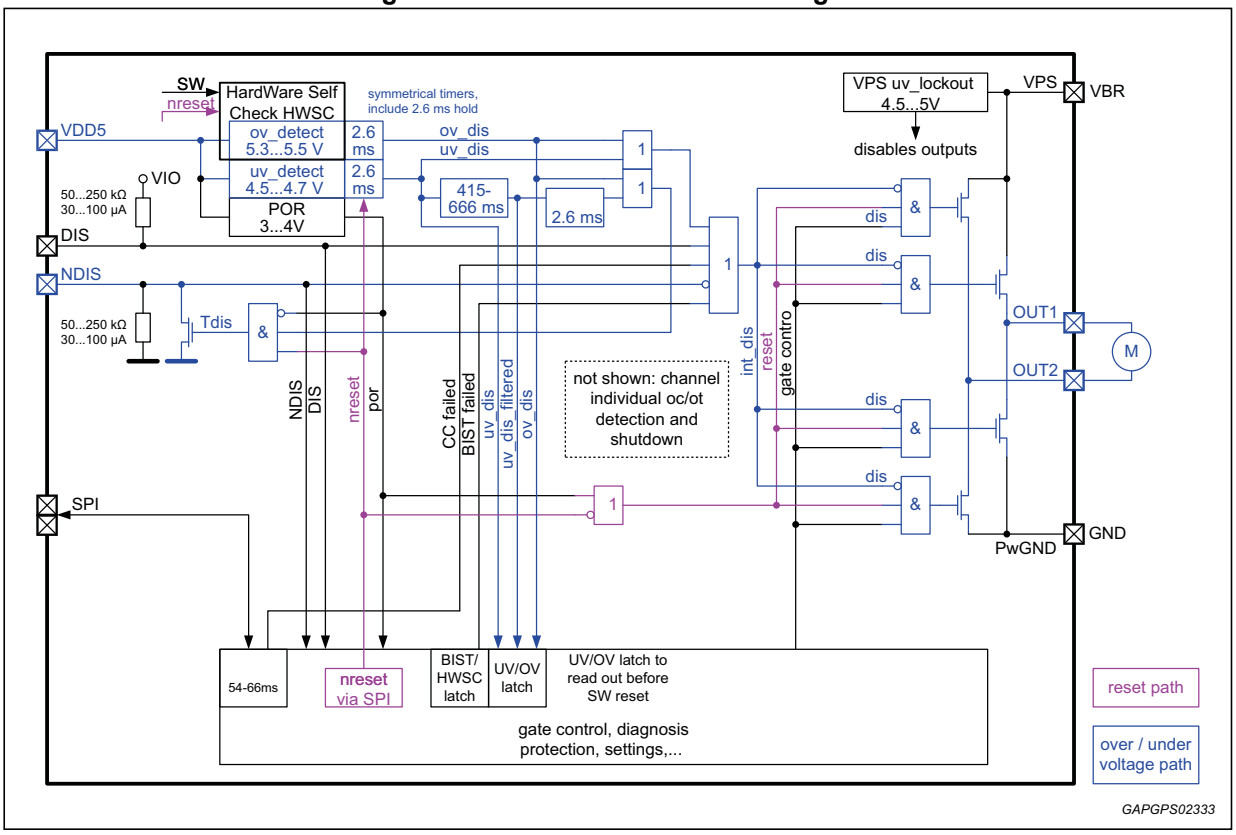
The digital input DIS and the digital bidirectional (input/output) NDIS are both disabling pins managed by the ucontroller. In order to double check the status of the device, a SOPC (Switch-off Path Check) procedure can be performed. In case the ucontroller decides under a particular set of conditions to disable the bridge, an action which can be done by putting DIS=1 or NDIS=0, there exist two *real time* bits called DIS_status and NDIS_status that can be monitored by reading them back through SPI in the answer to *Status-request1* (0x8000).

It is important to note that in case of the Vdd5 UV/OV Fault has been pointed out by the diagnosis, the NDIS pin will be internally put to LOW no matter the ucontroller command.

These are the unique cases the bidirectional functionality of NDIS is used in L9960 (NDIS becomes an OUT).

Either the ucontroller programmed action on DIS/NDIS and a Fault that put into Hi-Z will put the *bridge_en=0*. (see *Section 3.13* for details).

Figure 24. DIS/NDIS architecture diagram



3.12 Tristate procedure

When DIS pin is set to HIGH, the device "Enters in Tristate". At this time the only possible diagnosis is the OFF-Diagnosis (ON-Diagnosis is not available). In order to perform the OFF-Diagnosis, DIS signal has to remain HIGH at least for a minimum time T_{hz} (typical value T_{hz} = 250 ms) as in datasheet described. Once we are sure no Faults are present in the OFF-Diagnosis, we can put DIS pin to LOW, this way the device "Exits from Tristate".

The action of exiting from Tristate implies a procedure involving timings that has to be carefully respected.

Entering in tristate procedure

- DIS rising edge
- DIS HIGH

WAIT with DIS HIGH for at least 250 ms (if not respected, the OFF-Diagnosis will not be triggered and answer to frame #9 will be 0x9006).

Exiting from tristate procedure

- DIS fall edge

WAIT with DIS LOW for at least 1 µs[6] until the rising edge of IN1 or IN2 pins.

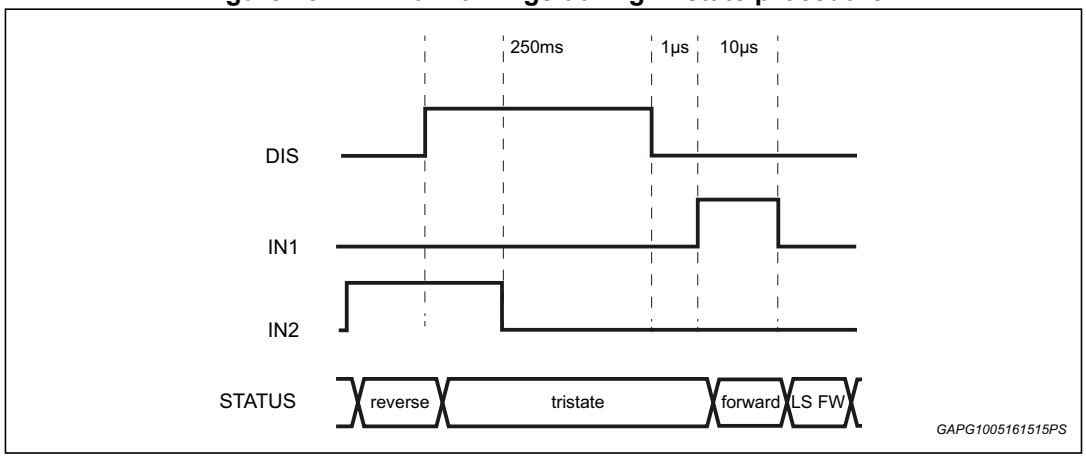
- IN1 **or** IN2 rising edge (for IN1 IN2 mode).

WAIT with IN1 **or** IN2 HIGH for at least 1 µs minimum pulse duration[7].

- PWM rising edge (in normal mode).

The rising edge of the chosen signal, (IN1 **or** IN2) will be seen as the valid PWM signal rising edge that cause the device exiting from Tristate and start working again based on the state of IN1/IN2 input signals.

Figure 25. Minimum timings during Tristate procedure



In case of PWM/DIR mode, any toggling of DIR input (on both directions) in correspondence with the first PWM rising edge, after the device power-up, must be avoided.

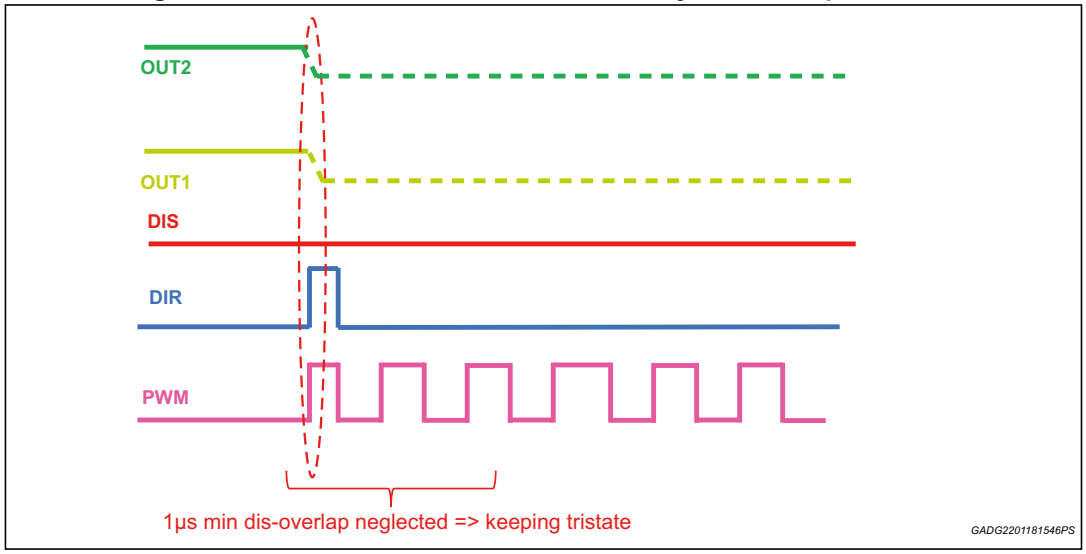
The same requirement is valid in case of IN1/IN2 mode. In correspondence of the first IN1 (or IN2) rising edge, IN2 (or IN1) must be stable.

6. This "1 µs delay" is a Design restriction, it is an internal timing needed to corretly perform the "Exit from Tristate" procedure. It has to be assured by customer this minimum timing is not violated. For application scenarios in which synchronicity between signals can be lost, it is recommended to use higher delays between DIS fall edge and IN1 or IN2 rising edge. We here recommend to use at least 10 µs delay.
7. By the other hand, this timing should be respected in order to let the logic rightly understand the command (High / Low). **We here recommend to use at least 10 µs delay**. For application values, please see *Section 3.3*.

A minimum dis-overlap of 1 µs between these two input signals shall be respected, otherwise the H-Bridge stage cannot exit from Tristate, and enters in a self-protection state.

As showed in the images below, taking as example PWM/DIR mode, once the H-Bridge stage is locked in tristate, due to the violation of this dis-overlap, it remains in this condition even if actuation trials are performed, simply toggling PWM input.

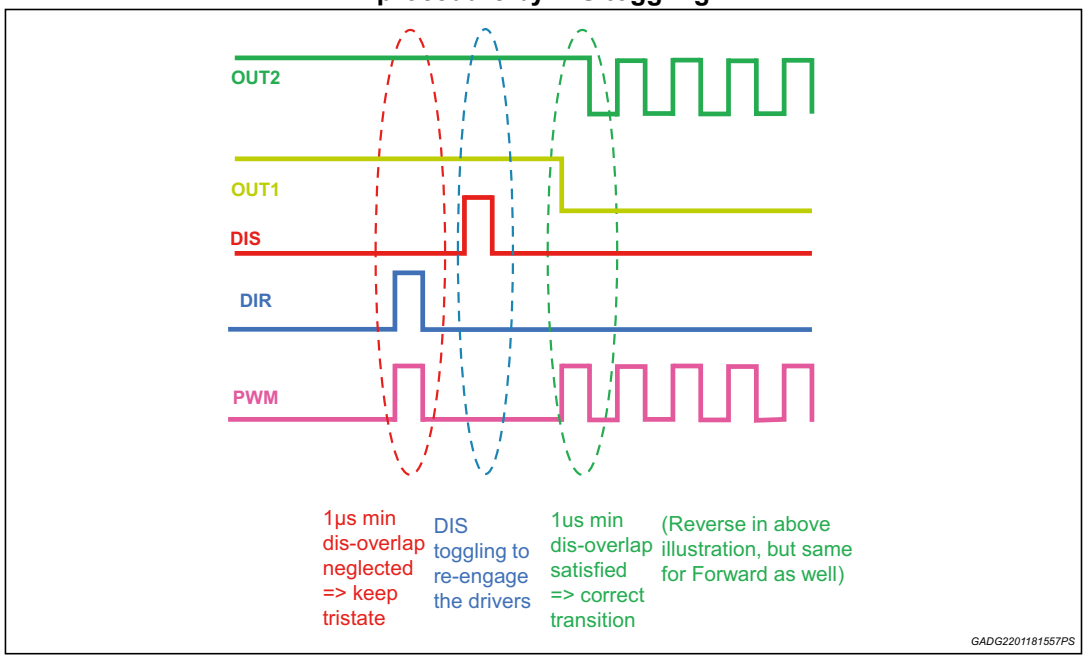
Figure 26. Tristate Lock condition caused by dis-overlap violation



The way to exit from this locked condition and re-engage the bridge is DIS input toggling, as required whenever any faulty condition puts the stage in tristate.

Once this is toggled, a PWM input rising edge, makes the driver enabled (see image below).

Figure 27. Tristate Lock condition caused by dis-overlap violation and re-engagement procedure by DIS toggling



3.13 General diagnosis

This section aims to explain the process of dealing with Faults in L9960. That can be possible by understanding the Diagnosis Strategy. The H-bridge has two possible diagnosis implemented, Off- and On-state Diagnosis:

3.13.1 Off-state diagnosis

Off-state Diagnosis is only applicable during the *disable* state of the device, that is when DIS pin is set to HIGH. If we send a request for triggering the Diag-Off diagnosis (0x9002), we have to notice that if during the on-state there was a previous fault reported in NGFAIL (NGFAIL=0), then the Diag-Off is not allowed. So, in order to make the Diag-off available, firstly we have to clear the NGFAIL bit by an SPI read (DIAG_CLR_EN=1) before requesting for a Diag-Off.

Even if Diag-Off is allowed, there is a minimum time we have to wait in order to have the Diag Off done, this time is 250 ms. If the time DIS=1 is however t < 250 ms, then Diag Off is not done, so the response on MISO will be "111". But if we wait for the necessary 250 ms, the diagnosis will be done, and a different value from "111" will be obtained. Errors covered by Off-state Diagnosis include: Short to Ground, Short to Battery, and Open Load. Nevertheless, when the falling edge on DIS arrives, all the registers will be reset, and because the default value for *Diag Off state* is "111", we will newly obtain "111" on the response field.

In order to check for the presence of faults when device is *disabled*, *Diag-Off* must be always requested (0x9002 TRIG=1), and disabled (0x9001 TRIG=0) in order to see the result of Diag-Off process on SPI register. Please pay attention to that, because if Diag-Off is not requested, it will not be performed, and consequently the errors in the *disable* state covered by Diag-Off diagnosis will not be reported.

Practical cases

Here below some scenarios that can be faced when dealing with the bridge and it is desired to perform Diag-OFF.

Case 1. You are in “normal mode” with no fault (NGFAIL=1), then you decide to put the bridge into tristate with a rising edge on DIS pin in order to perform OFF-Diagnosis. The Diag-Off is allowed and will be performed if DIS is HIGH for at least 250 ms.

Case 1.1 The case of performing several Diag-Off: If an Open-Load is performed at bridge disabled, the OL flag will be set in SPI registers after sending the sequence:

0x9002 (TRIG=1) -> 0x9001 (TRIG=0)

After having removed the OL event, a *new sequence* will result in “No failure / Diag done”. If now we force a Short-to-ground, the fault will be available in SPI registers by newly perform the *sequence* resulting in a “Short-to-Ground” in OFF-Diagnosis.

Case 2. You are in “normal mode” and arrives a fault that puts NGFAIL=0. Because of NGFAIL=0, Diag-OFF is not allowed. Nevertheless, you could perform Diag-OFF in the following cases:

Case 2.1 You clear the ON-Diagnosis putting newly NGFAIL=1. *(You know there was a fault, you removed the fault, and you decide to go ahead and perform Diag-OFF)*.

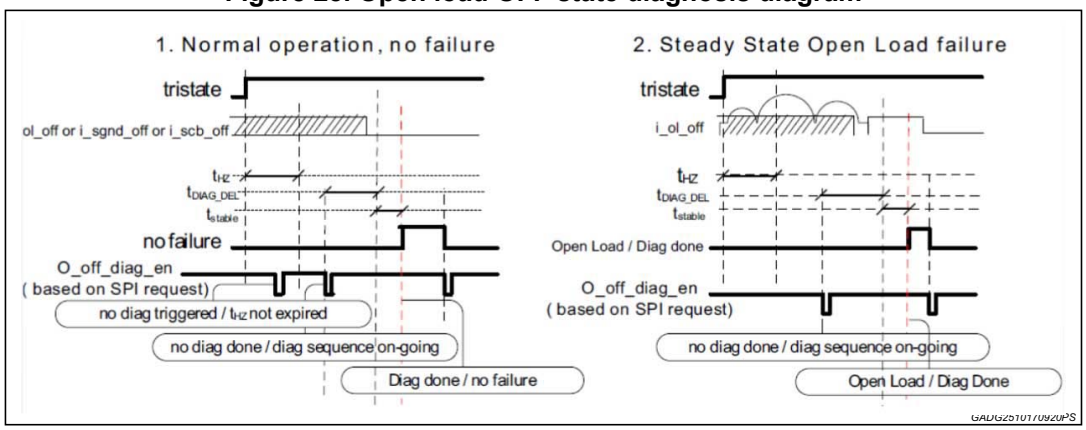
Case 2.2 The only way to perform OFF-Diagnosis with NGFAIL=0 is that the Fault which puts the NGFAIL to “0” is one of these set: Short2Battery, Short2GND, or Open-LoadOFF. *(This situation is intended to remark you can perform several diags. during DIS=HIGH, and even if NGFAIL=0 you can continue asking for new Diag-OFF)*.

Open load in OFF issues

The timings required for OFF diagnosis are shown in the *Figure 28* and reported in product datasheet. Starting from DIS rising edge, once the time t_{HZ} is elapsed, the OFF diagnosis can be activated by SPI request (TRIG bit). Once the diagnostic procedure is triggered via SPI, a T_diag_del blanking time (typ 750 µs) is applied, in order to allow the internal nodes reaching stable values. During the blanking time, the diagnostic comparator output is actually ignored.

Only after blanking time elapsed, the OFF diagnosis is started, lasting Tstable_off time (typ. 40 µs). If the diagnosis comparator output is switching during Tstable_off, the filter time is retriggered at each edge. The diagnostic is actually confirmed as reliable only when the comparator output remains stable during the total Tstable_off time.

Figure 28. Open load OFF state diagnosis diagram



The OFF diagnosis could be sensitive to noise and coupling of disturbances (antenna effect), considering that the current involved during OFF diagnosis (performed by current comparisons) is in the order of the µA (the same order of magnitude of the disturbing signal). This could happen, in particular way, in case of applicative environments with long wire harness between the ECU and the motor, where it is more likely to have such a kind of parasitic coupling.

Moreover, in case of Open Load, no current is sourced or sink by the ASIC. However, the boundary between Open Load detection zone and No Faults zone (load connected), could have very low values (the lowest is 30 µA), and a glitch coming to OUT1 can induce, even for a short time, a spike of current whose amplitude is enough to produce a wrong diagnosis result.

This happens, more precisely, if the glitch triggers a change at the output of the comparator (after being stable for all the duration T_stable_off) just at the time of the cycle when the diagnosis result is updated into the internal register.

The eventual spurious diagnostic can be actually avoided through a proper filtering strategy implemented into the application software.

By the way, an alternative countermeasure may be to introduce, a hardware filter, by increasing the value of the capacitors connected to OUT1 and OUT2. By the way, the effectiveness and feasibility of such a hardware countermeasure should be evaluated case by case, depending on the minimum ON/OFF time, ie depending on the maximum PWM frequency with minimum or maximum duty cycle applied.

In the following, a few calculations in order to estimate the maximum allowed value that is able to ensure the correct device functionality, on what concerns the behavior in OFF condition.

The limiting parameter is the time T_diag_del (time required to have on OUT1 the final value fixed by the internal voltage regulator, starting from battery level), that, in the worst case is 600 µs (the shortest value).

The following condition (worst-case) should be satisfied:

$$t = (C * V\_max) / I\_min < 600\ \mu s;$$

where I_min = 1.5 mA (from data available from the device characterization).

$$V\_max = VB\_max - V\_reg\_min = 18\ V - 1.3\ V = 16.7\ V.$$

We should, therefore, have:

$$C < ((600\ \mu s) * I\_min) / V\_max;$$

Replacing the values above we find that the maximum value for C is 54 nF.

3.13.2 ON-state diagnosis

In order to have the Diag-On diagnosis active, the DIS pin has to be set to LOW. The *realtime* state of the bridge is reported in the *bridge_en* response bit and its meaning is as follows: If the bit *bridge_en*=1, then the H-bridge is in ON state, but if *bridge_en*=0 the H-bridge is in *3-state*. In both cases the applicable diagnosis is the On-state diagnosis.

Note: The check for the Open Load in on-state is not done if the bridge is in limitation.

List of Faults covered by the L9960 On-diagnosis (Disabling and Non Disabling Faults):

1. Disabling faults:

Both DISABLE and TRISTATE states put OUTPUTS in Hi-Z, which in L9960 represents a Battery voltage level because of the presence of pull-ups on OUTPUTS. The difference between DISABLE and TRISTATE is only from the logic point of view. The logic block needs the "initialization procedure" described below in order to unlock latched bits.

1.1. Real-time monitored faults:

OUTPUTS in TRISTATE. Even if the information regarding the Fault remains in the latched bits, after fault condition disappears, the bridge restarts working again because the relative real-time bits do not highlight fault condition any more. The cases are two:

VPS UV = Battery undervoltage;

TSD = Thermal shutdown.

1.2. Initialization-procedure-required faults:

OUTPUTS DISABLED. Therefore, after fault condition disappears, toggling on DIS pin and wait for the next rising edge on PWM are actions required to restart working again. This required procedure is called "the initialization procedure" and affects to:

OVC = Overcurrent;

VDD OV = Vdd5 overvoltage;

VDD UV = Vdd5 undervoltage;

CC Error = communication check Fail.

2. Neither disable nor tristate faults:

Those faults which perform no action on OUTPUT stage in case of flag set. The Fault to consider is only visible in the diagnosis data. Below, there are some examples:

OL ON = Open load in active;

I LIM = Current limitation;

OTWARN = Over temperature warning.

A detailed table containing the Faults covered by the On-Diagnosis can be found below.

Table 4. ON-Diagnosis faults

Issue to consider	Realtime bit	Latched bit	Effect on Output	DIAG_ CLEAR_EN(1)	Effect on latched bits after SPI read	Action for coming back to operating
VPS UV	VPS_UV	VPS_UV_REG	Tristate Tristate	1 0	POR value Kept value	No action No action
Two VPS UV events in a time window	–	UV_CNT_REACH (if UV_PROT=1)	Tristate Disabled	1 0	POR value Kept value	Next PWM DIS + PWM
TSD	NOTSD	NOTSD_REG	Tristate Tristate	1 0	POR value Kept value	Next PWM Next PWM
OVC	–	OCHx,OCLx	Disabled Disabled	1 0	POR value Kept value	Next PWM DIS + PWM
VDD OV(2)	VDD_OV	VDD_OV_REG	Disabled Disabled	1 0	POR value Kept value	Next PWM Next PWM
VDD UV(2)	VDD_UV	VDD_UV_REG	Disabled Disabled	1 0	POR value Kept value	Next PWM Next PWM
CC Error	–	CC_latch_status	Disabled Disabled	1 0	POR value Kept value	Next PWM DIS + PWM
OL ON	–	OL_ON_STATUS	No effect	X	POR value	No action
OT WARN	OTWARN	OTWARN_REG	No effect	X	POR value	No action

1. Not reading a latched bit is an action equivalent to read it using DIAG_CLEAR_EN=0. After that, the additional action for exiting from TRISTATE is functionally equivalent to exiting from DISABLE using DIAG_CLEAR_EN=1.
2. Because of NDIS pin goes LOW, there is no need to perform toggling on DIS to come back to normal operating.

3.14 Open load in active mode

This section is intended to describe the behaviour of our device when bridge is working in *Normal mode* and the load is suddenly removed. There is the extra possibility of using Open Load detection in *IN1 IN2 mode* in the Reverse direction, which means IN1=0 and IN2 switching. (Forward is forbidden).

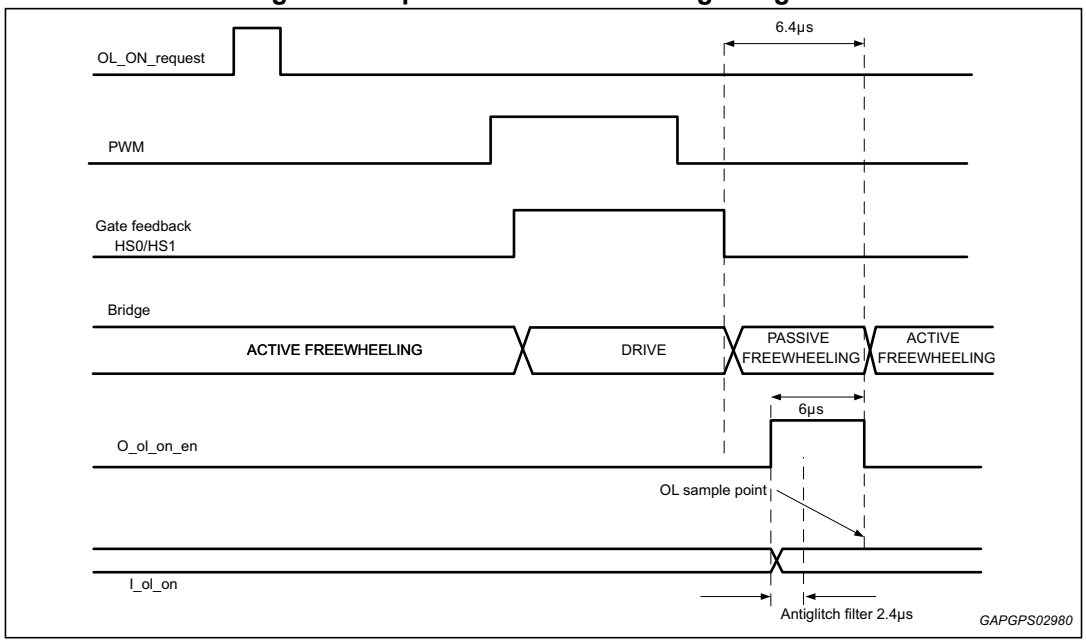
Open Load in Active is available only if the relative diagnosis is requested (OL_ON = 1).

If the OL in Active is already triggered (OL_ON=1), even if its cancellation is requested before PWM fall edge (OL_ON=0), the OL in Active check will be performed. L9960 checks for the Open Load while bridge is in its *Passive Freewheeling* phase. When Open Load request is sent, the Freewheeling time T_{SW} is enlarged up to cover a time window of t = 6.4 µs, which starts with the falling edge of *Gate Feedback H0/H1* signal. This timing is made up of: o_ol_on_en signal which lasts HIGH for 6 µs, and other 400 ns (which corresponds to a time equal to two clock cycles) added because of re-synchronizing purposes.

A digital degliching filter has been implemented in order to assure the proper Open Load detection, it has a value of t = 2.4 µs (400 ns of re-synchronization already considered). That is the time during which the output of OUT comparator *(i_ol_on signal)* will be masked. Deglich filter starts after *o_ol_on_en* signal rise edge comes up. The final value Open Load / No Open Load will be write into SPI register at the falling edge of *o_ol_on_en* signal. Open Load status is coded in two bits and could be subsequently obtained as part of the 16-bit SPI frame as answer to *status-request2* command (0x8003).
After time window for the Open Load detection is finished, the bridge is put in its Active *Freewheeling* phase allowing to efficiently dissipate the energy stored in the load.

Here below the timings involved in the Open Load detection in case the cross-conduction low current filter is disabled (*TSW_low_current* = "0"). By the other hand, if due to a reset condition the cross-conduction filter is active (*TSW_low_current* = "1"), what we will obtain is a similar picture, but this time the trigger for the Open Load check will be the more lasting signal between *Gate Feedback H0/H1* and *i_on_out*. (Please see *Section 3.10*).

Figure 29. Open load in active timings diagram



3.15 Diagnosis reset strategy

When diagnosis bits are latched they can only be released by one of these conditions:

- Transition from "Disable" (High) to "Enable" (Low) on DIS pin.
- Reset condition: Power On Reset or Software reset.
- Diagnosis register read by SPI depending on DIAG_CLR_EN bit status.

1) Transition from "Disable" (High) to "Enable" (Low) on DIS pin

In order to assure the Disable signal is active, it must remain a minimum of 5 µs HIGH. After this filtering time, the bridge is put into disabled mode. The bridge exits from disabled mode by the DIS falling edge, and will definitely come back to the normal mode at the next PWM raising edge if (DIS=L && NDIS=H). (Please, see section *Section 3.12* for details).

2) There are two possible Reset conditions: Power on reset or software reset

2.1) Power on reset: When V_{DD5} is below *Vdd5_por* threshold, the POR (an internal low active signal) is set to LOW and the bridge is put into RESET state. After 300 µs the POR signal is released putting the bridge into *3-state*. In order to exit from *3-state* in a safer way, we could send a request for the LBIST trigger, and if at the end of the HWSC/LBIST check the result is successful (no problems found), then the bridge is put into *disable state* waiting for the next raising edge of PWM for turning back to the *normal state*.

2.2) Software reset: It acts only on digital parts of the device. The SPI command sequence in "restart trigger" register in case of Communication Check disabled could be:

– 0x2401 → SW reset - active

– 0x2201 → request for HWSC/LBIST

– 0x2000 → HWSC/LBIST not requested

HWSC/LBIST

After HWSC/LBIST=111, the bridge exists from 3-state. As long as the HWSC/LBIST has not been performed (indicated by the signal HWSC/LBIST_done = "0") the bridge outputs remain disabled in tri-state. The full HWSC + LBIST process lasts for t=4.5 ms.

Regarding the need of sending two times the HWSC Trigger request:

If there is no SPI communication (SPI frame) sent in a time interval of T_{cc} = 66 ms, it will cause a CC error (NGFAIL=0) after HWSC Trigger (0x2201) because the HWSC Trigger resets Config_CC to the default value "1" enabling the Communication Check. In case that SPI frame refresh period is higher than T_{cc} time, the device outputs are switched to tri-state and are reactivated again with the next SPI frame if "Config_CC=0". Therefore, if $T_{spi} > T_{cc}$, a second "restart trigger" frame with bit Config_CC=”0” (either 0x2000 or 0x2201) is required in order to restart working again after the HWSC has passed. This second HWSC Trigger request will be ignored if HWSC_LBIST=111 (passed), however the Communication Check will be disabled allowing to restart working again (CC by-passed). (Please, see *Section 3.8* for details).

By the other hand, if the SPI communication is send in a time Tspi < Tcc there is no need to send 2 times the HWSC Trigger, the bridge will start working again because no CC error.

3) Diagnosis register read by SPI depending on DIAG_CLR_EN bit status

Here below the latched bits dependence with respect to DIAG_CLR_EN bit state and the value we will obtain after an SPI read into the proper register of those latched bits. Value can be kept or can be reset to default value (referred as POR value):

Table 5. Diagnosis registers and DIAG_CLEAR_EN dependence

Lathed bit ID	DIAG_CLR_EN	Result on bit(s) after SPI READ
VPS_UV_REG	1	POR value
	0	keeps value
VDD_UV_REG	1	POR value
	0	keeps value
VDD_OV_REG	1	POR value
	0	keeps value
NOTSD_REG	1	POR value
	0	keeps value
OCH0, OCH1, OCL0, OCL1	1	POR value
	0	keeps value
Error_count[3:0] (Over Current event counter)	1	POR value
	0	keeps value
DIAG_OFF[2:0] VDD_OV_L[2:0] ILIM_REG OTWARN_REG OTSD_CNT OL_ON_STATUS CC_latch_status	X X X X X X X	POR value POR value POR value POR value POR value POR value POR value

The below sentence is an example of what described in the Diagnosis Reset Strategy for the latched bits:

"In case of DIAG_CLR_EN set to LOW, the over-current, over-temperature diagnostic bits can NOT be cleared by SPI read and therefore, the bridge is kept in tri-state until a transition from LOW to HIGH on DIS pin or RESET condition."

It refers to the case of those errors which could lead to a dangerous situation (like overcurrent). In those cases, after the bridge is put in Hi-Z due to the fault, if we do not want to continue working after a diagnosis READ, then we have to be sure that DIAG_CL_EN="0".
At this point we can exit from 3-state only by a (SW reset ‖POR‖ toggle on DIS pin), but not after a SPI READ of the diagnosis.

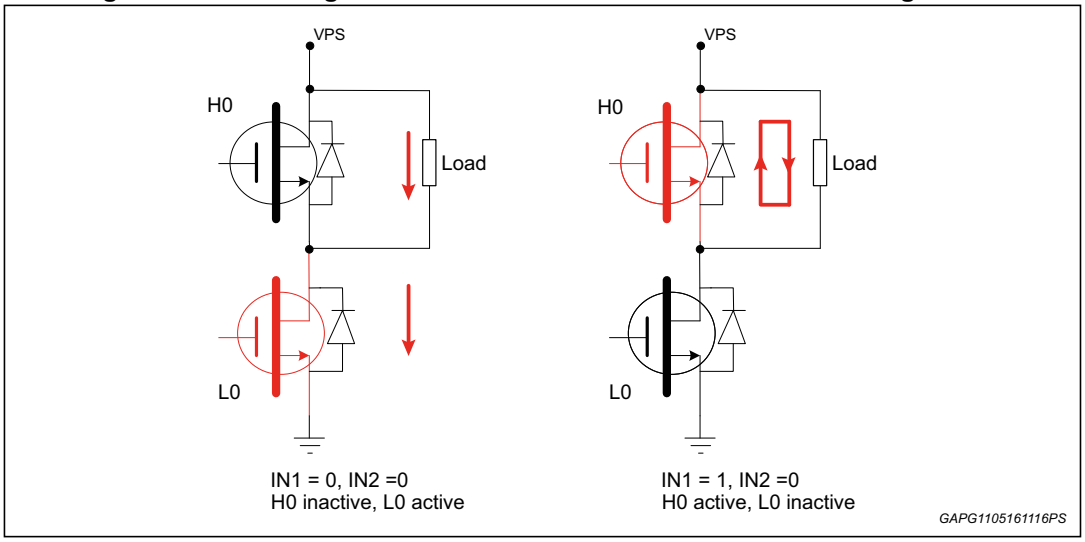
3.16 LSD driver vs. H-bridge configuration

L9960 can be configured as low–side driver by connecting the load between OUT1 and battery with OUT2 floating; this kind of configuration is often used for driving external solenoids. The selected mode for taking advantage of the LSD driver capability is the IN1/IN2 mode, and it has to be configured with IN1 toggling and IN2 = "0".

Some considerations have to be taken into account when using LSD configuration instead of H-bridge configuration (the recommended configuration) in terms of Diagnosis response. The set of available diagnosis will be slightly different and some thresholds differ from the ones present in the H-bridge configuration.

This is how the LSD driver configuration works (For the H-bridge, see *Figure 1*):

Figure 30. How integrated MOS work in the Low-Side driver configuration



For characterizing the LSD driver configuration ON/OFF diagnosis availability we have used a load R = 2.5 Ω , L = 150 mH.

Please, note that this value of inductance is higher than the maximum described in Datasheet for the H-bridge configuration (Please see table 5 in L9960 Datasheet for the maximum allowed RL load in H-bridge configuration). However, because from the LSD point of view the inductance value has a low weight on diagnosis results, when we are working in LSD driver configuration, we can use values of inductance higher than the one present in Datasheet for the H-bridge configuration.

ON state diagnosis

L9960 has some diagnosis that will link the behaviour of an output with respect to the other one. For example, in H-bridge configuration the Current Limitation switches OFF the driven HSD forcing both LSDs to recirculate, this is possible because we use a load connected between both outputs and make use of that close circuit to dissipate an excess of load current.

However in LSD driver configuration there is no load connected between outputs, therefore some ON Diagnosis will have different interpretation based on which configuration we are using: H-bridge or LSD driver.

Below we summarize what is working different or not working in the ON Diagnosis when we use LSD driver instead of H-bridge (taken as reference).

Table 6. ON diagnosis table comparison

Configuration	Short to Vps	Short to GND	Open load in ON	Current limitation	Current limitation thermal reduction
H-bridge	Working	Working	Working	Working	Working
LSD driver	LS0 over-current protection threshold enlarges by ±5% for each level with respect to each one of the 4 Ioc values present for H-Bridge Mode	HS0 over-current protection threshold enlarges by ±5% for each level with respect to each one of the 4 Ioc values present for H-Bridge Mode	Not working correctly, SPI Fault Bit (OL ON STATUS) has to be not considered. OL_ON must be set to "0"	Not working correctly, SPI Fault Bit (ILIM_REG) has to be neglected.	Not working correctly, SPI Fault Bit (ILIM_REG) has to be neglected.

OFF diagnosis coverage

OFF state diagnostic comparators are connected to OUT1 only.

Open Load expected threshold: From simulation data we expect a threshold for the Open Load in OFF about 95 kΩ @ Vps = 18 V in case L9960 is used as single LSD driver. On the other hand the threshold for the Open Load detection should be about 50 kΩ @Vps = 18 V in case L9960 is used as H-bridge (full bridge).

1. We start using a load with value R = 2.5 Ω L = 150 mH in **LSD driver configuration** and observed below results depending on applied condition:
   - **No Fault injection** OFF-Diagnosis results in short-to-battery always highlighted. (see *Note below*)
   - **Short-to-battery** OFF-Diagnosis results in short-to-battery always highlighted.
   - **Short-to-ground** OFF-Diagnosis results in short-to-ground always highlighted.
   - **Open Load condition** OFF-Diagnosis results in Open Load always highlighted.

Note: We increase resistive contribution from 2.5 Ω in the No Fault condition in order to describe and characterize in which way the load value alters the OFF-Diagnosis capability for Fault detection:
From 2.5 Ω up to 80 kΩ the OFF-Diagnosis highlighted short-to-battery. Between 85 kΩ and 95 kΩ OFF-Diagnosis does not work, this is because we are close to the OL threshold; the

device is unable to distinguish between short-to-battery and open load. Due to an unstable diagnostics input during T_{stable_off}, the observed consequence is that OFF-Diagnosis remains active for $T_{timeout}$ (8.4 ms typ.) waiting for a stable result. Starting from 95 kΩ fault detection is working again and OFF-Diagnosis highlights Open Load.

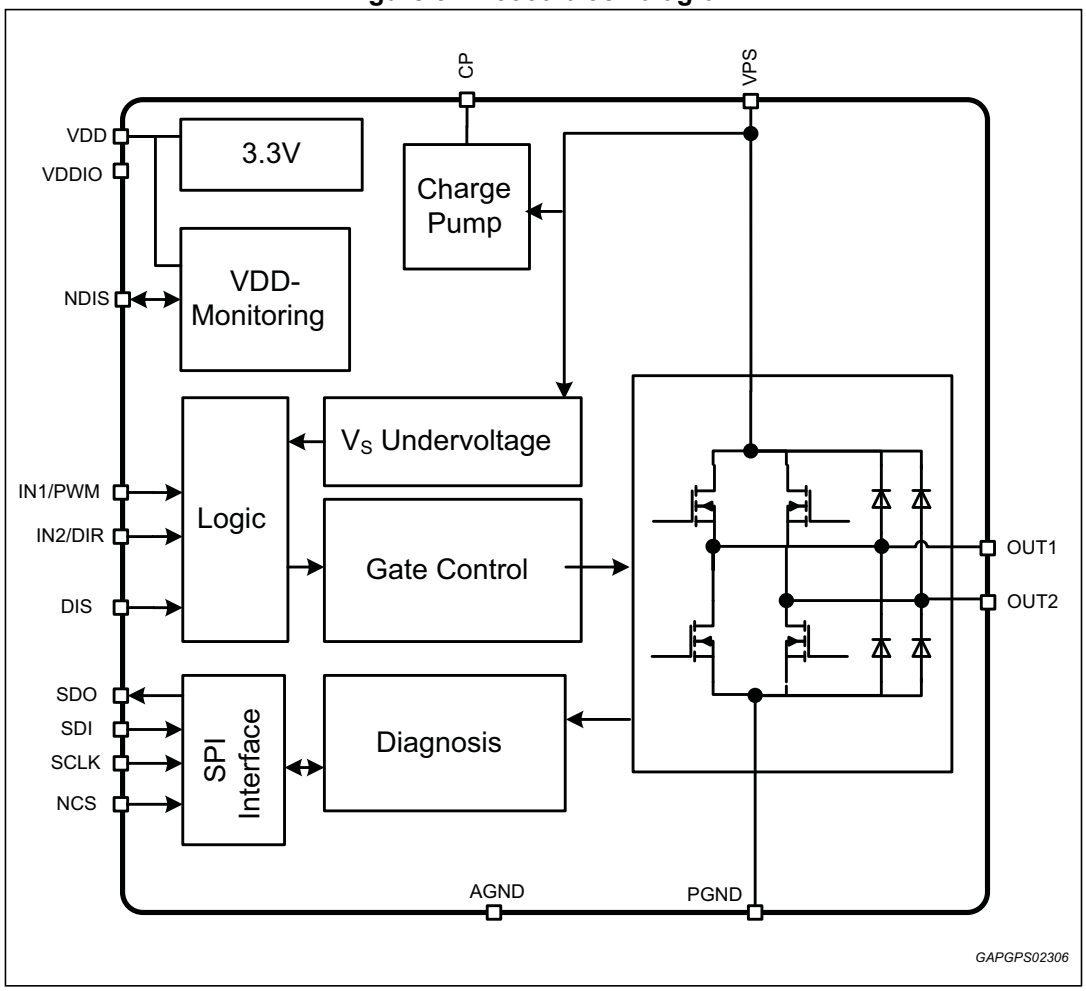
The device detects Short-to-Battery and Short-to-Ground with the load R = 2.5 Ω, L = 150 mH.

2. We start using a load with value R = 2.5 Ω L = 10 mH in **H-bridge configuration** and observed below results depending on applied condition:
   - **No Fault injection** OFF-Diagnosis results in no fault always highlighted. (see *Note below*)
   - **Short-to-battery** OFF-Diagnosis results in short-to-battery always highlighted.
   - **Short-to-ground** OFF-Diagnosis results in short-to-ground always highlighted.
   - **Open Load condition** OFF-Diagnosis results in Open Load always highlighted.

Note: We increase resistive contribution from 2.5 Ω in the No Fault injection condition in order to describe and characterize in which way the load value alters the OFF-Diagnosis capability for Fault detection:
From 2.5 Ω up to 35 kΩ the OFF-Diagnosis highlighted no fault. At 43 kΩ it is possible to have OL or NO Fault because this value is very close to the threshold for the OL in OFF Diagnosis in the H-bridge configuration, the result of the diagnosis depends on thermal conditions (resistive load increases with temperature, so with dissipation the resitance raises a little its nominal value in this way; at the beginning of the trial and at room temperature the result is No Fault, at the end it could be also Open Load). At 55 kΩ OFF-Diagnosis always highlights Open Load in OFF. Above 55 kΩ threshold, the OFF-Diagnosis will always highlight an Open Load in OFF state.

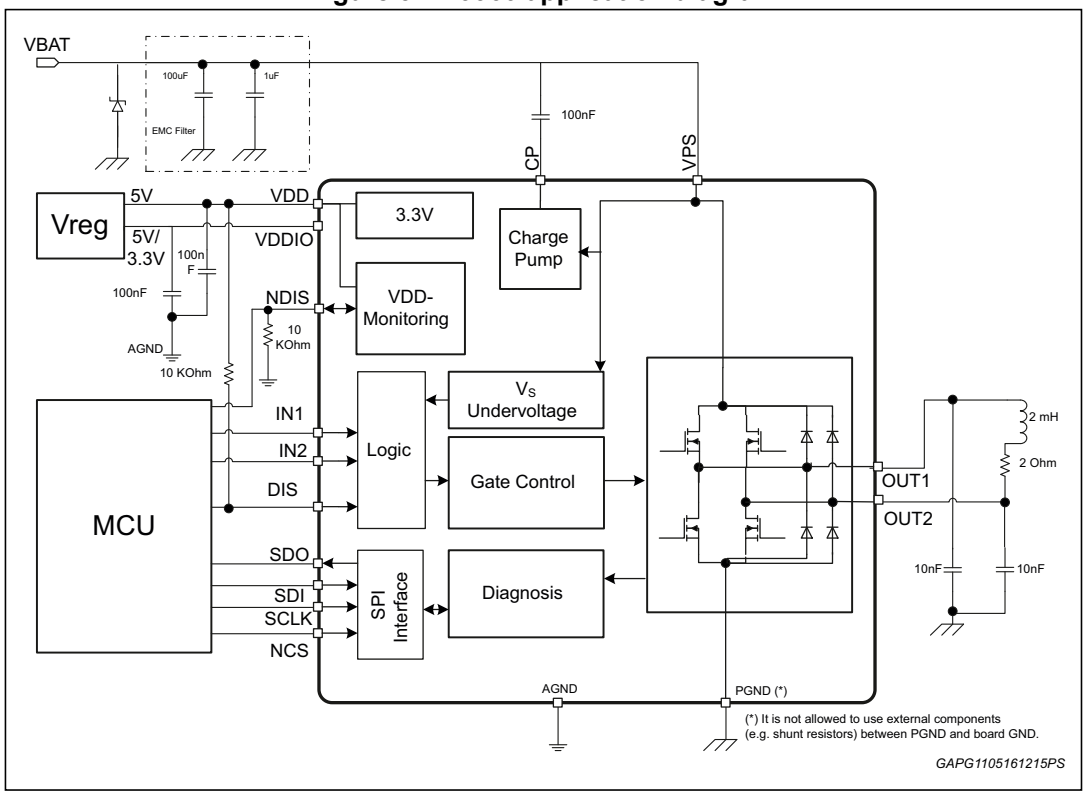
4 Block diagram

Figure 31. L9960 block diagram



5 Application description

Figure 32. L9960 application diagram



6 Revision history

Table 7. Document revision history

Date	Revision	Changes
03-Jun-2016	1	Initial release.
21-Jun-2016	2	Updated: – *Section 3.12: Tristate procedure*; – *Section 3.13.1: Off-state diagnosis*; – *Section 3.13.2: ON-state diagnosis*; – *Table 5: Diagnosis registers and DIAG_CLEAR_EN dependence on page 40*; – *Section 3.16: LSD driver vs. H-bridge configuration*.
25-Oct-2017	3	Updated *How to enable in IN1 IN2 mode on page 24*; Added *Open load in OFF issues on page 34*.
27-Mar-2018	4	Updated: *Section 3.3: Usable DT in Normal / IN1 IN2 mode*; *Section 3.12: Tristate procedure*.
29-May-2018	5	Added in cover page the L9960T product name and updated *Introduction* paragraph.