SLLIMM-nano 2nd series small low-loss intelligent molded module

Introduction

The SLLIMM-nano (small low-loss intelligent molded module) 2nd series is ST's new family of very compact, high efficiency, dual-in-line intelligent power modules, with optional extra features. This family is designed with an improved package structure to achieve higher power levels in applications such as dishwashers, refrigerator compressors, air conditioning fans, dryers, draining and recirculation pumps and in low-power industrial applications, such as small fans, pumps, tools, etc.

This new series both complements and surpasses the original SLLIMM-nano series in terms of features, package types and flexibility.

The SLLIMM-nano 2nd series features:

- expanded line-up to 8 A with trench field stop (TFS) IGBT technology for efficiency improvement
- improved thermal performance (up to 40% thermal resistance reduction for 3 A size IPM)
- slots for easy heat sink fixing
- two different lead options: zig-zag leads (fully compatible with previous series) and in line leads (for a more compact size even)
- double stand-off option: with or without
- NTC thermistor embedded on all the product family
- improved isolation rating to 1500 Vrms/min

The SLLIMM-nano 2nd product family combines optimized silicon chips, integrated in three main inverter blocks:

- power stage
  - six very fast IGBTs
  - six freewheeling diodes
- driving network
  - three high voltage gate drivers
  - gate resistors
  - three bootstrap diodes
- protection and optional features
  - op-amp for advanced current sensing
  - comparator for fault protection against overcurrent and short-circuit
  - smart shutdown function
  - NTC thermistor
  - dead-time, interlocking function and undervoltage lockout

Thanks to its great compactness, the fully-isolated N2DIP-26L SLLIMM-nano 2nd series package is the ideal solution for applications requiring reduced assembly space even with heat sink, without sacrificing thermal performance and reliability.

The aim of this application note is to provide a detailed description of the SLLIMM-nano 2nd series, providing the guidelines to motor drive designers for an efficient, reliable, and fast design when using this new product family from ST.

1 Differences between the SLLIMM-nano 1st and 2nd series

The SLLIMM-nano 2nd series offers some improvements with respect to the previous series, especially from a package point of view, in order to massively improve thermal performance by allowing a heat sink to be affixed easily thanks to the dedicated slots on the body package. This offers additional lead and stand-off options for the entire assembly process and space-constraint application requirements.

The main differences are listed in Table 1. Main differences.

Table 1. Main differences

Series	SLLIMM-nano 1st series	SLLIMM-nano 2nd series
PN	STGIPNxxH60yy	STGIPQxxH60yy STGIPQxxC60yy
IGBT technology	Planar	Planar and Trench gate field stop
Current capability I_C (@ 25 °C)	3 A	From 3 to 8 A
Package	NDIP-26L	N2DIP-26L
Slots for heat sink fixing	No	Yes
IGBT thermal resistance (R_{thJC})	STGIPN3H60yy: 16.5 °C/W	STGIPQ3H60yy: 10 °C/W (-40% referred to 3 A SLLIMM-nano 1st series) STGIPQ5C60yy: 9.2 °C/W STGIPQ4C60yy: 10 °C/W STGIPQ8C60yy: 6.5 °C/W
Thermal resistance (R_{thJA})	50 °C/W	44 °C/W
NTC thermistor	Yes (in some PNs)	Yes (all PNs)
Lead options	Zig-zag leads	Zig-zag leads In line leads
Stand-off option	With stand-off	With stand-off Without stand-off
V_{ISO}	1000 Vrms/min	1500 Vrms/min

For all the main differences in the specifications and recommended operating conditions, please refer to the relevant product datasheet.

1.1 Product synopsis

The SLLIMM-nano 2nd series family has been designed to satisfy the requirements of a wide range of final applications up to 600 W, such as:

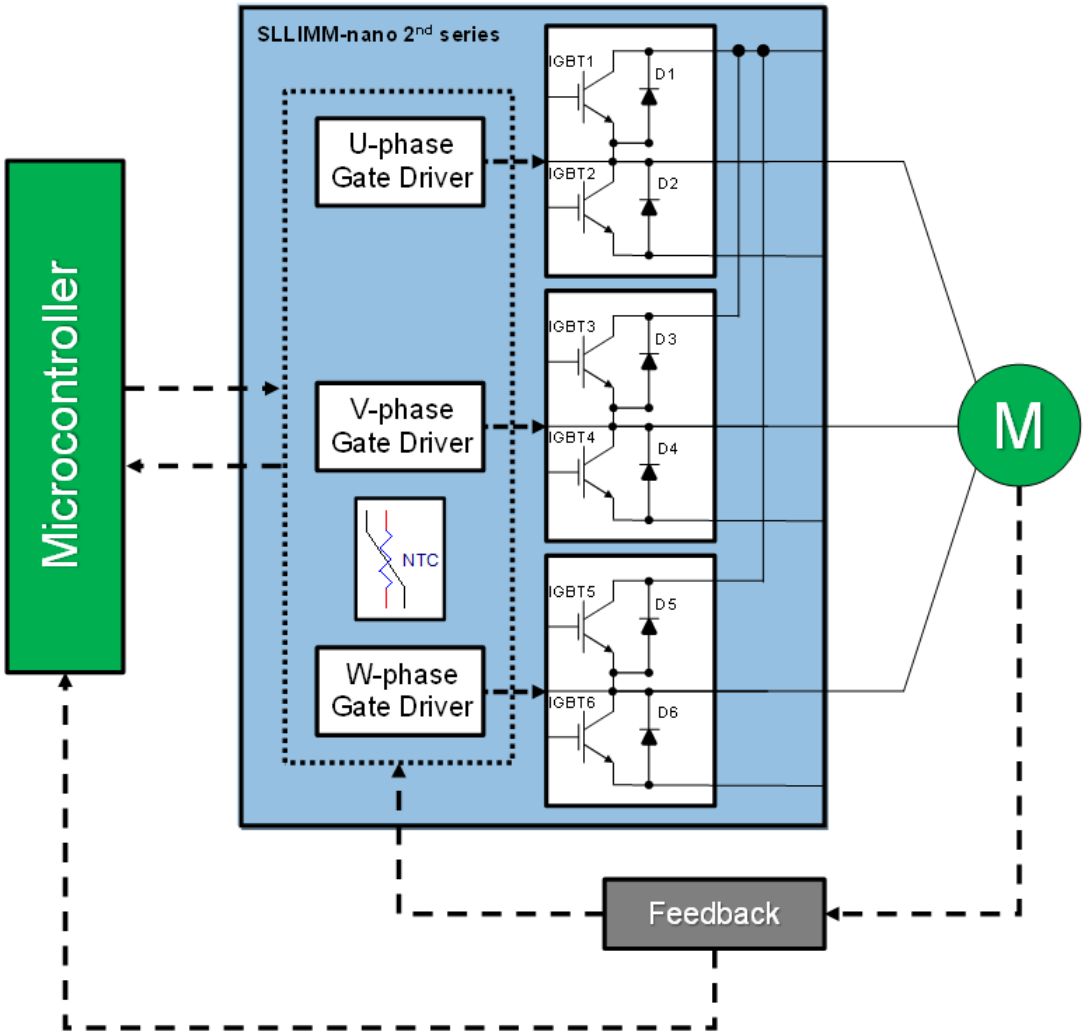
- dishwashers
- refrigerator compressors
- air conditioning fans
- dryers
- draining and recirculation pumps
- low power industrial applications
- small fans, pumps and tools

The main features and integrated functions can be summarized as follows:

- 600 V, 3, 4, 5 and 8 A ratings
- 3-phase IGBT inverter bridge including:
  - six low-loss IGBTs
  - six low forward voltage drop and soft recovery freewheeling diodes
- three control ICs for gate driving and protection including:
  - smart shutdown function
  - comparator for fault protection against overcurrent and short-circuit
  - op-amp for advanced current sensing
  - three integrated bootstrap diodes
  - interlocking function
  - undervoltage lockout
  - NTC thermistor
- open emitter configuration for individual phase current sensing
- very compact and fully isolated package
- integrated gate resistors for optimum IGBT switching speed setting
- proper biasing of gate driver

Figure 1 shows the block diagram of SLLIMM-nano 2nd series included in the inverter solution.

Figure 1. **SLLIMM-nano 2nd series block diagram**



The power devices (IGBTs and freewheeling diodes) incorporated in the half bridge block are tailored for a motor drive application, delivering the greatest overall efficiency thanks to the optimized trade-off between conduction and switching power loss and very low EMI generation, as a result of reduced dV/dt and di/dt.

The IC gate drivers are a fully featured version which provides advanced options for a sophisticated control method and protection. The fully isolated N2DIP-26L package offers a high level of compactness, very useful applications with reduced space, at the same time maintaining high thermal performance and reliability levels.

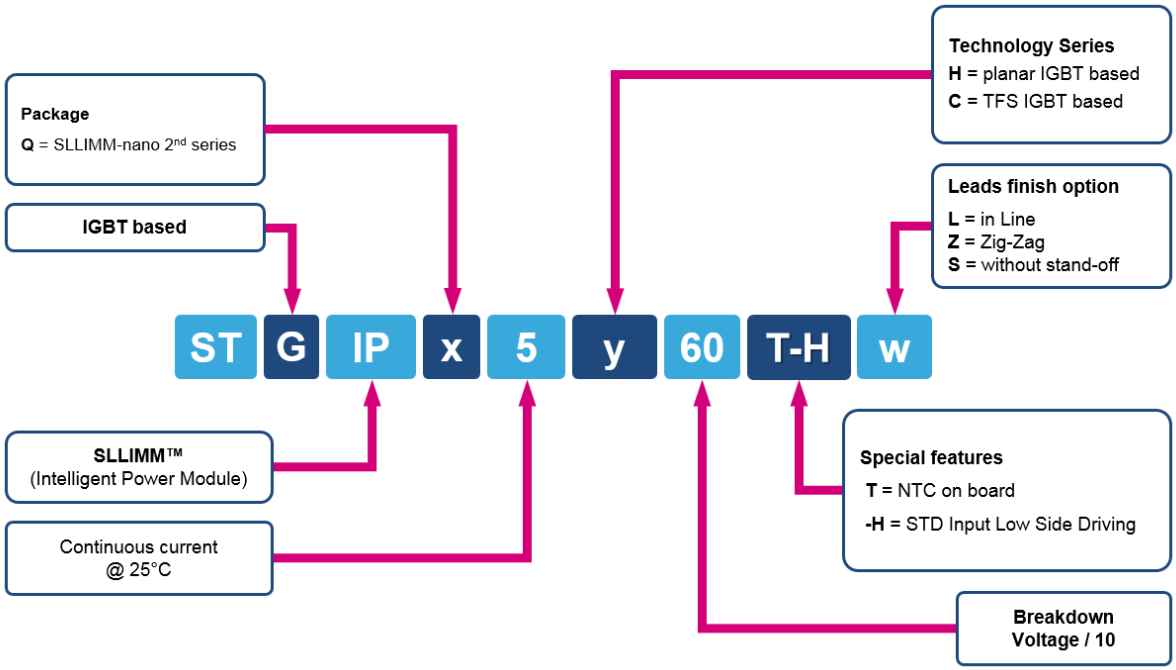
1.2 Product line-up and nomenclature

Table 2. SLLIMM-nano 2nd series line-up

Features	STGIPQ3H60T-Hyy	STGIPQ4C60T-Hyy	STGIPQ5C60T-Hyy	STGIPQ8C60T-Hyy
Power switch type	IGBT+FWD	IGBT+FWD	IGBT+FWD	IGBT+FWD
Voltage (V)	600	600	600	600
Current at T_C = 25 °C (A)	3	6	5	8
IGBT R_{thJC} max (°C/W)	10	10	9.2	6.5
Diode R_{thJC} max (°C/W)	15	15	15	15
R_{thJA} max (°C/W)	44	44	44	44
Package	N2DIP-26L	N2DIP-26L	N2DIP-26L	N2DIP-26L
Package size (mm) X, Y, Z	32.15x12.45x4.1	32.15x12.45x4.1	32.15x12.45x4.1	32.15x12.45x4.1
Integrated bootstrap diode	Yes	Yes	Yes	Yes
SD function	Yes	Yes	Yes	Yes
Comparator for fault protection	Yes	Yes	Yes	Yes
Smart shutdown function	Yes	Yes	Yes	Yes
Op-amp for advanced current sensing	Yes	Yes	Yes	Yes
Interlocking function	Yes	Yes	Yes	Yes
Undervoltage lockout	Yes	Yes	Yes	Yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)
NTC thermistor	Yes	Yes	Yes	Yes
3.3 / 5 V input interface compatibility	Yes	Yes	Yes	Yes
High side IGBT input signal	Active High	Active high	Active high	Active high
Low side IGBT input signal	Active High	Active high	Active high	Active high
V_{ISO} (Vrms/min)	1500	1500	1500	1500

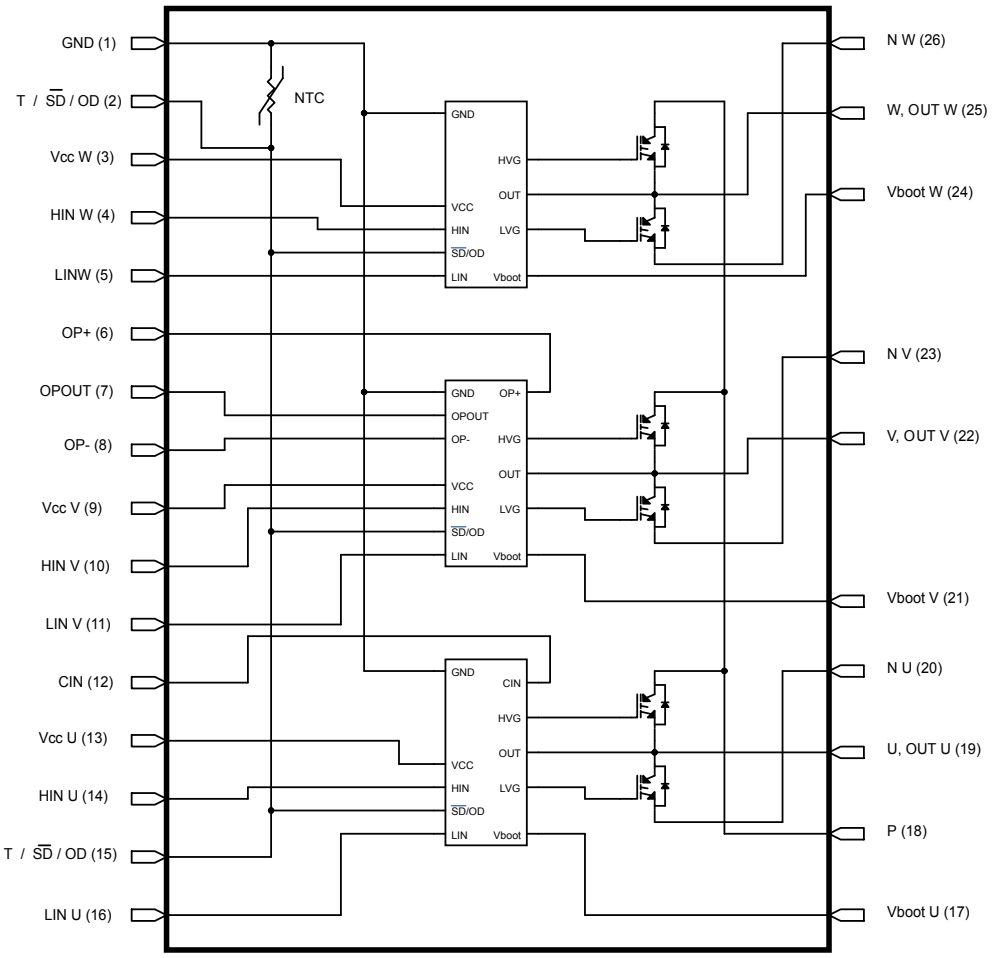
Please refer to www.st.com for the complete product portfolio.

Figure 2. **SLLIMM-nano 2nd series nomenclature**



1.3 Internal circuit

Figure 3. **Internal circuit of the STGIPQ5C60T-Hyy**



1.4 Absolute maximum ratings

The absolute maximum ratings represent the extreme capability of the device and they can be normally used as a worst case design limit condition. It is important to note that the absolute maximum value is given according to a set of testing conditions such us temperature, frequency, voltage, etc. The device performance can change according to the applied condition.

The SLLIMM-nano 2nd series specifications are described below by using the STGIPQ5C60T-Hyy datasheet as an example. Please refer to the respective product datasheets for a detailed description of all the types.

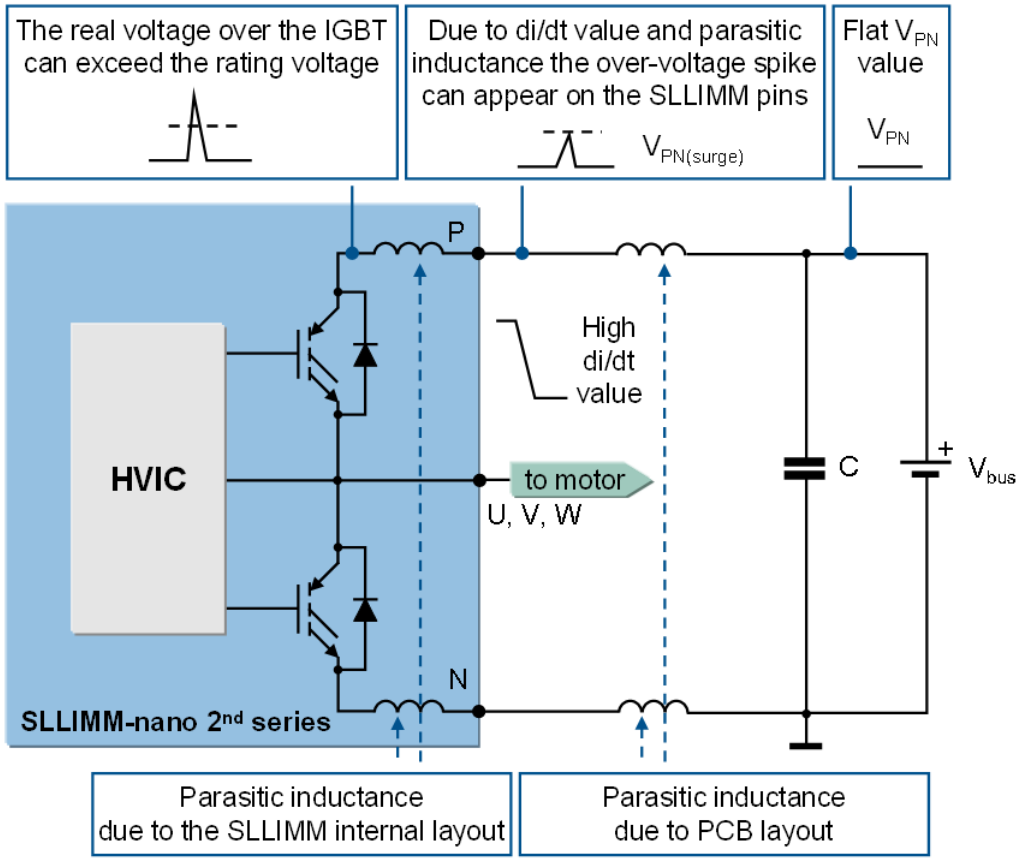
Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Collector emitter voltage (V_{IN} = 0)	600	V
I_C	Continuous collector current each IGBT	5	A
I_C	Peak collector current each IGBT (less than 1ms)	10	A
P_{TOT}	Total dissipation at T_C=25 °C each IGBT	13.6	W

1. *Applied between HINx, LINx and GND for x = U, V, W.*
2. *Pulse width limited by max. junction temperature.*

- V_{CES}: collector emitter voltage
  - The power stage of SLLIMM-nano 2nd series is based on IGBTs (and freewheeling diodes) having 600 V_{CES} rating. Generally, considering the intelligent power module internal stray inductances during commutations which can generate surge voltages, the maximum allowed surge voltage between P-N ($V_{PN(surge)}$) is lower than V_{CES}, as shown in Figure 4. At the same time, considering also the surge voltage generated by the stray inductance between the device and the DC-link capacitor, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) must be even lower than $V_{PN(surge)}$. Thanks to the small package size and the lower working current, this phenomenon is less marked in the SLLIMM-nano 2nd series than the larger intelligent power module.

Figure 4. Stray inductance components of the output stage



- I_C: continuous collector current for each IGBT
  - I_C is the allowable DC current continuously flowing at the collector electrode.

Table 4. Control part (STGIPQ5C60T-Hyy)

Symbol	Parameter	Value	Unit
V_{CC}	Low voltage power supply	-0.3 to 21	V
V_{BOOT}	Bootstrap voltage	-0.3 to 620	V
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W and GND	V_{boot} - 21 to V_{boot} + 0.3	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} + 0.3	V
V_{IN}	Logic input voltage applied between HINx, LINx and GND	-0.3 to 15	V
VT/ $\overline{SD}$ / OD	Open drain voltage	-0.3 to 15	V
ΔV_{OUT} /dt	Allowed output slew rate	50	V/ns

- V_{CC}: low voltage power supply
  - V_{CC} represents the supply voltage of the control part. Local filtering is recommended to enhance the SLLIMM-nano 2nd series noise immunity. Generally, the use of one electrolytic capacitor (with a greater value but not negligible ESR) and one smaller ceramic capacitor (hundreds of nF) that is faster than the electrolytic capacitor to provide current, is recommended. Please refer to Table 5 in order to properly drive the SLLIMM-nano 2nd series.

Table 5. Supply voltage and operation behavior

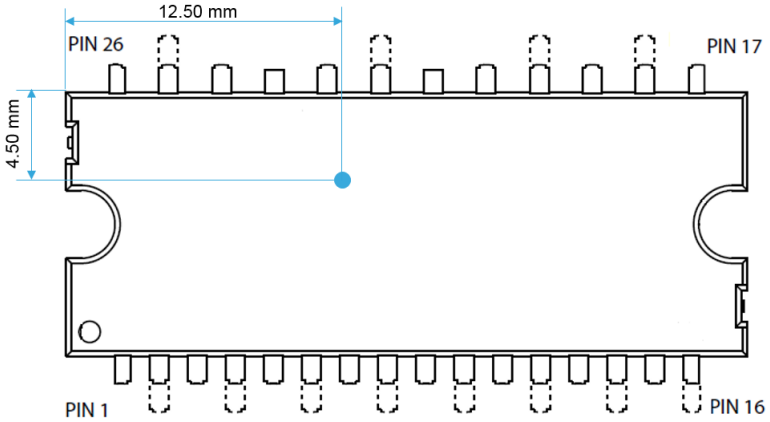
V_{CC} voltage (typ. value)	Operating behavior
< 12 V	As the voltage is lower than the UVLO threshold, the control circuit is not fully turned on. Perfect functionality cannot be guaranteed.
12 V – 15 V	Typical operating conditions.
> 21 V	Control circuit is destroyed.

Table 6. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	1500	V_{rms}
T_j	Power chips operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

The figure below shows the case temperature measurement point for all package lead options, right above the power chip. To obtain accurate temperature information, mount a thermocoupler on the heat sink surface at this specific location. For non-complementary switching schemes, the highest T_C point occurs at a different position. In this case, the measurement location is over the point where the highest power chip temperature is generated.

Figure 5. **TC measurement point**



2 Electrical characteristics and functions

In this section the main electrical characteristics of the power stage are discussed, together with a detailed description of all the SLLIMM-nano 2nd series functions.

2.1 IGBTs

The SLLIMM-nano 2nd series achieves power savings in the inverter stage thanks to the use of IGBTs manufactured with the proprietary advanced PowerMESH™ and trench field stop process. These power devices are optimized for typical motor control switching frequency and offer an excellent trade-off between voltage drop ($V_{CE(sat)}$) and switching energy (E_{on} and E_{off}), and therefore minimize the two major sources of energy loss (conduction and switching) reducing the environmental impact of daily-use equipment. A full analysis on the power loss of the complete system is reported in Section 4 Power loss and dissipation.

2.2 Freewheeling diodes

ST's Turbo 2 ultrafast high voltage diodes have been selected for the SLLIMM-nano 2nd series and carefully tuned to achieve the best t_{rr}/V_F trade-off and softness as freewheeling diodes in order to further improve the total performance of the inverter and significantly reduce the electromagnetic interference (EMI) in motor control applications, which are quite sensitive to this phenomena.

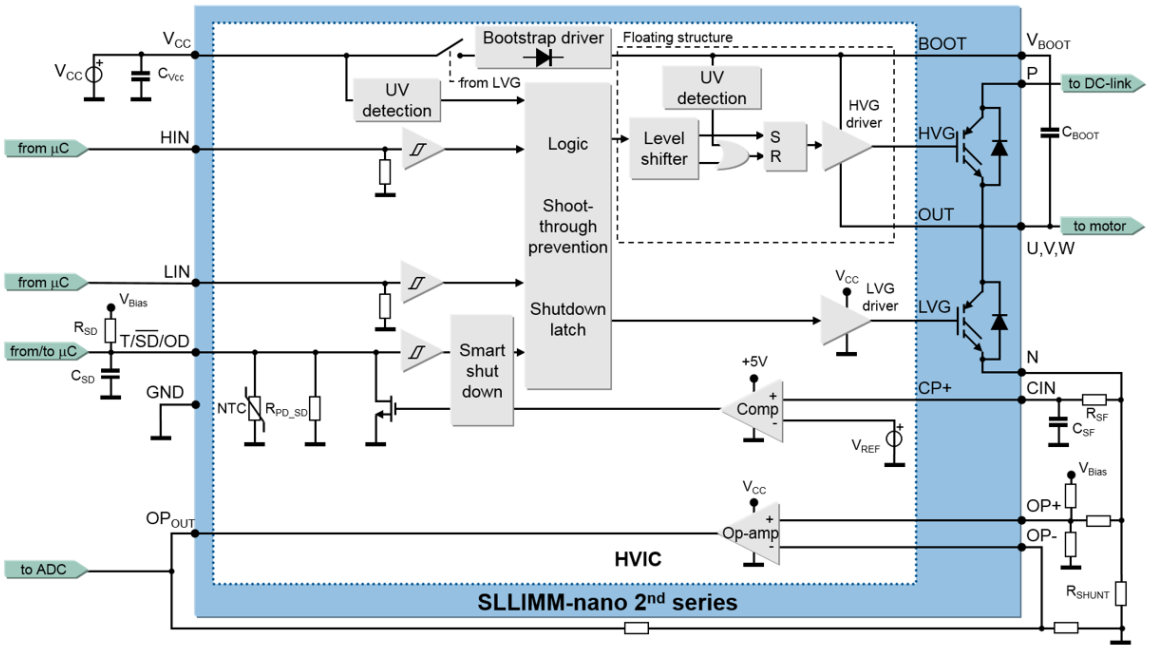
2.3 High voltage gate drivers

The SLLIMM-nano 2nd series is equipped with a versatile high voltage gate driver IC (HVIC), designed using BCD offline (bipolar, CMOS, and DMOS) technology and particularly suited to field oriented control (FOC) motor driving applications, and is able to provide all the functions and current capability necessary for high side and low side IGBT driving. This driver includes patented internal circuitry which replaces the external bootstrap diode.

Each high voltage gate driver chip controls two IGBTs in half bridge topology, offering basic functions such as interlocking, integrated bootstrap diode, and also advanced features such as smart shutdown (patented), fault comparator, and a dedicated high performance op-amp for advanced current sensing. A schematic summary of the features by device are listed in Table 2. SLLIMM-nano 2nd series line-up.

In this application note, the main characteristics of a high voltage gate drive related to the SLLIMM-nano 2nd series are discussed. For further information, please refer to application note AN2738, available on st.com.

Figure 6. **High voltage gate driver block diagram**



2.3.1 Logic inputs

All the HINx and LINx logic inputs are provided with hysteresis (~1 V) for low noise sensitivity and are TTL/CMOS 3.3 V compatible. Thanks to this low voltage interface logic compatibility, the SLLIMM-nano 2nd series can be used with any type of high performance controller, such as microcontrollers, DSPs or FPGAs. As shown in the block diagram in Figure 6, the logic inputs have internal pull-down resistors in order to set a proper logic level in case of interruption in the logic lines. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. This simplifies the interface circuit by eliminating the six external resistors, thereby reducing cost, board space and component count.

The typical values of the integrated pull-down resistors are shown in Table 7:

Table 7. **Integrated pull-down resistor values**

Input pin	Input pin logic	Internal pull-down
High side gate driving HIN_U, HIN_V, HIN_W	Active high	375 kΩ
Low side gate driving LIN_U, LIN_V, LIN_W	Active high	375 kΩ
T / $\overline{SD}$ / OD shutdown	Active low	50 kΩ

2.3.2 High voltage level shift

The built-in high voltage level shift allows direct connection between the low voltage control inputs and the high voltage power half bridge in any power application up to 600 V. It is obtained thanks to the BCD offline technology which integrates, in the same die, bipolar devices, low and medium voltage CMOS for analog and logic circuitry and high voltage DMOS transistors with a breakdown voltage in excess of 600 V. This key feature eliminates the need for external optocouplers, resulting in significant reduction in component count and power loss. Other advantages are high-frequency operation and short input-to-output delays.

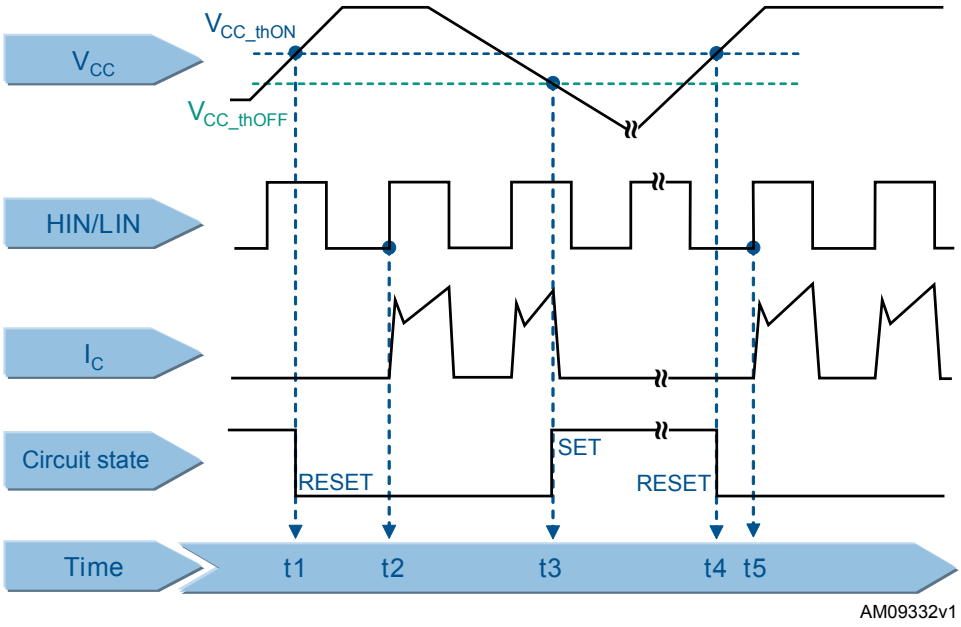
2.3.3 Undervoltage lockout

The SLLIMM-nano 2nd series supply voltage V_{CC} is continuously monitored by undervoltage lockout (UVLO) circuitry which turns off the gate driver outputs when the supply voltage goes below the $V_{CCH\_th(off)}$ threshold specified on the datasheet, and turns on the IC when the supply voltage goes above the $V_{CCH\_th(on)}$ voltage. A hysteresis of about 1.5 V is provided for noise rejection purposes. A high voltage floating supply V_{boot} is also provided with similar undervoltage lockout circuitry. When the driver is in UVLO condition, both gate driver outputs are set to low level, setting the half bridge power stage output to high impedance.

The timing chart of the undervoltage lockout is plotted in Figure 7 and is based on the following steps:

- t1: when the V_{CC} supply voltage rises to the $V_{CCH\_th(on)}$ threshold, the gate driver starts to work after the next input signal HIN/LIN is on. The circuit state becomes RESET.
- t2: input signal HIN/LIN is on and the IGBT is turned on.
- t3: when the V_{CC} supply voltage goes below the $V_{CCH\_th(off)}$ threshold, the UVLO event is detected. The IGBT is turned off in spite of the input signal HIN/LIN. The state of the circuit is now SET.
- t4: the gate driver re-starts once the V_{CC} supply voltage again rises to the $V_{CCH\_th(on)}$ threshold.
- t5: The input signal HIN/LIN is on and the IGBT is turned on again.

Figure 7. Timing chart of the undervoltage lockout function



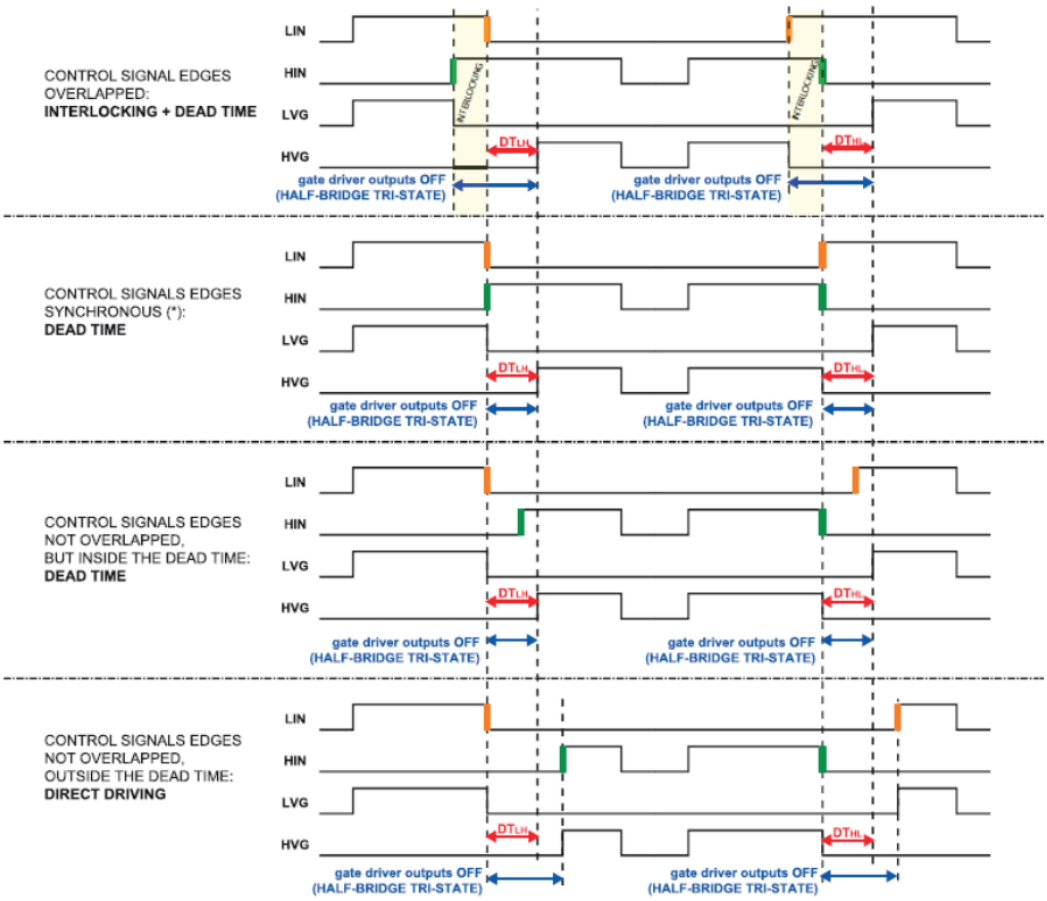
2.3.4 Interlocking function and dead time

In order to prevent possible cross-conduction between high side and low side IGBTs, the SLLIMM-nano 2nd series provides interlocking functions, which is a logic operation setting both the outputs to low level when the inputs are simultaneously active, as shown in Table 8. Interlocking function truth table. Even if an internal dead time is fixed as a default (180 ns typ.) between the falling edge transition of one driver output and the rising edge of the other output, the external dead time value set by application firmware is mandatory to avoid cross-conduction. External dead time is dominant over internal dead time, and it is recommended to set it in accordance with the datasheet value.

Table 8. Interlocking function truth table

Condition	Logic input (V_I)		Outputs	
	LIN	HIN	LVG	HVG
Interlocking half bridge tri-state	H	H	L	L
0 “logic state” half bridge tri-state	L	L	L	L
1 “logic state” low side direct driving	H	L	H	L
1 “logic state” high side direct driving	L	H	L	H

Figure 8. Timing chart of dead time function



2.3.5 Comparators for fault sensing

The SLLIMM-nano 2nd series integrates one comparator intended for advanced fault protection, such as overcurrent, overtemperature or any other type of fault measurable via a voltage signal. The comparator has an internal reference voltage, V_{REF} specified in the datasheet, on its inverting input (see Figure 6. High voltage gate driver block diagram), while the non-inverting input is available on the CIN pin. The comparator input can be connected to an external shunt resistor, in order to implement a simple overcurrent or short-circuit detection function, as discussed in detail in Section 2.3.6 Short-circuit protection and smart shutdown function.

2.3.6 Short-circuit protection and smart shutdown function

The SLLIMM-nano 2nd series is able to monitor the output current and provide protection against overcurrent and short-circuit conditions in a very short time (comparator triggering to high/low side driver turn-off propagation delay t_{isd} = 200 ns), thanks to the smart shutdown function. This feature is based on innovative patented circuitry which provides intelligent fault management and greatly reduces the protection intervention delay independent of the protection time duration, which can be set as desired by the user.

Considering the internal schematic diagram of this product family, the smart shutdown feature is directly implemented on phase U, while the V and W phase protection is linked to the U IC gate driver thanks to an internal connection with the SD pin.

As already mentioned in Section 2.3.5 Comparators for fault sensing and as shown in Figure 6. High voltage gate driver block diagram, the comparator input can be connected to an external shunt resistor, R_{SHUNT}, in order to implement a simple overcurrent detection function. An RC filter network (R_{SF} and C_{SF}) is necessary to prevent erroneous operation of the protection. The output signal of the comparator is fed to an integrated MOSFET with the open drain available on the T / $\overline{SD}$ / OD pin, shared with the $\overline{SD}$ input. When the comparator triggers, the U IC gate driver is set in shutdown state and its outputs are set to low level, leaving the half bridge in tri-state. In common overcurrent protection architectures, the comparator output is usually connected to the SD input and an external RC network (R_{SD} and C_{SD}) is connected to this $\overline{SD}$ / OD line in order to provide a mono-stable circuit which implements a protection time when a fault condition occurs.

Also, the outputs of the V and W IC gate drivers are set to low level, but not before the SD voltage reaches its low level threshold.

Finally, the smart shutdown structure allows immediate turn off of the U output gate driver in case of fault, latching the turn-on of the open drain MOSFET, until the $\overline{SD}$ signal has reached its lower threshold. After the $\overline{SD}$ signal goes below the lower threshold, the open drain is switched off (see Figure 13).

Since the protection of the V and W phases is linked to the $\overline{SD}$ level, a delay time, mainly due to the R_{SD}-C_{SD} network, is added for the shutdown of their outputs. Therefore, in order to implement effective protection, the $\overline{SD}$ network must be designed with special attention. For further details please refer to Section 2.3.7 Timing chart of short-circuit protection and smart shutdown function.

An NTC thermistor for temperature monitoring is internally connected in parallel to the SD pin in order to perform temperature monitoring using the same T / $\overline{SD}$ / OD pin. The NTC thermistor is in parallel with internal pull-down resistor (R_{PD_SD}) and the equivalent resistance is shown in Figure 9. Both temperature monitoring and SD function can coexist on the same pin if a proper external pull-up resistor R_{SD} is designed (refer to Figure 6). Therefore, to avoid undesired shutdown, the T / $\overline{SD}$ / OD voltage should be kept higher than the high-level logic threshold by setting the R_{SD} to 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU power supplies, respectively (see Figure 10).

The block diagram of the smart shutdown architecture is depicted in Figure 12.

Figure 9. **Equivalent resistance (NTC//RPD_SD)**

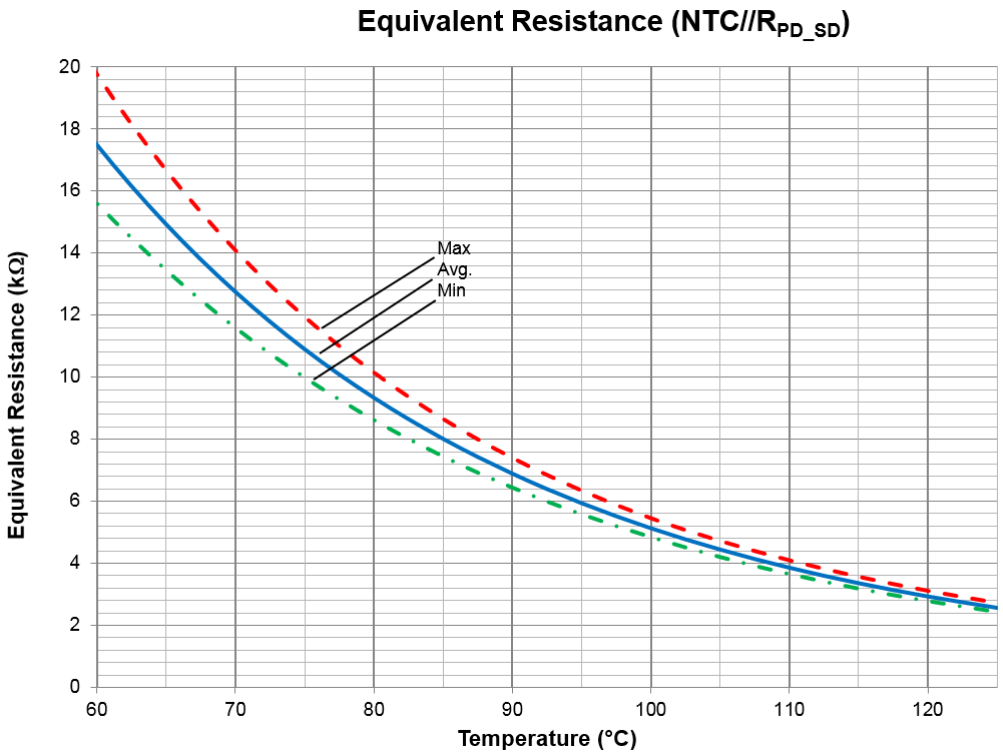


Figure 10. **Voltage of T / SD / OD pin according to NTC temperature**

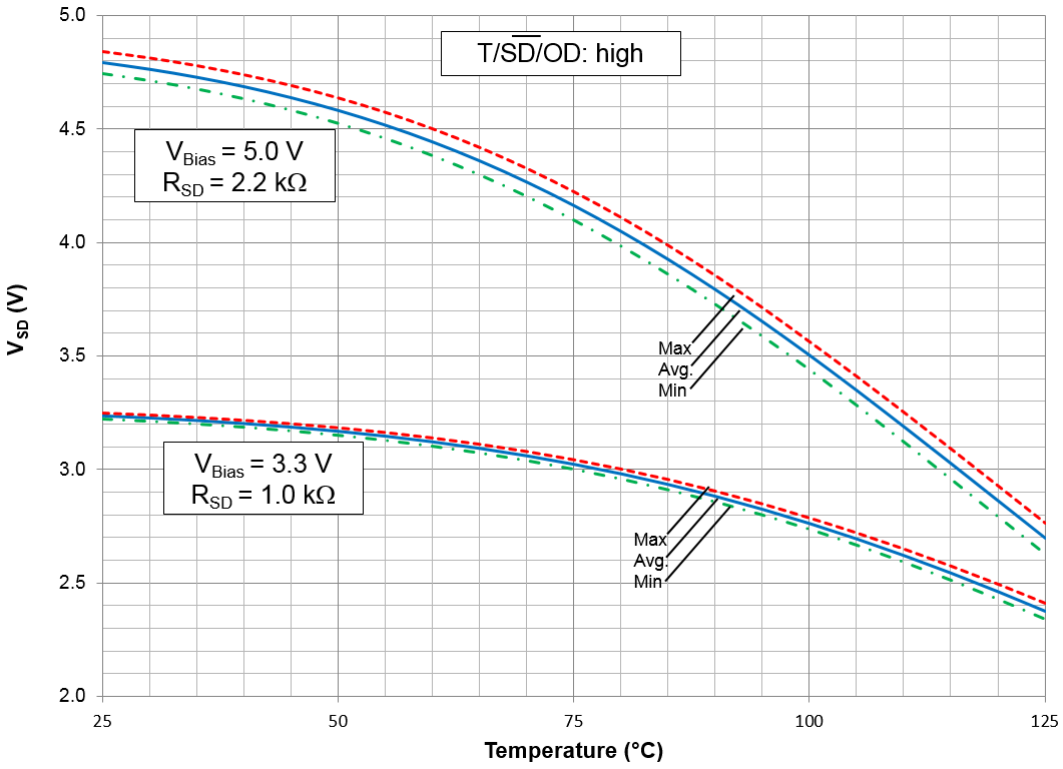


Figure 11 shows the NTC thermistor position inside the SLLIMM-nano 2.

Figure 11. **NTC thermistor position (top view)**

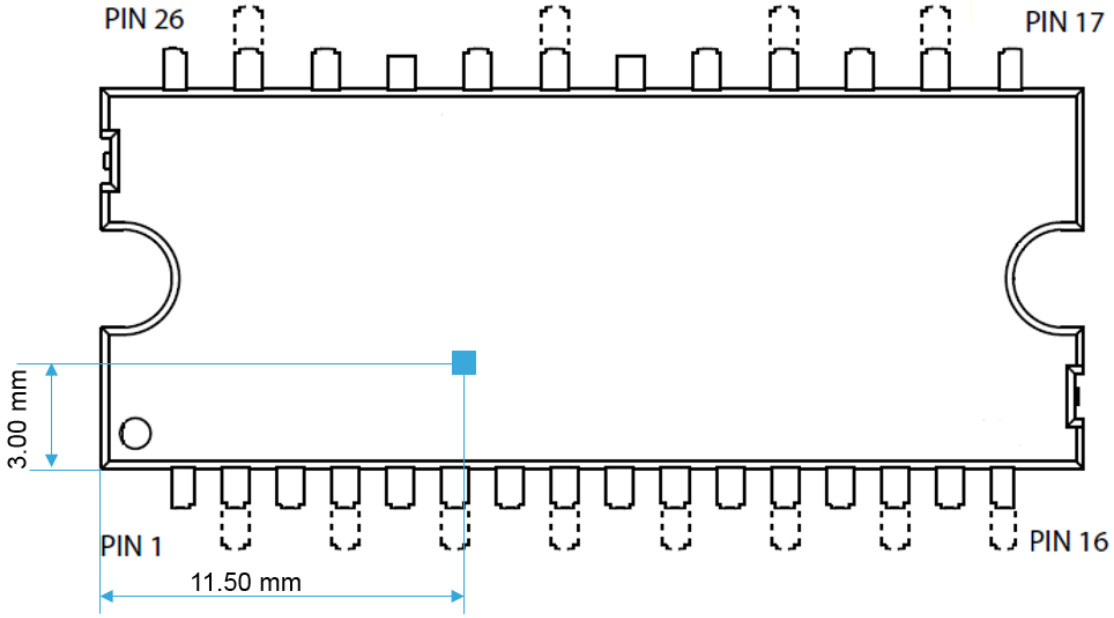
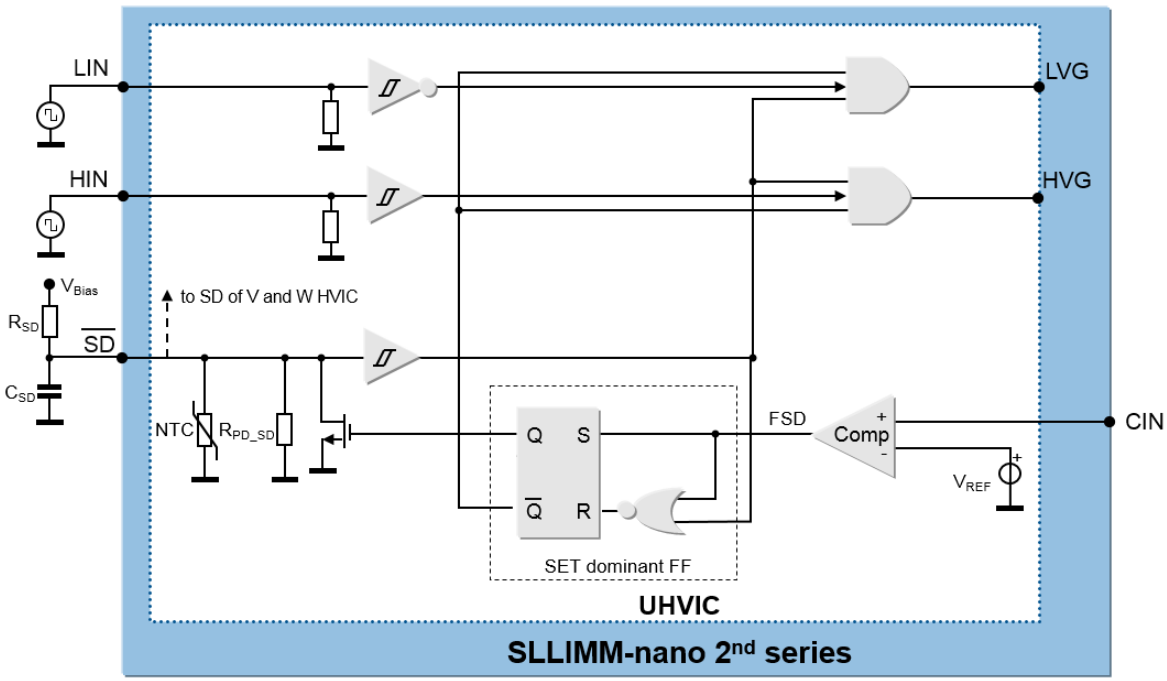


Figure 12. **Smart shutdown equivalent circuitry**



In normal operation, the outputs follow the commands received from the respective input signals.

When a fault detection event occurs, the fault signal (FSD) is set to high by the fault detection circuit output and the FF receives a SET input signal. Consequently, the aFF outputs set the SLLIMM-nano 2nd series output signals to low level and, at the same time, turn on the open drain MOSFET which works as active pull-down for the SD signal. Note that the gate driver outputs stay at low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal could be returned to low level immediately after the fault sensing. In fact even if the FF is reset by the falling edge of the $\overline{SD}$ input, the SD signal also works as enable for the outputs, thanks to the two AND ports. Moreover, once the internal open drain transistor has been activated, due to the latch, it cannot be turned off until the $\overline{SD}$ pin voltage reaches the low logic level. Note that since the FF is SET dominant, oscillations of the $\overline{SD}$ pin are avoided if the fault signal remains steady at high level.

2.3.7 Timing chart of short-circuit protection and smart shutdown function

With reference to Figure 13, the short-circuit protection is based on the following steps:

- t1: when the current is lower than the maximum allowed level, the SLLIMM-nano 2nd series works in normal operation.
- t2: when the current reaches the maximum allowed level (I_{SC}), an overcurrent/short-circuit event is detected and the protection is activated. The voltage across the shunt resistor, and then on the CIN pin, exceeds the V_{REF} value, the comparator triggers, setting the U IC gate driver in shutdown state and both its outputs are set to low level leading the half bridge into tri-state. The smart shutdown (in the U IC gate driver) switches off the U phase IGBT gates (HVG, LVG) through a preferential path (200 ns typical internal delay time) and at the same time switches on the M1 internal MOSFET. The SD signal starts the discharge phase and its value drops with a time constant τ_A (SD activation time constant). The time constant of τ_A is given by:

Equation 1

$$\tau_A = \left(R_{ON\_OD} // R_{SD} // R_{PD\_SD} // R_{NTC}\right) \cdot C_{SD} \cong R_{ON\_OD} \cdot C_{SD} \quad (1)$$

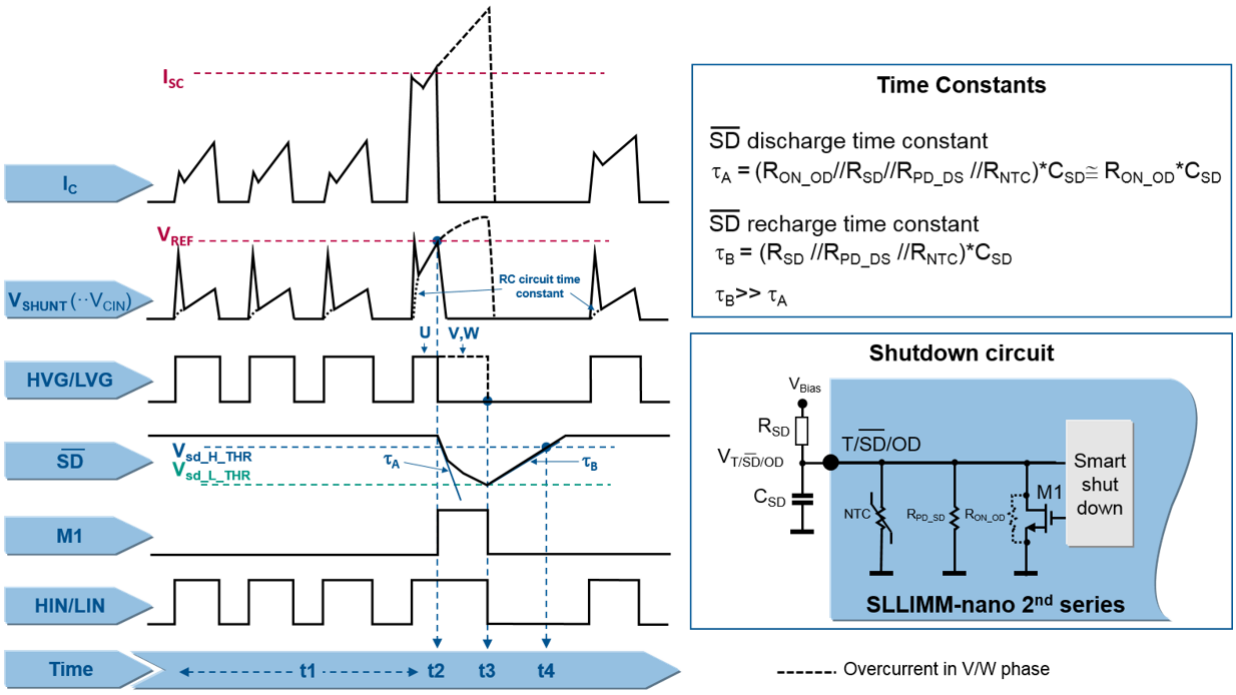
- t3: the SD signal reaches the lower threshold $V_{sd\_L\_THR}$, even the outputs of the V and W IC gate drivers are set to low and the control unit switches off all the HIN and LIN input. The smart shutdown is disabled (M1 off) and SD can rise with a time constant τ_B (SD re-enabling time constant), given by:

Equation 2

$$\tau_B = \left(R_{SD} // R_{PD\_SD} // R_{NTC}\right) \cdot C_{SD} \quad (2)$$

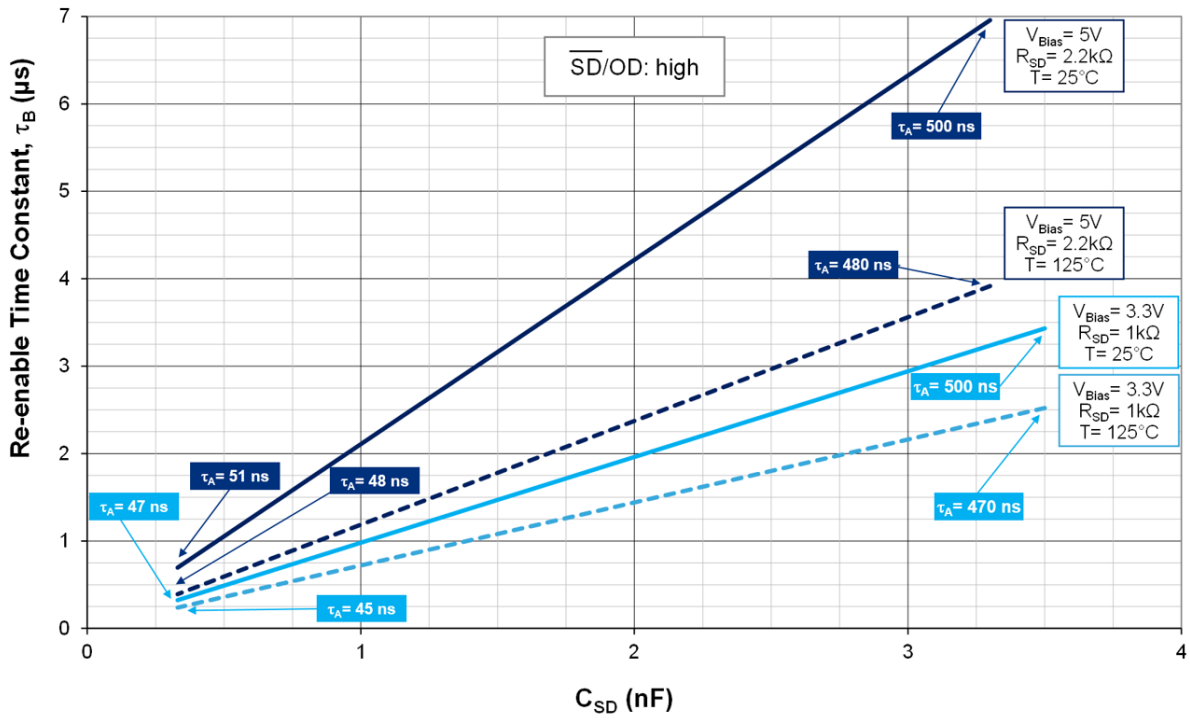
- t4: when the $\overline{SD}$ signal reaches the upper threshold $V_{sd\_H\_THR}$, the system is re-enabled.

Figure 13. **Timing chart of smart shutdown function**



As shown in Equation 1 and Equation 2, the time constants τ_A and τ_B are even functions of the NTC resistor value (which depends on temperature). Therefore, Figure 14 shows the behavior of τ_B (SD re-enabling time constant) as a function of the C_{SD} capacitor and parameterized with NTC temperature. The suggested range of the C_{SD} value is defined to have τ_A (SD activation time constant) no higher than 500 ns for effective protection.

Figure 14. **Re-enabling time constant, τ_B**



2.3.8 Current sensing shunt resistor selection

As previously discussed, the shunt resistors, R_{SHUNT}, externally connected between the N pin and ground (see Figure 6) are used to implement the overcurrent detection. When the output current exceeds the short-circuit reference level (I_{SC}), the CIN signal overtakes the V_{REF} value and the short-circuit protection is active. For reliable and stable operation, the current sensing resistor should be of a high quality, low tolerance non-inductive type. In fact, stray inductance in the circuit, which includes the layout, the RC filter, and also the shunt resistor, must be minimized in order to avoid undesired short-circuit detection. For these reasons, the shunt resistor and filtering components must be placed as close as possible to the SLLIMM-nano 2nd series pins (for additional suggestions, refer to Section 5.2). The value of the current sense resistor can be calculated by following different guidelines, functions of the design specifications, or requirements. A common criterion is presented here based on the following steps:

- Defining the overcurrent threshold value (I_{SC}). For example, it can be fixed considering the IGBT typical working current in the application and adding 20-30% as overcurrent.
- Calculation of the shunt resistor value according to the conditioning network. An example of the conditioning network is shown in Figure 18.
- Selection of the closest shunt resistor commercial value.

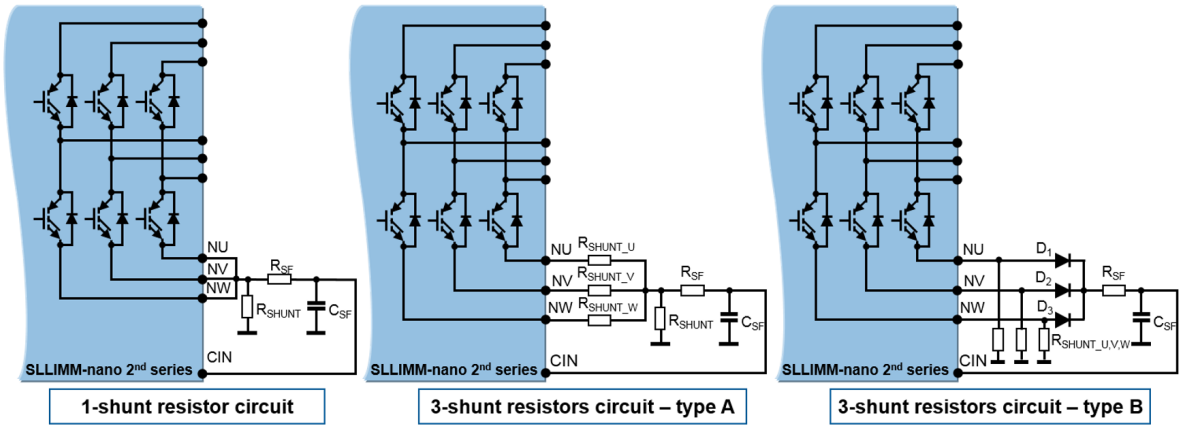
Equation 3

$$P_{SHUNT}\left(T\right) = \frac{R_{SHUNT} \cdot I_{RMS}^2}{\Delta P(T)\%} \quad (3)$$

2.3.9 RC filter network selection

Two options for the shunt (1- or 3-shunt) resistor circuit can be adopted in order to implement different control and short-circuit protection techniques. For 3-shunt resistor configurations, the figure below shows two simple overcurrent protection variants: type A, using an additional shunt resistor (R_{SHUNT}) and type B, using a diode OR gate circuit.

Figure 15. Examples of SC protection circuit



An RC filter network is required to prevent undesired short-circuit operation due to the noise on the shunt resistor. All of the solutions allow detection of the total current in all the three phases of the inverter. The filter is based on the R_{SF} and C_{SF} network and its time constant is given by:

Equation 4

$$t_{SF} = R_{SF} \cdot C_{SF} \quad (4)$$

In addition to the RC time constant, the turn-off propagation delay of the gate driver, t_{isd} (specified in the datasheet) and the IGBT turn-off time, t_{off}, (in the range of tens of ns), must be considered in the total delay time (t_{Total}), which is the time necessary to completely switch off the IGBT once the short-circuit event is detected. Therefore, the t_{Total} is calculated as follows:

Equation 5

$$t_{Total} = t_{SF} + t_{isd} + t_{off} \quad (5)$$

and the t_{SF} is recommended to be set no higher than 1 µs.

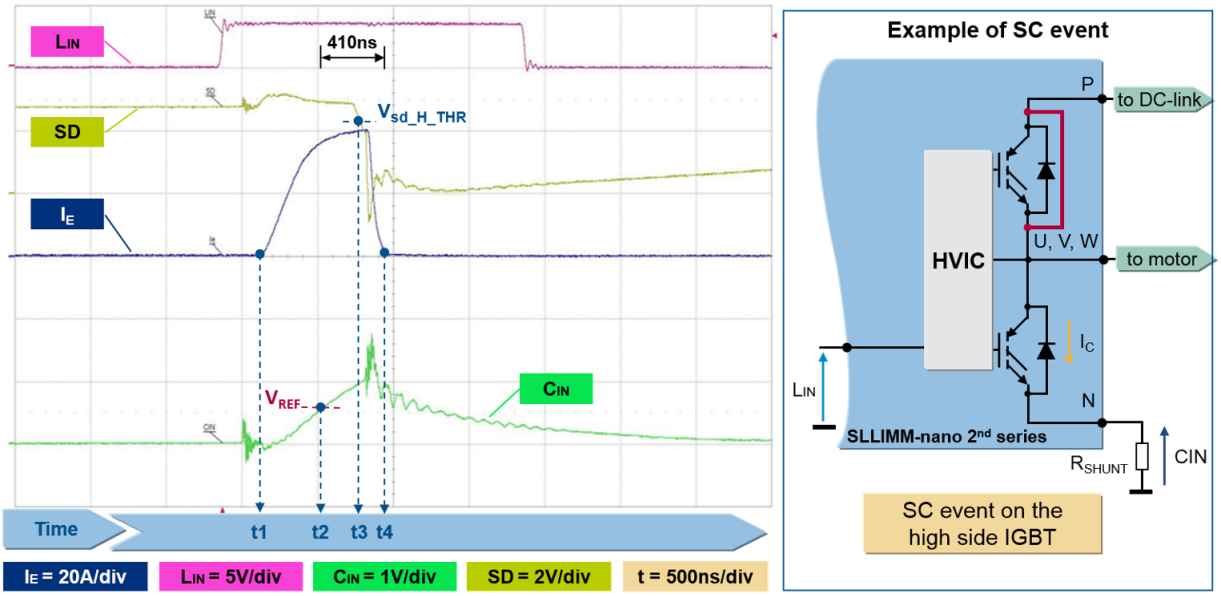
In the case of a 3-shunt resistor circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) able to monitor each phase of current.

An example of a short-circuit event is shown in Figure 16, where it is possible to observe the very fast protection, thanks to the smart shutdown function, against fault events. The main steps are:

- t1: collector current I_C starts to rise. SC event is not detected yet due to the RC network on the CIN pin
- t2: voltage on V_{CIN} reaches the V_{REF}. SC event is detected and the smart shutdown starts to turn off the U IC gate driver.
- t3: the SD is activated and even the V and W IC drivers are turned off
- t4: the IGBT is definitively turned off in 410 ns (including the $t_{d(off)}$ time of the IGBT) from SC detection.

Finally, the total disable time is t4-t1.

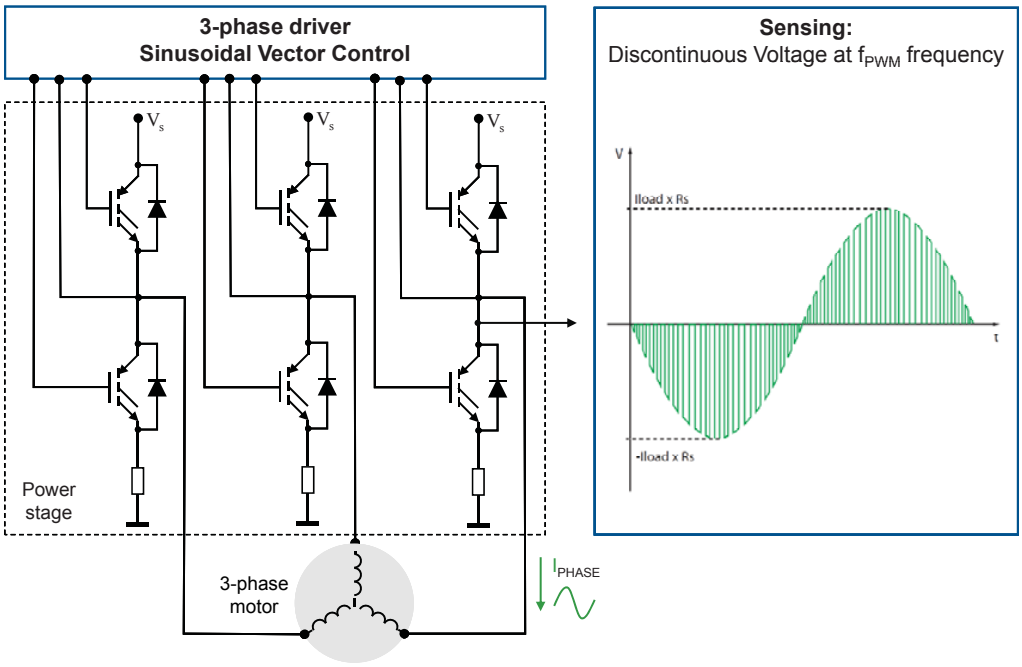
Figure 16. Example of SC event



2.3.10 Op-amp for advanced current sensing

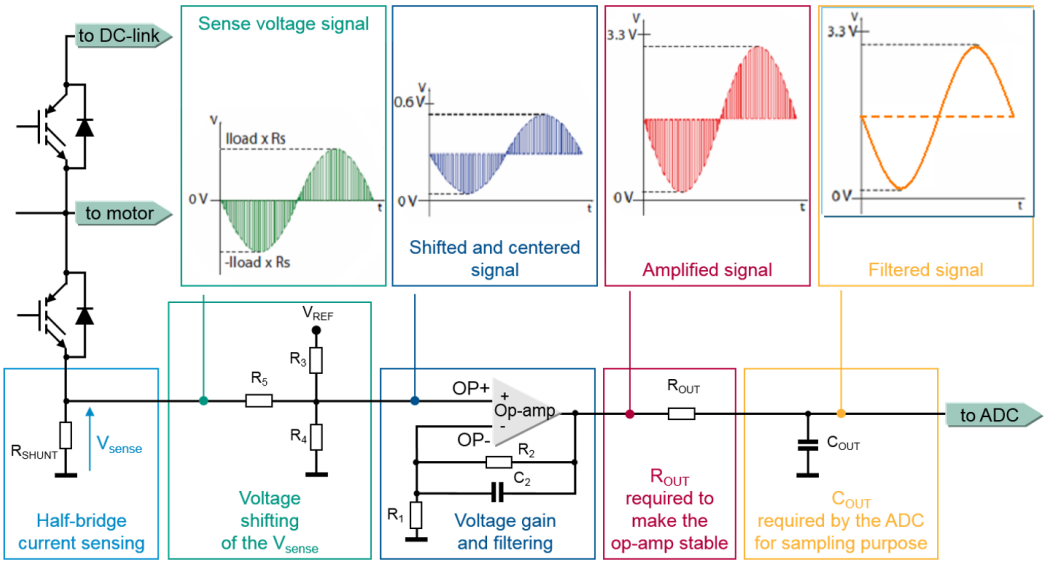
The SLLIMM-nano 2nd series also integrates one operational amplifier optimized for field oriented control (FOC) applications. In a typical FOC application the currents in the three half bridges are sensed using a shunt resistor. The analog current information is transformed into a discontinuous sense voltage signal, having the same frequency as the PWM signal driving the bridge. The sense voltage is a bipolar analog signal, the sign of which depends on the direction of the current (see Figure 17):

Figure 17. **3-phase system**



The sense voltage signals must be provided to an A/D converter. They are usually shifted and amplified by dedicated op-amps in order to exploit the full range of the A/D converter. The typical scheme and principle waveforms are shown in Figure 18:

Figure 18. **General advanced current sense scheme and waveforms**



ADCs used in vector control applications have a typical full scale range (FSR) of about 3.3 V. The sense signals must be shifted and centered on FSR/2 voltage (about 1.65 V) and amplified with a gain which provides matching between the maximum value of the sensed signal and the FSR of the ADC.

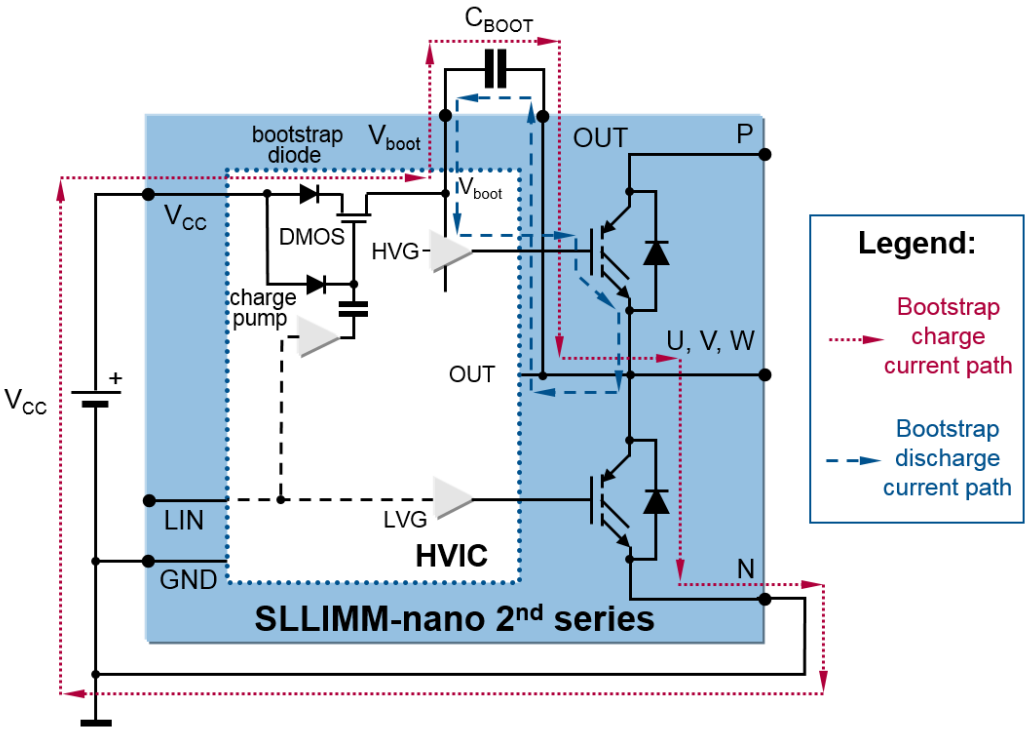
2.3.11 Bootstrap circuit

In the 3-phase inverter the emitters of the low side IGBTs are connected to the negative DC bus (V_{DC-}) as common reference ground, which allows all low side gate drivers to share the same power supply, while the emitter of high side IGBTs is alternately connected to the positive (V_{DC+}) and negative (V_{DC-}) DC bus during running conditions.

A bootstrap method is a simple and cheap solution to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode. The SLLIMM-nano 2nd series family includes a patented integrated structure that replaces the external diode. It is realized with a high voltage DMOS driven synchronously with the low side driver (LVG) and a diode in series. An internal charge pump provides the DMOS driving voltage.

The operation of the bootstrap circuit is shown in Figure 19. The floating supply capacitor C_{BOOT} is charged from the V_{CC} supply when the V_{OUT} voltage is lower than the V_{CC} voltage, through the bootstrap diode and the DMOS path with reference to the “bootstrap charge current path”. During the high side IGBT on-phase, the bootstrap circuit will provide the right gate voltage to properly drive the IGBT (see “Bootstrap discharge current path” in the diagram below). This circuit is iterated for all the three half bridges.

Figure 19. Bootstrap circuit



The value of the C_{BOOT} capacitor should be calculated according to the application conditions and must take the following into account:

- The voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level for the IC driver. This will enable the high side IGBT to work with a correct gate voltage (lower dissipation and better overall performance). Please consider that if a voltage below the UVLO threshold is applied on the bootstrap channel, the IC disables itself (no output) without any fault signal.
- The voltage across C_{BOOT} is affected by different components such as the drop across the integrated bootstrap structure, drop across the low side IGBT, and others.
- When the high side IGBT is on, the C_{BOOT} capacitor discharges mainly to provide the right IGBT gate charge but other phenomena must be considered such as leakage currents, quiescent current, etc.

2.3.12 Bootstrap capacitor selection

A simple method to properly size the bootstrap capacitor considers only the amount of charge that is needed when the high voltage side of the driver is floating and IGBT gate is driven once. This approach does not take into account either the duty cycle of the PWM, or the fundamental frequency of the current. Observations on PWM duty cycle, type of modulation (six-step, 12-step and sine-wave) must be considered with their own peculiarities to achieve optimal bootstrap circuit sizing. During the bootstrap capacitor charging phase, the low side IGBT is on and the voltage across C_{BOOT} (V_{CBOOT}) can be calculated as follows:

Equation 6

$$V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{CE(sat)max} \quad (6)$$

where:

V_{CC}: supply voltage of gate driver

V_F: bootstrap diode forward voltage drop

$V_{CE(sat)max}$: maximum emitter collector voltage drop of the low side IGBT

$V_{RDS(on)}$: DMOS voltage drop

The dimension of the bootstrap capacitance C_{BOOT} value is based on the minimum voltage drop (ΔV_{CBOOT}) to guarantee when the high side IGBT is on, and it must be:

Equation 7

$$\Delta V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{GE(min)} - V_{CE(sat)max} \quad (7)$$

under the condition:

Equation 8

$$V_{CBOOT(min)} > V_{BS\_th(on)} \quad (8)$$

where:

$V_{GE(min)}$: minimum gate emitter voltage of high side IGBT

$V_{BS\_th(on)}$: bootstrap turn-on undervoltage threshold (maximum value, see datasheet)

Considering the factors contributing to a decrease in V_{CBOOT}, the total charge supplied by the bootstrap capacitor (during high side on phase) is:

Equation 9

$$Q_{TOT} = Q_{GATE} + \left(I_{LKGE} + I_{QBO} + I_{LK} + I_{LKDiode} + I_{LKCap}\right) \cdot t_{Hon} + Q_{LS} \quad (9)$$

where:

Q_{GATE}: total IGBT gate charge

I_{LKGE}: IGBT gate emitter leakage current

I_{QBO}: bootstrap circuit quiescent current

I_{LK}: bootstrap circuit leakage current

$I_{LKDiode}$: bootstrap diode leakage current

I_{LKCap}: bootstrap capacitor leakage current (relevant when using an electrolytic capacitor but can be ignored if other types of capacitors are used)

t_{Hon}: high side on time

Q_{LS}: charge required by the internal level shifters

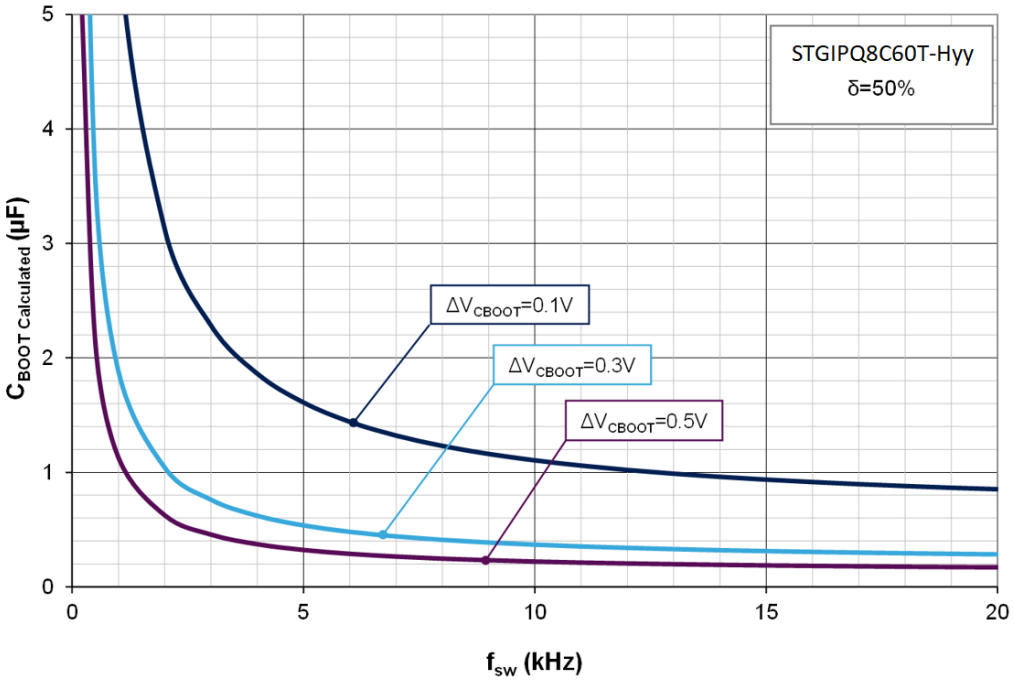
Finally, the minimum size of the bootstrap capacitor is:

Equation 10

$$C_{BOOT} = \frac{Q_{TOT}}{\Delta V_{CBOOT}} \quad (10)$$

For easier selection of the bootstrap capacitor, Figure 20 shows the behavior of C_{BOOT} (calculated) versus switching frequency (f_{sw}), with different values of ΔV_{CBOOT}, corresponding to (Equation 10) for continuous sinusoidal modulation and for the STGIPQ8C60T-Hyy (worst case) and a duty cycle δ = 50%. For all the other devices, the bootstrap capacitor can be calculated using the same curve.

Figure 20. Bootstrap capacitor vs. switching frequency



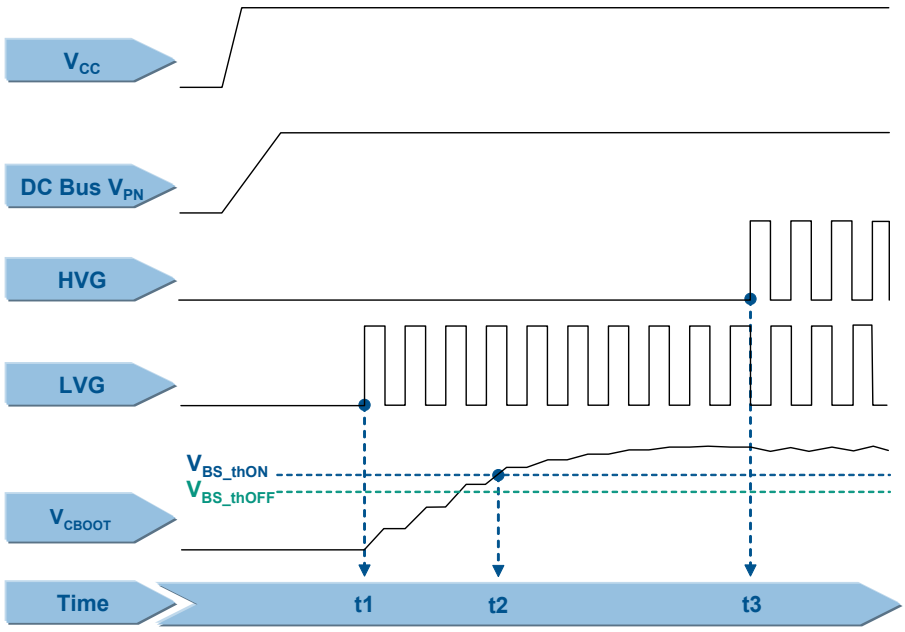
Considering the limit cases during the PWM control and further leakages and dispersions in the board layout, the capacitance value to use in the bootstrap circuit must be two or three times higher than the C_{BOOT} calculated in the graph of Figure 20. The bootstrap capacitor should have a low ESR value for good local decoupling, therefore, if an electrolytic capacitor is used, one parallel ceramic capacitor placed directly on the SLLIMM-nano 2nd series pins is highly recommended.

2.3.13 Initial bootstrap capacitor charging

During the startup phase, the bootstrap capacitor must be charged for a suitable time to complete the initial charging time (t_{CHARGE}) which is, at least, the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold $V_{BS\_th(on)}$, as previously stated in (Equation 8). For a normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold $V_{BS\_th(off)}$ throughout the working conditions. For the startup period, only the low side IGBT is switched on and just after this phase the PWM is run, as shown in the following steps of Figure 21. Initial bootstrap charging time:

- t1: the bootstrap capacitor starts to charge through the low side IGBT (LVG)
- t2: the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold $V_{BS\_th(on)}$
- t3: the bootstrap capacitor is fully charged, this enables the high side IGBT and the C_{BOOT} capacitor starts to discharge in order to provide the right IGBT gate charge. The bootstrap capacitor recharges during the on state of low side IGBT (LVG).

Figure 21. **Initial bootstrap charging time**



The initial charging time is given by Equation 11 and must be, for safety reasons, at least three times longer than the calculated value.

Equation 11

$$t_{CHARGE} \geq \frac{C_{BOOT} \cdot R_{DS(on)}}{\delta} * ln\left(\frac{V_{CC}}{\Delta V_{CBOOT}}\right) \quad (11)$$

where δ is the duty cycle of the PWM signal and $R_{DS(on)}$ is 120 Ω typical value, as shown in the datasheet.

A practical example can be done by considering a motor drive application where the PWM switching frequency is 16 kHz, with a duty cycle of 50%, and ΔV_{CBOOT} = 0.1 V (this means a gate driver supply voltage V_{CC} = 16.9 V). From the graph in Figure 20 the bootstrap capacitance is 0.9 µF, therefore the C_{BOOT} can be selected by using a value between 2.2 and 3.3 µF. According to the commercial value the bootstrap capacitor can be 2.2 µF. From Equation 11, the initial charging time is:

Equation 12

$$t_{CHARGE} \geq \frac{2.2 \cdot 10^{-6} \cdot 120}{0.5} \cdot ln\left(\frac{16.9}{0.1}\right) = 2.7ms \quad (12)$$

For safety reasons, the initial charging time must be at least 8.1 ms.

3 Package

The N2DIP-26L is a 26 lead dual-in-line transfer mold package capable of meeting the demanding cost and size requirements of consumer appliance inverters. It consists of a copper lead frame with power stage and control stage soldered on it and housed using the transfer molding process. The excellent thermal properties of the copper allows good heat distribution and heat transfer. The thickness and the layout of the lead frames has been optimized to further reduce thermal resistance compared to the previous series.

Furthermore, this new package is designed to allow a better and more easily screwed-on heat sink thanks to the dedicated slots for screws placed on the short side of the package. This characteristic allows the SLLIMM-nano 2nd series to be used in higher power level applications than the 1st series. The new series is offered in two lead options: zig-zag and in-line leads.

The zig-zag leads option is pin-to-pin compatible with previous series for a natural extension targeting higher power-level sockets.

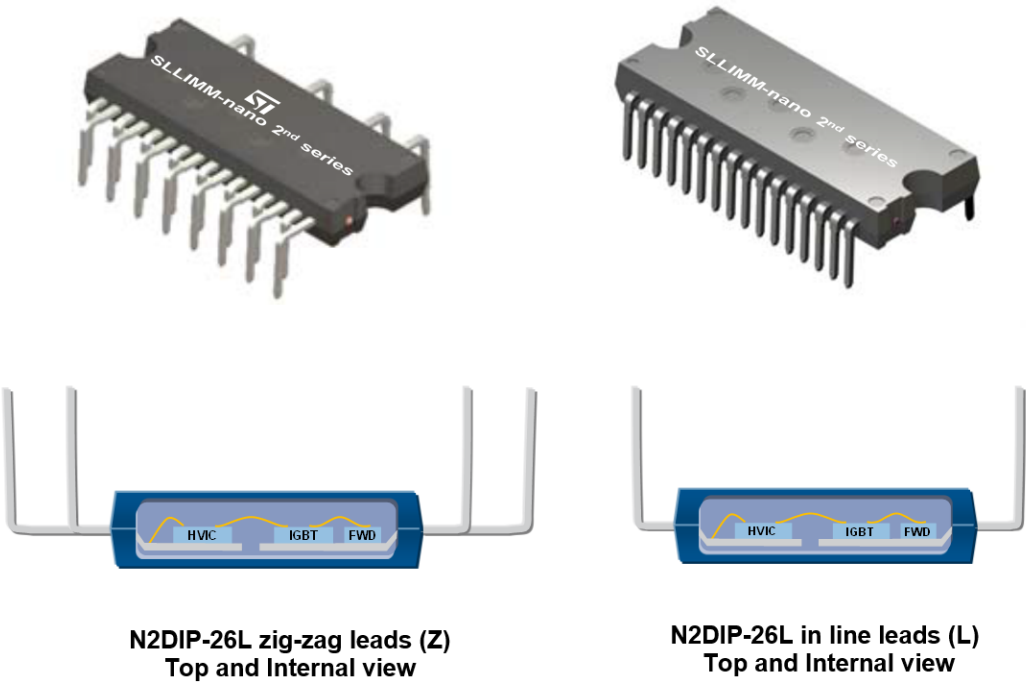
The new in-line leads option offers further compactness thanks to the aligned leads and satisfies the needs of applications with space constraint requirements.

Both lead options have been designed to maximize the distance between the high voltage and low voltage pins, by placing the relevant pins on the opposite side of the package. This is mainly useful to keep a safe distance between high voltage and low voltage pins and for easy PCB layout.

3.1 Package structure

The Figure 22 shows images and the internal structure of the N2DIP-26L package.

Figure 22. Images and internal view of N2DIP-26L package

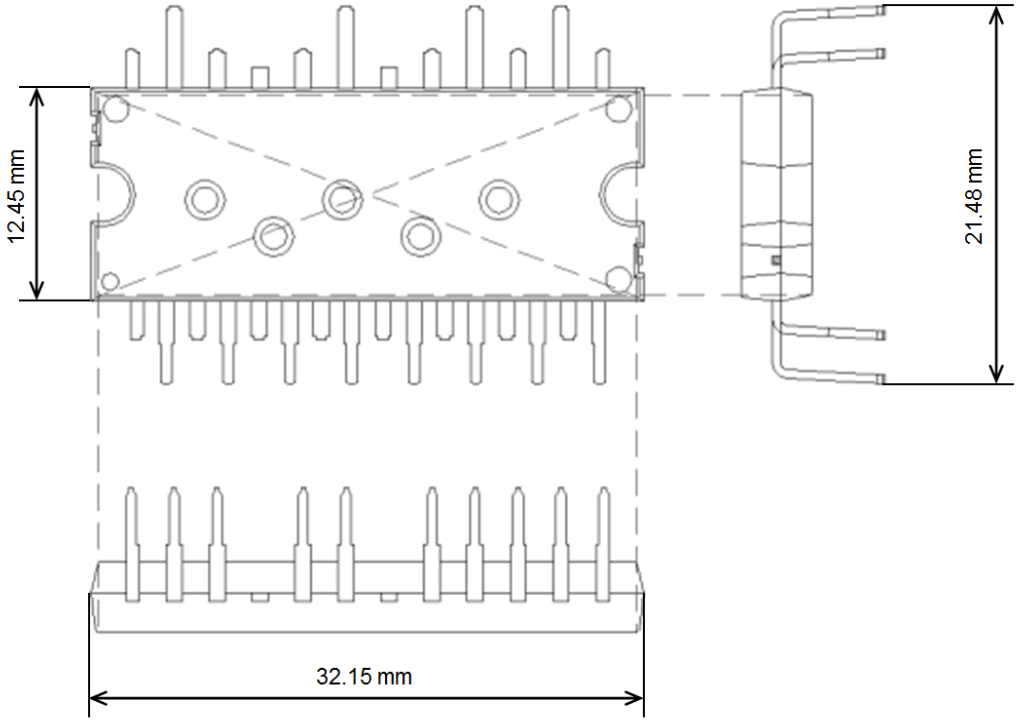


N2DIP-26L zig-zag leads (Z)
Top and Internal view

N2DIP-26L in line leads (L)
Top and Internal view

3.2 Package outline and dimensions

Figure 23. **N2DIP-26L package outline**



3.3 Input and output pin description

This section defines the input and output pins of the SLLIMM-nano 2nd series. For a more accurate description and layout suggestions, please consult the relevant sections.

Table 9. **Input and output pins**

Pin #	Name	Description
1	GND	Ground
2	T / $\overline{SD}$ / OD	NTC thermistor / shut down logic input (active low) / open drain (comparator output)
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High side logic input for W phase
5	LIN W	Low side logic input for W phase (active high)
6	OP+	Op-amp non inverting input
7	OP_{OUT}	Op-amp output
8	OP-	Op-amp inverting input
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High side logic input for V phase
11	LIN V	Low side logic input for V phase (active high)
12	CIN	Comparator input
13	V_{CC} U	Low voltage power supply U phase

Pin #	Name	Description
14	HIN U	High side logic input for U phase
15	T / $\overline{SD}$ / OD	NTC thermistor / Shut down logic input (active low) / open drain (comparator output)
16	LIN U	Low side logic input for U phase (active high)
17	V_{boot} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT U	U phase output
20	N U	Negative DC input for U phase
21	V_{boot} V	Bootstrap voltage for V phase
22	V, OUT V	V phase output
23	N V	Negative DC input for V phase
24	V_{boot} W	Bootstrap voltage for W phase
25	W, OUT W	W phase output
26	N W	Negative DC input for W phase

High side bias voltage pins / high side bias voltage reference

Pins: V_{bootU}-U, V_{bootV}-V, V_{bootW}-W

- The bootstrap section is designed to realize a simple and efficient floating power supply, in order to provide the gate voltage signal to the high side IGBTs.
- The SLLIMM-nano 2nd series family integrates the bootstrap diodes. This helps customers to reduce cost, board space, and number of components.
- The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high side IGBTs.
- Each bootstrap capacitor is charged from the V_{CC} supply during the on-state of the corresponding low side IGBT.
- To prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.
- The value of bootstrap capacitors is strictly related to the application conditions. Please consult Section 2.3.11 Bootstrap circuit for more information.

Gate driver bias voltage

Pins: $V_{CC\ U}$, $V_{CC\ V}$, $V_{CC\ W}$

- Control supply pins for the built-in ICs.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitors should be mounted close to these pins.

Gate drive supply ground

Pin: GND

- Ground reference pin for the built-in ICs.
- To avoid noise influences, the main power circuit current should not be allowed to flow through this pin (see Section 5.2 Layout suggestions).

Signal input

Pins: HIN_U, HIN_V, HIN_W; LIN_U, LIN_V, LIN_W:

- These pins control the operation of the built-in IGBTs.
- The signal logic of HIN_x and LIN_x pins is active high. The IGBT associated with each of these pins is turned on when a sufficient logic (higher than a specific threshold) voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the device against noise influences. RC coupling circuits should be adopted for the prevention of input signal oscillation. Suggested values are R=100 Ω and C=1 nF.

Internal non-inverting comparator

Pin: CIN

- The current sensing shunt resistor, connected on each phase leg, could be used by the internal comparator (pin CIN) to detect short-circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter (typically ~1 us) should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.
- If a voltage signal, higher than the specified V_{REF} (see datasheet), is applied to this pin, the SLLIMM-nano 2nd series automatically shuts down and the T / $\overline{SD}$ / OD pin is pulled down (to inform the microcontroller).

NTC thermistor / Shutdown / open drain

Pins: T / $\overline{SD}$ / OD

- There are two available pins of T / $\overline{SD}$ / OD which are exactly the same. They are placed on the opposite ends of the package in order to offer higher flexibility to the PCB layout. It is sufficient to use only one of two pins for the proper functioning of the device.
- The T / $\overline{SD}$ / OD pins work as an enable/disable pins.
- The signal logic of T / $\overline{SD}$ / OD pins are active low. The SLLIMM-nano 2nd series shuts down if a voltage lower than a specific threshold is applied to these pins, leading each half bridge in tri-state.
- The T / $\overline{SD}$ / OD status is connected also to the internal comparator status (Section 2.3.6 Short-circuit protection and smart shutdown function). When the comparator triggers, the T /SD / OD pin is pulled down acting as a FAULT pin.
- The T / $\overline{SD}$ / OD, when pulled down by the comparator, are open drain configured. The T / $\overline{SD}$ / OD voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.
- The T / $\overline{SD}$ / OD pin can be used for temperature monitoring as well, thanks to the co-packaged NTC thermistor. A resistor R_{SD} of 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU power supplies, respectively, is required to avoid undesired shutdown, along with a capacitor C_{SD} no higher than 1 us for effective protection. For further details, refer to Section 2.3.7 Timing chart of short-circuit protection and smart shutdown function.

Integrated operational amplifier

Pins: OP+, OP-, OP_{OUT}

- The op-amp is completely uncommitted.
- The op-amp performances are optimized for advanced control technique (FOC).
- Thanks to the integrated op-amp it is possible to realize compact and efficient board layout, minimizing the required BOM list.

Positive DC-link

Pin: P

- This is a DC-link positive power supply pin of the inverter and it is internally connected to the collectors of the high side IGBTs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a snubber capacitor close to this pin (typically, high voltage metal film capacitors of about 0.1 or 0.22 µF).

Negative DC-link

Pins: N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low side IGBT emitters of each phase.
- The power ground of the application should be separated from the logic ground of the system and they should be reconnected at one specific point (star connection).

Inverter power output

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

4 Power loss and dissipation

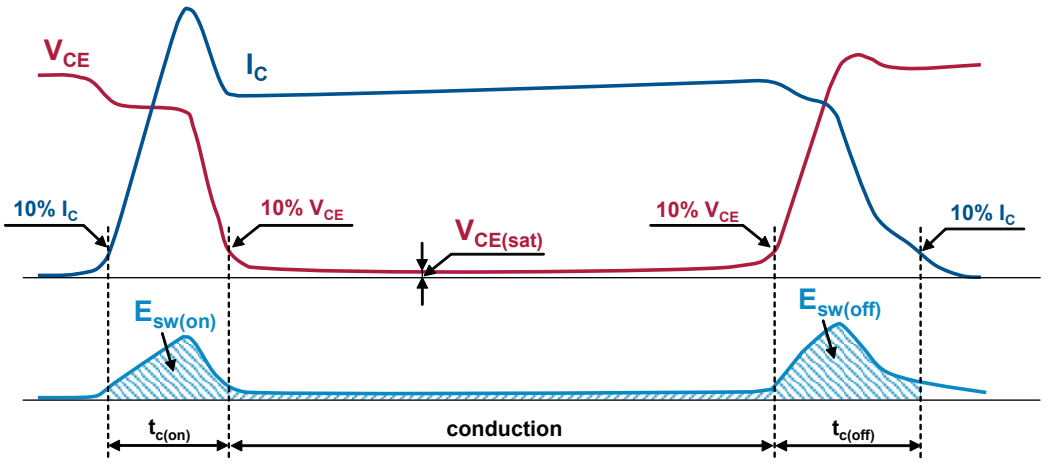
The total power loss in an inverter is comprised of conduction loss, switching loss, and off-state loss and they is essentially generated by the power devices of the inverter stage, such as the IGBTs and the freewheeling diodes. The conduction loss (P_{cond}) is the on-state loss during the conduction phase. The switching loss (P_{sw}) is the dynamic loss encountered during the turn-on and the turn-off. The off-state loss, due to the blocking voltage and leakage current, can be neglected. Finally, the total power loss is given by:

Equation 13

$$P_{tot} \approx P_{cond} + P_{sw} \tag{13}$$

Figure 24 shows a typical waveform of an inductive hard switching application such as a motor drive, where the major sources of power loss are specified.

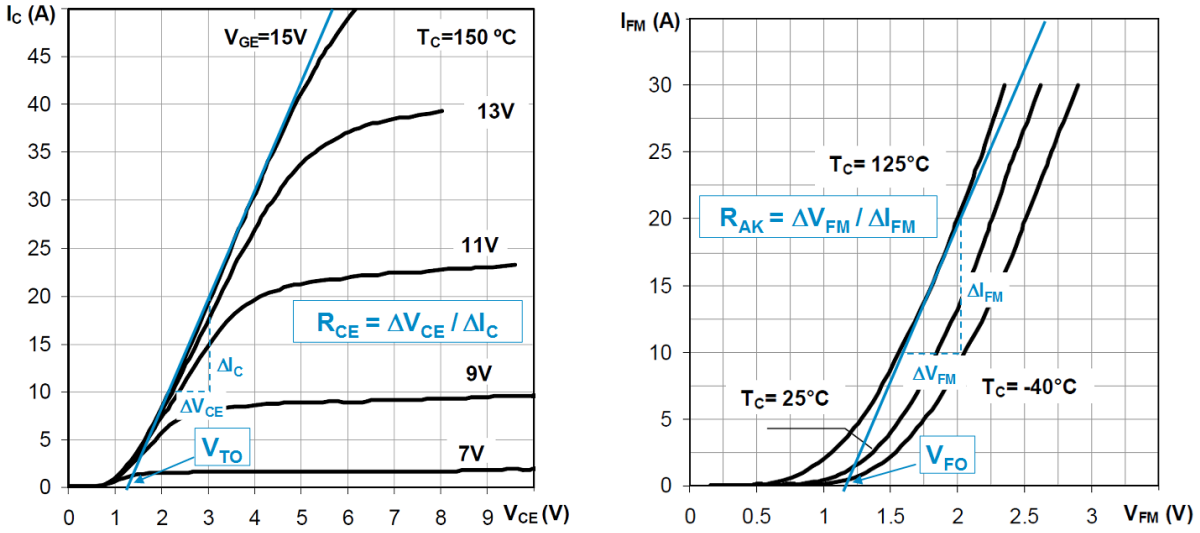
Figure 24. Typical IGBT power loss



4.1 Conduction power loss

The conduction loss is caused by IGBT and freewheeling diode forward voltage drop at rated current. They can be calculated using a linear approximation of the forward characteristics for both IGBT and diode, having a series connection of DC voltage source representing the threshold voltage, V_{TO} for IGBT, (and V_{FO} for diode) and a collector emitter on-state resistance, R_{CE}, (and anode cathode on-state resistance, R_{AK}), as shown in Figure 25, for reference.

Figure 25. **Examples of IGBT and diode approximation of the output characteristic**



Both forward characteristics are temperature-dependent, and thus must be considered under a specified temperature. The linear approximations can be translated for IGBT in the following equation:

Equation 14

$$v_{ce}(i_c) = V_{TO} + R_{CE} \cdot i_c \tag{14}$$

and, for freewheeling diode:

Equation 15

$$v_{fm}(i_{fm}) = V_{FO} + R_{AK} \cdot i_{fm} \tag{15}$$

The conduction loss of the IGBT and diode can be derived as the time integral of the product of conduction current and voltage across the devices, as follows:

Equation 16

$$P_{cond\_IGBT} = \frac{1}{T}\int_0^T v_{ce} \cdot i_c(t)\,dt = \frac{1}{T}\int_0^T \left(V_{TO} \cdot i_c(t) + R_{ce} \cdot i_c^2(t)\right)dt \tag{16}$$

Equation 17

$$P_{cond\_Diode} = \frac{1}{T}\int_0^T v_f \cdot i_f(t)\,dt = \frac{1}{T}\int_0^T \left(V_{FO} \cdot i_f(t) + R_{AK} \cdot i_f^2(t)\right)dt \tag{17}$$

where T is the fundamental period. The different utilization modes of SLLIMM-nano 2nd series, modulation technique, and working conditions make the power loss very difficult to estimate; it is therefore necessary to establish some starting points.

Assuming that:

1. the application is a variable voltage variable frequency (VVVF) inverter based on sinusoidal PWM technique
2. the switching frequency is high and therefore the output currents are sinusoidal
3. the load is ideal inductive

Under these conditions, the output inverter current is given by:

Equation 18

$$i = \hat{I}\cos(\theta\text{-}\varphi) \tag{18}$$

where Î is the current peak, θ stands for ωt and ϕ is the phase angle between output voltage and current.

The conduction power loss can be obtained as:

Equation 19

$$P_{\text{cond\_IGBT}} = \frac{V_{\text{TO}} \cdot \hat{I}}{2\pi} \int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} \xi \cos(\theta - \varphi) d\theta + \frac{R_{\text{CE}} \cdot \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} \xi \cos^2(\theta - \varphi) d\theta \quad (19)$$

Equation 20

$$P_{\text{cond\_Diode}} = \frac{V_{\text{FO}} \hat{I}}{2\pi} \int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} (1 - \xi) \cos(\theta - \varphi) d\theta + \frac{R_{\text{AK}} \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} (1 - \xi) \cos^2(\theta - \varphi) d\theta \quad (20)$$

where ξ is the duty cycle for this PWM technique and is given by:

Equation 21

$$\xi = \frac{1 + m_a \cdot cos\theta}{2} \quad (21)$$

and m_a is the PWM amplitude modulation index.

Finally, solving Equations Equation 19 and Equation 20, we have:

Equation 22

$$P_{\text{cond\_IGBT}} = V_{\text{TO}} \cdot \hat{I} \left(\frac{1}{2\pi} + \frac{m_a \cdot cos\varphi}{8} \right) + R_{\text{CE}} \cdot \hat{I}^2 \left(\frac{1}{8} + \frac{m_a \cdot cos\varphi}{3\pi} \right) \quad (22)$$

Equation 23

$$P_{\text{cond\_Diode}} = V_{\text{FO}} \cdot \hat{I} \left(\frac{1}{2\pi} - \frac{m_a \cdot cos\varphi}{8} \right) + R_{\text{AK}} \cdot \hat{I}^2 \left(\frac{1}{8} - \frac{m_a \cdot cos\varphi}{3\pi} \right) \quad (23)$$

and therefore, the conduction power loss of one device (IGBT and diode) is:

Equation 24

$$P_{\text{cond}} = P_{\text{cond\_IGBT}} + P_{\text{cond\_Diode}} \quad (24)$$

Of course, the total conduction loss per inverter is six times this value.

4.2 Switching power loss

The switching loss is the power consumption during the turn-on and turn-off transients. As shown in Figure 24. Typical IGBT power loss, it is given by the pulse of power dissipated during the turn-on (t_{on}) and turn-off (t_{off}). Experimentally, it can be calculated by the time integral of the product of the collector current and collector-emitter voltage for the switching period. In any case, the dynamic performances are strictly related to many parameters such as voltage, current and temperature, so it is necessary to use the same conduction power loss assumptions (Section 4.1 Conduction power loss) to simplify the calculations.

Under these conditions, the switching energy loss is given by:

Equation 25

$$E_{\text{on}}(\theta) = \hat{E}_{\text{on}} \cos(\theta - \varphi) \quad (25)$$

Equation 26

$$E_{\text{off}}(\theta) = \hat{E}_{\text{off}} \cos(\theta - \varphi) \quad (26)$$

where $\hat{E}_{on}$ and $\hat{E}_{off}$ are the maximum values taken at T_{jmax} and $\hat{I}_c$, θ stands for ωt and ϕ is the phase angle between output voltage and current.

Finally, the switching power loss per device depends on the switching frequency (f_{sw}) and is calculated as follows:

Equation 27

$$P_{sw} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi}\left(E_{IGBT} + E_{Diode}\right)\cdot f_{sw}d\theta = \frac{\left(E_{IGBT} + E_{Diode}\right)\cdot f_{sw}}{\pi} \quad (27)$$

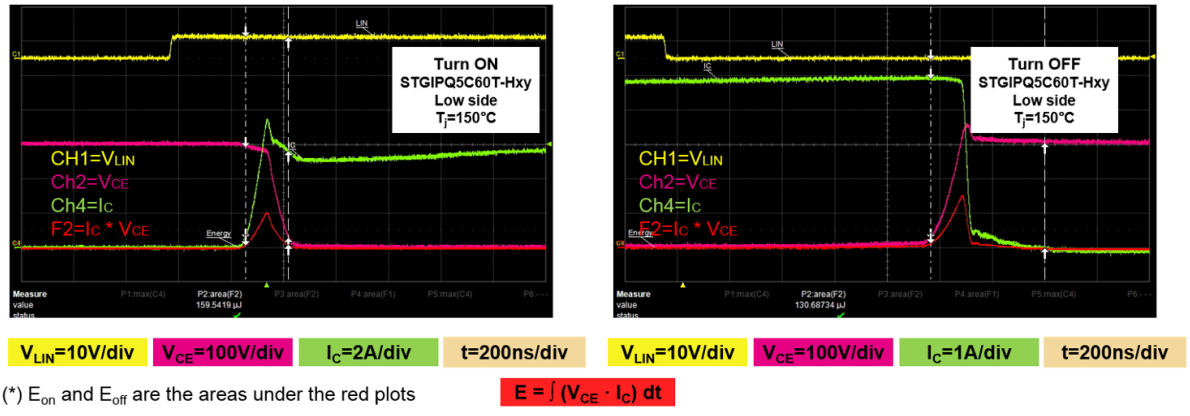
where E_{IGBT} and E_{Diode} are the total switching energy for the IGBT and freewheeling diode, respectively. Also in this case, the total switching loss per inverter is six times this value.

Figure 26 shows the real turn-on and turn-off waveforms of STGIPQ5H60T-Hyy under the following conditions:

- V_{PN} = 300 V, I_C = 5 A, T_j = 150 °C with inductive load on full bridge topology, taken on the low side IGBT.

The red plots represent instantaneous power as a result of I_C (in green) and V_{CE} (in pink) waveform multiplication, during the switching transitions. The areas under these plots are the switching energies computed by graphic integration, thanks to the digital oscilloscope.

Figure 26. Typical switching waveforms of the STGIPQ5H60T-Hyy



(*) E_{on} and E_{off} are the areas under the red plots

$E = \int (V_{CE} \cdot I_C)\, dt$

4.3 Thermal impedance overview

During operation, power loss generates heat which elevates the temperature in the internal semiconductor junctions, limiting its performance and lifetime. To ensure safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system.

The most common schemes are based on one heat sink designed for free conventional air flow or, in some cases, for forced air circulation. Free conventional air flow systems require larger heat sinks (about 50% bigger) than a forced air based heat sink, for a given thermal resistance. Therefore, the choice of the cooling system becomes the starting point for the application designer and the thermal aspect of the system is one of the key factors in designing high efficiency and high reliability equipment. In this respect, the package and its thermal resistance plays a fundamental role.

Thermal resistance quantifies the ability of a given thermal path to transfer heat in the steady-state and is generally expressed as the ratio between the temperature increase above the reference and the relevant power flow:

Equation 28

$$R_{th} = \frac{\Delta T}{\Delta P} \quad (28)$$

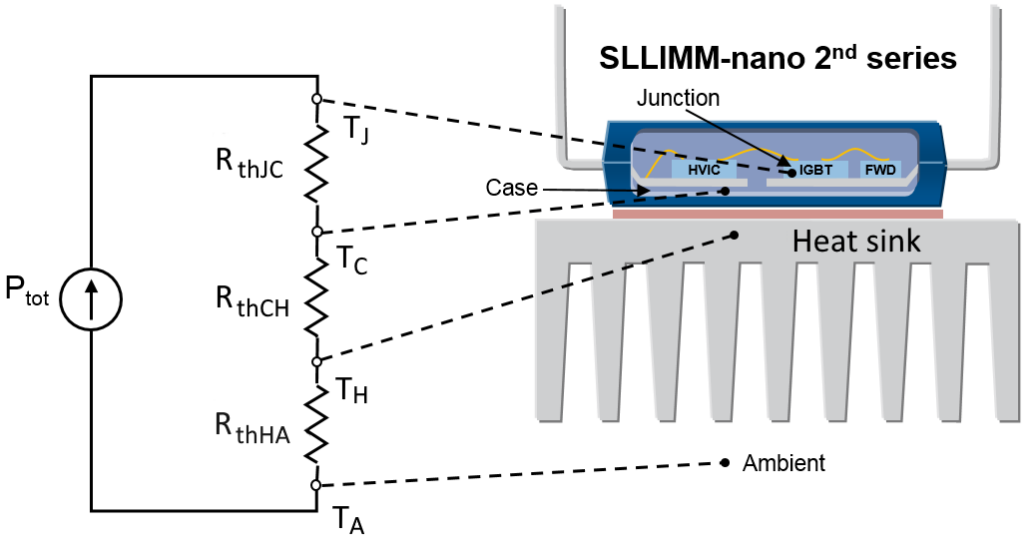
The thermal resistance specified in the datasheet is the junction-case R_{thJC}, defined as the temperature difference between the junction and case reference divided by the power dissipation per device:

Equation 29

$$R_{\mathrm{thJC}} = \frac{T_J - T_C}{P_D} \tag{29}$$

The full molded package is used as the cooling interface to the heat sink. Thermal grease or some other thermal interface material between the backside and the heat sink is used to reduce the thermal resistance of the interface (R_{thCH}) and, of course, depends on the material and its thickness. Basically, the sum of the three thermal resistance components above gives the thermal resistance between junction and ambient R_{thJA}, as shown in the figure below.

Figure 27. Equivalent thermal circuit with heat sink single IGBT



As the power loss P_{tot} is cyclic, the transient thermal impedance must also be considered. It is defined as the ratio between the time dependent temperature increase above the reference, $\Delta T(t)$, and the relevant heat flow:

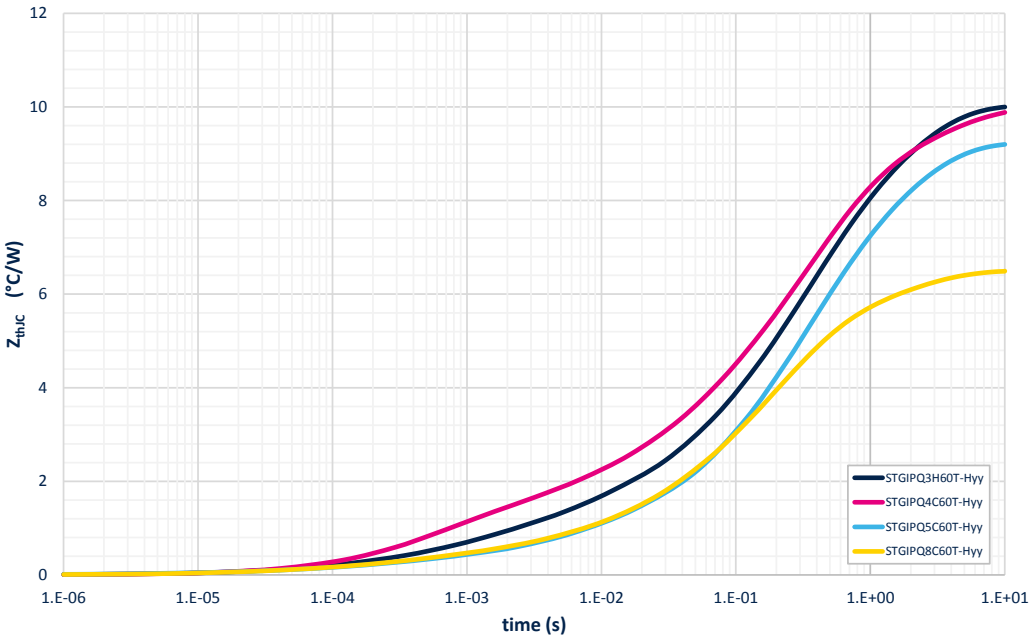
Equation 30

$$Z_{\mathrm{th}}\left(t\right) = \frac{\Delta T(t)}{\Delta P} \tag{30}$$

Contrary to what we have already seen regarding the thermal resistance, the thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM-nano 2nd series.

For example, Figure 28 shows thermal impedance from junction-to-case curve for a single IGBT of SLLIMM-nano 2nd series.

Figure 28. **Thermal impedance ZthJC curve for a single IGBT**



More generally, in the case of the device, power is time-dependent too. The device temperature can be calculated by using the convolution integral method applied to the Equation 30, as follows:

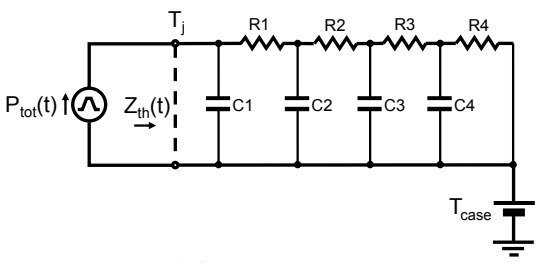
Equation 31

$$\Delta T(t) = \int_0^t Z_{\text{th}}(t-\tau) \cdot P(\tau) d\tau \quad (31)$$

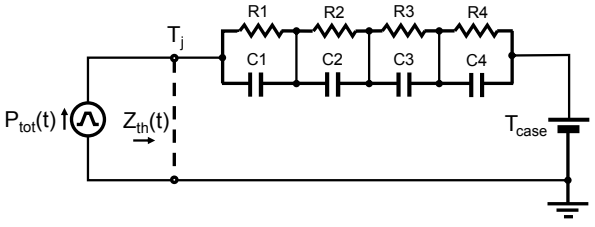
An alternative method, very useful for the simulator tools, is the transient thermal impedance model, which provides a simple method to estimate the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance $Z_{th(t)}$ can be transformed into an electrical equivalent RC network. The number of RC sections increases the model detail, therefore a fourth order model based on the Cauer network has been adopted to improve the accuracy of the model, as shown in Figure 29.

Figure 29. **RC Cauer and Foster thermal networks**



RC Cauer thermal network



RC Foster thermal network

Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances respectively. The case temperature is represented with a DC voltage source and it can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from that equation and are defined in the Table 10.

Table 10. **Cauer and Foster RC thermal network elements for SLLIMM-nano 2nd series**

Element	STGIPQ3H60T-Hyy		STGIPQ4C60T-Hyy		STGIPQ5C60T-Hyy		STGIPQ8C60T-Hyy	
	Cauer	Foster	Cauer	Foster	Cauer	Foster	Cauer	Foster
R1 (°C/W)	0.2	0.1	1.5	4.7	0.1	0.075	0.2	0.17
R2 (°C/W)	1.2	1.1	2.3	1.4	0.6	0.5	1	0.8
R3 (°C/W)	4.5	3.4	4.5	1.7	4	4	3.7	3.5
R4 (°C/W)	4.1	5.4	1.7	2.2	4.5	4.63	1.6	2
C1 (W·s/°C)	0.2E-03	0.22E-03	0.43E-03	0.64E-01	0.14E-03	0.19E-03	0.36E-03	0.4E-03
C2 (W·s/°C)	0.12E-02	0.12E-02	0.10E-01	0.45E-03	0.15E-02	0.13E-02	0.37E-02	0.45E-02
C3 (W·s/°C)	0.25E-01	0.23E-01	0.59E-01	0.125E-01	0.24E-01	0.29E-01	0.31E-01	0.35E-01
C4 (W·s/°C)	0.23	0.2	1.46	1.18	0.22	0.27	0.72	0.6

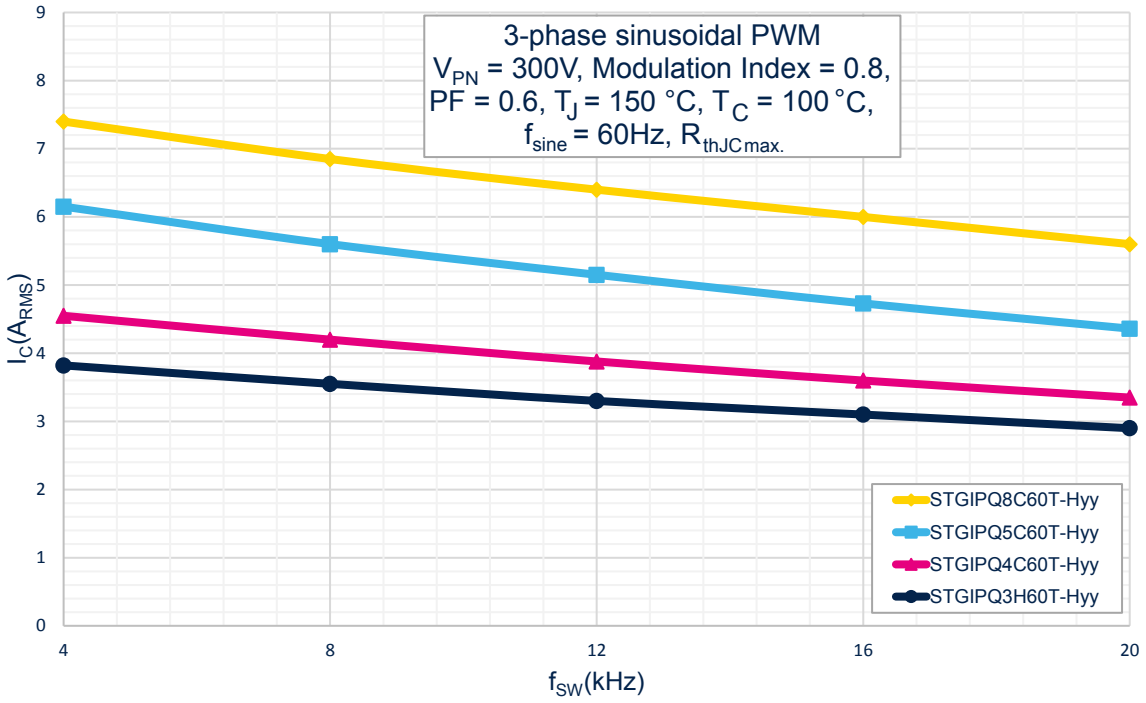
4.4 Power loss calculation example

As a result of the power loss calculation and thermal aspects discussed in the previous sections, we are able to simulate the maximum $I_{C(RMS)}$ current versus switching frequency curves for a VVVF inverter using a 3-phase sinusoidal PWM to synthesize sinusoidal output currents.

The curves graphed in Figure 30 represent the maximum current managed by the SLLIMM-nano 2nd series in safety conditions, when the junction temperature rises to the maximum junction temperature of 150 °C and the case temperature is 100 °C, which is a typical operating condition to guarantee the reliability of the system. These curves, which are functions of the motor drive typology and control scheme, are simulated under the following conditions:

- V_{PN} = 300 V, MI = 0.8, PF = 0.6, T_j = 150 °C, T_{case} = 100 °C, f_{sine} = 60 Hz, max value of R_{thJC}, typical $V_{CE(sat)}$ and E_{tot} values.

Figure 30. **Maximum I_C(RMS) current vs. fsw (simulated curves)**



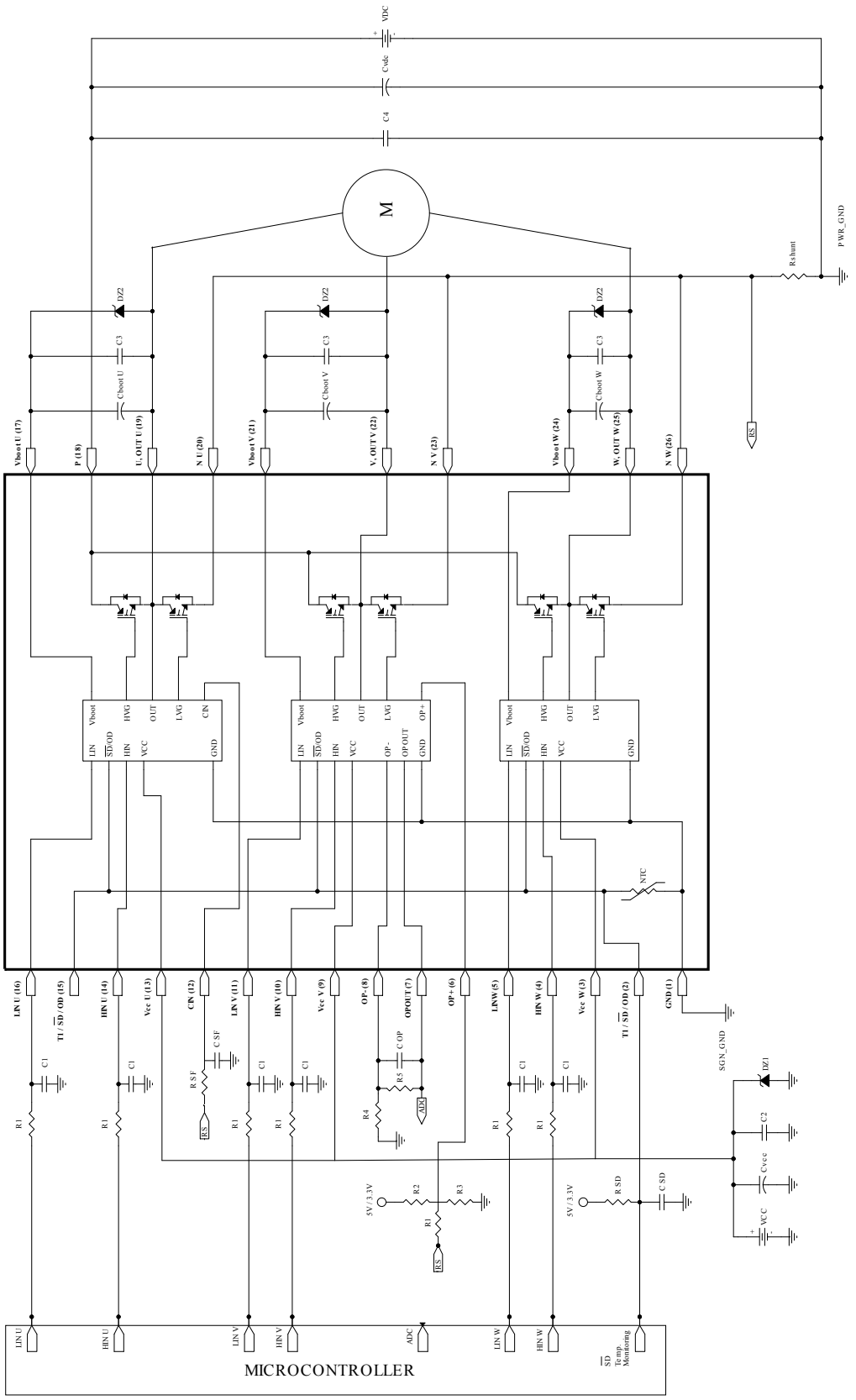
5 Design and mounting guidelines

In this section the main layout suggestions for an optimized design and major mounting recommendations to appropriately handle and assemble the SLLIMM-nano 2nd series family, will be introduced.

5.1 Typical circuit and recommendations

The figure below shows a typical application circuit using the SLLIMM-nano 2nd series, including signal interfaces with the MCU.

Figure 31. **Typical application circuit**



Below are some hardware and PCB layout recommendations:

1. Input signals HIN and LIN are active-high logic. A 375 kΩ typ. pull-down resistor is built-in for each high-side input. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is suggested. The filters should be implemented with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
2. Bypass capacitor C_{VCC} (aluminum or tantalum) is recommended to reduce the transient circuit demand on the power supply. In addition, a decoupling capacitor C2 (100 to 220 nF, with low ESR, low ESL) is suggested to reduce high frequency switching noise distributed on the power supply lines. It must be placed as close as possible to the VCC pin and in parallel with the bypass capacitor.
3. The use of the RC filter (R_{SF}, C_{SF}) to help prevent malfunction of the protection circuit is recommended. The time constant (R_{SF} x C_{SF}) should be set to 1 us and the filter placed as close as possible to the CIN pin.
4. The SD pin is an input/output pin (open drain type if used as output). An integrated NTC thermistor is connected internally between the SD pin and GND. The pull-up resistor R_{SD} causes the voltage V_{SD-GND} to decrease as the temperature increases. To always maintain the voltage above the high-level logic threshold, use a 1 kΩ or 2.2 kΩ pull-up resistor for a 3.3 V or 5 V MCU power supply, respectively. Size the filter on SD appropriately to obtain the desired restart time after a fault event, and place it as close as possible to the SD pin.
5. Decoupling capacitor C3 (100 to 220 nF, with low ESR and low ESL) in parallel with each Cboot is recommended in order to filter high frequency disturbances. Both Cboot and C3 must be placed as close as possible to the U, V, W and Vboot pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.
6. A Zener diode (Dz1) between each V_{CC} pin and GND, and in parallel (Dz2) with each Cboot is suggested in order to prevent overvoltage.
7. Capacitor C4 (100 to 220 nF, low ESR and low ESL) in parallel with the electrolytic capacitor Cvdc is recommended in order to prevent surge destruction. Both capacitors C4 and Cvdc should be placed as close as possible to the IPM (C4 has priority over Cvdc).
8. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
9. Low inductance shunt resistors should be used for phase leg current sensing.
10. In order to avoid malfunction, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
11. It is recommended to connect SGN_GND to PWR_GND at only one point (near the shunt resistor terminal), in order to avoid any malfunction due to power ground fluctuation.

5.2 Layout suggestions

PCB layout optimization for high voltage, high current and high switching frequency applications is a critical factor. PCB layout is a complex matter involving several aspects such as track length and width and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application function properly and achieve expected performance. On the other hand, PCBs without careful layout can generate EMI issues (both induced and perceived by the application), can provide overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.

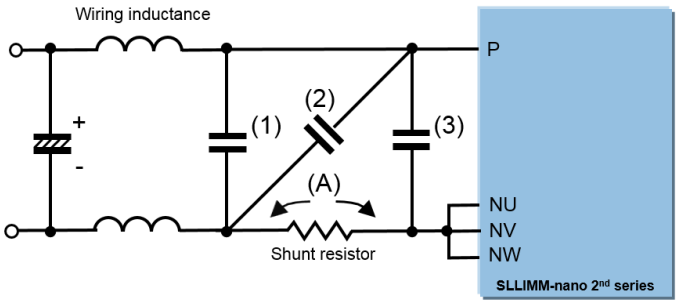
The compactness of the SLLIMM-nano 2nd series solution, which offers an optimized gate driving network and reduced parasitic elements, allows designers to concentrate on other issues such as the ground or noise filter. In any case, to avoid the aforementioned conditions, the following general PCB layout guidelines and suggestions should be followed for 3-phase applications.

For more information please refer to application note AN4694.

5.2.1 General suggestions

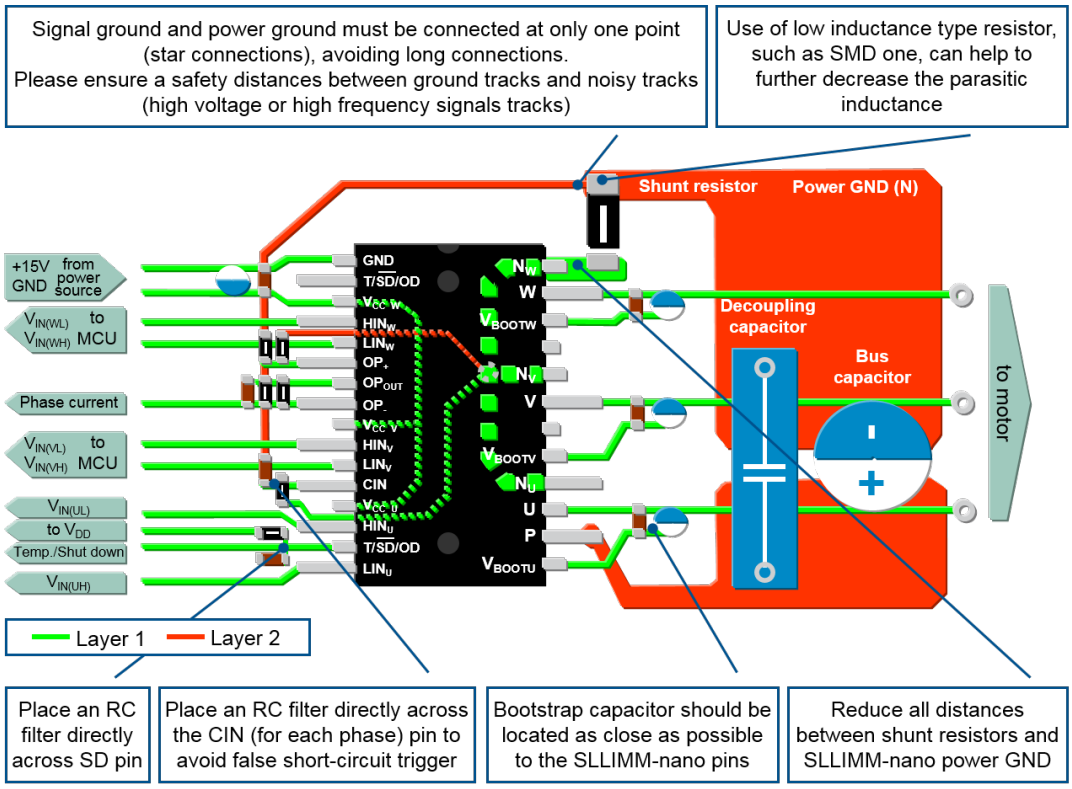
1. PCB traces should be designed as short as possible and the area of the circuit (power or signal) minimized to reduce the sensitivity of such structures to surrounding noise.
2. Ensure a good distance between switching lines with high voltage transitions and the signal lines sensitive to electrical noise. Specifically, the tracks of each OUT phase carrying significant currents and voltages should be separated from logic lines and analog op-amp and comparator sensing circuits.
3. Place the R_{SENSE} resistors as close as possible to the low-side pins of the SLLIMM-nano 2nd series (N U, N V and N W). Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the SLLIMM-nano 2nd series directly to the cold terminal of sense resistors. Use a low inductance type resistor, such as an SMD resistor instead of long lead type resistors, to help further decrease parasitic inductance.
4. Avoid any ground loop. Only a single path must connect two different ground nodes.
5. Place each RC filter as close as possible to the SLLIMM-nano 2nd series pins in order to increase their effectiveness.
6. Fixed voltage tracks such as GND or HV lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines (e.g., OUT U, OUT V and OUT W).
7. Generally, it is recommended to connect each half bridge ground in a star configuration and the three R_{SENSE} very close to each other and to the power ground.
8. In order to prevent surge destruction, the wiring between the snubber capacitor and the P N pins should be as short as possible. The use of a high frequency, high voltage non-inductive capacitor of about 0.1 or 0.22 µF is recommended. In order to effectively suppress the surge voltage, the snubber capacitor has to be placed in position (2) in Figure 32. The position (1) is incorrect for effective surge voltage suppression. If the capacitor is placed on the position (3), the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor with possible undesired protection activation, even if the surge suppression effect is the greatest. Finally, position (2) is the right compromise. The parasitic inductance on the A tracks (including that of the shunt resistor) should be as small as possible in order to suppress the surge voltage

Figure 32. Recommended snubber capacitor position



In Figure 33, general suggestions for all SLLIMM-nano products are summarized.

Figure 33. **General suggestions**



6 Mounting and handling instructions

Some basic assembly rules must be followed in order to limit thermal and mechanical stress and optimize the thermal conduction and electrical isolation for the N2DIP-26L package when mounting a heat sink.

Moreover, semiconductors are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. Static discharges caused by human touch or by processing tools may cause high-current and/or high-voltage pulses which may damage or even destroy sensitive semiconductor structures. Integrated circuits (ICs) may also be charged by static during processing. If discharging takes place too quickly (“hard” discharge), it may cause peak loads and consequent damage.

Make careful choices regarding workspaces, personal equipment and processing and assembly equipment.

6.1 Heat sink mounting

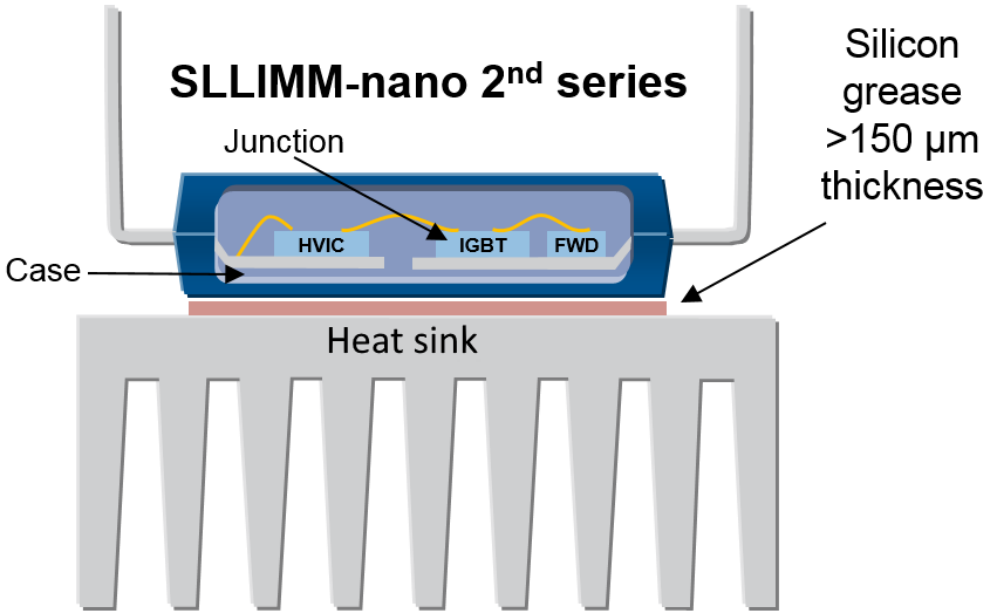
When attaching a heat sink to a SLLIMM-nano 2nd series, do not apply excessive force to the device for assembly. Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions. Do not touch the heat sink when the SLLIMM-nano 2nd series is operational to avoid burn injury.

To get the most effective heat dissipation, enlarge the contact area as much as possible to minimize the contact thermal resistance. Properly apply thermal-conductive grease over the contact surface between modules and heat sinks, is also useful for preventing contact surfaces from corrosion. Apply a minimum 150 µm layer of thermal grease to the module base plate or to the heat sink, as shown in the figure below. Use a torque screwdriver to fasten to the max specified torque rating. Exceeding the maximum torque may lead to module damage or degradation.

Remove any dirt from the contact surface.

Ensure the grease quality remains constant over time and is able to perform long-term over a wide operating temperature range.

Figure 34. Recommended silicon grease thickness and positioning



6.1.1 Mounting torque

Mounting torque and heat sink flatness specifies the correct fastening torque. Inappropriate mounting can damage the device and over tightening the screws may cause DBC substrate or molding compound cracks. Avoid mechanical stress due to tightening on one side only. It is recommended to first lightly fasten both screws fastening them permanently to the specified torque value with a torque wrench.

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3	Recommended 0.55 N•m	0.40	0.55	0.70	N•m
Device flatness	See Figure 35		0		+100	µm
Heat sink flatness	See Figure 36		-50		+100	µm

The following two figures provide device and heat sink flatness details, respectively.

Figure 35. Device flatness specification

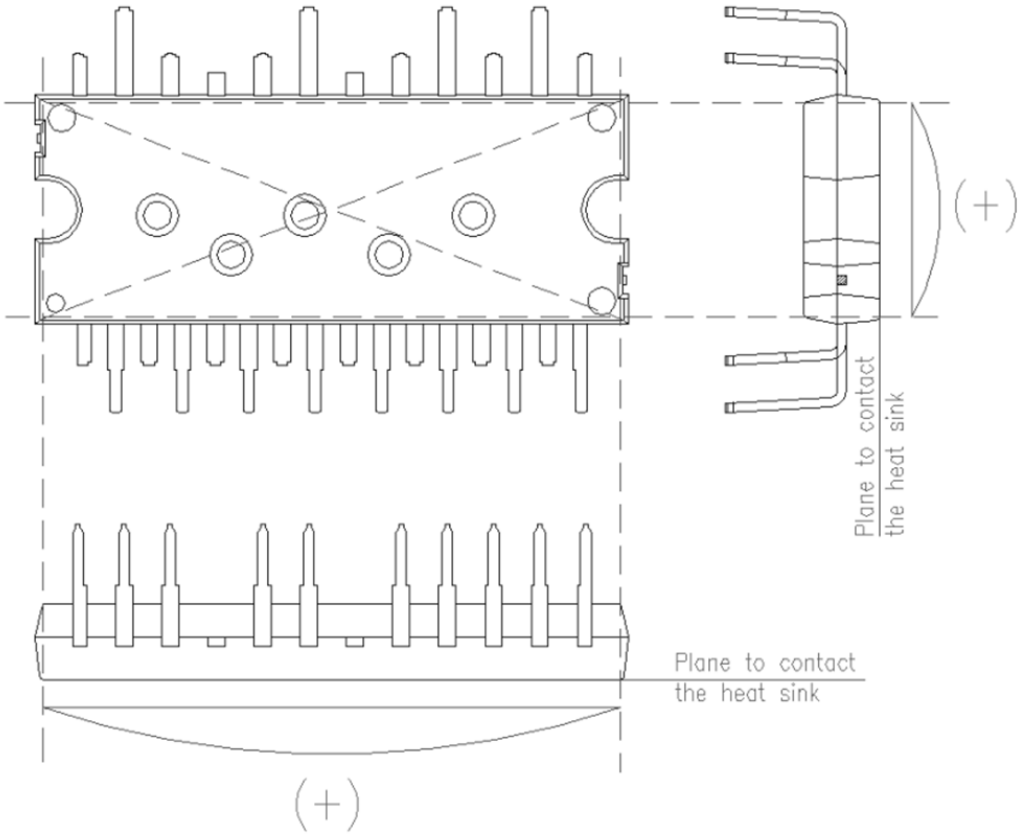
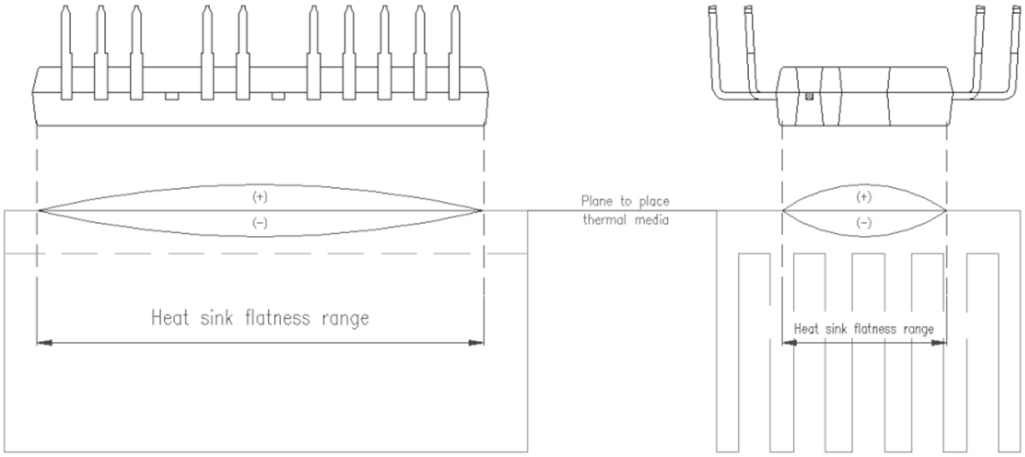


Figure 36. **Heat sink flatness specification**



Do not exceed the specified fastening torque. Over-tightening the screws may cause ceramic or molding compound cracks and heat-fin threaded hole destruction.

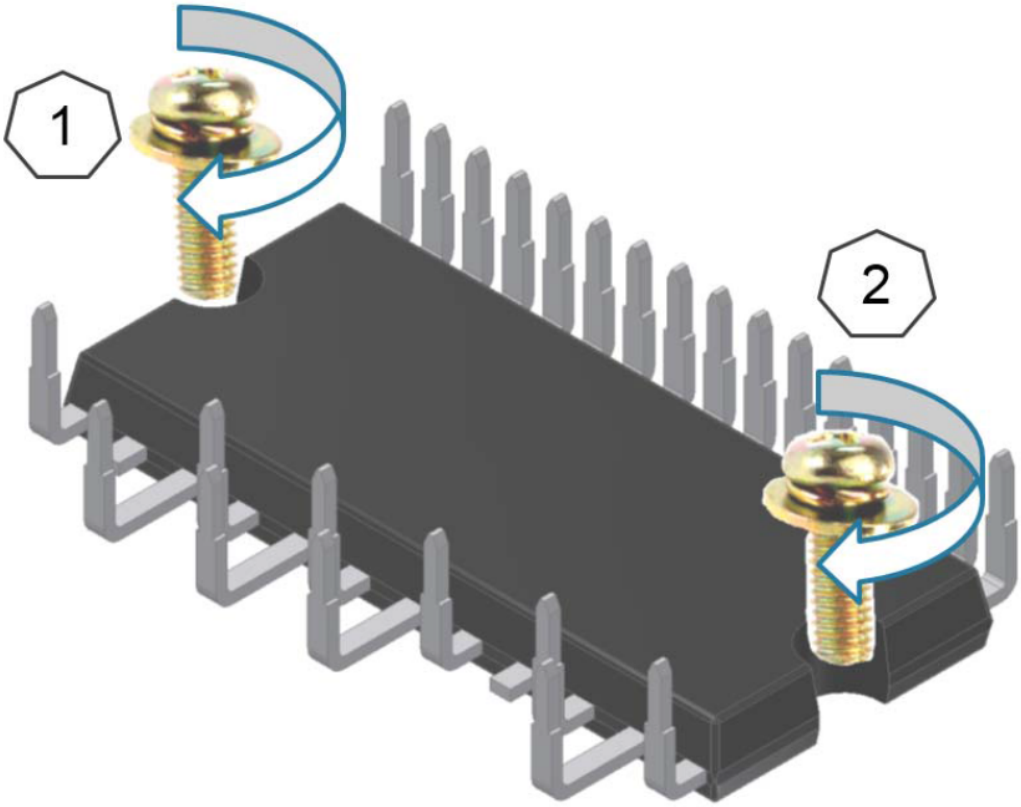
Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance.

Figure 37 shows the recommended fastening sequence for mounting screws. ST recommends temporarily tightening mounting screws with the fixing torque set at 0.1/0.2 Nm and then permanently screwing them with a torque of 0.55 Nm (0.70 Nm max.) crosswise.

1. Fasten temporarily in the sequence 1 → 2
2. Screw down permanently in the sequence 1 → 2

When using electrical or pneumatic screwdrivers, ST suggests limiting the revolution to 200 rpm as the rapid impact of the screw may damage the module's plastic body.

Figure 37. **Recommended mounting screw fastening sequence**



Many other precautions regarding handling and contamination, ESD, storage, transportation and soldering should be considered, and further details are available in technical note TN1221.

7 References

1. STGIPQ3H60T-Hyy datasheet
2. STGIPQ5C60T-Hyy datasheet
3. AN4043 – “SLLIMM-nano”
4. AN4694 – “EMC design guides for motor control applications”
5. TN1221 – “Mounting instruction for SLLIMM-nano 2nd series”
6. STGIPQ4C60T-Hyy datasheet
7. STGIPQ8C60T-Hyy datasheet

Revision history

Table 11. **Document revision history**

Date	Version	Changes
01-Jul-2016	1	Initial release.
27-Oct-2021	2	Updated line-up value from 5 to 8 A in cover page. Updated Table 1. Main differences, Section 1.1 Product synopsis, Table 2. SLLIMM-nano 2nd series line-up, Figure 20. Bootstrap capacitor vs. switching frequency, Figure 28. Thermal impedance ZthJC curve for a single IGBT, Figure 29. RC Cauer and Foster thermal networks, Table 10. Cauer and Foster RC thermal network elements for SLLIMM-nano 2nd series, Figure 30. Maximum I_C(RMS) current vs. fsw (simulated curves) and Section 7 References. Minor text changes.

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