AN4822
Application note

Migrating between STM32L476xx/486xx and STM32L496xx/4A6xx microcontrollers

Introduction

For designers of the STM32 microcontroller applications, being able to replace easily one microcontroller type by another in the same product family is an important asset. Migrating an application to a different microcontroller is often needed, when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate an existing design between the STM32L476xx/486xx and the STM32L496xx/4A6xx microcontrollers. All the most important information is grouped here. Three aspects need to be considered for the migration: the hardware, the peripheral and the firmware.

This document lists the full set of features available for the STM32L476xx/486xx and the STM32L496xx/4A6xx devices.

To fully benefit from this application note, the user should be familiar with the STM32 microcontrollers documentation available on *www.st.com* with a particular focus on:

- STM32L4x6 advanced ARM®-based 32-bit MCUs (RM0351)
- STM32L4x6 datasheets.

Table 1. Applicable products

Type	Part number
STM32L486xx	STM32L486JG, STM32L486QG, STM32L486RG, STM32L486VG, STM32L486ZG
STM32L476xx	STM32L476JE, STM32L476JG, STM32L476ME, STM32L476MG, STM32L476QE, STM32L476QG, SMT32L476RC, SMT32L476RE, SMT32L476RG, SMT32L476VC, SMT32L476VE, SMT32L476VG, SMT32L476ZE, SMT32L476ZG
STM32L4A6xx	STM32L4A6AG, STM32L4A6QG, STM32L4A6RG, STM32L4A6VG, STM32L4A6ZG
STM32L496xx	STM32L496AE, STM32L496AG, STM32L496QE, STM32L496QG, STM32L496RE, STM32L496RG, STM32L496VE, STM32L496VG, STM32L496ZE, STM32L496ZG

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1 Hardware migration guide

1.1 PCB design compatibility

The STM32L476xx/486xx devices do not share all the packages with the STM32L496xx/4A6xx microcontrollers. *Table 2* illustrates for each common package the pinout/ballout compatibility.

Table 2. Package availability and PCB design compatibility

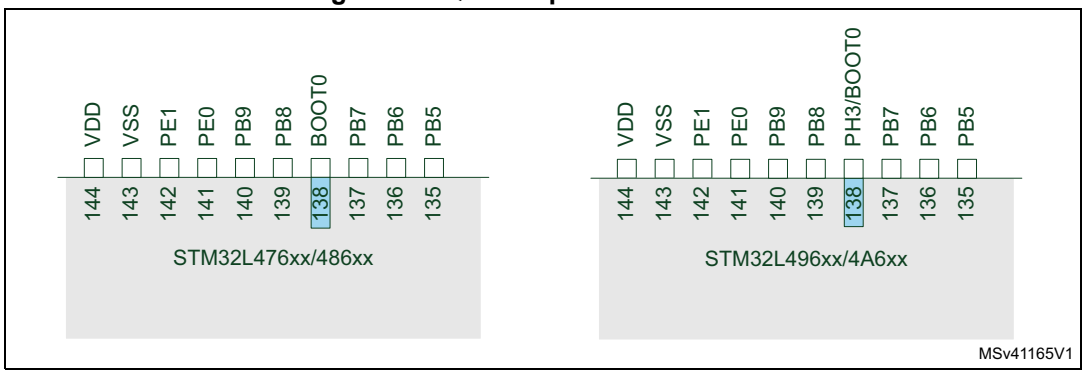
Package	STM32L496xx /4A6xx	STM32L476xx /486xx	Pinout/ballout difference	PCB design modification
LQFP144 (20 x 20)	X	X	Minor	Not mandatory(1)
LQFP100 (14 x14)	X	X	Minor	Not mandatory(1)
LQFP64 (10 x 10)	X	X	Minor	Not mandatory(1)
UFBGA169 (7 x 7)	X	-	-	-
UFBGA132 (7 x 7)	X	X	Minor	Not mandatory(1)
WLCSP81	-	X(2)	-	-
WLCSP72	-	X	-	-
WLCSP100	X	-	-	-

1. There is no change required from an application moving from the STM32L476xx/486xx to the STM32L496xx/4A6xx devices. For a migration from the STM32L496xx/4A6xx to the STM32L476xx/486xx devices, the PH3 GPIO is lost. Note that there is no alternate function attached to this IO for the STM32L496xx/4A6xx devices.
2. Only for the STM32L476xx microcontrollers.

1.1.1 LQFP144 package

Figure 1 illustrates the LQFP144 pinout differences between the STM32L476xx/486xx and the STM32L496xx/4A6xx microcontrollers.

Figure 1. LQFP144 pinout differences



1. For the highlighted (blue) terminals, the BOOT0 pin for the STM32L476xx/486xx devices is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers

On the LQFP144 package, for the terminal 138, the BOOT0 pin for the STM32L476xx/486xx is replaced by a BOOT0 pin shared with a GPIO for the

STM32L496xx/4A6xx devices. This update is done in order to offer a maximum of flexibility if managing the BOOT0 function by option bytes for these last products.

By default, the STM32L496xx/4A6xx devices are configured to use this pin as BOOT0 pin, the same configuration as the STM32L476xx/486xx microcontrollers, in order to keep direct compatibility with the STM32L476xx/486xx PCB. *Table 3* lists the LQFP144 pinout differences between STM32L476xx/486xx and STM32L496xx/4A6xx microcontrollers.

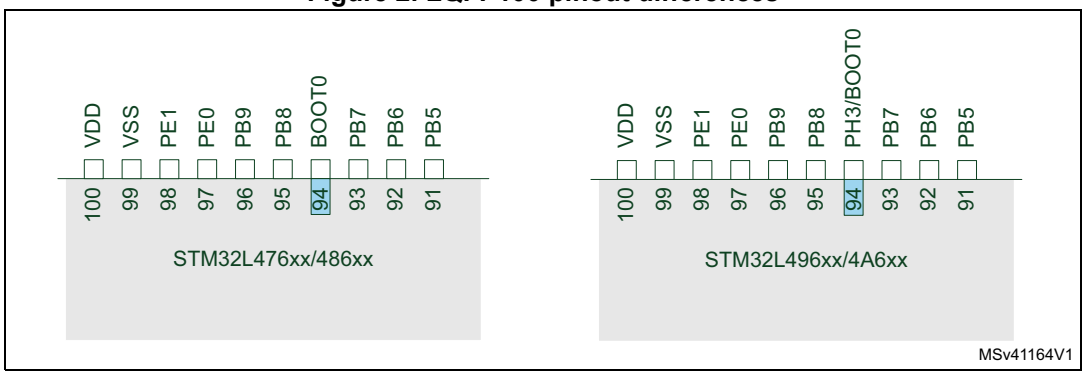
Table 3. List of LQFP144 pinout differences

Terminal	STM32L476xx/486xx	STM32L496xx/4A6xx
138	BOOT0	PH3/BOOT0

1.1.2 LQFP100 package

Figure 2 illustrates the LQFP100 pinout differences between the STM32L476xx/486xx and the STM32L496xx/4A6xx microcontrollers.

Figure 2. LQFP100 pinout differences



1. For the highlighted (blue) terminals, the BOOT0 pin for the STM32L476xx/486xx devices is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers

On the LQFP100 package, for the terminal 94 the BOOT0 pin for the STM32L476xx/486xx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers. This update is done in order to offer a maximum of flexibility if managing the BOOT0 function by option bytes for these last products.

By default, the STM32L496xx/4A6xx and STM32L496xx/4A6xx microcontrollers are configured to use this pin as BOOT0 pin, the same configuration as the STM32L476xx/486xx microcontrollers, in order to keep direct compatibility with the STM32L476xx/486xx PCB.

Table 4 lists the LQFP100 pinout differences between STM32L476xx/486xx and STM32L496xx/4A6xx microcontrollers.

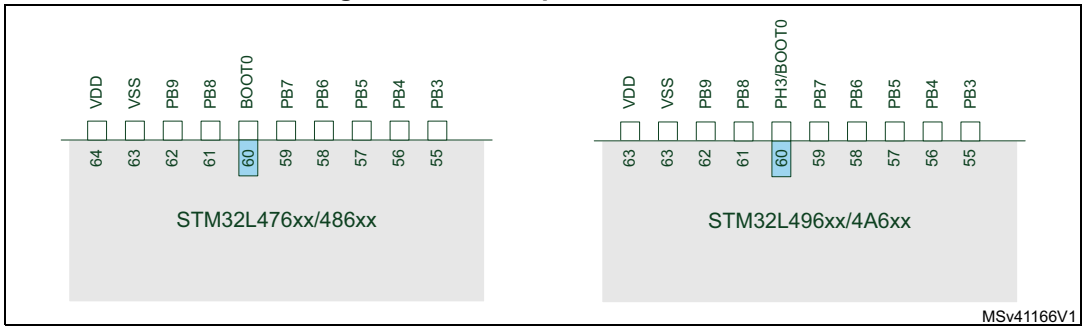
Table 4. List of LQFP100 pinout differences

Terminal	STM32L476xx/486xx	STM32L496xx/4A6xx
94	BOOT0	PH3/BOOT0

1.1.3 LQFP64 package

Figure 3 illustrates the LQFP64 pinout differences between the STM32L476xx/486xx and the STM32L496xx/4A6xx microcontrollers.

Figure 3. LQFP64 pinout differences



1. For the highlighted (blue) terminals, the BOOT0 pin for the STM32L476xx/486xx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers,

On the LQFP64 package, for the terminal 60 the BOOT0 pin for the STM32L476xx/486xx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers. This update is done in order to offer a maximum of flexibility if managing the BOOT0 function by option bytes for these last products.

By default, the STM32L496xx/4A6xx microcontrollers are configured to use this pin as BOOT0 pin, the same configuration as the STM32L476xx/486xx microcontrollers, in order to keep direct compatibility with the STM32L476xx/486xx PCB. *Table 5* lists the LQFP64 pinout differences between STM32L476xx/486xx and STM32L496xx/4A6xx microcontrollers.

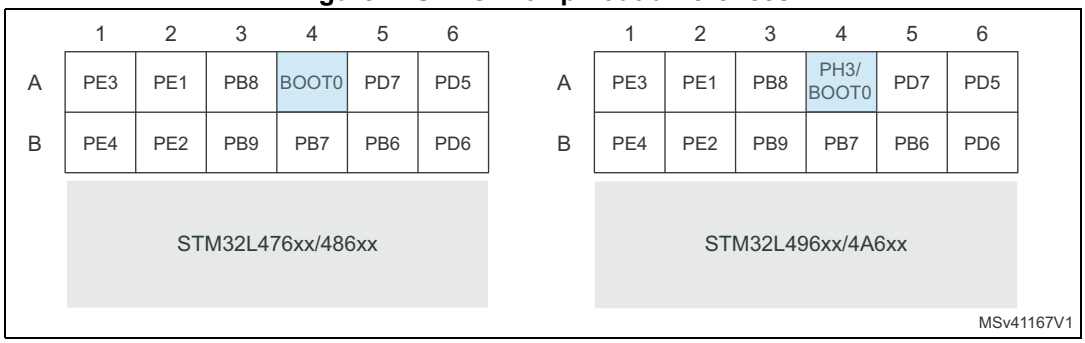
Table 5. List of LQFP64 pinout differences

Terminal	STM32L476xx/486xx	STM32L496xx/4A6xx
60	BOOT0	PH3/BOOT0

1.1.4 UFBGA132 package

Figure 4 illustrates the UFBGA132 pinout differences between the STM32L476xx/486xx and the STM32L496xx/4A6xx microcontrollers

Figure 4. UFBGA132 pinout differences



1. For the highlighted (blue) terminals, the BOOT0 pin for the STM32L476xx/486xx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers.

On the UFBGA132 package, the BOOT0 pin for the STM32L476xx/486xx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L496xx/4A6xx microcontrollers. This update is done in order to offer a maximum of flexibility if managing the BOOT0 function by option bytes for these last products.

By default, the STM32L496xx/4A6xx microcontrollers are configured to use this pin as BOOT0 pin, the same configuration as the STM32L476xx/486xx microcontrollers, in order to keep direct compatibility with the STM32L476xx/486xx PCB.

SMPS packages

Some devices of the STM32L4 Series offer a package option allowing the connection of an external SMPS.

This is done through two VDD12 pins that are replacing two existing pins in the baseline package.

Compatibility is kept between derivatives of the STM32L4 Series regarding those two VDD12 pins (the pins replaced are different across package types but are the same for all derivatives on similar packages).

Please refer to the product datasheets for more details.

2 Peripheral migration guide

2.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals which can be classified in three groups:

- Peripherals that are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- Peripherals that are shared by all products but have only minor differences (in general to support new features), so migration from one product to another is very easy and does not need any significant new development effort.
- Peripherals that have considerable changes from one product to another (new architecture or new features for example). For this group of peripherals, the migration requires a new development at application level.

Table 6 summarizes the available peripherals and their compatibility for the STM32L476xx/486xx and STM32L496xx/4A6xx microcontrollers.

Table 6. Peripheral compatibility analysis between STM32L496xx/4A6xx and STM32L476xx/486xx microcontrollers(1)

Peripherals		TM32L496xx /4A6xx	STM32L476xx /486xx	Compatibility	
				Software	Comments
Flash memory(2)	Size (byte)	1 M	1 M	-	-
	Bank	Dual	Dual		
SRAM (Kbyte)	SRAM1	256	96	-	The SRAM2 may be contiguous to the SRAM1 (physical address is still in 0x1000 0000) in STM32L496xx/4A6xx microcontrollers only
	SRAM2(3)	64	32		
FMC (external memory controller for static memory)		YES	YES	YES	FMC and QUADSPI are instantiated in two different AHB slave ports in STM32L496xx/4A6xx microcontrollers
QUADSPI(4)		YES	YES	YES	Dual-Flash mode features added + 1 additional bit DHHC to delay data output into the STM32L496xx/4A6xx microcontrollers only
Timers	Advanced control	2 (16-bit)	2 (16-bit)	YES	-
	General purpose	5 (16-bit) 2 (32-bit)	5 (16-bit) 2 (32-bit)	YES YES	
	Basic	2 (16-bit)	2 (16-bit)	YES	

Table 6. Peripheral compatibility analysis between STM32L496xx/4A6xx and STM32L476xx/486xx microcontrollers(1) (continued)

Peripherals		TM32L496xx /4A6xx	STM32L476xx /486xx	Compatibility	
				Software	Comments
Timers (continued)	Low power	2 (16-bit)	2 (16-bit)	YES	-
	Systick timer	1	1	YES	
	Independent watchdog timer	1	1	YES	
	Window watchdog timer	1	1	YES	
Communication interfaces	SPI	3	3	YES	-
	I2C	4	3	YES	
	USART UART LPUART	3 2 1	3 2 1	YES YES YES	Additional features in STM32L496xx/4A6xx(5) - -
	SAI	2	2	YES	-
	CAN	2	1	YES	
	USB	OTG FS with clock recovery	OTG FS without clock recovery	YES	Additional clock source (HSI48) in STM32L496xx/4A6xx
	SDMMC	YES	YES	YES	Additional clock source (HSI48) in STM32L496xx/4A6xx
	SWPMI	YES	YES	YES	-
RTC		YES	YES	YES	APB clock control added (see RCC) in STM32L496xx/4A6xx
Tamper pins		YES up to 3	YES up to 3	YES	-
LCD		YES	YES	YES	-
Random generator		YES	YES	YES	Additional clock source (HSI48) in STM32L496xx/4A6xx
GPIOs wake up pins I/Os down to 1.08 V		YES up to 136 YES up to 5 YES up to 14	YES up to 114 YES up to 5 YES up to 14	YES YES YES	Additional I/O PH3 multiplexed with BOOT0 in STM32L496xx/4A6xx
Capacitive sensing		YES up to 24	YES up to 24	YES	-
DFSDM		YES	YES	YES	-
12-bit ADC	Instance	3	3	MOSTLY	No need to control the analog switch from GPIOx_ASCR registers in STM32L496xx/4A6xx (done automatically)
	number of channels	24	24		
12-bit DAC		2	2	YES	-

Table 6. Peripheral compatibility analysis between STM32L496xx/4A6xx and STM32L476xx/486xx microcontrollers(1) (continued)

Peripherals	TM32L496xx /4A6xx	STM32L476xx /486xx	Compatibility	
			Software	Comments
Internal voltage reference buffer	1	1	YES	VREFBUF is disabled for package lower than 100-pin
Analog comparator	2	2	YES	-
operational amplifiers	2	2	YES	-
EXTI	YES	YES	YES	-
RCC	YES	YES	YES	New bit in STM32L496xx/4A6xx: – To stop the APB clock of the RTC keeping ON the RTC kernel clock in sleep or run modes – New HSI48 to manage the clock recovery for USB. It can be the clock source for the RNG and the SDMMC as well – HSI16 can be connected to SAI when there is no PLL ON (audio flow detection) – MCO can also output HSI48 – PLL P dividers increased possible values – More bit to calibrate HSITRIM
PWR(6)	YES	YES	YES	Pull-up/pull-down control bit for stand-by mode for PH3 in STM32L496xx/4A6xx
SYSCFG(7)	YES	YES	YES	SRAM2 write protection area increased due to larger SRAM2 size in STM32L496xx/4A6xx

1. The gray-background cells highlight the main improvements of STM32L496xx/4A6xx versus STM32L476xx/486xx devices.
2. Refer to the *Chapter 2.3: Flash memory on page 12* for more details
3. Refer to the *Section 2.5: SRAM2 memory on page 15* for more details
4. Refer to the *Section 2.6: QUADSPI peripheral on page 15* for more details
5. Refer to the *Section 2.11: USART peripheral on page 25* for more details
6. Refer to the *Section 2.9: Power controller on page 22* for more details
7. Refer to the *Section 2.10: System configuration controller (SYSCFG) on page 24* for more details

Below peripherals are only available on STM32L496xx/4A6xx devices:

- Hash processor (HASH)
- Digital camera interface (DCMI)
- Chrom-ART accelerator™ controller (DMA2D)

Most of the bugs known for the STM32L476xx/486xx microcontrollers have been corrected for the STM32L496xx/4A6xx microcontrollers. Please refer to the corresponding product errata sheets to find out the remaining bugs.

2.2 Register boundary addresses of peripherals

Table 7 compares the peripherals register boundary addresses for STM32L496xx/4A6xx versus STM32L476xx/486xx microcontrollers.

Table 7. Peripherals register boundary addresses comparison

Peripheral	Bus	STM32L496xx/4A6xx base address	STM32L476xx/486xx base address
HASH	AHB2	0x5006 0400	NA
DCMI	AHB2	0x5005 0000	NA
GPIOI	AHB2	0x4800 2000	NA
DMA2D	AHB1	0x4002 B000	NA
I2C4	APB1	0x4000 8400	NA
CAN2	APB1	0x4000 6800	NA

Note: The Quad-SPI is mapped on AHB3 on STM32L476xx/486xx microcontrollers and on AHB4 on STM32L496xx/4A6xx microcontrollers. The base address is kept the same.

2.3 Flash memory

The differences between the Flash interface on STM32L496xx/4A6xx and the Flash interface on STM32L476xx/486xx microcontrollers are indicated in *Table 8*.

Table 8. Flash memory differences between STM32L496xx/4A6xx and STM32L476xx/486xx

Flash	STM32L496xx/4A6xx	STM32L476xx/486xx
Main/program memory	0x08000000 up to 0x080FFFFF	
	Up to 1Mbytes Split in 2 banks 256 pages of 2 Kbytes per bank	
Features	Read while write (RWW) Dual bank boot	
Wait states	Up to 4 (depending on the supply voltage and the frequency)	
Flash empty check	YES	NO
Protections	Write protection: 2 areas per bank 1 PCROP area per bank	
One time programmable (OTP) memory	1 Kbyte	

Table 8. Flash memory differences between STM32L496xx/4A6xx and STM32L476xx/486xx (continued)

Flash	STM32L496xx/4A6xx	STM32L476xx/486xx
Interface	0x4002 2000 - 0x4002 23FF	
Option bytes	Bank 1: 0x1FFF 7800 - 0x1FFF 780F Bank 2: 0x1FFF F800 - 0x1FFF F80F	
	nBOOT0	NA
	nSWBOOT0	NA
	SRAM2_RST	
	SRAM2_PE	
	nBOOT1	
	DUALBANK	
	BFB2	
	WWDG_SW	
	IWDG_STDBY	
	IWDG_STOP	
	IWDG_SW	
	nRST_SHDW	
	nRST_STDBY	
	nRST_STOP	
	BOR_LEV	
	RDP	
	PCROP1_STRT	
	PCROP1_END	
	WRP1A_STRT	
	WRP1A_END	
	WRP1B_STRT	
	WRP1B_END	
	PCROP2_STRT	
	PCROP2_END	
	WRP2A_STRT	
	WRP2A_END	
	WRP2B_STRT	
	WRP2B_END	

Table 9 highlights in the gray-background cells the new bits specified for the STM32L496xx/4A6xx microcontrollers.

Table 9. User and read protection option bytes(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	nBOOT0	nSWBOOT0	SRAM2_RST	SRAM2_PE	nBOOT1	Res	DUAL BANK	BFB2	WWDG_SW	IWDG_STDBY	IWDG_STOP	IWDG_SW
-	-	-	-	r	r	r	r	r	-	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	nRST_SHDW	nRST_STDBY	nRST_STOP	Res	BOR_LEV[2:0]			RDP[7:0]							
-	r	r	r	-	r	r	r	r	r	r	r	r	r	r	r

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

2.4 Boot modes

The boot mode selection changes slightly between STM32L496xx/4A6xx and STM32L476xx/486xx microcontrollers. The aim of this improvement is to share BOOT0 input pin with a GPIO (PH3) and to add option bits to choose if BOOT0 value is coming from the IO pin or from the option bit value. *Table 10* presents the STM32L496xx/4A6xx microcontrollers boot modes and highlight in gray-background cells the new modes. *Table 11* presents the STM32L476xx/486xx microcontrollers boot modes.

Table 10. Boot modes for STM32L496xx/4A6xx(1)

Boot memory space	nBOOT1 option bit	nBOOT0 option bit	BOOT0 pin (PH3)	nSWBOOT0 option bit
Main Flash	do not care	do not care	0	1
Main Flash	do not care	1	do not care	0
Embedded SRAM1	0	do not care	1	1
Embedded SRAM1	0	0	do not care	0
System Flash	1	do not care	1	1
System Flash	1	0	do not care	0

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 11. Boot modes for STM32L476xx/486xx

Boot memory space	BOOT1	BOOT0 pin
Main Flash	do not care	0
System Flash	0	1
Embedded SRAM1	1	1

2.5 SRAM2 memory

There are very few differences between the STM32L496xx/4A6xx and the STM32L476xx/486xx microcontrollers concerning the SRAM2 memory as shown in *Table 12*.

Table 12. SRAM2 differences between STM32L496xx/4A6xx and STM32L476xx/486xx

SRAM2	STM32L496xx/4A6xx	STM32L476xx/486xx
Size	64 KB	32 KB
Address	0x1000 0000 - 0x1000 FFFF	0x1000 0000 - 0x1000 7FFF
Parity check	YES	
Write protection	YES - 1 KB granularity	
Read protection	RDP	
SRAM2 Erase	System reset or Software reset	
SRAM2 contiguous with SRAM1	YES	NO

The following STM32L476xx/486xx limitation has been fixed for the STM32L496xx/4A6xx microcontrollers: if a read occurs during an erase operation, the CPU will not be stalled and the value returned is deterministic and equal to 0x0000 0000.

2.6 QUADSPI peripheral

The main difference between the STM32L496xx/4A6xx and the STM32L476xx/486xx QUADSPI peripheral is the dual-Flash mode that is available only on the STM32L496xx/4A6xx microcontrollers (see *Table 13*). This feature allows to read two serial memories simultaneously.

The number of Quad-SPI alternate functions is higher on the STM32L496xx/4A6xx microcontrollers, since there are additional dedicated alternate functions for the second memory interface (BK2_NCS, BK2_IO0, BK2_IO1, BK2_IO2, BK2_IO3).

Table 13. QUADSPI differences between STM32L496xx/4A6xx and STM32L476xx/486xx

QUADSPI	STM32L496xx/4A6xx	STM32L476xx/486xx
Dual-Flash mode	YES	NO

Table 14 and *Table 15* highlight on the gray-background cells the bits that are different between the STM32L496xx/4A6xx and the STM32L476xx/486xx microcontrollers.

Table 14. QUADSPI_CR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRESCALER								PMM	APMS	Res	TOIE	SMIE	FTIE	TCIE	TEIE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	FTHRES				FSEL	DFM	Res	SSHIFT	TCEN	DMAEN	ABORT	EN
-	-	-	-	rw	rw	rw	rw	rw	rw	-	rw	rw	w1s	rw	w1s

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

The bit FSEL is used to select which Flash interface to use when in single-Flash mode while the bit DFM is used to set the dual-Flash mode.

Table 15. QUADSPI_CCR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DDRM	DHHC	Res	SIOO	FMODE[1:0]		DMODE		Res	DCYC[4:0]					ABSIZE	
rw	rw	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABMODE		ADSIZE		ADMODE		IMODE		INSTRUCTION[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

The bit DHHC, available only for the STM32L496xx/4A6xx microcontrollers, allows to delay the data on the data lines by 1/4 of a QUADSPI output clock cycle.

2.7 Interrupt vector

Table 16 presents the differences between the STM32L496xx/4A6xx and the STM32L476xx/486xx microcontrollers, in terms of interrupt vectors.

Table 16. Interrupt vector differences between STM32L496xx/4A6xx and STM32L476xx/486xx

Position	STM32L496xx/4A6xx	STM32L476xx/486xx
82	CRS	NA
83	I2C4_EV	
84	I2C4_ER	
85	DCMI	
86	CAN2_TX	
87	CAN2_RX0	
88	CAN2_RX1	
89	CAN2_SCE	
90	DMA2D	

2.8 Reset and clock control (RCC)

Table 17 highlights the main differences related to RCC (reset and clock controller) between the STM32L496xx/4A6xx and the STM32L476xx/486xx microcontrollers.

Table 17. RCC differences between STM32L496xx/4A6xx and STM32L476xx/486xx

RCC	STM32L496xx/4A6xx	STM32L476xx/486xx
	Clock sources	
USB OTG FS RNG/SDMMC	– MSI clock – PLL /Q – PLLSAI1 /Q – HSI48	– MSI clock – PLL /Q – PLLSAI1 /Q
USARTs	USART1: – APB2 clock – HSI16 – LSE – SYSCLK USART 2 and 3: – APB1 clock – HSI16 – LSE – SYSCLK	
	UART 4 and 5: –APB1 clock –HSI16 –LSE –SYSCLK	
LPUART1	– APB1 clock – HSI16 – LSE – SYSCLK	
I2Cs	– APB1 – HSI16 – SYSCLK	
SPIs	– APB2 Clock for SPI1 – APB1 clock for SPI2 and SPI3	
SAI1, SAI2	– PLLSAI1 clock /P divider – PLLSAI2 clock /P divider – PLL clock /P divider – HSI16 for audio flow detection	– PLLSAI1 clock /P divider – PLLSAI2 clock /P divider – PLL clock /P divider
QUADSPI	– AHB clock	
IWDG	– LSI clock	

Table 17. RCC differences between STM32L496xx/4A6xx and STM32L476xx/486xx (continued)

RCC	STM32L496xx/4A6xx	STM32L476xx/486xx
	Clock sources	
WWDG	– APB1 clock	
ADC	– SYSCLK – PLLSAI1 R divider	
SWPMI	– HSI16 clock – APB1 clock	
RTC	– HSE/32 – LSE – LSI – Register clock disabling (not the kernel one) in run or sleep modes – RTCAPBEN in RCC_APB1ENR1 register – RTCAPBSMEN in RCC_APB1SMENR1 register	– HSE/32 – LSE – LSI
LCD	– HSE/32 – LSE – LSI	
MCO	– LSI – LSE – SYSCLK – HSI16 – HSE – PLLCLK – MSI – HSI48	– LSI – LSE – SYSCLK – HSI16 – HSE – PLLCLK – MSI
PLL	3 PLLs (PLL, PLLSAI1, PLLSAI2)	
PLLP divider	PLLP 2 to 31	PLLP: 7 or 17
HSI16	HSITRIM[6:0]	HSITRIM[4:0]
HSI48	RC with clock recovery used for USB/RNG/SDMMC	NA

The modifications done at register level for the STM32L496xx/4A6xx microcontrollers are highlighted with gray-background cells in *Table 18*

Table 18. RCC register map(1)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	RCC_CR	Res.	Res.	PLLSAI2RDY	PLLSAI2ON	PLLSAI1RDY	PLLSAI1ON	PLLRDY	PLLON	Res.	Res.	Res.	Res.	CSSON	HSEBYP	HSERDY	HSEON	Res.	Res.	Res.	Res.	HSIASFS	HSIRDY	HSIKERON	HSION	MSI RANGE [3:0]				MSIRGSEL	MSIPLLEN	MSIRDY	MSION
	Reset value	-	-	0	0	0	0	0	0	-	-	-	-	0	0	0	0	-	-	-	-	0	0	0	0	0	1	1	0	0	0	1	1
0x04	RCC_ICSCR	Res	HSITRIM[6:0]							HSICAL[7:0]								MSITRIM[7:0]								MSICAL[7:0]							
	Reset value	-	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
0x08	RCC_CFGR	Res.	MCO PRE [2:0]			MCOSEL [3:0]				Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	STOPWUCK	Res.	PPRE2 [2:0]			PPRE1 [2:0]			HPRE [3:0]				SWS [1:0]		SW [1:0]	
	Reset value	-	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	RCC_PLL CFGR	PLLP DIV[4:0]					PLLR [1:0]		PLLREN	Res.	PLLQ [1:0]		PLLQEN	Res.	Res.	PLLP	PLLPEN	Res.	PLLN [6:0]							Res.	PLLM [2:0]			Res.	Res.	PLL SRC [1:0]		
	Reset value	0	0	0	0	0	0	0	0	-	0	0	0	-	-	0	0	-	0	0	1	0	0	0	0	-	0	0	0	-	-	0	0
0x10	RCC_ PLLSAI1 CFGR	PLLSAI1P DIV[4:0]					PLL SAI1R [1:0]		PLLSAI1REN	Res.	PLL SAI1 Q [1:0]		PLLSAI1QEN	Res.	Res.	PLLSAI1P	PLLSAI1PEN	Res.	PLLSAI1N [6:0]							Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value	0	0	0	0	0	0	0	0	-	0	0	0	-	-	0	0	-	0	0	1	0	0	0	0	-	-	-	-	-	-	-	-
0x14	RCC_ PLLSAI2 CFGR	PLLSAI2P DIV[4:0]					PLL SAI2R [1:0]		PLLSAI2REN	Res.	PLL SAI2 Q [1:0]		PLLSAI2QEN	Res.	Res.	PLLSAI2P	PLLSAI2PEN	Res.	PLLSAI2N [6:0]							Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value	0	0	0	0	0	0	0	0	-	0	0	0	-	-	0	0	-	0	0	1	0	0	0	0	-	-	-	-	-	-	-	-
0x18	RCC_CIER	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSI48RDYIE	LSECSSIE	Res.	PLLSAI2RDYIE	PLLSAI1RDYIE	PLLRDYIE	HSERDYIE	HSIRDYIE	MSIRDYIE	LSERDYIE	LSIRDYIE
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0	0	0	0	0	0
0x1C	RCC_CIFR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSI48RDYF	LSECSSF	CSSF	PLLSAI2RDYF	PLLSAI1RDYF	PLLRDYF	HSERDYF	HSIRDYF	MSIRDYF	LSERDYF	LSIRDYF
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0
0x20	RCC_CICR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSI48RDYC	LSECSSC	CSSC	PLLSAI2RDYC	PLLSAI1RDYC	PLLRDYC	HSERDYC	HSIRDYC	MSIRDYC	LSERDYC	LSIRDYC
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0
0x28	RCC_ AHB1RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DMA2DRST	TSCRST	Res.	Res.	Res.	Res.	CRCRST	Res.	Res.	FLASHRST	Res.	Res.	Res.	Res.	Res.	Res.	DMA2RST	DMA1RST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	-	-	-	0	-	-	0	-	-	-	-	-	-	0	0

Table 18. RCC register map[1] (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x2C	RCC_ AHB2RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RNGRST	HASH1RST	AESRST	Res.	DCMIRST	ADCRST	OTGFSRST	Res.	Res.	Res.	GPIOIRST	GPIOHRST	GPIOGRST	GPIOFRST	GPIOERST	GPIODRST	GPIOCRST	GPIOBRST	GPIOARST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	0	0	0	-	-	-	0	0	0	0	0	0	0	0	0
0x30	RCC_ AHB3RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	QSPIRST	Res.	Res.	Res.	Res.	Res.	Res.	FMCRST	
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	-	0	
0x38	RCC_ APB1RSTR1	LPTIM1RST	OPAMPRST	DAC1RST	PWRRST	Res.	USBFSRST	CAN1RST	CRSRST	I2C3RST	I2C2RST	I2C1RST	UART5RST	UART4RST	USART3RST	USART2RST	Res.	SPI3RST	SPI2RST	Res.	Res.	Res	Res.	LCDRST	Res.	Res.	Res.	Res.	TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
	Reset value	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	-	0	0	-	-	-	-	-	-	-	-	0	0	0	0	0	0
0x3C	RCC_ APB1RSTR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LPTIM2RST	Res.	Res.	SWPMI1RST	I2C4RST	LPUART1RST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	0	0	0
0x40	RCC_ APB2RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DFSDMRST	Res.	SAI2RST	SAI1RST	Res.	Res.	TIM17RST	TIM16RST	TIM15RST	Res.	USART1RST	TIM8RST	SPI1RST	TIM1RST	SDMMCRST	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SYSCFGRST
	Reset value	-	-	-	-	-	-	-	0	-	0	0	-	-	0	0	0	-	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	0
0x48	RCC_AHB1 ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DMA2DEN.	TSCEN	Res.	Res.	Res.	Res.	CRCEN	Res.	Res.	FLASHEN	Res.	Res.	Res.	Res.	Res.	Res.	DMA2EN	DMA1EN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	-	-	-	0	-	-	1	-	-	-	-	-	-	0	0
0x4C	RCC_AHB2 ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RNGEN	HASH1EN.	AESEN	Res.	DCMIEN	ADCEN	OTGFSEN	Res.	Res.	Res.	GPIOIEN	GPIOHEN	GPIOGEN	GPIOFEN	GPIOEEN	GPIODEN	GPIOCEN	GPIOBEN	GPIOAEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	-	0	0	0	-	-	-	0	0	0	0	0	0	0	0	0
0x50	RCC_AHB3 ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	QSPIEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	FMCEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	-	-	0
0x58	RCC_ APB1ENR1	LPTIM1EN	OPAMPEN	DAC1EN	PWREN	Res.	USBFSEN	CAN1EN	CRSEN	I2C3EN	I2C2EN	I2C1EN	UART5EN	UART4EN	USART3EN	USART2EN	Res.	SP3EN	SPI2EN	Res.	Res.	WWDGEN	RTCAPBEN	LCDEN	Res.	GPIOIEN	GPIOHEN	GPIOGEN	GPIOFEN	GPIOEEN	GPIODEN	GPIOCEN	GPIOBEN	GPIOAEN
	Reset value	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	-	0	0	-	-	0	1	0	-	0	0	0	0	0	0	0	0
0x5C	RCC_ APB1ENR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LPTIM2EN	Res.	Res.	SWPMI1EN	I2C4EN	LPUART1EN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	0	0	0

Table 18. RCC register map[1] (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x60	RCC_ APB2ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DFSDMEN	Res.	SAI2EN	SAI1EN	Res.	Res.	TIM17EN	TIM16EN	TIM15EN	Res.	USART1EN	TIM8EN	SPI1EN	TIM1EN	SDMMC1EN	Res.	Res.	FIREWALLEN	Res.	Res.	Res.	Res.	Res.	Res.	SYSCFGEN
	Reset value	-	-	-	-	-	-	-	0	-	0	0	-	-	0	0	0	-	0	0	0	0	0	-	-	0	-	-	-	-	-	-	0
0x68	RCC_ AHB1SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DMA2DSMEN.	TSCSMEN	Res.	Res.	Res.	CRCSMEN	Res.	Res.	SRAM1SMEN	FLASHSMEN	Res.	Res.	Res.	Res.	Res.	Res.	DMA2SMEN	DMA1SMEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	-	-	-	1	-	-	1	1	-	-	-	-	-	-	1	1
0x6C	RCC_ AHB2SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RNGSMEN	HASH1SMEN	AESSMEN	Res.	DCMISMEN.	ADCFSSMEN	OTGFSSMEN	Res.	Res.	SRAM2SMEN	GPIOISMEN	GPIOHSMEN	GPIOGSMEN	GPIOFSMEN	GPIOESMEN	GPIODSMEN	GPIOCSMEN	GPIOBSMEN	GPIOASMEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	1	1	1	-	1	1	1	-	-	1	1	1	1	1	1	1	1	1	1
0x70	RCC_ AHB3SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	QSPISMEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	FMCSEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	1
0x78	RCC_ APB1SM ENR1	LPTIM1SMEN	OPAMPSMEN	DAC1SMEN	PWRSMEN	Res.	.USBFSSMEN	CAN1SMEN	CRSSMEN	I2C3SMEN	I2C2SMEN	I2C1SMEN	UART5SMEN	UART4SMEN	USART3SMEN	USART2SMEN	Res.	SP3SMEN	SPI2SMEN	Res.	Res.	Res.	WWDGSMEN	RTCAPBENSMEN	LCDSMEN	Res.	Res.	Res.	Res.	TIM7SMEN	TIM6SMEN	TIM5SMEN	TIM4SMEN	TIM3SMEN	TIM2SMEN
	Reset value	1	1	1	1	-	1	1	1	1	1	1	1	1	1	1	-	1	1	-	-	1	1	1	-	-	-	1	1	1	1	1	1
0x7C	RCC_ APB1SM ENR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LPTIM2SMEN	Res.	Res.	SWPMI1SMEN	IC24SMEN.	LPUART1SMEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	1	1	1
0x80	RCC_ APB2SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DFSDMSMEN	Res.	SAI2SMEN	SAI1SMEN	Res.	Res.	TIM17SMEN	TIM16SMEN	TIM15SMEN	Res.	USART1SMEN	TIM8SMEN	SPI1SMEN	TIM1SMEN	SDMMCSMEN	Res.	Res.	Res.	Res.	Res.	LPTIM2SMEN	Res.	Res.	Res.	Res.	SYSCFGSMEN
	Reset value	-	-	-	-	-	-	-	1	-	1	1	-	-	1	1	1	-	1	1	1	1	1	-	-	-	-	-	1	-	-	-	-	1
0x88	RCC_CCIPR	DFSDMSEL	SWPMI1SEL	ADCSEL		CLK48SEL		SAI2SEL		SAI1SEL		LPTIM2SEL		LPTIM1SEL		I2C3SEL		I2C2SEL		I2C1SEL		LPUART1SEL		USART5SEL		USART4SEL		USART3SEL		USART2SEL		USART1SEL	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x90	RCC_BDCR	Res.	Res.	Res.	Res.	Res.	Res.	LSCOSEL	LSCOEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	BDRST	RTCEN	Res.	Res.	Res.	Res.	Res.	RTC SEL [1:0]		LSECSSD		LSECSSON	LSE DRV [1:0]		LSEBYP	LSERDY	LSEON
	Reset value	-	-	-	-	-	-	0	0	-	-	-	-	-	-	-	0	0	-	-	-	-	-	0	0	-	0	0	0	0	0	0	0

Table 18. RCC register map[1] (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x94	RCC_CSR	LPWRSTF	WWDGRSTF	IWDGRSTF	SFTRSTF	BORRSTF	PINRSTF	OBLRSTF	FIREWALLRSTF	RMVF	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	MSIS RANGE[3:0]				Res.	Res.	Res.	Res.	Res.	Res.	LSIRDY	LSION
	Reset value	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	0	1	1	0	-	-	-	-	-	-	0	0
0x98	RCC_CRRCR	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	HSI48CAL[8:0]									Res	Res	Res	Res	Res	HSI48RDY	HSI48ON
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X	X	X	X	X	-	-	-	-	-	0	0
0x9C	RCC_CCIPR 2	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	I2C4SEL	
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers

Note: CLK48SEL = 0x00 into the RCC_CCIPR register selects now HSI48 as 48 MHz clock source for USB, RNG or SDMMC in the STM32L496xx/4A6xx microcontrollers.

2.9 Power controller

Table 19 shows the PVM differences between the STM32L496xx/4A6xx and the STM32L476xx/486xx microcontrollers

Table 19. PVM differences between STM32L496xx/4A6xx and STM32L476xx/486xx

PVM	STM32L496xx/4A6xx	STM32L476xx/486xx
PVM1	Power: VDDUSB VPVM1 (Around 1.2V) EXTI line 35	
PVM2	Power: VDDIO2 VPVM2 (Around 0.9V) EXTI line 36	
PVM3	Power: VDDA VPVM3 (Around 1.65V) EXTI line 37	
PVM4	Power: VDDA VPVM4 (Around 2.2V) EXTI line 38	

The gray-background cells in *Table 20* to *Table 23* highlight the bits available in STM32L496xx/4A6xx microcontrollers.

Table 20. PWR_PUCRH register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PU31	PU31	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PU15	PU14	PU13	PU12	PU11	PU10	PU9	PU8	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 21. PWR_PUCRI register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PU31	PU31	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PU15	PU14	PU13	PU12	PU11	PU10	PU9	PU8	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 22. PWR_PDCRH register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD31	PD31	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 23. PWR_PDCRI register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PD31	PD31	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
-	rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

2.10 System configuration controller (SYSCFG)

The gray-background cells in *Table 24* to *Table 28* highlight the bit available in STM32L496xx/4A6xx microcontrollers.

Table 24. SYSCFG_CFGR1 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FPU_IE[5.0]						Res	Res	I2C4_FMP	I2C3_FMP	I2C2_FMP	I2C1_FMP	I2C_PB9_FMP	I2C_PB8_FMP	I2C_PB7_FMP	I2C_PB6_FMP
rw	rw	rw	rw	rw	rw	-	-	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	BOOSTEN	Res	Res	Res	Res	Res	Res	Res	FWDIS
-	-	-	-	-	-	-	rw	-	-	-	-	-	-	-	-

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 25. SYSCFG_EXTICR1 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI3[3:0]				EXTI2[3:0]				EXTI1[3:0]				EXTI0[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 26. SYSCFG_EXTICR2 register (1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI7[3:0]				EXTI6[3:0]				EXTI5[3:0]				EXTI4[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 27. SYSCFG_EXTICR3 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI11[3:0]				EXTI10[3:0]				EXTI9[3:0]				EXTI8[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 28. SYSCFG_EXTICR4 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI15[3:0]				EXTI14[3:0]				EXTI13[3:0]				EXTI12[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

2.11 USART peripheral

The difference between the STM32L496xx/4A6xx and the STM32L476xx/486xx microcontrollers is mainly due to the USART additional feature supporting the ISO7816-3 smartcard protocol.

Table 29, *Table 30* and *Table 31* highlight with gray-background cells the new bits present in the STM32L496xx/4A6xx registers compared to the STM32L476xx/486xx.

Table 29. USARTx_CR3 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	TCBGTIE	Res	WUFIE	WUS		SCARCNT[2:0]			Res
-	-	-	-	-	-	-	rw	-	rw	rw	rw	rw	rw	rw	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEP	DEM	DDRE	OVRDIS	ONEBIT	CTSIE	CTSE	RTSE	DMAT	DMAR	SCEN	NACK	HDSEL	IRLP	IREN	EIE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 30. USARTx_ISR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	TCBGT	Res	Res	REACK	TEACK	WUF	RWU	SBKF	CMF	BUSY
-	-	-	-	-	-	r	-	-	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABRF	ABRE	Res	EOBF	RTOF	CTS	CTSIF	LBDF	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
r	r	-	r	r	r	r	r	r	r	r	r	r	r	r	r

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 31. USARTx_ICR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	WUCF	Res	Res	CMCF	Res
-	-	-	-	-	-	-	-	-	-	-	w	-	-	w	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	EOBCF	RTOCF	Res	CTSCF	LBDCF	TCBGTCF	TCCF	Res	IDLECF	ORECF	NCF	FECF	PECF
-	-	-	w	w	-	w	w	w	w	-	w	w	w	w	w

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

2.12 Interconnect matrix

The STM32L496xx/4A6xx microcontrollers interconnect matrix is an enlarged set of the STM32L476xx/486xx interconnect matrix since the number of peripherals is increased.

In particular the STM32L496xx/4A6xx microcontrollers interconnect matrix includes one additional master for DMA2D and the QUADSPI/FMC slave is split into two separate slave ports. Please refer to the *Table 6 on page 9* to figure out the differences between the products.

2.13 DMA

There are two DMA master interfaces for the STM32L496xx/4A6xx microcontrollers as well as for the STM32L476xx/486xx microcontrollers. The DMA channels connections corresponding to peripherals that are present only for STM32L496xx/4A6xx microcontrollers, are left free for STM32L476xx/486xx microcontrollers.

2.14 Debug

For the debug module, the gray-background cells in *Table 32* highlight the bits that are available only in the STM32L496xx/4A6xx microcontrollers.

Table 32. DBGMCU_APB1FZR1 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPTIM1_STOP	Res	Res	Res	Res	DBG_CAN2_STOP	DBG_CAN_STOP	Res	DBG_I2C3_STOP	DBG_I2C2_STOP	DBG_I2C1_STOP	Res	Res	Res	Res	Res
rw	-	-	-	-	rw	rw	-	rw	rw	rw	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	DBG_IWDG_STOP	DBG_WWDG_STOP	DBG_RTC_STOP	Res	Res	Res	Res	DBG_TIM7_STOP	DBG_TIM6_STOP	DBG_TIM5_STOP	DBG_TIM4_STOP	DBG_TIM3_STOP	DBG_TIM2_STOP
-	-	-	rw	rw	rw	-	-	-	-	rw	rw	rw	rw	rw	rw

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

Table 33. DBGMCU_APB1FZR2 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	DBGLPTIM2_STOP	Res	Res	Res	DBG_I2C4_STOP	Res
-	-	-	-	-	-	-	-	-	-	rw	-	-	-	rw	-

1. The gray-background cells highlight information that is available only for STM32L496xx/4A6xx microcontrollers.

2.15 GPIO registers

In STM32L496xx/4A6xx devices, there is not need to control the ADC output analog switch from the GPIOx_ASCR registers.

As a result, those registers are not present on STM32L496xx/4A6xx devices.

3 Revision history

Table 34. Document revision history

Date	Revision	Changes
20-Feb-2017	1	Initial release.
29-Mar-2017	2	Updated: – Columns header in *Table 6* – USARTs part of *Table 17* – 0x14 and 0x68 data in *Table 18* – PU14 in *Table 21* – PD13 and PD15 in *Table 23*. Removed DBG_I2C4_STOP in *Table 32*. Added *Table 33: DBGMCU_APB1FZR2 register*.
20-Apr-2017	3	Updated: – *Table 1: Applicable products* – *Table 6: Peripheral compatibility analysis between STM32L496xx/4A6xx and STM32L476xx/486xx microcontrollers* (comment on 12-bit ADC). Added *Section 2.15: GPIO registers*.