PCB design guidelines for the BlueNRG-1 and BlueNRG-2 devices

Introduction

The devices, member of the BlueNRG family, are very low power Bluetooth® low energy (BLE) devices compliant with Bluetooth specifications.

Bluetooth low energy technology operates in the same spectrum range (2400 - 2483.5 MHz, ISM band) as classical Bluetooth technology, but uses a different set of channels. Bluetooth low energy technology has 40 channels (37 data channels + 3 advertising channels) of 2 MHz band. Within the channel, data is transmitted using GFSK (Gaussian frequency shift modulation). The bit rate is 1 Mbit/s, and the maximum transmit power is 10 mW (10 dBm).

Further details are given in volume 6 part A of the Bluetooth Core Specification V4.0.

The BlueNRG family is composed as follows:
- BlueNRG = single-mode network processor, Bluetooth v4.0 compliant
- BlueNRG-MS = single-mode network processor, Bluetooth v4.1 compliant
- BlueNRG-1 = single-mode system-on-chip (application processor), Bluetooth v5.0 compliant
- BlueNRG-2 = single-mode system-on-chip (application processor), Bluetooth v5.0 compliant

The BlueNRG-1 and BlueNRG-2 devices are provided in QFN32 and WLCSP34 pins packages.

ST provides all necessary source files (reference designs) for customers that want to speed-up their developing.

This application note is intended to accompany the reference designs of the QFN32 and WLCSP34 pin application board and provide detailed information regarding the design decisions employed within STMicroelectronics designs. In addition, it details the design guidelines for developing a generic radio frequency application using a BlueNRG-1 or BlueNRG-2 device.

The RF performance and the critical maximum peak voltage, spurious and harmonic emission, receiver matching strongly depend on the PCB layout as well as the selection of the matching network components.

For optimal performance, STMicroelectronics recommends the use of the PCB layout design hints described in the following sections. Also, but not less important, STMicroelectronics strongly suggest to use the BOM defined in the reference design, BOM that guarantee, with a good PCB design, the correct RF performance.

For further information, visit the STMicroelectronics web site at www.st.com.

AN4819 - Rev 2 - November 2018
For further information contact your local STMicroelectronics sales office.

www.st.com

1   Reference schematics

Different application boards were developed to show the BlueNRG-1 and BlueNRG-2 devices functionality. The schematics of the different application boards are reported in the next pictures and refer to the different possible combinations:

1.   QFN32 SMD discrete balun, DC-DC converter ON (see
2.   QFN32 SMD discrete balun, DC-DC converter OFF
3.   QFN32 Integrated balun, DC-DC converter ON
4.   CSP SMD discrete balun, DC-DC converter ON
5.   CSP IPD integrated balun, DC-DC converter ON

All the layout guidelines described in the next paragraphs have to be applied to all these application boards.

Figure 1. **SMD discrete balun, DC-DC converter ON**

Figure 2. SMD discrete balun, DC-DC converter OFF

Figure 3. Integrated balun, DC-DC converter ON
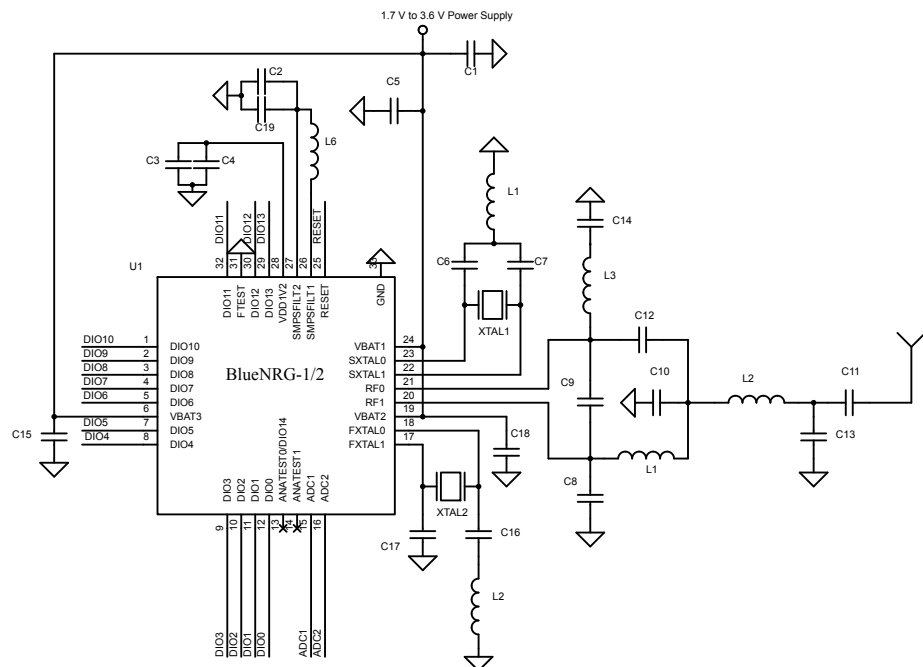
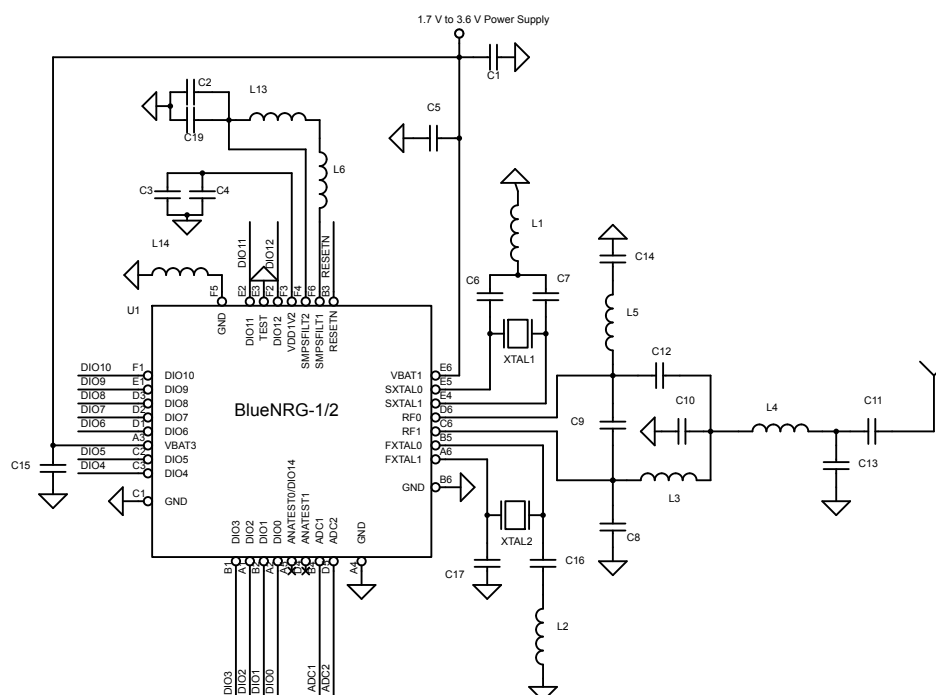**Figure 4. CSP34 SMD discrete balun, DC-DC converter ON**

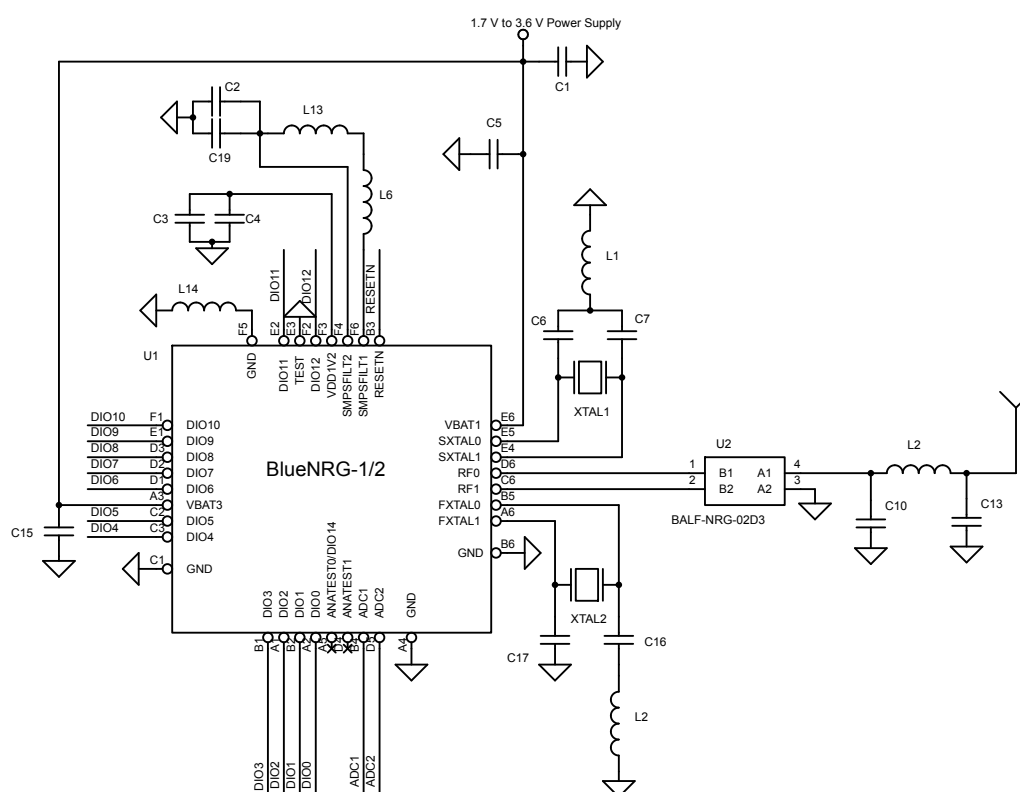
Figure 5. CSP34 IPD integrated balun, DC-DC converter ON

Table 1. BlueNRG-1 application board external components description

Components	Description
C1, C5, C15	Decoupling capacitors for battery voltage
C2, C19	DC-DC converter filtering capacitors
C3, C4	Decoupling capacitor for on-chip 1.2 V voltage regulator
C8, C9, C10, C11, C12, C13, C14	RF discrete balun filter/matching capacitors
C6, C7	XTAL1 capacitors
C16, C17	XTAL2 capacitors
L6, L13	DC-DC converter inductor
L3, L4, L5	RF discrete balun filter/matching inductors
L1	XTAL1 filtering inductor
L2	XTAL2 filtering inductor
L14	Filtering inductor
XTAL1	Low frequency crystal
XTAL2	High frequency crystal
U1	BlueNRG-1/2 devices
U2	Integrated balun

2 Components dimensioning

The chosen of the external components is very important for correct application functionality. In the next paragraph the description of the main components, their functionality and how to choose them is described.
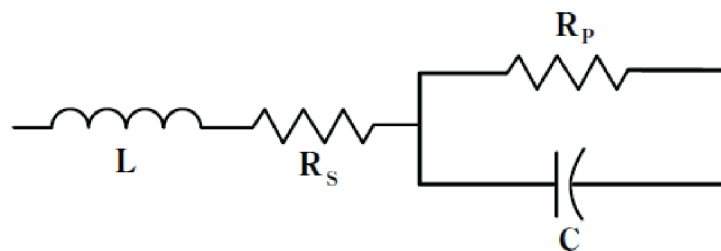
2.1 Capacitors

A capacitor is a passive electrical component used to store energy in an electrical field. The forms of practical capacitors vary widely, but all contain at least two electrical conductors separated by a dielectric.

Capacitors differ from each other for construction techniques and materials used to manufacture. A lot of different types of capacitors exist (double-layer, polyester, polypropylene and so on), but this document will focus on the surface mount versions of ceramics only. The other types of capacitors are not indicated for characteristic or cost for the application targeted in this document.

A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is shown in Figure 6. Capacitor equivalent circuit.

Figure 6. Capacitor equivalent circuit

Typically for the capacitors are defined the ESR (equivalent series resistance) and the ESL (equivalent series inductance). The term ESR combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection. Same considerations for the ESL that is the equivalent series inductor comprised of three components: pad layout, capacitor height and power plane spreading inductance.

The main differences between ceramic dielectric types are the temperature coefficient of capacitance and the dielectric loss. COG and NP0 (negative-positive-zero, i.e ±0) dielectrics have the lowest losses and are used in filtering, matching and so on.

For RF parts it is generally recommended that multilayer (or monolithic) ceramic capacitors with a COG dielectric material, which is a highly stable class I dielectric offering a linear temperature coefficient, low loss and stable electrical properties over time, voltage and frequency.

For RF decoupling purposes select a capacitor value such that for the frequency to be decoupled is close to or just above the series resonant frequency (SRF) of the capacitor. At SRF the parasitic impedance resonates with the device capacitance to form a series tuned circuit and the impedance presented by the capacitor is the effective series resistance (ESR).

For DC blocking or coupling applications at RF, typically a capacitor with low insertion loss and a good quality factor is required. Since a capacitor's quality factor is inversely proportional to its ESR, select a capacitor with a

low ESR and ensure that the SRF of the capacitor is greater than the frequency of operation. If the working frequency is above the SRF of the capacitor, it will appear inductive.

All the capacitors of the BlueNRG-1 and BlueNRG-2 application boards used for the matching network and for the crystals have to be COG.

2.2 Inductors

An inductor is a passive electrical component used to store energy in its magnetic field. Any conductor has inductance. An inductor is typically made of a wire or other conductor wound into a coil, to increase the magnetic field.

Inductors differ from each other for construction techniques and materials used to manufacture. A lot of different types of inductors exist (air core inductor, ferromagnetic core inductor and variable inductor), but this document will focus on the inductors useful for RF only. Usually in RF the air core inductors are used. The term air core describes an inductor that does not use a magnetic core made of ferromagnetic material, but coil wound on plastic, ceramic, or other nonmagnetic form. They are lower inductance than ferromagnetic core coils, but are used at high frequencies because they are free from energy losses called core losses.

Usually the real circuit of an inductor is composed of a series resistance and a parallel capacitor. The parallel capacitor is considered to be the inter-winding capacitance that exists the turns of the inductor. If the inductor is placed over a ground plane then this capacitance will also include the capacitance that exists between the inductor and the ground plane. The series resistor can be considered as the resistance of the inductor winding.

In term of circuit performance, as already mentioned for the capacitors, the self-resonant frequency and the quality factor are the main inductor parameters, especially for the circuit where the losses need to be minimized. At the self-resonant frequency, the inductor impedance is at maximum. For frequency above the self-resonance the inductor behavior change and it will appear capacitive.

In general wirewound inductors have a higher quality factor than a multilayer equivalent. They will also reflect and radiate more energy which can give rise to higher emission levels, especially in term of self-coupling. Inductive coupling can give rise to undesired circuit operation: to minimize coupling mount the inductors in sensitive circuit areas at 90 degrees to one another.

In the BlueNRG-1 or BlueNRG-2 application boards two different inductor types are used:

1. DC-DC converter coil: the nominal value is 10 uH, a 4.7 uH can be used. The DCR has to be less than 1 ohm, the rated current has to be higher than 100 mA.
2. DC-DC noise filtering inductor, 15 nH usually.
3. DC-DC ground noise filtering, 4.7 nH usually.
4. RF matching and filtering coil: in this case the best solutions are the high Q coils, but a good compromise between application costs versus RF performances is to choose an inductor with a medium Q.

The 15 nH and 4.7 nH inductors are necessary when the supply voltage is higher or equal to 3 V. Regarding to supply voltage lower than 3 V the 15 nH and 4.7 nH inductors can be not used.

2.3 External quartz

The BlueNRG-1/2 include a high frequency and a low frequency integrated oscillators that required two external crystals.

The BlueNRG-1/2 include a fully integrated, low power 16/32 MHz Xtal oscillator with an embedded amplitude regulation loop. In order to achieve low power operation and good frequency stability of the Xtal oscillator, certain considerations with respect to the quartz load capacitance C0 need to be taken into account. Figure 7. Diagram of the BlueNRG1,2 amplitude regulated oscillator shows a simplified block diagram of the amplitude regulated oscillator used on the BlueNRG family.
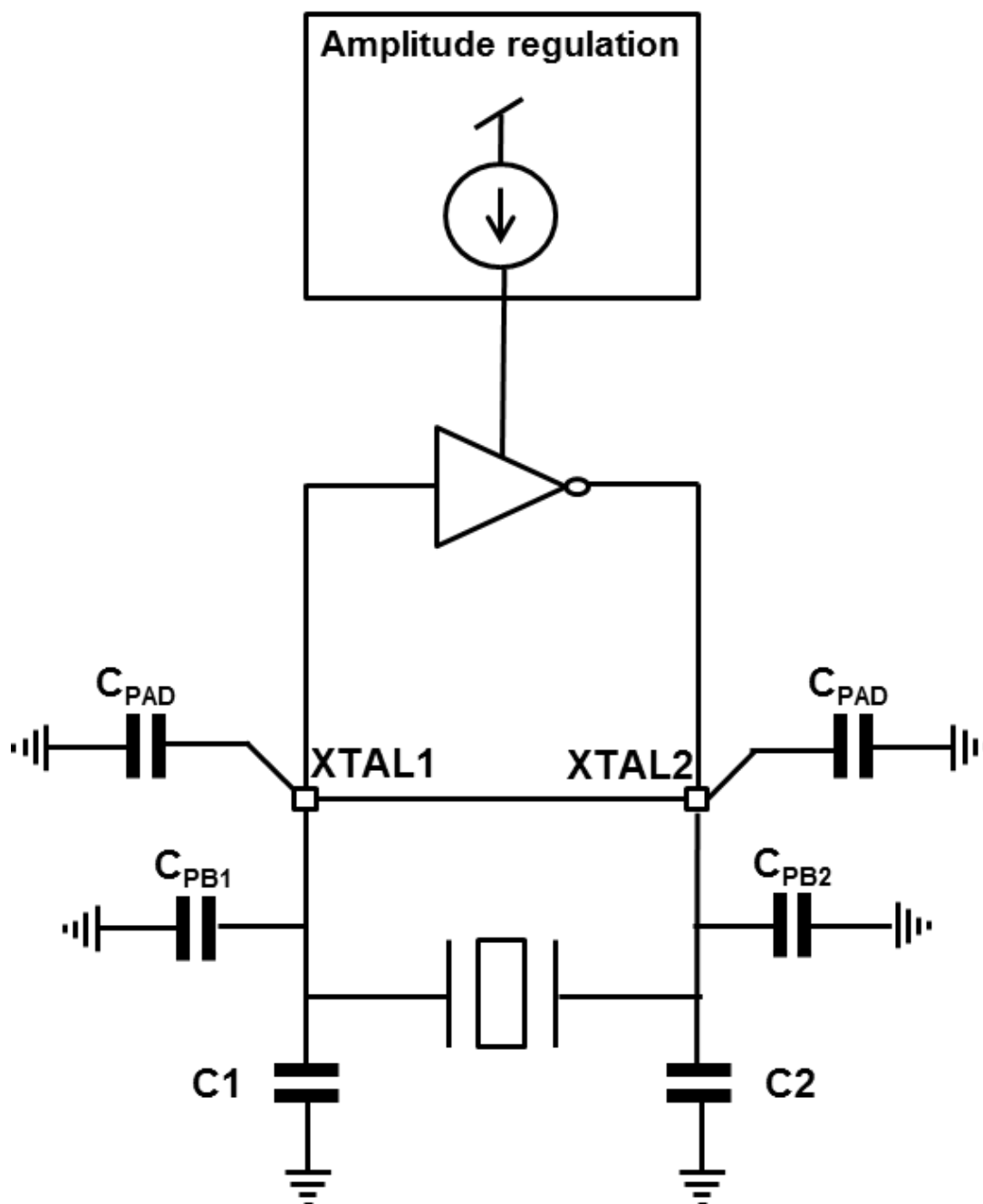
Low power consumption and fast startup time is achieved by choosing a quartz crystal with a low load capacitance C0. A reasonable choice for capacitor C0 is 15 pF. To achieve good frequency stability, the following equation needs to be satisfied:

$$C_0 = \frac{C_1' * C_2'}{C_1' + C_2'}$$

Where $C_1' = C_1 + C_{PCB1} + C_{PAD}$, $C_2' = C_2 + C_{PCB2} + C_{PAD}$, where C_1 and C_2 are external (SMD) components, C_{PCB1} and C_{PCB2} are PCB routing parasites and C_{PAD} is the equivalent small-signal pad-capacitance. The value of C_{PAD} is around 0.5 pF for each pad. The routing parasites should be minimized by placing quartz and C_1/C_2 capacitors

close to the chip, not only for an easier matching of the load capacitance C_0, but also to ensure robustness against noise injection. Connect each capacitor of the Xtal oscillator to ground by a separate via.

Regarding the low frequency crystal oscillator the same consideration has to be done.

It is important to underline that the BlueNRG-1/2 integrate an internal low frequency RC oscillator that can be used without external quartz. The customer can choose to use the internal or the external one. The BlueNRG1/2 also integrate an internal high frequency RC oscillator, but it is disabling after an initial system bootstrap and it is necessary to use external quartz for radio operations.

3 Two or four layers application board

Different approach can be taken when an application board is designed:

1. Two-layer solution
2. More-layer solution

3.1 Two-layer solution

When it is possible to route all the tracks on two layers and a cheaper solution is requested, a two layers application board can be designed.

Figure 9. Two-layer application board stack-up
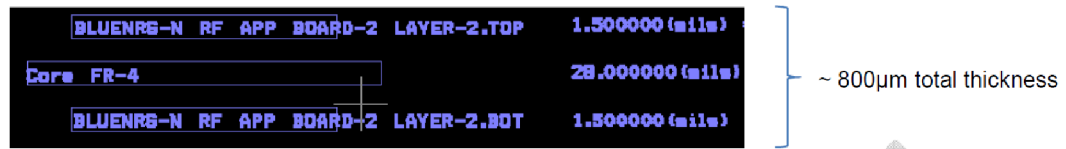
The suggested thickness of the board is about 800 µm.

The two layers have to be so distributed:

1. TOP layer: used for RF signal and routing.
2. BOTTOM layer: used for grounding under the RF zones and for routing in the other part.

The two-layer solution is indicated for the QFN package. It is possible to design a two-layer board for the WLCSP package, but two limitations are present:

1. Only a limited number of GPIOs can be used
2. A reduction of the RF performance happens

3.2 More-layer solution

When it is not possible to route all the tracks on two layers and/or a cheaper solution is not requested, a more-layer application board can be designed. This is the case, for example, for the WLCSP package where a six-layer solution is suggested, see Figure 10. Six-layer application board stack-up.

Figure 10. Six-layer application board stack-up
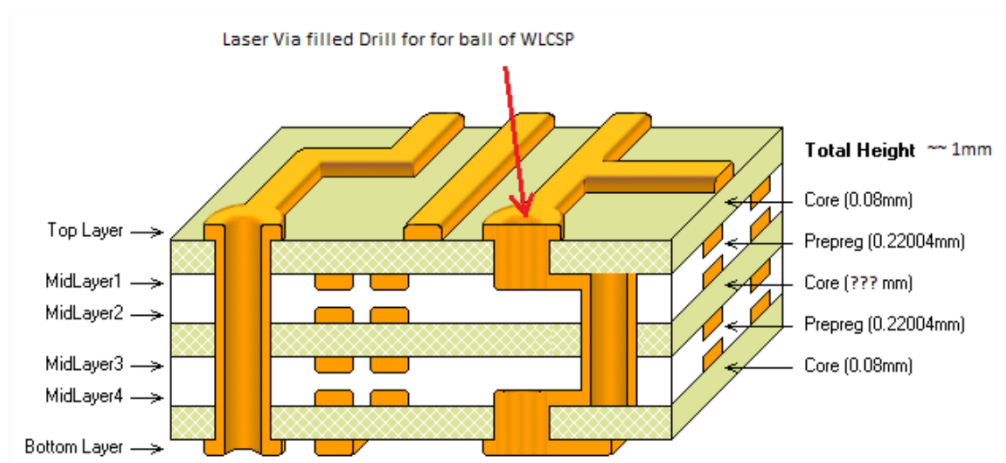
In the six-layer solution the following stack-up is used:

Table 2. **Stack-up for a six-layer board**

Layer	Stack-up	Material	Thickness [um]
		Soldermask	18
L1	TOP	Cu + Plating	36
		Prepreg	64
L2	MID1	Cu + Plating	36
		Prepreg	216
L3	MID2	Cu	30
		Core	203
L4	MID3	Cu	30
		Prepreg	216
L5	MID4	Cu + Plating	36
		Prepreg	64
L6	BOTTOM	Cu + Plating	36
		Soldermask	18
		Total thickness	1001

4 QFN package layout recommendation

The application board TOP layer layout using the BLueNRG-1/2 is shown in Figure 11. BlueNRG-1/2 application board TOP layer.

Figure 11. BlueNRG-1/2 application board TOP layer
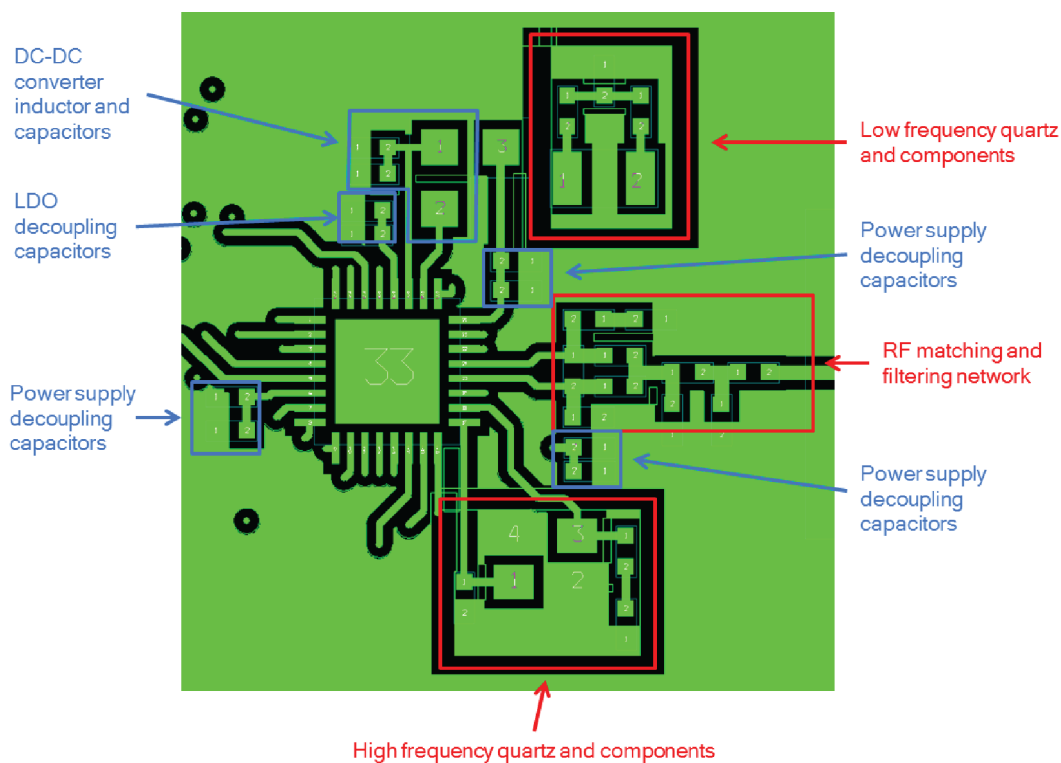
It is very important to connect very well the ground of the exposed pad of the QFN32 to the ground of the application board. So a lot of vias are necessary to be sure that the parasitic inductor introduced from each via is negligible.

Figure 12. Vias on the exposed pad of the QFN32 package
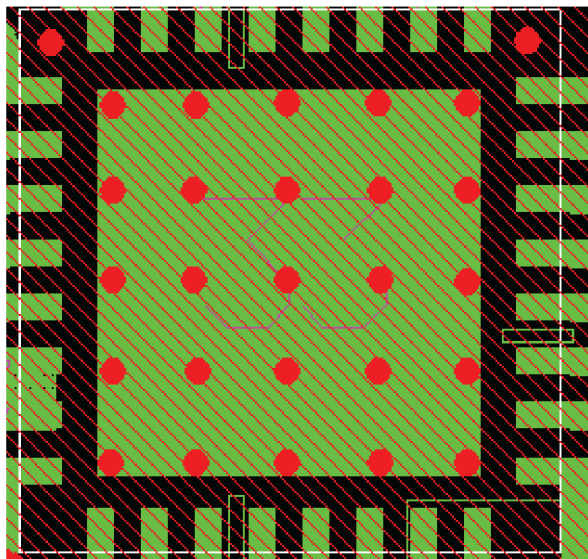
The ground of the two external crystals has to be isolated from the ground of the RF part of the board. This is because the RF ground is "dirty" and this signal can disturbs the correctly functionality of the two crystals.

Also to reduce the coupling effects some cunning have to be taken:

1. In the high frequency crystal (XTAL2) the load capacitor of the FXTAL0, pin 18, has to be connected to ground in series with an inductor (see Figure 13. High frequency crystal inductor);

2. In the low frequency crystal (XTAL1) the ground parts of two load capacitors have to be connected together and, after, connected to the ground by an inductor.

3. The two tracks that connect the low frequency crystal to the SXTAL0 and SXTAL1, pins 23 and 22, have to be put in layer different from the TOP.

Figure 13. High frequency crystal inductor
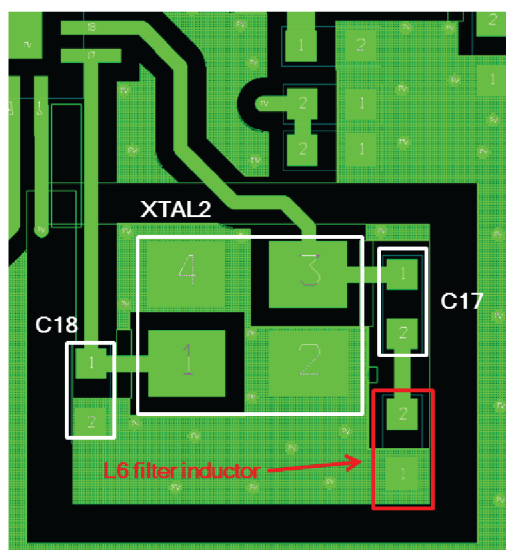
Figure 14. Low frequency crystal inductor and tracks
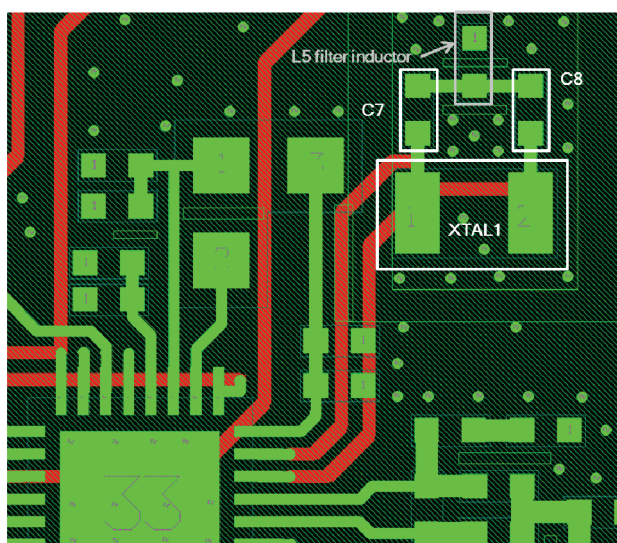
The DC-DC converter area is very sensitive and it is necessary to pay attention on the layout of this part. This is because the DC-DC converter generates ground noise that can get coupled on surrounding ground reducing the sensitivity and high frequency components can be coupled onto RF part.

So to ensure a correct layout it is necessary of:

1. Providing efficient filtering by placing capacitors as close as possible from the BlueNRG-1/2
2. Reducing parasitic ensuring wide and short connections to BlueNRG.

In Figure 15. DC-DC converter layout zone the suggested layout is shown:

Figure 15. DC-DC converter layout zone
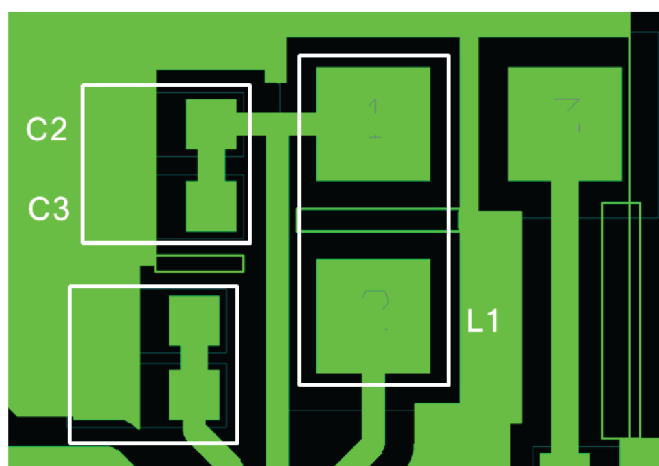
Special care has to be taken in the placement of the supply voltage filtering capacitors. It is in fact important to ensure efficient filtering placing these capacitors as close as possible from their dedicated pins on the BlueNRG-1/2.

The TX/RX part of the BlueNRG-1/2 is a very sensitive part. The discrete balun has to be placed as close as possible to the TX/RX pins. The traces that connect the RF pins to the balun network (differential trace) should be of equal length. If the two differential signals are un-balanced, common-mode issues can be generated. The differential traces have to be routed closely together. Differential receivers are designed to be sensitive to the difference between a pair of inputs, but also to be insensitive to a common-mode shift of those input. Therefore, if any external noise is coupled equally into the differential traces, the receiver will be insensitive to this (common mode coupled) noise. More closely differential traces are routed together, more equal will any coupled noise be on each trace, therefore better will be the rejection of the noise in the circuit.

The parallel inductors in the balun (and in general) should be mutually perpendicular to avoid mutual couplings. If no perpendicular position is possible, turn away their interposing capacitors or resistors.

The interconnections between the elements are not considered transmission lines because their lengths are much shorter than the wavelength and, thus, their impedance is not critical. As results, their recommended width is smallest possible. In this way, the parasitic capacitances to ground can be minimized.

Figure 16. Discrete balun layout zone
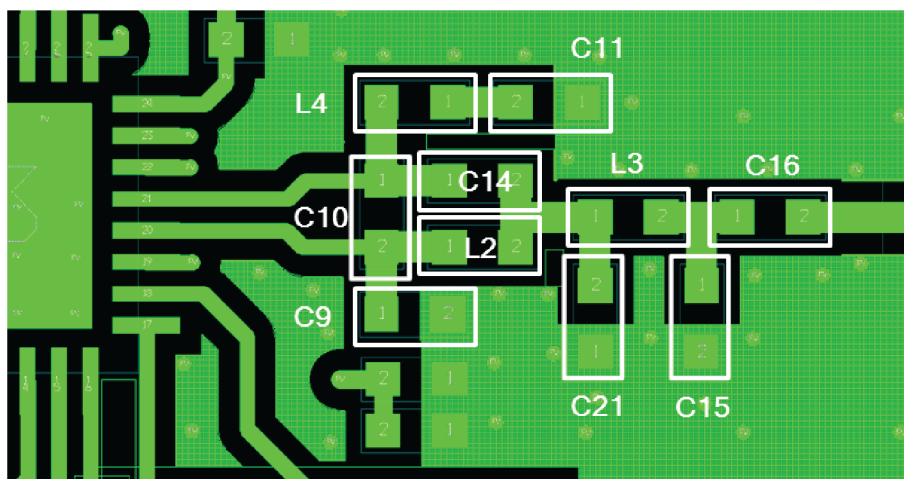
An application board using an integrated balun was designed also. The integrated balun was developed internally to STMicroelectronics and can be used only with the BlueNRG-1/2 devices. It is absolutely necessary to follow the layout rules described in the balun datasheet (BALF-NRG-02D3 [3]).
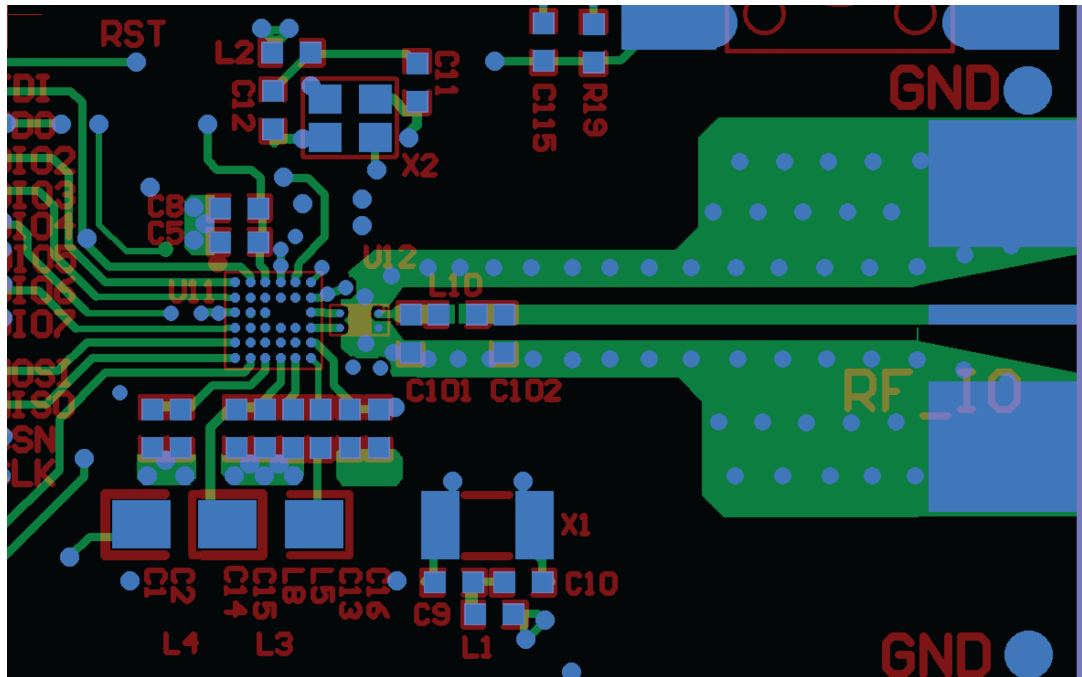
Pin ANATEST1 must be left not connected.

Pin ANATEST0/DIO14 must be left not connected if not used as GPIO.

5 CSP package layout recommendation

Concerning WLCSP package of the BlueNRG family, a six-layer approach has been used.

Figure 17. WLCSP board top layer

The DC-DC converter is the most sensitive area and it is necessary to pay attention on the layout of this part. This is because the DC-DC converter generates noise that is injected onto the ground of the board and can couple with passive components reducing sensitivity. So to ensure a correct layout it is necessary:

1. Insert a 15 nH inductor in series to the 10 uH inductor to filter the high frequency noise

2. Insert a 4.7 nH inductor between the SMPS ground, F5 ball, and the ground of the board to reduce the high frequency noise introduced from the SMPS ground in the application

3. Providing efficient filtering by placing the SMPS capacitors as close as possible to the BlueNRG-1/2

4. Connect together the ground of the 4.7 nH inductor with the ground of the SMPS capacitors on the top layer and, after, connect to the general ground of the board by multiple vias

The two inductors of 15 nH and 4.7 nH are necessary when the supply voltage is higher or equal to 3 V. For supply voltage lower than 3 V the two inductors can be not used. In the figure below the suggested layout for the DC-DC part is shown:

Figure 18. WLCSP board top layer 2
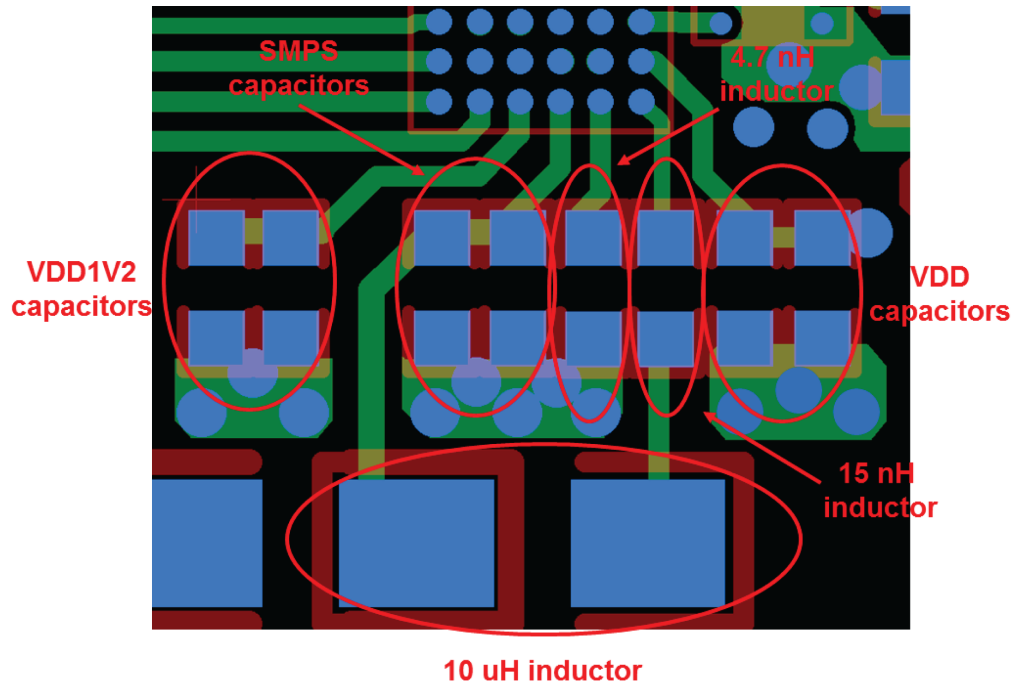
The RF section is based on the IPD integrated balun BALF-NRG-02D3. The correct layout for the BALF is described in the balun datasheet [3], so this document has to be used as reference. After the BALF balun a pi-network is suggested if the matching or the out of band attenuation have to be improved. After the pi-network a 50 Ω track is required.

Figure 19. WLCSP board top layer 3
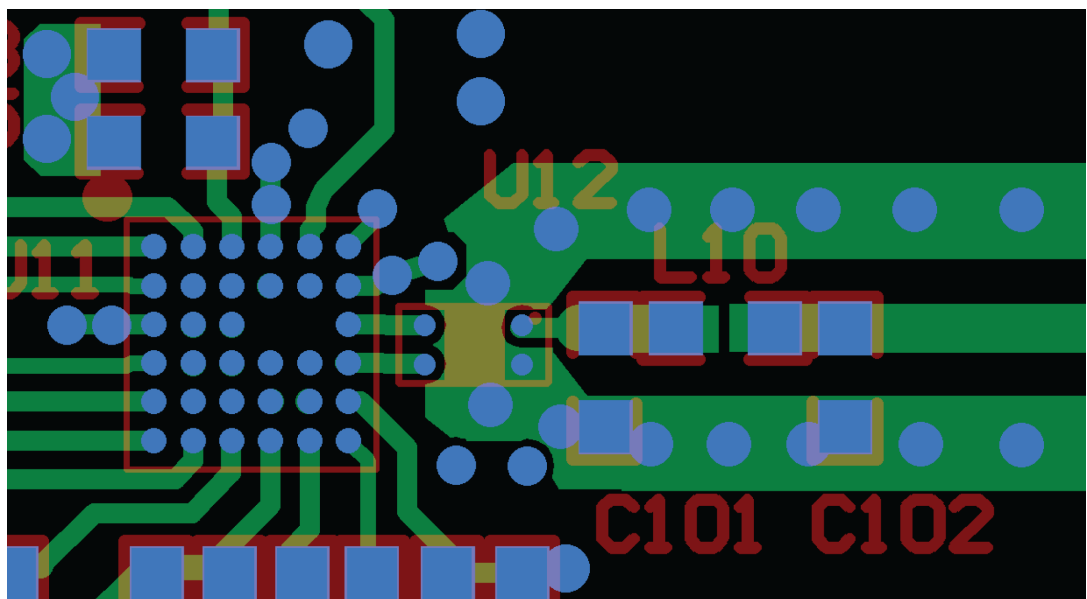
The internal balls of the WLCSP package are connected in the MID1 layer by laser vias. The MID1 layer, put at 64 um from the top layer, is utilized for the routing of the tracks. Two important points have to be highlighted:

1. Do not use ground layer below the RF zone, this ground would be too close to the top layer (see figure below).
2. Do not route tracks below the RF zone, this could degrade the RF performance (figure below).

3. Route the LSXTAL tracks in the MID1 layer (figure 20) or in a lower layer. Do not use the top layer to route these tracks to avoid coupling with the RF signal.

The ground of the LSXTAL has to be isolated from the ground of the RF part of the board. This is because the RF ground is "dirty" and this signal can disturb the correct work of the two crystals. Also the ground parts of two load capacitors have to be connected together and, after, connected to the ground by an inductor.

Figure 20. WLCSP board mid1 layer
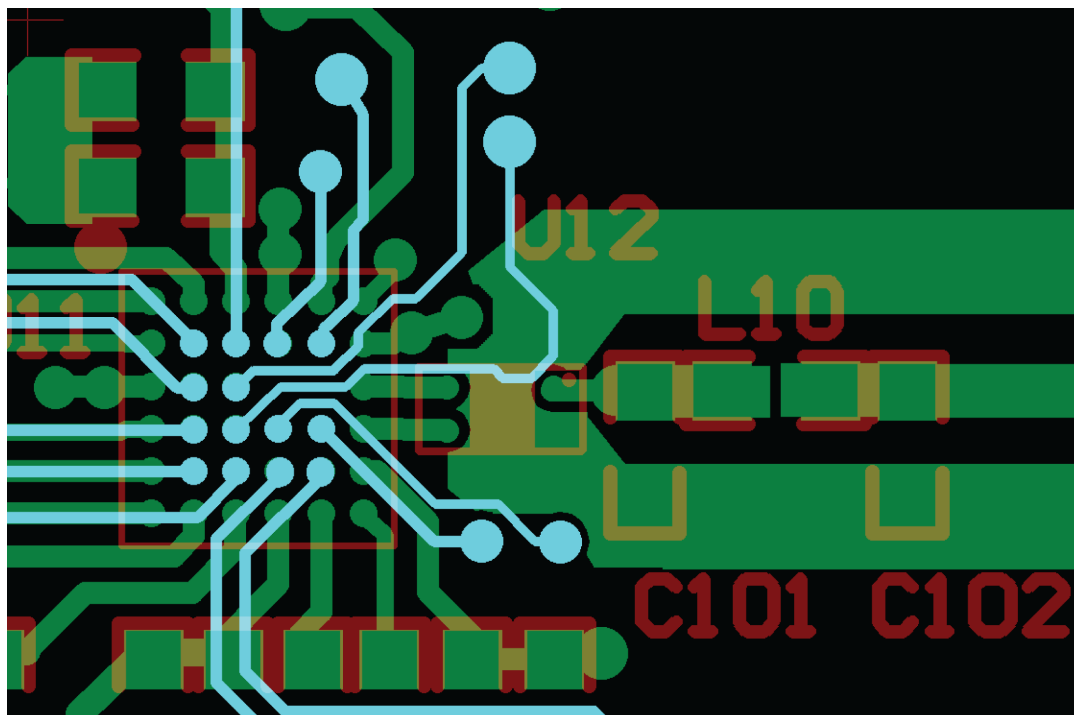
Figure 21. **LSXTAL connection in the MID1 layer**
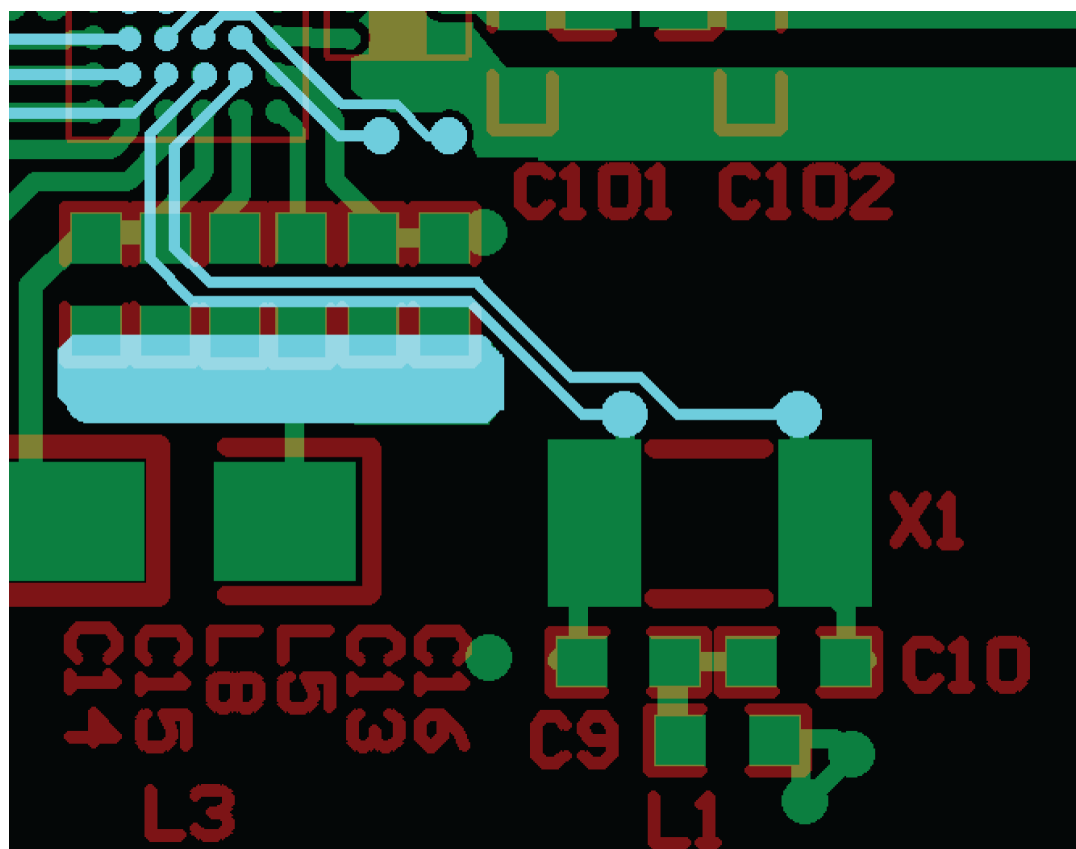
Another important point in the design of the board is the connection between the HSXTAL and the WLCSP package. Use the same approach for the LSXTAL: the connection between the BlueNRG-1/2 devices and the HSXTAL has to be done in a layer different from the top layer to avoid interaction with the RF part. In the layout the connection is in the bottom layer, see figure below.

As for the LSXTAL, the ground of the HSXTAL has to be isolated from the ground of the RF part of the board.

The ground parts of two load capacitors can be connected to the ground of the board in two different ways:

• Connect the load capacitor of the FXTAL0 to ground in series by an inductor
• Connect the ground parts of two load capacitors together and, after, connected to the ground by an inductor, as reported in the figure below

Figure 22. **HSXTAL connection in the bottom layer**
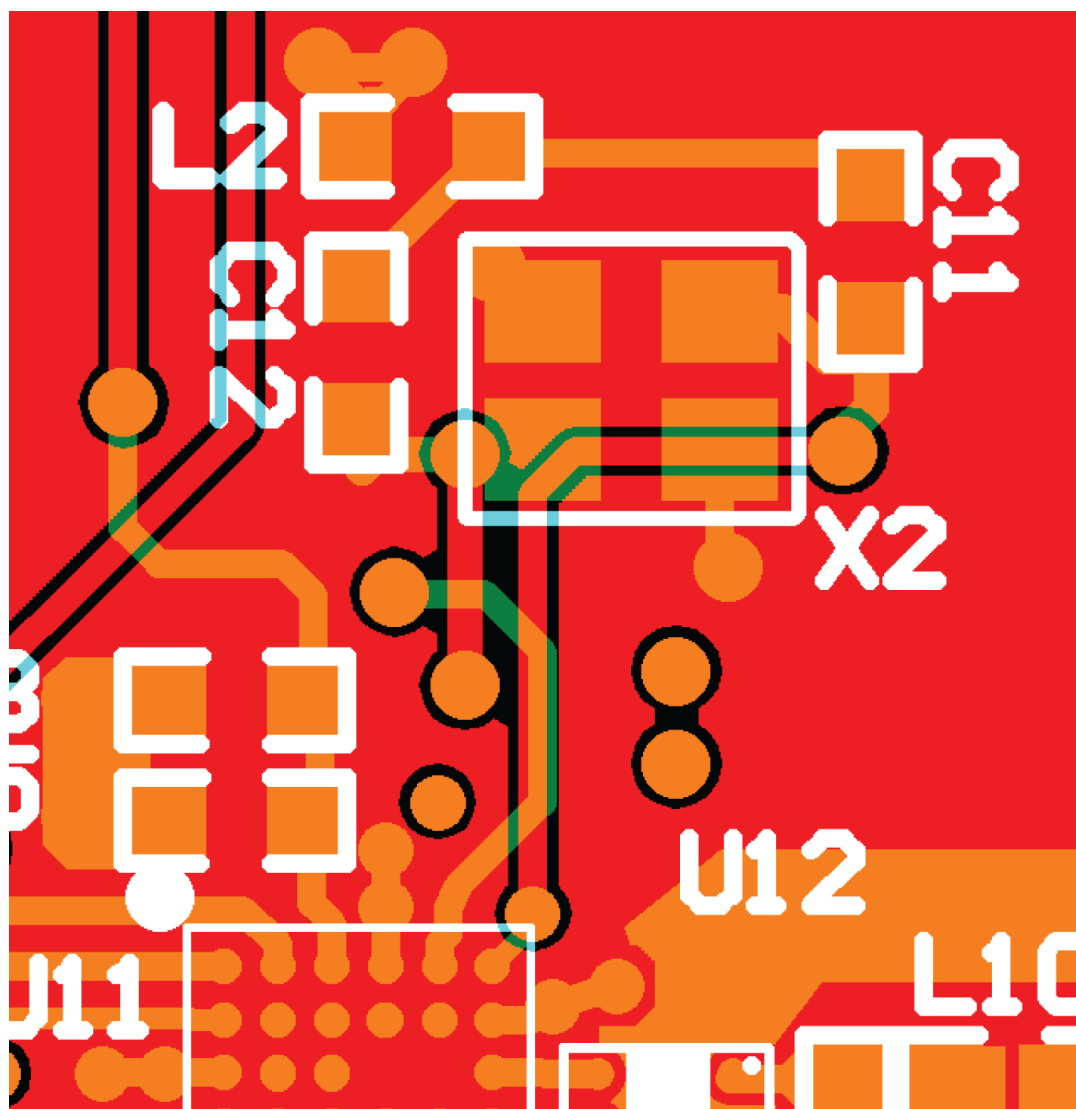
The ground of the WLCSP package is more delicate than the equivalent of the QFN package, so it is very important to create an accurate ground connection. WLCSP package has 3 ground balls (A4, B6 and C1) plus a ground dedicated for the DC-DC (F5). Do not connect the ground balls with the ground present on the top layer. It is better to use two ground vias for each ball to be sure to obtain a good ground connection, see red circles in figure 22. The reference ground layer is put on the MID2 layer with a distance of 316 µm. Thanks to the 6 layers it is possible to route all the connection tracks without using the MID2 layer that is left entirely as ground, see figure below.

Pin ANATEST1 must be left not connected.

Pin ANATEST0/DIO14 must be left not connected if not used as GPIO.

Figure 23. WLCSP ground pin connection
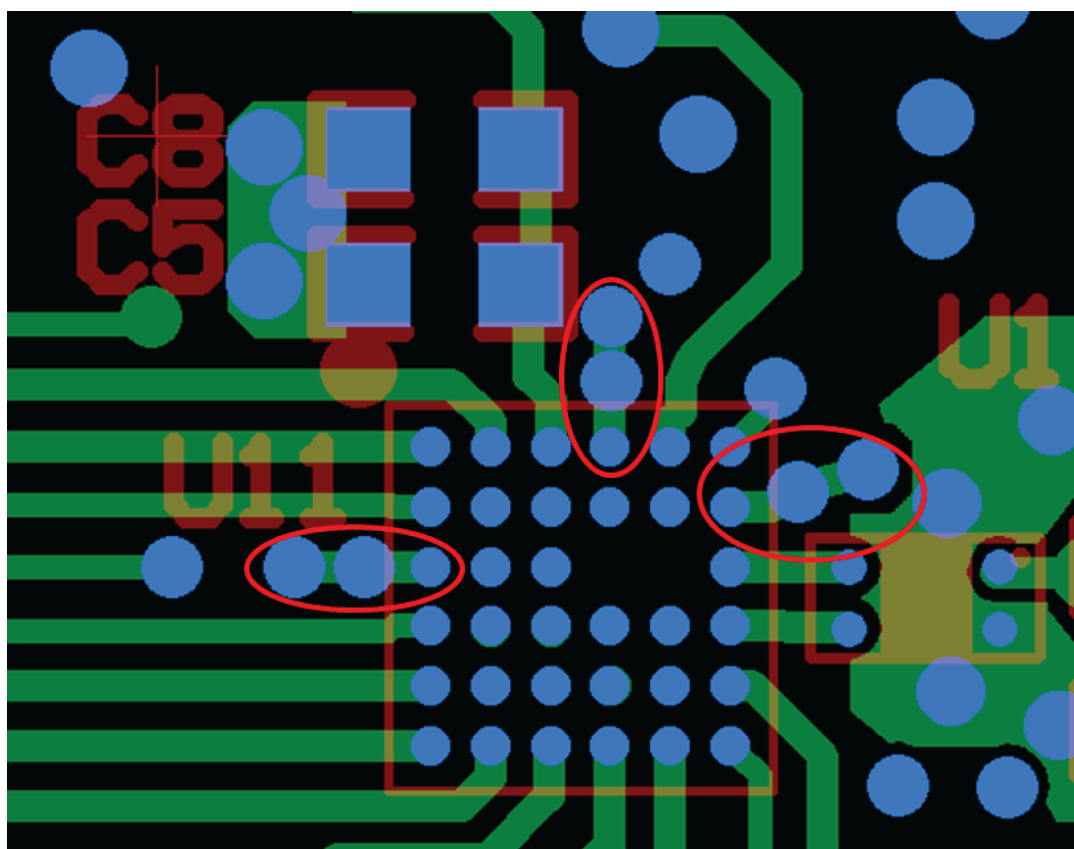
Figure 24. Mid2 ground layer
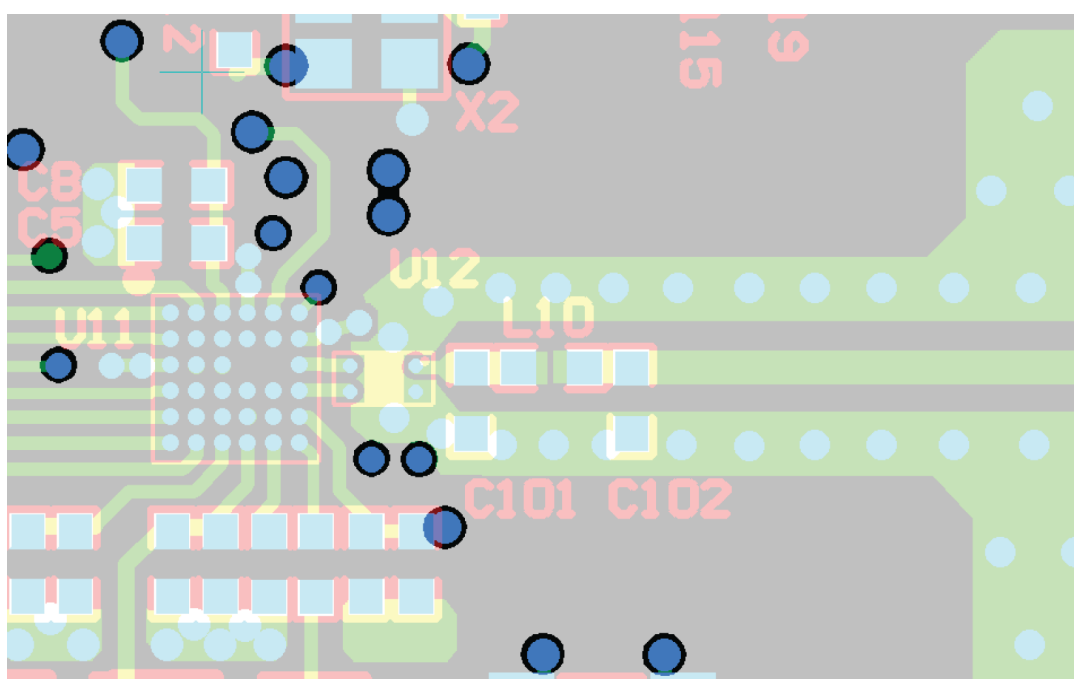
6 Reference

1. BlueNRG-1 datasheet rev 6
2. BlueNRG-2 datasheet rev 5
3. BALF-NRG-02D3 datasheet rev 3

Revision history

Table 3. Document revision history

Date	Version	Changes
30-Jun-2016	1	Initial release.
27-Nov-2018	2	Added references to the BlueNRG-2 device. Updated Section 4 QFN package layout recommendation. Added Section 5 CSP package layout recommendation. Minor text changes throughout the document.