AN4798
Application note

VIPower OMNIFET III hardware design guide

Introduction

The aim of this document is to provide the design engineers with a comprehensive “tool kit” in order to better understand the behavior of VIPower low-side switches thus allowing easier design.

Today’s VIPower low-side switches represent the 3rd generation of smart power drivers (the so called OMNIFET III) developed using STMicroelectronics’ M0-5 VIPower® technology.

In this latest generation of drivers, all the experience and know-how from previous generations have been implemented in order to improve robustness, increase functionality, and raise package density.

The complexity of a modern low-side driver (LSD) is still relatively low compared to many other logic ICs. However, the combination of digital logic functions with analog power structures supplied by an unstabilized automotive battery system across a wide temperature range is very challenging for such a device.

Today’s OMNIFET III devices meet all the above criteria, providing an optimal price/performance ratio.

This product family is available in two pinout options (three and five pin option). The three-pin option makes the product a perfect replacement for a standard Power MOSFET. The five-pin option offers additionally a dedicated supply pin and a status pin to perform diagnostics.

Contents

List of tables

List of figures

1 Device blocks description

The M0-5 low-side drivers are manufactured using ST's proprietary VIPower® technology. The devices are designed to drive 12 V automotive resistive as well as inductive and capacitive loads connected to the battery. A 5 V CMOS compatible interface to a microcontroller unit is provided.

The products feature a very low quiescent current to preserve battery charge during standby mode. Overvoltage clamp structure protects the devices effectively from "ISO 7637-2:2004(E)" pulses (with the exception of load dump pulses, unclamped or clamped above 40 V).

Reverse battery protection is provided in conjunction with external components (refer to *Section 3.2: Reverse battery protection for OMNIFET III*). Note that no protection features operate under reverse battery conditions.

M0-5 low-side drivers integrate advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown. A dedicated status digital output pin delivers diagnostic functions both in ON-state, in case of chip overtemperature, and in OFF-state in case of open-load.

1.1 Overvoltage clamp protection

Figure 1. Block diagram – clamp protection

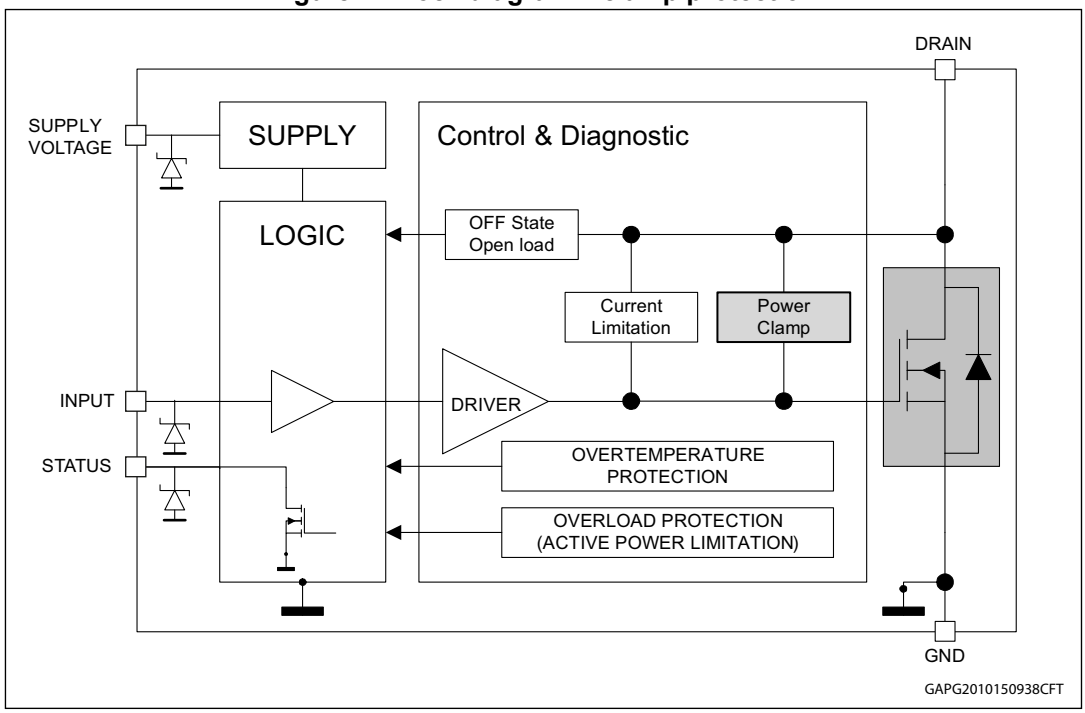
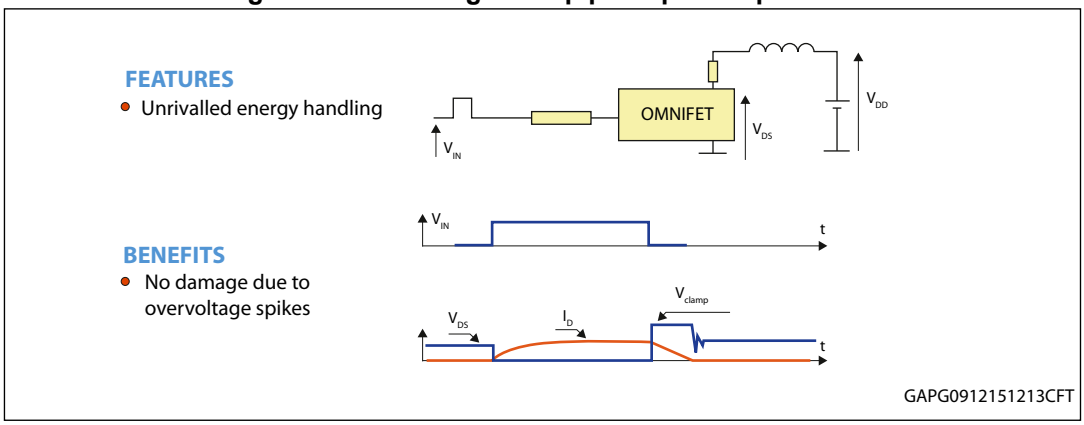
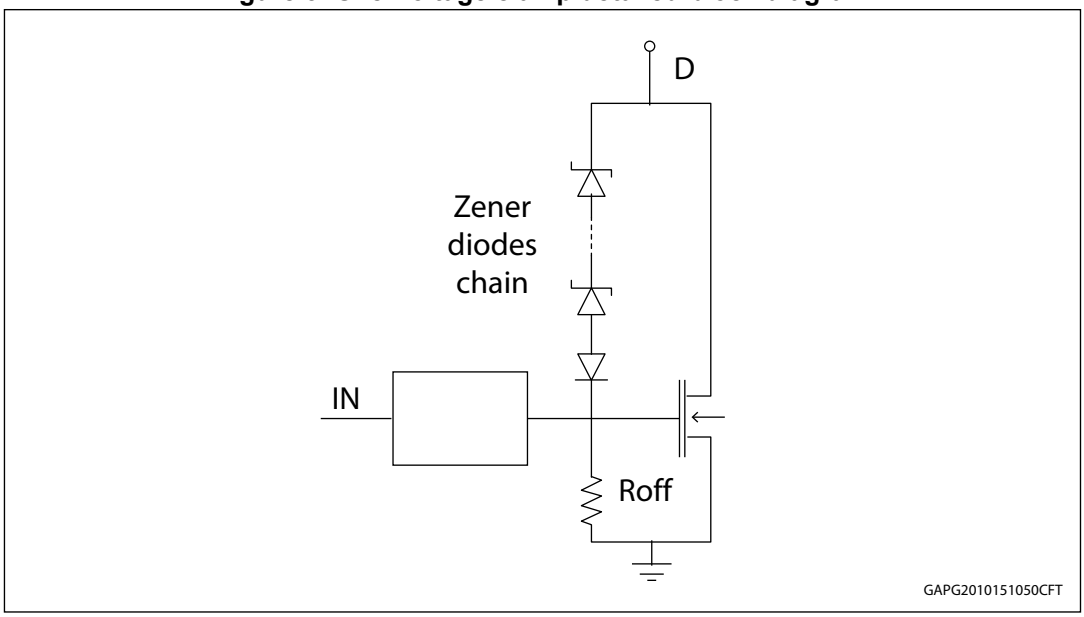


Figure 2. Overvoltage clamp principle of operation



This feature improves OMNIFET's energy capability to handle inductive loads versus a standard Power MOSFET. At device switch-off, the energy stored in the load inductance is dissipated in the device.

Figure 3. Overvoltage clamp detailed block diagram



As soon as the IN signal toggles from high to low, the Power MOSFET is switched off by the turn-off network model by Roff. While the gate voltage goes to zero, the drain voltage rises until reaching the Zener diode chain voltage. Current flow through the clamp allows switching the Power MOSFET back on. Its operating mode is now in full saturation. Once the load energy decays, the drain voltage starts to drop and the Power MOSFET switches definitely off. The chain breakdown voltage of the Zener diode is designed to be lower than the Power MOSFET intrinsic breakdown (BVdss) in all environmental conditions and even at the maximum drain current. The OMNIFET's ability to switch itself on at an output voltage lower than the intrinsic breakdown improves its energy capability against a non-protected Power MOSFET.

Relevant parameters: V_{clamp}, E_{as}.

1.2 Linear current limitation block

Figure 4. Block diagram – current limitation block

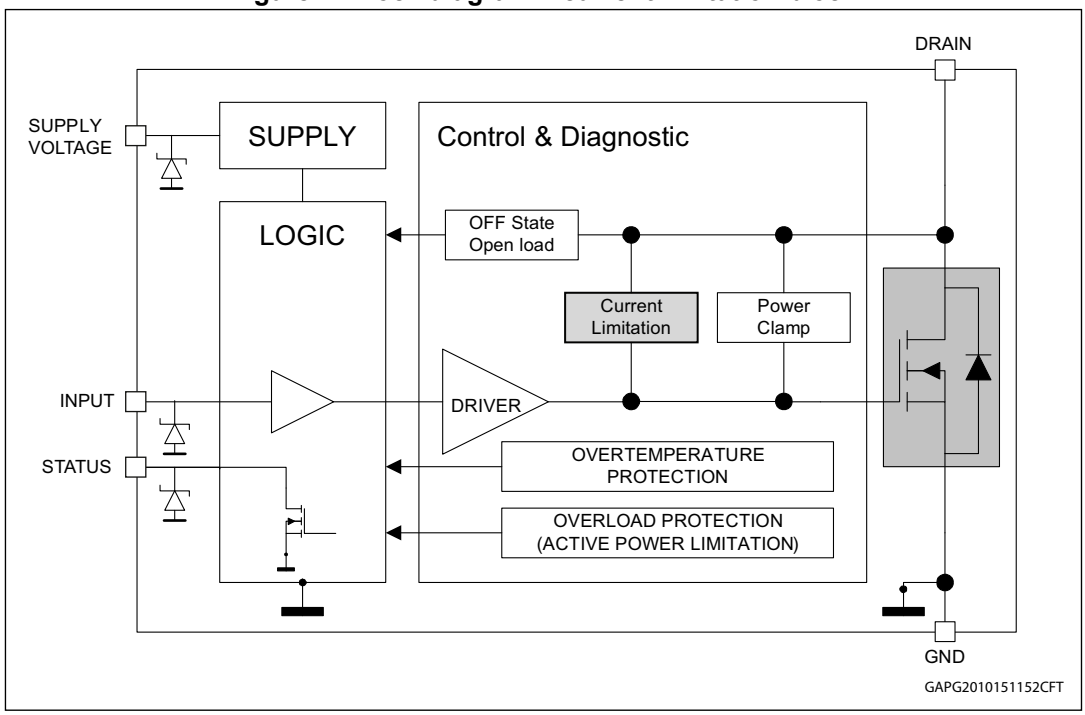
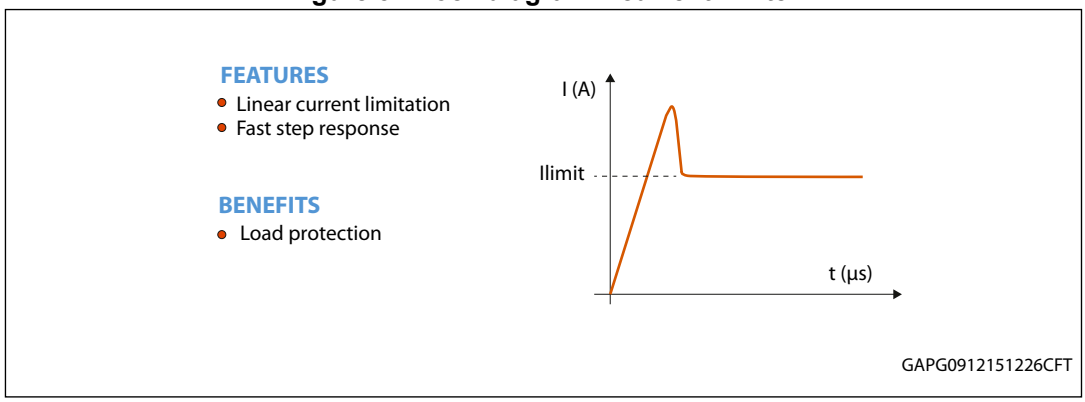


Figure 5. Block diagram – current limiter

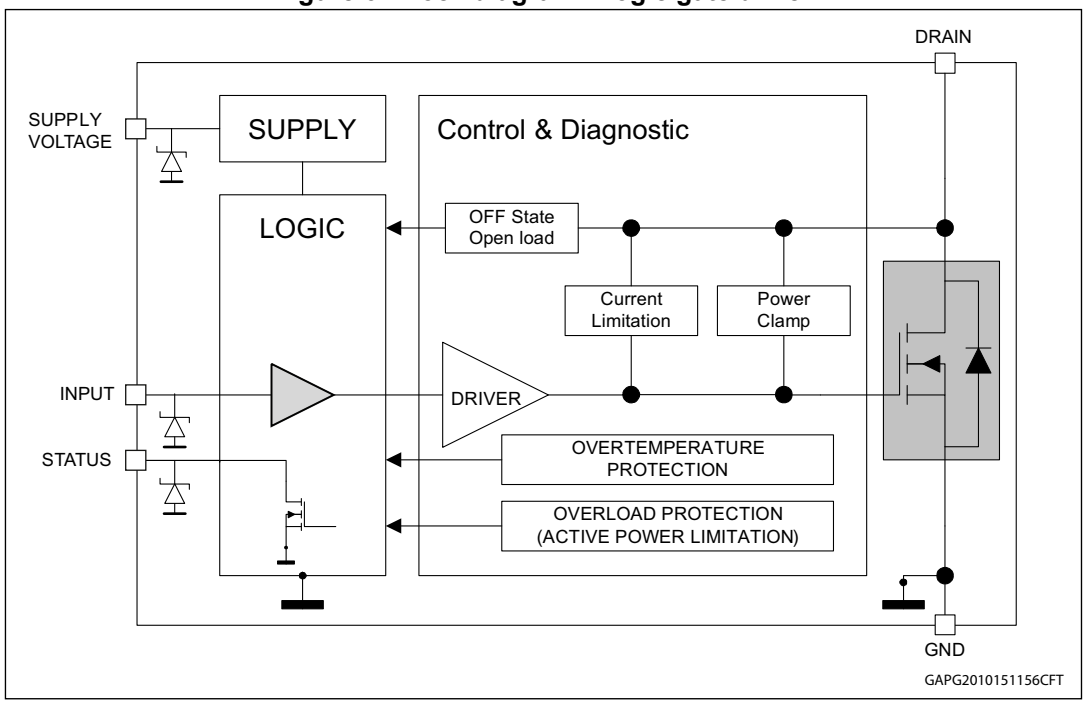


Using a senseFET technique, the drain current is compared with a built-in reference current. As soon as the designed drain current level is exceeded, the gate driver voltage is reduced in order to limit the current at the given value. This prevents the occurence of current crowding events that could lead to the almost instantaneous device failure in case of shorted load. When the current limiter is active, the device operates in linear region, so power dissipation may trigger the overtemperature shutdown.

Relevant parameters: I_{limH}, I_{limL}, t_{dIlim}

1.3 Logic and gate control block and power stage

Figure 6. Block diagram – logic/gate driver



OMNIFET III are switches designed to be driven by logic-level TTL/CMOS circuits. The current consumption of the input/supply pin was optimized to be as low as possible in order to limit the power dissipation in the external TTL/CMOS driver. The Power MOSFET gate is decoupled from the input by internal circuitry.

All protections (overvoltage, current limitation, overtemperature, power limitation) take control of the Power MOSFET gate to either switch it off (overtemperature, power limitation) or to lower the gate voltage (current limiter, overvoltage).

Relevant parameters are: V_{supply}, V_{SCL}, I_S, I_{ISS}, V_{il}, I_{il}, V_{ih}, I_{ih}, $V_{i(hyst)}$, V_{ICL}, V_{inth}, switching characteristics, R_{ON}, I_{DSS}.

1.4 Overtemperature protection and thermal sensor blocks

Figure 7. Block diagram – overtemperature protection

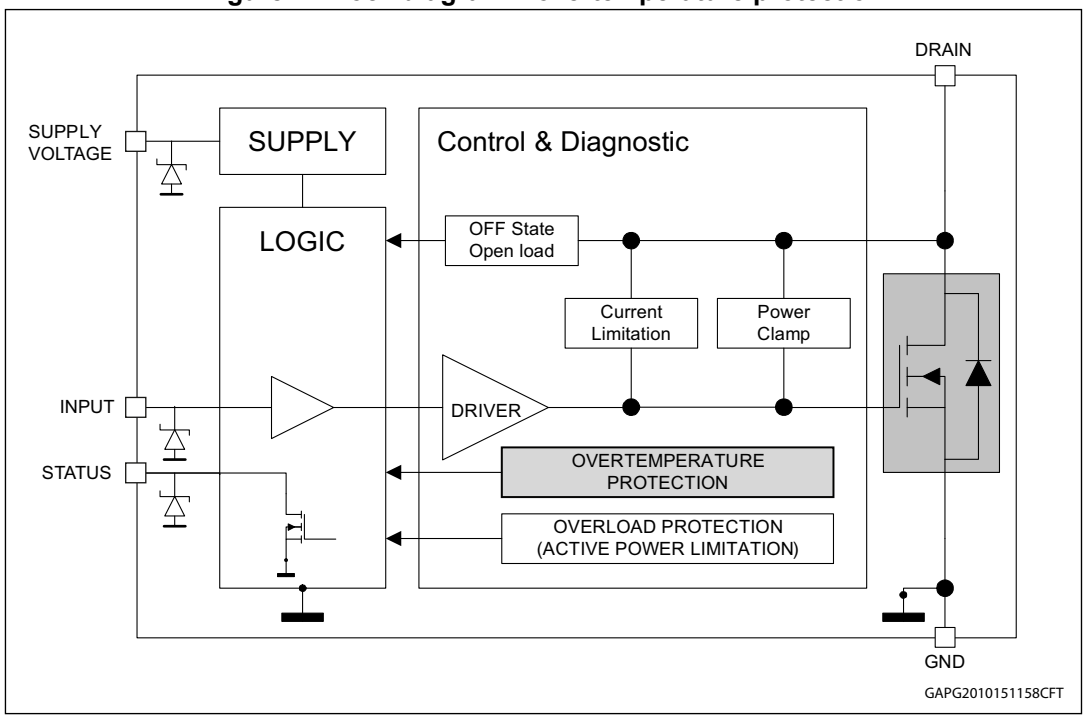


Table 1. Protection features

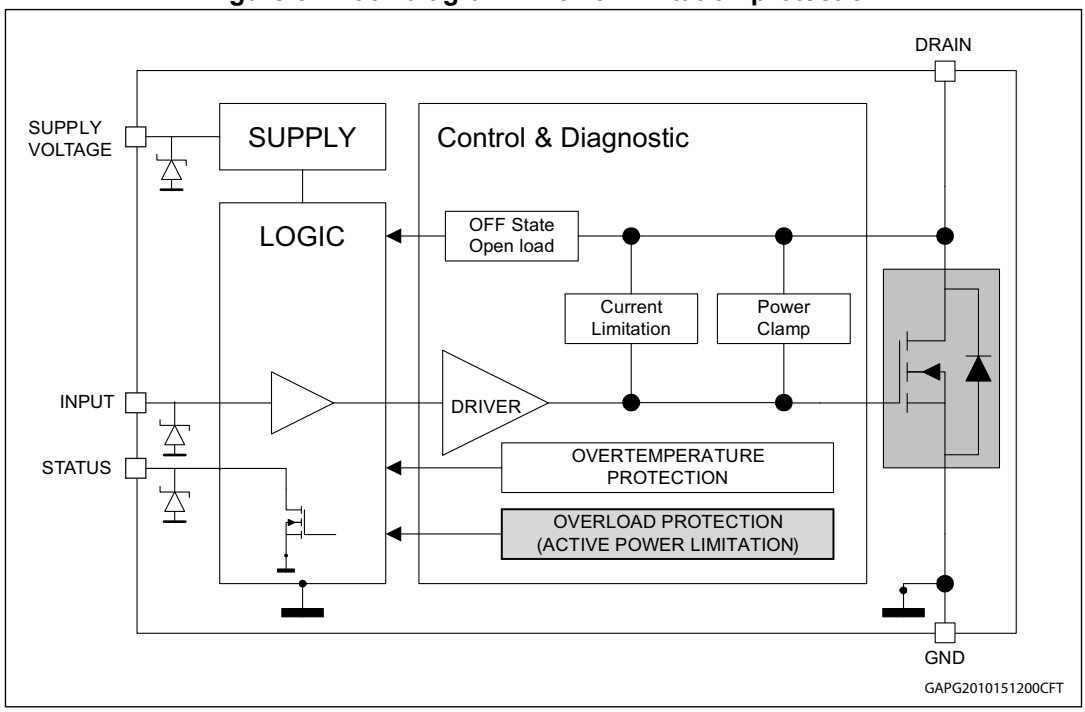
Features	Benefits
Short-circuit protection	High safety in all environmental and operating conditions
Overtemperature protection	
Automatically restarts at Reset temperature (typ. 5 °C lower than thermal shutdown (Tsd))	

This feature is based on the detection of the internal Power MOSFET temperature by a thermal sensor (hot sensor) which is built inside of it while the device is turned on. Its placement allows fast and accurate detection of the Power MOSFET junction temperature. In case of a thermal shutdown event, the device is automatically restarted when the junction temperature falls to, typically, 7 °C below the thermal shutdown temperature. Another thermal sensor is placed in the device logic (cold sensor). This second sensor, combined with the first one, allows the implementation of the power limitation feature.

Relevant parameters are: T_{TSD} (shutdown temperature), T_R (reset temperature), T_{HYST}.

1.5 Power limitation block

Figure 8. Block diagram – Power limitation protection



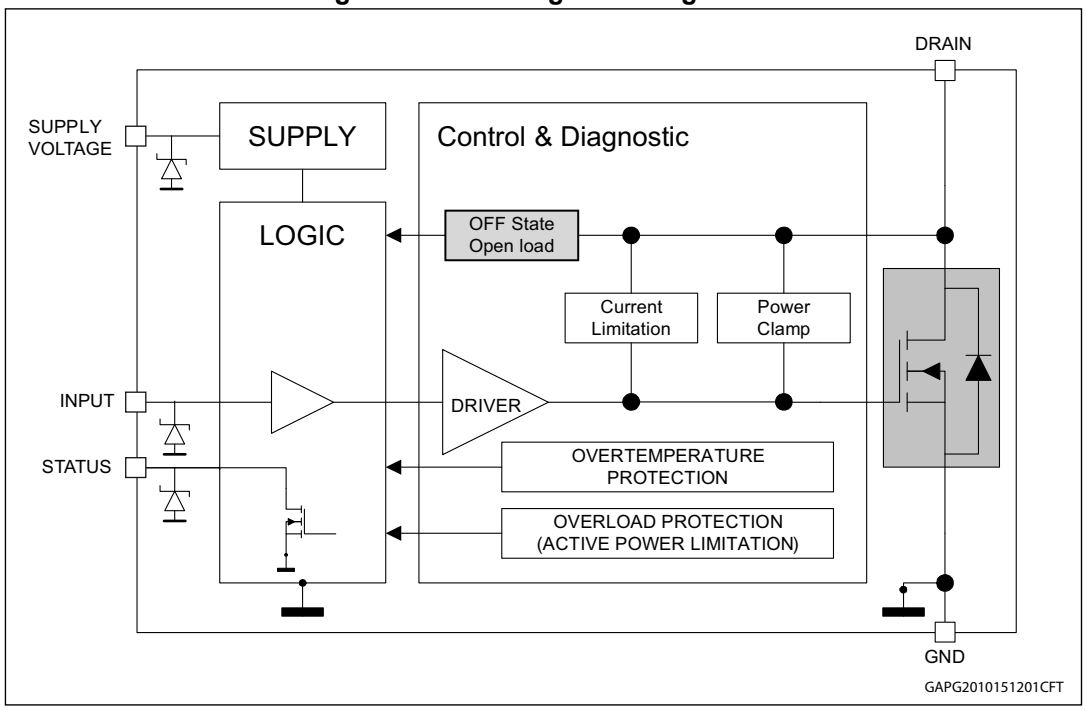
In case of overload conditions, the measurement of the temperature gradient between the hot sensor, placed in the Power MOSFET, and the cold sensor, which is placed in the control stage and can sense the package slug temperature, allows to limit the instantaneous (or almost instantaneous) power dissipation. As soon as the temperature difference between the hot and cold sensor reaches a certain threshold, the Power MOSFET is switched off and is restarted once the hysteresis threshold is reached. This offers improved ruggedness when the device is in overload conditions compared to a temperature control which is based on the reading of the Power MOSFET absolute temperature (like the OMNIFET II product family).

Relevant parameters are: no parameter specified in the datasheet. This feature is part of the device protection strategy.

1.6 Diagnostic block

In ON-state the overtemperature shutdown occurs typically at 175 °C. When this happens the device is shut down and the status feedback is provided by a LOW level on the status pin. The device is automatically restarted (auto-restart function) when the junction temperature drops below the thermal hysteresis value (T_R). The status low level is cleared as soon as T_j drops below T_{RS} where T_R-T_{RS} is typically 5 °C. The status pin has a wider hysteresis in order to obtain a stable diagnostic during overtemperature events.

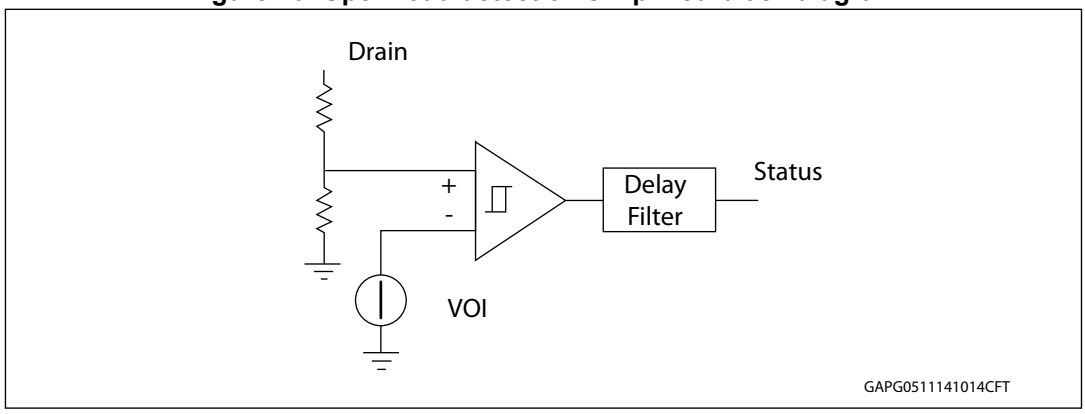
Figure 9. Block diagram – diagnostic



Status low output voltage is given by V_{stat}.

The status pin provides an open-load in OFF-state feedback. If the load is present, the Power MOSFET drain is pulled up to the battery voltage.

Figure 10. Open-load detection simplified block diagram



If a load is missing (open-load) the drain voltage goes to zero through the internal resistive divider as per the figure above. An internal comparator detects this condition and sends this information to the status pin that is made up of a simple low-voltage switch in open-drain configuration. Filtering is built in order to avoid false diagnostic during the switch-off. In other words, the open load in OFF-state diagnostic is provided with a delay after the falling edge of the input. The delay time is dimensioned to be longer than the maximum Power MOSFET turn-off time.

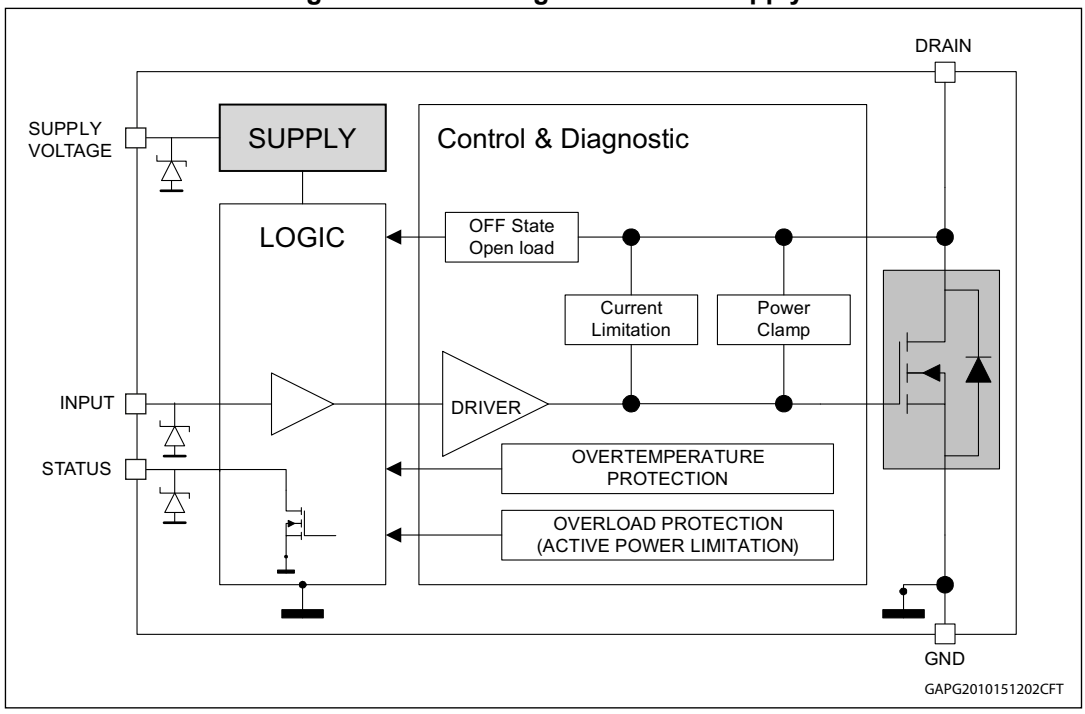
Relevant parameters are: status pin (V_{stat}, I_{lstat}, C_{stat}, V_{stcl}), open-load detection (V_{ol}, td(oloff)), overtemperature protection (T_{TSD}, T_R, T_{RS}, T_{HYST}).

1.7 Supply block

The device is supplied by a dedicated pin called “supply”. It is used to supply the Power MOSFET gate and the internal logic. In the 5-pin configuration, the device is intended to be permanently supplied in on and in OFF-state in order to provide the OFF-state diagnosis. For lower quiescent current consumption, the V_{supply} can be switched off synchronously to the input signal. The intrinsic protection functions of the device, such as the power clamp, are functional even without V_{supply}.

In the 3-pin configuration, the supply pin is internally connected to the input pin, which means the device is on when input is high, and off when input is low. In this condition the logic functions that must be active are supplied by the Power MOSFET drain itself.

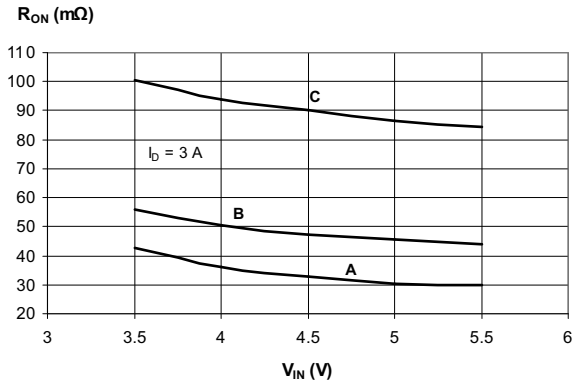
Figure 11. Block diagram – device supply



Low V_{supply} voltages derate the Power MOSFET R_{DSON}.

Typical derating values (R_{DSON} versus V_{supply}) are reported in *Figure 12*:

Figure 12. (VNL5050x) Static drain source on-resistance vs. input voltage



A: T_j = -40°C B: T_j = 25°C C: T_j = 150°C

Note: Input and supply pins connected together

GAPG1612130710CFT

1.8 Pin protections

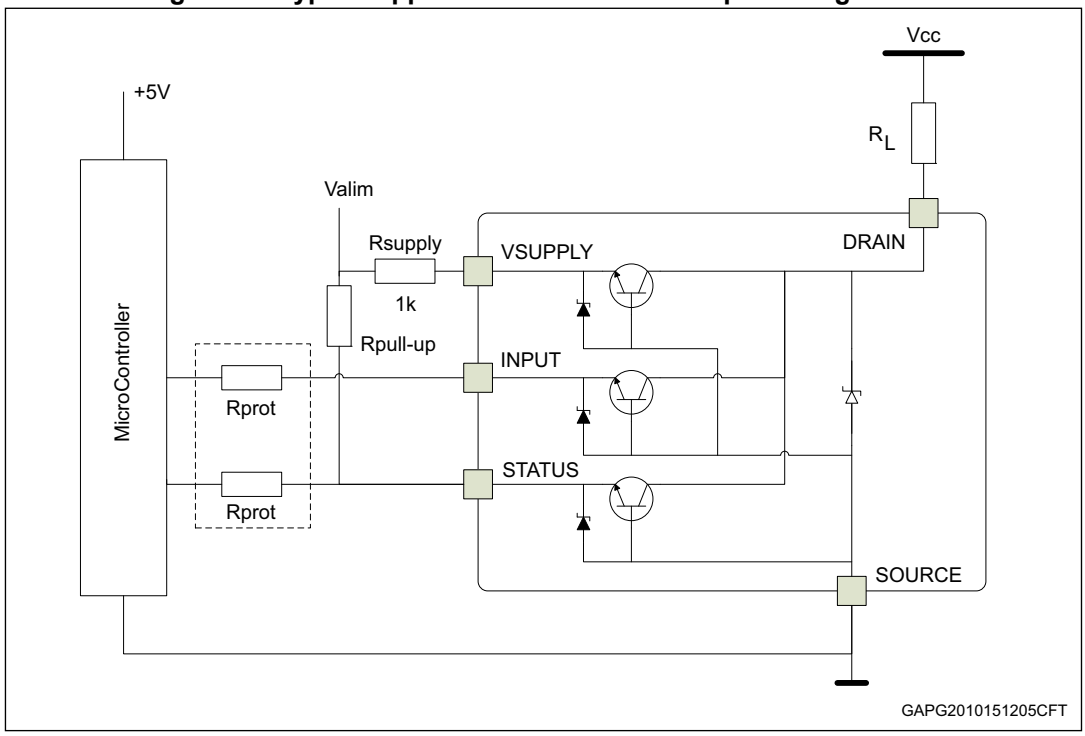
OMNIFET III have been designed to be compliant with common automotive standards, including ESD according to HBM and CDM models.

Relevant parameters are: Vesd1, Vesd2.

2 Application schematic options

2.1 5-pin configuration (permanent V_{supply})

Figure 13. Typical application schematics – 5-pin configuration

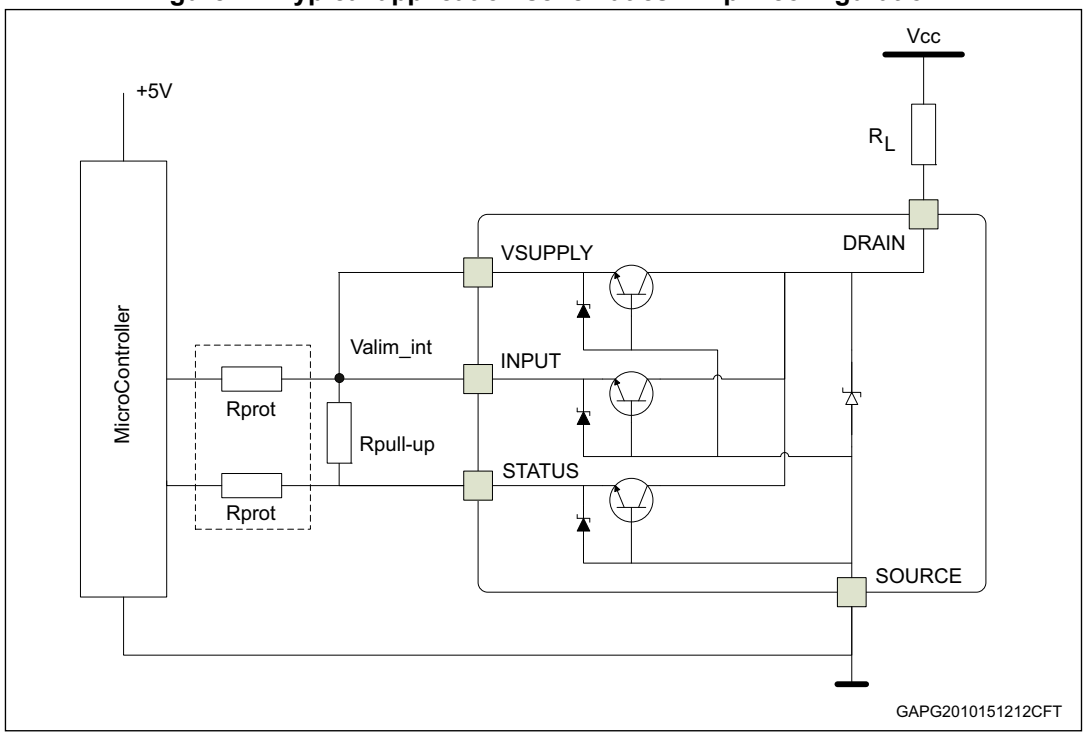


In the 5-pin configuration full diagnostic functions are available through the dedicated digital status pin, including:

- OFF-state: open-load/short to GND (V_{OL} detection threshold: min(0.6 V) – typ(1.2 V) – max(1.7 V)
- ON-state: overtemperature

2.2 4-pin configuration (switched V_{supply}) with diagnostics

Figure 14. Typical application schematics – 4-pin configuration



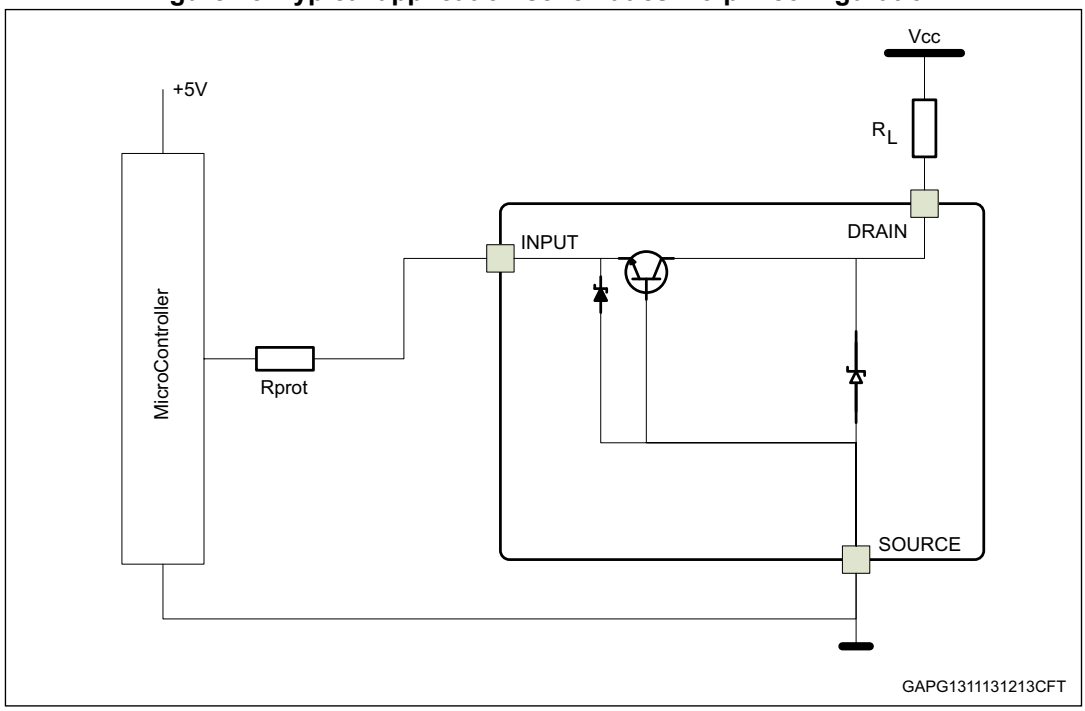
In the 4-pin configuration the device is supplied through the input pin (by internal connection of the input and supply), while status diagnosis is not available.

With the 4-pin configuration a reduced diagnostic function is available only in the ON-state through the dedicated digital status pin:

- ON-state: overtemperature

2.3 3-pin configuration (switched supply with no diagnostic)

Figure 15. Typical application schematics – 3-pin configuration



In the 3-pin configuration the device is supplied through the input pin (by internal connection of the INPUT and VSUPPLY), while STATUS diagnosis is not available.

2.4 Key parameters for driver circuit design

The driving circuit that controls the device must be chosen taking into account the device input characteristics:

- V_{INTH} (input threshold voltage) valid for the three-pin option that indicates as the Power MOSFET is a logic level Power MOSFET suitable to be driven with either a 5 V TTL driving circuit or directly by a 5 V microcontroller generic I/O.
- I_{ISS} and I_{IH} (supply current from input/supply pin) that help to define the maximum drop across the external driver equivalent output resistor ($\equiv R_{supply}$)
- V_{ICL} and V_{SCL} (input-source/supply-source clamp voltage) that indicate the maximum voltage that can be applied to the input/supply pins
- I_{IN} and I_S (maximum input/supply current in the datasheet's *Absolute maximum ratings* section) that indicate the maximum current that can flow through the ESD Zener of the input/supply pins before the device destruction or malfunction
- V_{supply}: the minimum value of this parameter that still allows proper Power MOSFET driving. This value makes the component incompatible with the 3.3 V bus

2.4.1 Description of external components

$R_{Pull\text{-}up}$: since the status is an open drain pin, a resistor is needed to fix the high-voltage level during normal operation and to detect the low-voltage level when a fault occurs. The

resistor has to be dimensioned in order to pull up the status above the logic high-voltage level based on the status pin maximum leakage current (I_{LSTAT}) and to ensure that the maximum value of the low voltage level is lower than the logic low voltage level (usually 0.5 V) based on the internal status N-MOS $R_{ds,on}$ in low-side configuration. The latter characteristic is described by the Status low output voltage (V_{STAT}) parameter. Values are shown in the following table.

Table 2. External resistor $R_{Pull-up}$ dimensioning

Diagnostic state	5 pin configuration (see *Figure 13*)	4 pin configuration (see *Figure 14*)
No fault	$V_{STATUS\_pin} = V_{alim,min} - R_{Pull-up} * I_{LSTAT} > V_{(logic\_high\_voltage\_level)}$ (i.e. 2.1 V)(1)	$V_{STATUS\_pin} = V_{alim\_int,min} - R_{Pull-up} * I_{LSTAT} > V_{(logic\_high\_voltage\_level)}$ (i.e. 2.1 V)(1)
Fault	$V_{STATUS\_pin} = V_{alim,max} * [R_{N\_MOS} / (R_{pull-up} + R_{N\_MOS})] < V_{(logic\_low\_voltage\_level)}$ (i.e. 0.9 V)	$V_{STATUS\_pin} = V_{alim\_int,max} * [R_{N\_MOS} / (R_{pull-up} + R_{N\_MOS})] < V_{(logic\_low\_voltage\_level)}$ (i.e.0.9 V)

1. $R_{N\_MOS} = V_{STAT}/1$ mA = 500 Ω, contribution due to the drop in the R_{prot} because the µC IO leakage is neglected.
V_{alim} is the supply voltage value either minimum or maximum.
$V_{alim\_int} = V_{alim} – R_{prot} * (I_I + I_S + I_{LSTAT})$

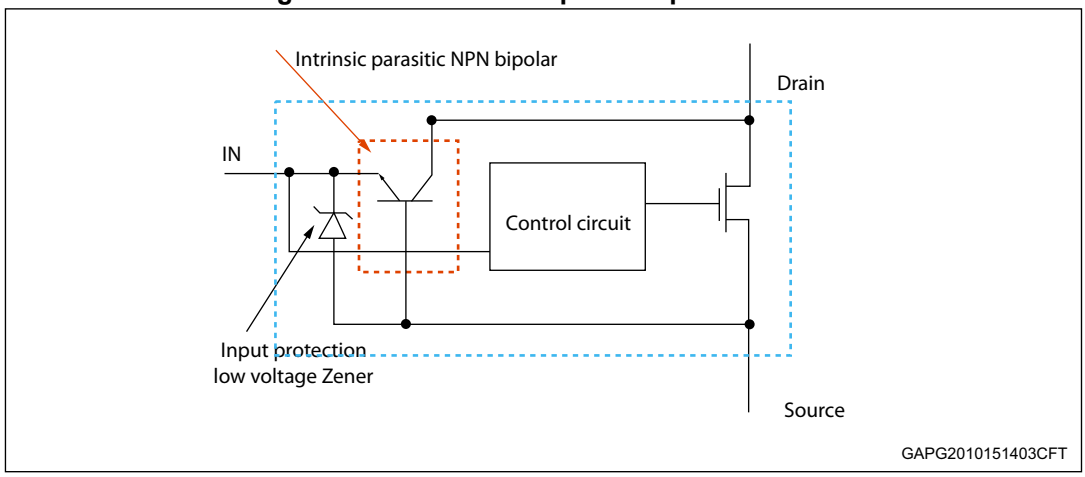
R_{Prot}: protection resistors are needed in series with the digital inputs in order to limit the current in the input structures as well as in the microcontroller I/O port structures to a safe value during transient and reverse battery conditions coupled directly or indirectly to the device drain.

The value of these resistors is a compromise between the leakage current of µC and the current required by the LSD input with the latch-up limit of µC I/Os. Values are shown in *Table 3*.

The I_{IN} has a maximum negative (current that flows out of the input device) limit as well. This current flows through two NP junctions in parallel: the base-emitter of the intrinsic NPN parasitic bipolar, structurally built-in the input pin ESD protection and the cathode-anode of the ESD Zener itself as shown in *Figure 16*. An excessive negative I_{IN} in the worst-case application condition, for instance when the OMNIFET maximum drain-source voltage is at the highest junction temperature, causes high power dissipation ($I_E * V_{CE} = I_{IN} * V_{CLAMP}$) inside the NPN leading to possible failure because of hot spot (secondary breakdown).

Note: I_E = NPN emitter current, V_{CE} NPN collector-emitter voltage.

Figure 16. OMNIFET simplified input structure



It is recommended not to exceed I_{IN} = -1 mA at least in normal operating conditions (V_{DRAIN} inside the car battery typical operating range i.e. up to 18 V). However, it is strongly recommended to keep V_{IN} referred to the OMNIFET source pin > -0.35 V. This corresponds to negligible negative I_{IN} even in the worst case (hot). This precaution avoids high power dissipation in the above mentioned intrinsic NPN in case of extreme applicative conditions where V_{DRAIN} is above the intrinsic BV_{CEO}.

Usually negative I_{IN} or V_{IN} values are caused in the application by a ground shift between the OMNIFET ground pin and the driving circuit ground. Extreme care must be taken to make sure that the above limit values are not reached even in dynamic conditions.

R_{supply}: protection resistor is needed in series with the supply pin in order to limit the current flowing inside the device when V_{DS} becomes either dynamically or statically negative. Values must be chosen according to the following table:

Table 3. External resistor dimensioning

Driver out voltage	5 pin configuration	3 & 4 pin configurations
< 5.5 V	IN: $0.7 / I_{latch\text{-}up} \le R_{prot} \le (V_{OH\mu C}\text{-}V_{IH,min}) / I_{IH,max}$ V_{supply}: $1\ K < R_{supply} < (V_{OHuC,min} - V_{supply,min}) / I_{ISS,max}$	$1\ K < R_{prot} < (V_{OHuC,min} - V_{supply,min}) / (I_{ISS,max} + I_{IH,max})$
> 5.5 V	IN: – $0.7 / I_{latchup} \le R_{prot} \le (V_{OH\mu C}\text{-}V_{IH,min}) / I_{IH,max}$ – $(V_{OH\mu C,max}$ - 5.5 V) / $R_{prot} < I_{IN(AMR)}$ V_{supply}: – $1\ K < R_{supply} < (V_{OHuC,min} - V_{supply,min}) / I_{ISS,max}$ – $(V_{OH\mu C,max}$ - 5.5 V) / $R_{supply} < I_{S(AMR)}$	$1\ K < R_{prot} < (V_{OHuC,min} - V_{supply,min}) / (I_{ISS,max} + I_{IH,max})$ $(V_{OH\mu C,max}$ - 5.5 V) / $R_{prot} < I_{IN(AMR)} + I_{S(AMR)}$

Where $I_{latch\text{-}up}$ is the µC I/O latch-up current, $V_{OH\mu C}$ is the µC I/O high voltage value.

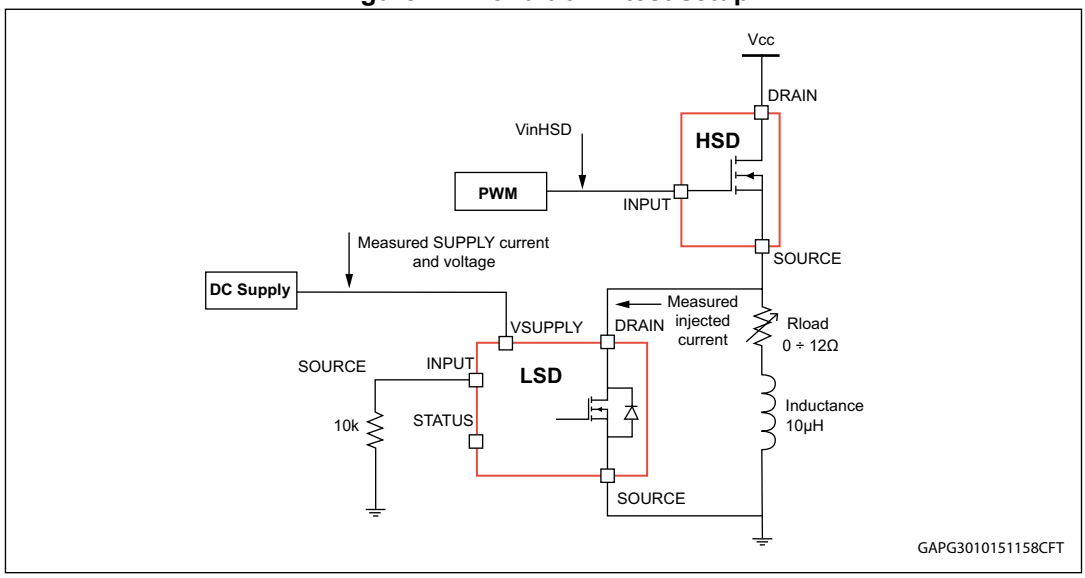
R_{supply} is mandatory to avoid possible device failures during operation. Two different operating conditions are here considered:

1. Condition 1: OMNIFET V_{DS} becomes either statically or dynamically negative (e.g. current recirculation typical of device usage in half/H bridge configurations);
2. Condition 2: external (not controlled by the device) fast dVds/dt applied.

Condition 1

This operating condition has been verified by the following test setup:

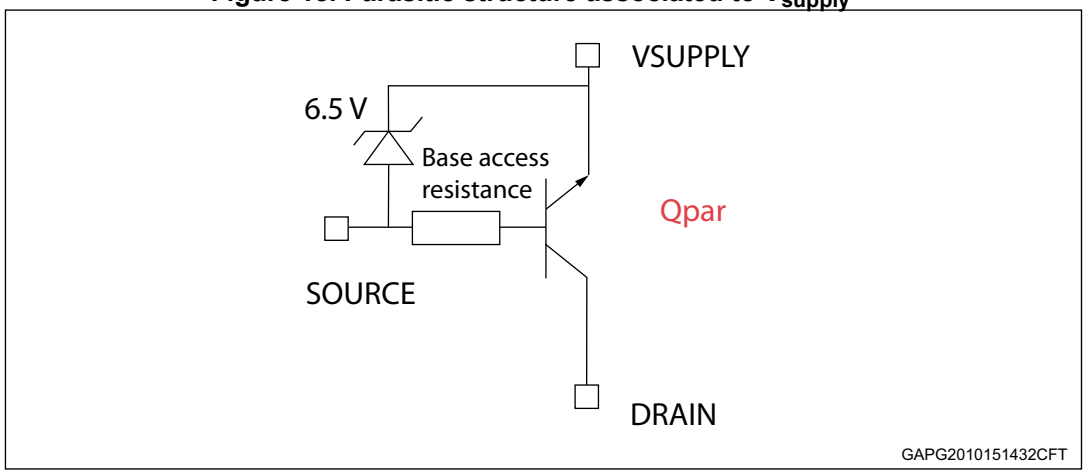
Figure 17. Condition 1 test setup



The LSD is the Device Under Test.

The HSD is switched on to store energy in the following inductor and is switched off to allow current recirculation through the LSD Power MOSFET body diode. The internal parasitic structure of the OMNIFET supply pin is shown below:

Figure 18. Parasitic structure associated to V_{supply} (a)



The above parasitic NPN between V_{supply} and drain, Q_{par}, causes V_{DS} to go negative; this causes additional current to flow through the V_{supply} pin, which leads to power dissipation in this NPN as per the formula below:

a. Zoom of *Figure 17*

Equation 1:

$P_{diss}(Q_{par}) = V_{ce} * I_e = (V_{supply} - V_{ds}) * I_{supply}$

If this latter value exceeds the NPN maximum power capability, the structure will fail.

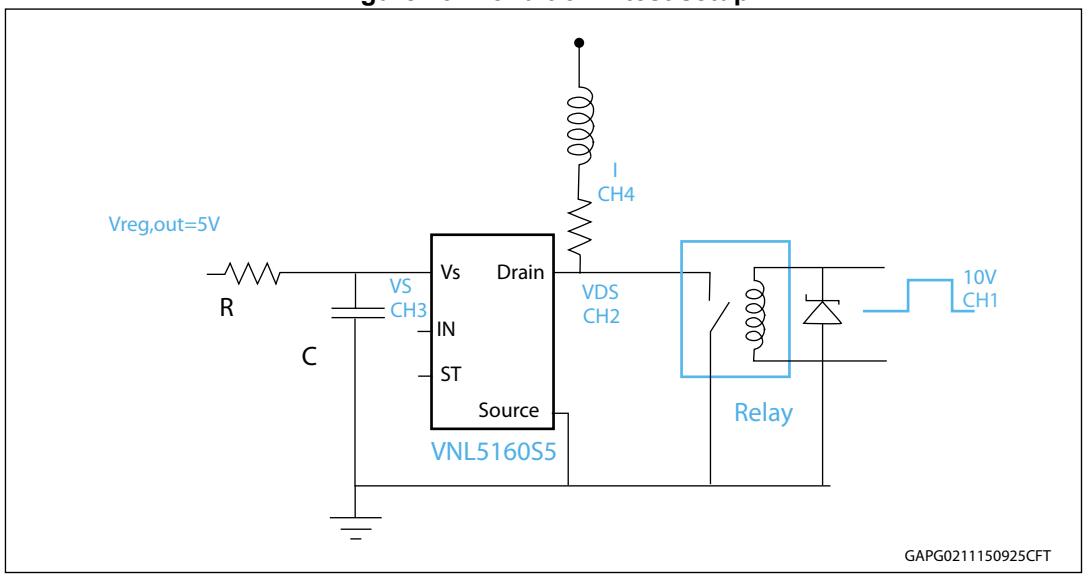
A solution to avoid the internal destruction of the device is to limit the above $P_{diss}(Q_{par})$ by reducing the emitter current (IE) value. This goal can be easily reached by adding R_{supply}. R_{supply} = 1 kΩ is already a good value to avoid failure since P_{diss} becomes few mW.

Condition 2

Q_{par} can also be dynamically triggered in case of fast dVds/dt. Critical dVds/dt could come from external events applied to the device drain (e.g. generic transients). The OMNIFET switching times are too slow to cause a device failure.

This condition has been verified by the following setup (assuming R = 0 Ω, C not mounted):

Figure 19. Condition 2 test setup



The relay, by itself, causes negative drain voltage and multiple high dVds/dt ringing due to its natural bouncing and thanks to the stray inductances in series to the OMNIFET source.

During negative drain voltage, current flows through the VNL5160S5-E body diode; Q_{par} operates in reverse conduction with current limited by the Q_{par} current gain itself. During subsequent high positive dVds/dt with high voltage, Q_{par} is still on at relatively high current. At this point Q_{par} could fail in short-circuit because of the extreme high peak power dissipation.

A capacitor (C) directly placed on the supply pin can still cause the device failure with the same failure mechanism (Q_{par} burnt) even with R_{supply}.

If a capacitor is present, during negative drain voltage, current flows through the VNL5160S5-E body diode; Q_{par} operates in reverse conduction with large dynamic current sustained by the C that gets discharged. During the subsequent high positive dVds/dt transient V_{DS} can exceed voltage values (> BVceo) while Q_{par} is still on and the capacitor at supply pin (C) is fully discharged (V_{supply} almost grounded). At this point Q_{par} fails for exceeded SOA (high peak $P_{diss}(Q_{par})$) because of the relatively high current caused by the C recharging.

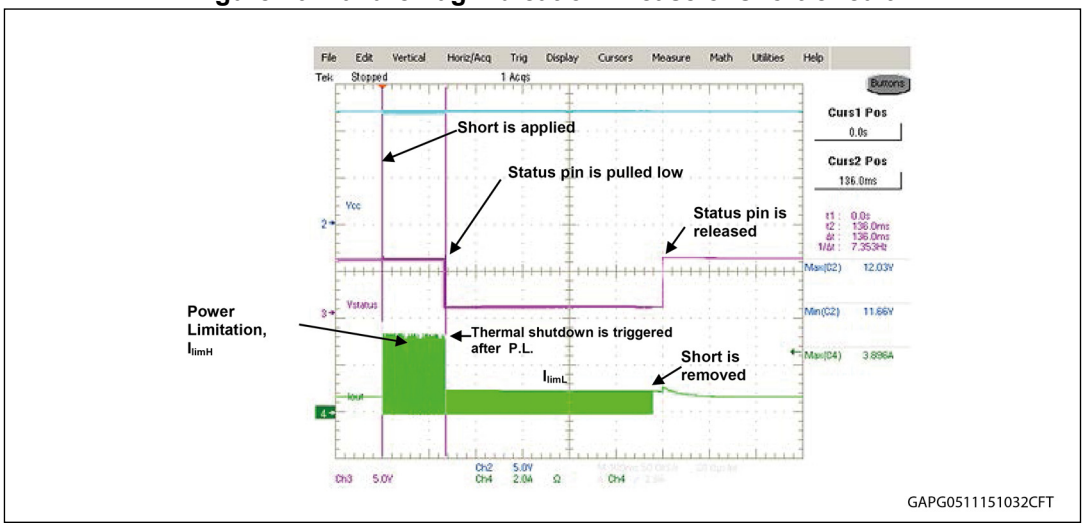
It is not recommended to place a filtering capacitor C directly on the supply pin unless the dVds/dt is smoothed by a filtering capacitor placed between the OMNIFET drain and source. The maximum allowed dVds/dt value is equal to 30 V/µs.

2.5 Diagnostic behavior: failure flag indication by the digital status pin

In case of overtemperature or open-load/short to V_{CC} in OFF-state, the fault condition is indicated by the status pin which is pulled low.

The typical behavior of a OMNIFET III low-side driver in case of overload or hard short-circuit while the device is on is shown in *Figure 20*:

Figure 20. Failure flag indication in case of short-circuit



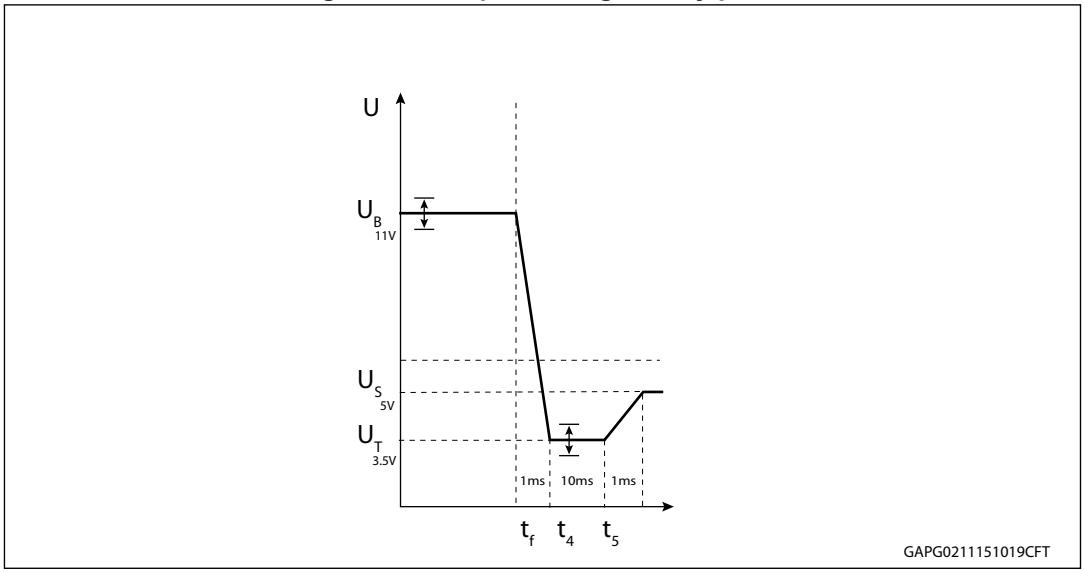
As soon as the short-circuit is applied, the drain current reaches its maximum value (I_{limH}) determined by the current limitation block. The active power limitation intervenes to protect the device from extremely high thermal gradients. The device temperature oscillates between thermal shutdown threshold and thermal reset when thermal shutdown is reached. The current limitation value is the I_{limL} while the status pin is pulled low.

When the short-circuit is removed, the current decreases to the nominal value and junction temperature starts to decrease because of the Power MOSFET reduced power dissipation. The status pin is released to the high logic level once the status reset temperature value (T_{RS}) is reached.

2.6 Extreme application conditions: severe cold cranking and DC condition

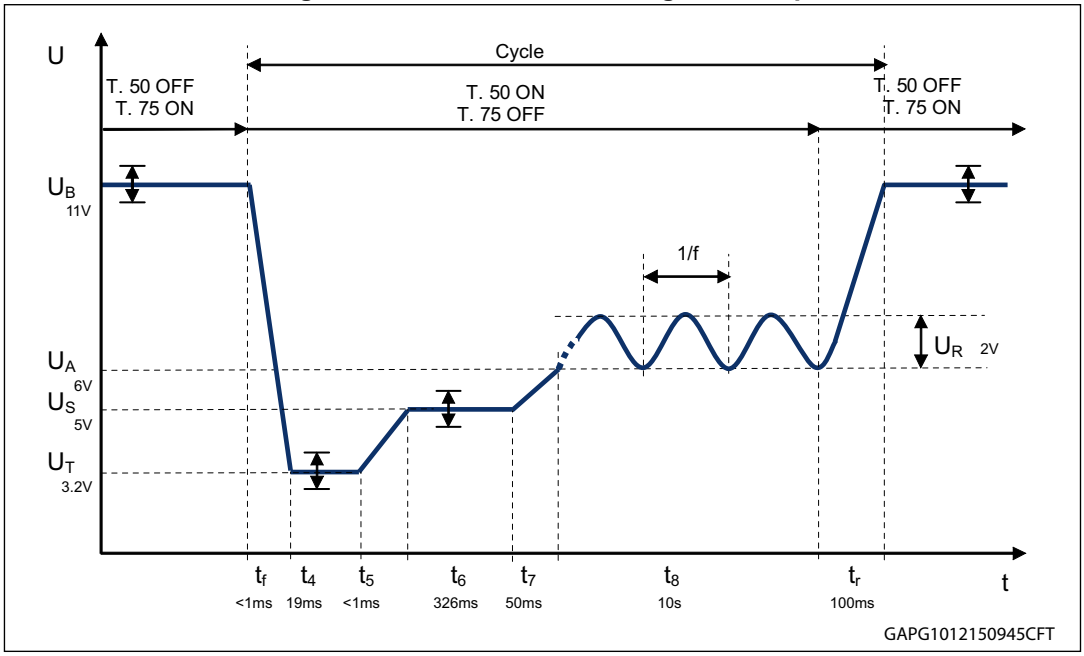
The following profile has been applied to the battery line (V_{BATT}):

Figure 21. Deep cranking battery pulse



The following setup has been used to perform the above test similar to the LV124 standard that refers to a pulse at minimum battery voltage (3.2 V) of 19 ms. The tests have been performed on both the three pin and five pin options.

Figure 22. Severe cold cranking test setup

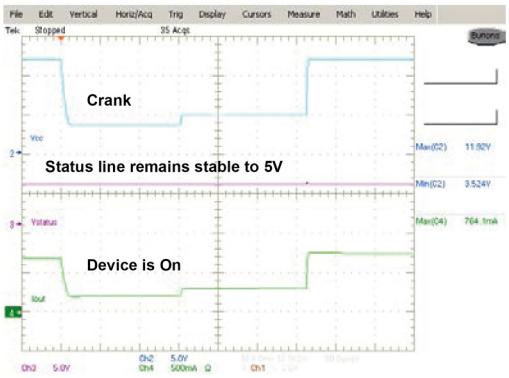


2.6.1 Device status: already on

In this test the device is already on, driving the nominal load while the battery crank occurs.

Example 1: VNL5300S5-E in ON-state driving the 5 W lamp

Figure 23. VNL5300S5-E in ON-state driving the 5 W lamp

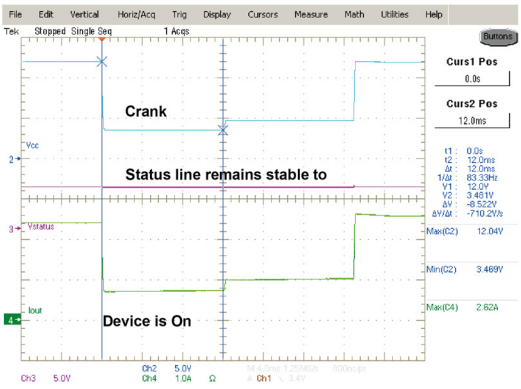


GAPG0511151115CFT

The device remains on during the battery crank since the capacitors on the battery line (C1 and C2) as well as the one on the voltage regulator output (C3) store enough charge to keep V_{supply} high (discharge current is 65 µA for 12 ms maximum).

Example 2: VNL5030S5-E in ON-state driving 21 W+10 W

Figure 24. VNL5030S5-E in ON-state driving 21 W+10 W



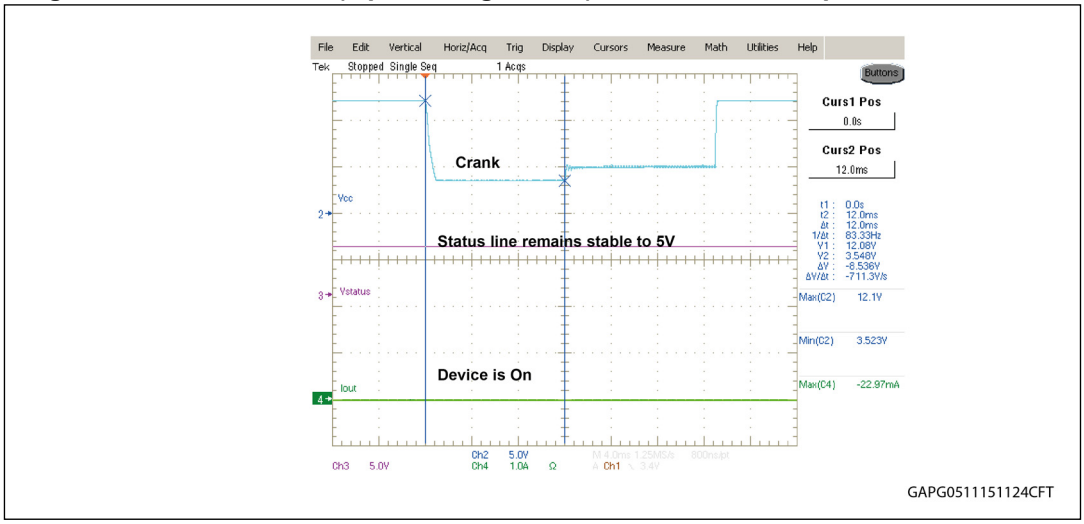
GAPG0511151118CFT

No difference was found between the 5-pin and the 4-pin configuration.

In the 3-pin configuration the status feedback is not available.

Example 3: VNL5030S5-E (5 pin configuration) in ON-state with open-load

Figure 25. VNL5030S5-E (5 pin configuration) in ON-state and open-load condition

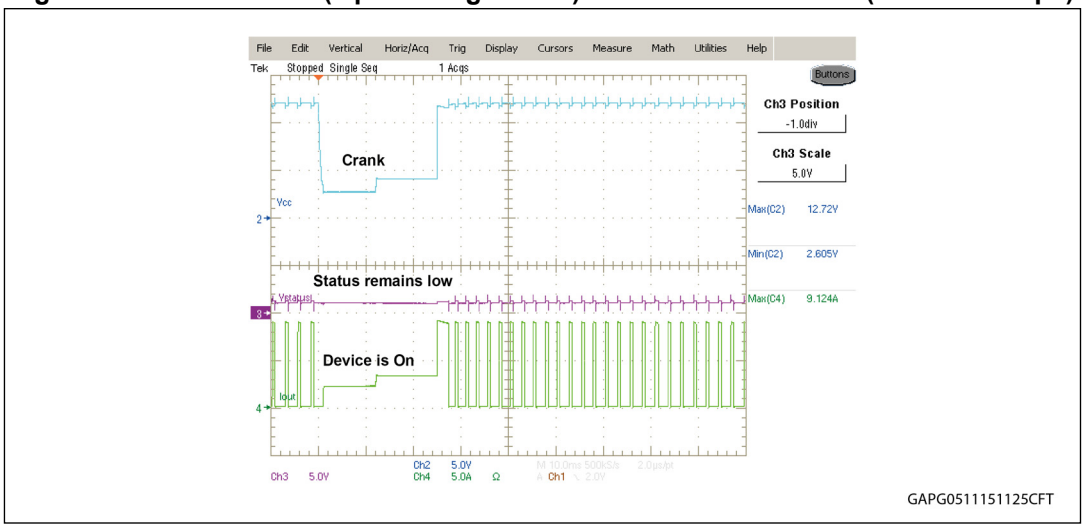


The status pin remains high even if $V_{DRAIN} < V_{OL}$ since no open-load detection is possible in ON-state.

The behavior of the 4-pin configuration is similar.

Example 4: VNL5050S5-E (5 pin configuration) in overload condition (3 x 21 W lamps)

Figure 26. VNL5050S5-E (5 pin configuration) in overload condition (3 x 21 W lamps)

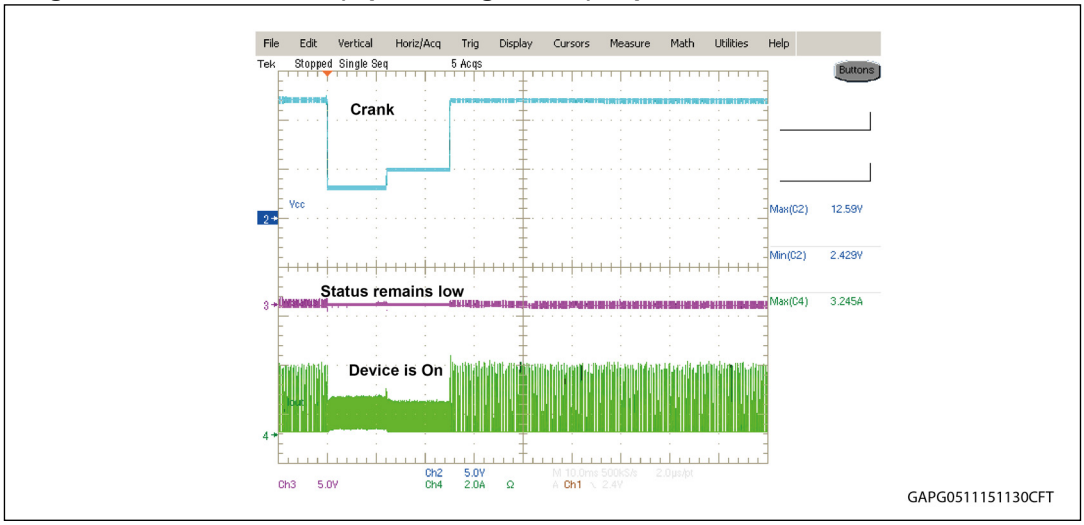


As soon as the thermal shutdown occurs, the status pin is pulled low. It remains low during the battery crank even if the load current decreases below the I_{limL}.

The behavior is similar for the 4-pin configuration.

Example 5: VNL5160S5-E (5 pin configuration) in permanent short-circuit condition

Figure 27. VNL5160S5-E (5 pin configuration) in permanent short-circuit condition

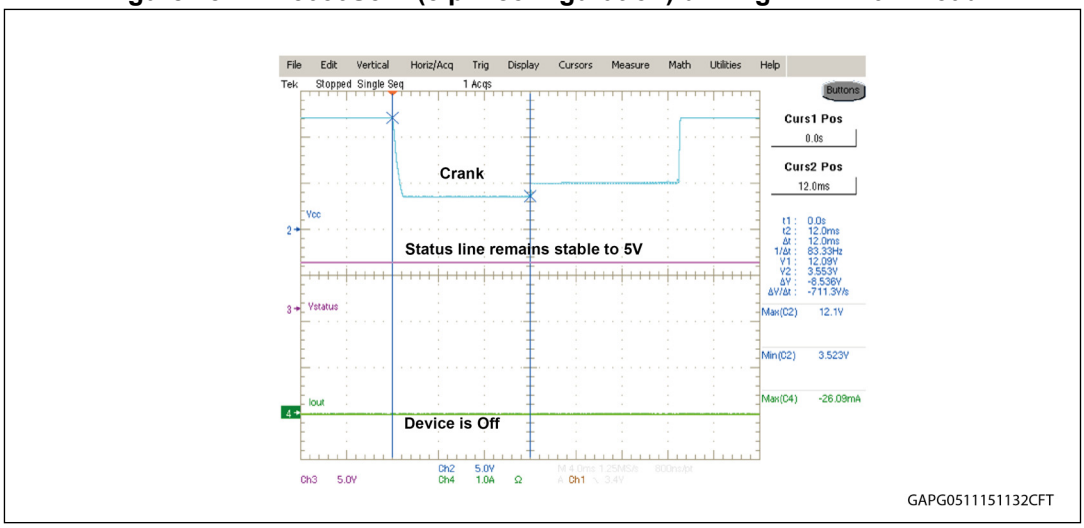


Same behavior between 5 and 4 pin configuration

2.6.2 Device status: off by the input

Example 6: VNL5030S5-E (5 pin configuration) with 21 W+10 W load

Figure 28. VNL5030S5-E (5 pin configuration) driving 21 W+10 W load

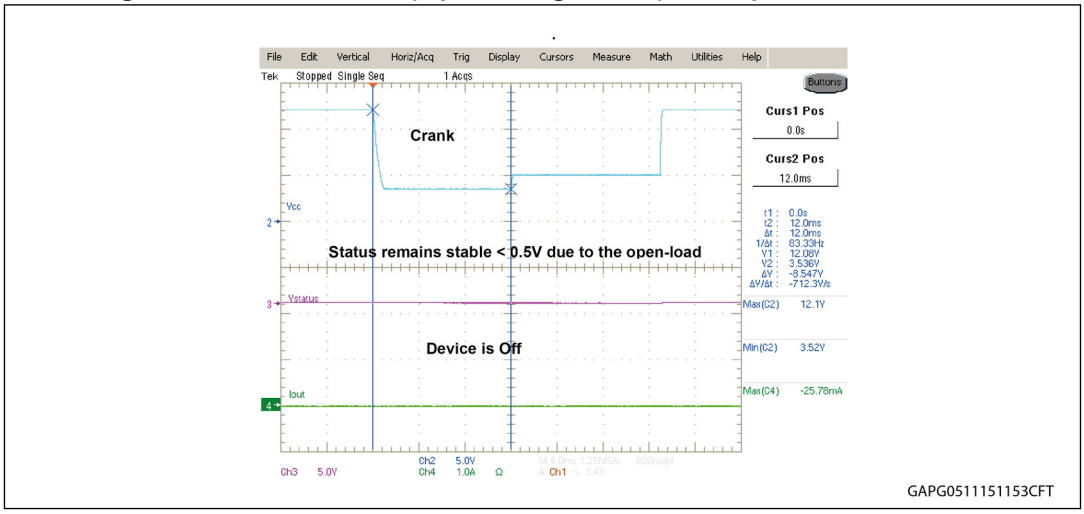


No difference has been found between the 5-and the 4-pin configuration. In the 3-pin configuration the status feedback is not available.

In the following case, as soon as the load is removed (open-load condition) and $V_{drain} < V_{ol}$ (open-load detection threshold), the status pin is pulled low.

Example 7: VNL5300S5-E (5 pin configuration) with open-load condition

Figure 29. VNL5300S5-E (5 pin configuration) with open-load condition



3 Reverse battery

3.1 Introduction

A universal problem in the automotive environment is the risk of damage when an end user inverts the battery polarity.

Users of battery-powered equipment expect safeguards to prevent damage to the internal electronics in the case of reverse battery installation. These safeguards can be either mechanical (use of special connectors) or electronic. Battery-powered equipment designers and manufacturers must ensure that any reverse current flow and reverse bias voltage is low enough to prevent damage to the equipment's internal electronics. To provide these electronic safeguards, different concepts applying passive or active reverse polarity protection are possible and described in this chapter.

Depending on the type of the device, specific protection must be implemented in order not to exceed the reverse capability of the device.

Reverse battery protection shall be inserted according to the recommendations given in this chapter. During reverse battery conditions the OMNIFET conducts through the body diode of the power MOSFET with the current limited by the external load. Since no device intrinsic protection schemes are active in reverse condition, special care must be taken on total power dissipation.

3.2 Reverse battery protection for OMNIFET III

Reverse battery protection schemes basically can be grouped into the following categories:

- Active or passive reverse polarity protection
- Reverse polarity protection can be either on battery line (V_{CC} terminal) or on GND line (GND terminal).

In most cases, the device itself is able to handle both static and dynamic reverse battery conditions. During this phase the main Power MOSFET is off and the current flows through its intrinsic anti-parallel diode.

In these conditions special care must be taken in order to ensure that:

1. The maximum junction temperature remains below 150 °C;
2. The load current (both peak and steady state) is lower than the absolute maximum ratings of the device (I_D, DC drain current).

In the first condition a proper thermal design is mandatory. The related datasheet contains the required information (device thermal impedance curves).

The formula to apply is:

Equation 2:

$$DTj = \int_0^{t,pulse} P_{diss} \times Zthj_{amb} \times dt$$

where $DTj = T_{j\_max} - T_{amb}$, $P_{diss} = V_{sd} * I_{load}$.

If both conditions are respected (T_{j_max} < 150 °C and I < -I_D), the reverse battery protection is needed only in case that the load must not be activated in such condition.

Table 4. Reverse battery protection concepts

Reverse battery protection concept	Active / passive	V_{CC} terminal / GND terminal
Schottky diode	Passive	V_{CC}
P-channel MOSFET	Active	V_{CC}
Reverse FET	Active	V_{CC}
N-channel MOSFET	Active	GND

3.2.1 Schottky diode

When the battery voltage is reversed, the Schottky diode is reverse–biased and only the rated leakage current IR flows. With respect to a standard diode, the Schottky diode has the advantage of a very low voltage drop in forward direction, hence power dissipation is reduced. However, the disadvantage of using a Schottky diode is that it is typically more expensive than a standard diode.

The procedure to properly choose the right device is reported below. The following parameters constitute the selection criteria:

- The average maximum current that flows through the load,
- The maximum repetitive peak reverses voltage $V_{RRM,}$
- The maximum ambient temperature T_{amb}

The following equation must be applied in all cases:

Equation 3:

$$T_{amb} + R_{th} \cdot P < T_{jMAX}$$

Equation 4:

$$P = V_{TO} \cdot I_{F(AV)} + rd \cdot I^2_{F(RMS)}$$

where:

$I_{F(AV)}$ = maximum average forward current

$I_{F\ (RMS)}$ = RMS forward current

R_{th} = thermal resistance (junction to ambient) for the device and mounting in use.

rd (small signal diode resistance) and VTO depend on the special characteristics of the diode.

One important aspect to take into account is the peak reverse voltage limit of the Schottky diode: V_{RRM} = 100 V seems a good compromise with respect to the “ISO 7637-2:2004(E)” pulse 1 Test levels IV. In case compliance with “ISO 7637-2:2011(E)” pulse 1 Test level IV is

required, V_{RRM} must be ≥ 150 V. The main drawback of this method is the power dissipation in the Schottky diode in forward direction.

Depending on the type of package and on the minimum R_{th} and maximum ambient temperature, the maximum affordable power dissipation in the Schottky diode is typically in the range of 1W. In consequence the maximum average forward current is limited to the range of 1 A – 2 A.

The direct diode reverse battery protection can also be replaced with a simple fuse. However, upon polarity reversal this fuse blows and the module needs to be replaced or repaired.

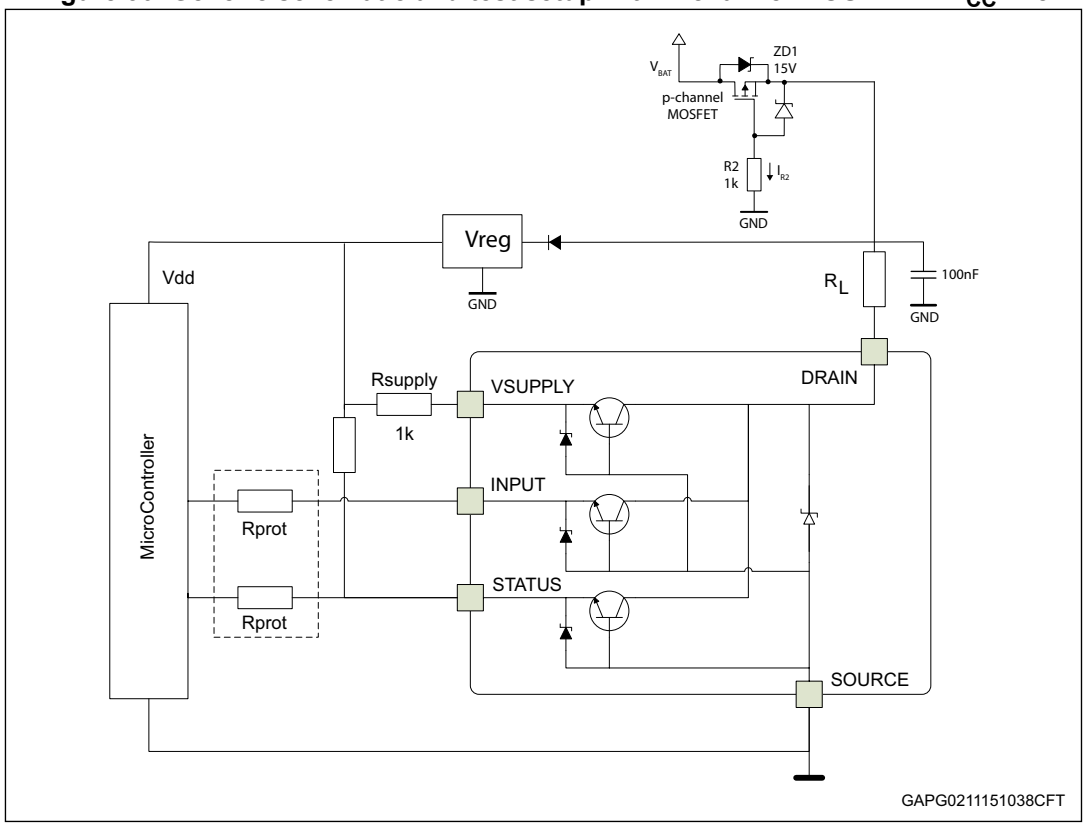
3.2.2 P-channel MOSFET in the V_{CC} line

The P-channel MOSFET is connected in a way that its gate is connected to GND via a resistor R2 and its drain to the V_{CC} pin, while the source acts as the reverse polarity protected supply. *Figure 30* shows a generic schematic.

It is important to insert the transistor in the right direction, because the P-channel MOSFET has an intrinsic anti-parallel body diode as well, which is in forward direction from drain to source.

By referring the gate signal to the ground line, the device is fully turned on when the battery is applied in the correct polarity.

Figure 30. Generic schematic and test setup with P-channel MOSFET in V_{CC} line



As soon as the battery voltage is applied, current flows through the body diode of the MOSFET until the Power MOSFET is switched on. The Zener diode clamps the gate of the

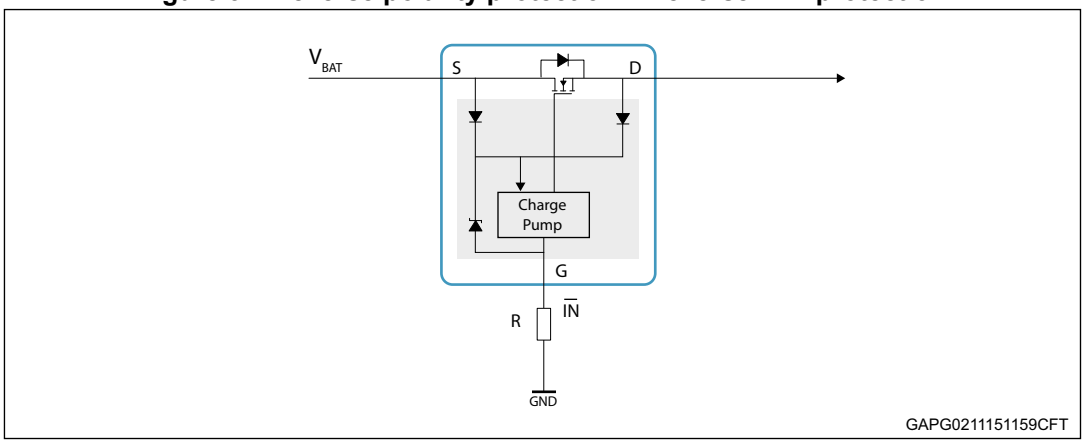
MOSFET to its Zener voltage in case of overvoltage on the battery track. In normal operation only the leakage current of the Z_{D1} Zener diode flows through R2 to GND. In order to minimize this current even at higher supply voltages, a diode with higher Zener voltage (i.e. 18V) may be chosen, however it shall be dimensioned to ensure that the Zener voltage is always kept safely below the maximum rated gate-source voltage V_{gs} of the P-channel MOSFET.

The resistor R2 limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging/discharging current of the gate. In addition, the resistor R2 together with the gate capacitance of the P-channel MOSFET determine the turn-off time when exposed to fast negative transients or abrupt reverse polarity according to LV 124: 2013-06 standard. 1 kΩ appears to be a good compromise between minimizing the charging/discharging current and ensuring a fast turn-off time. Due to the fact that the P-channel MOSFET carries also the load current, it needs to be properly dimensioned to handle the whole load current. A capacitor might be placed between the gate and the source of the P-channel MOSFET. The RC filter composed by R2 and C can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2004(E) pulse 1 test level IV, keeping the reverse polarity protection circuitry switched on.

3.2.3 Dedicated ST Reverse FET solution

The VN5R003H-E is a device made using STMicroelectronics' VIPower technology. It is intended to provide reverse battery protection to an electronic module. This device, which is composed of an N-channel MOSFET and its driver circuit, has two power pins (drain and source) and a control pin, $\overline{IN}$.

Figure 31. Reverse polarity protection – Reverse FET protection



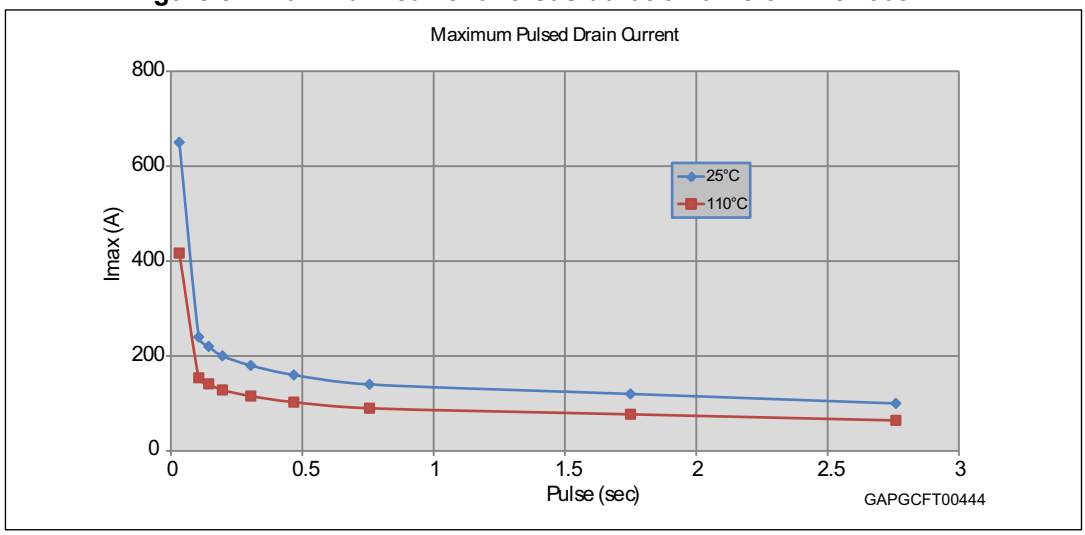
Note that a MOSFET has always an intrinsic anti-parallel body diode. If the $\overline{IN}$ voltage versus drain is negative, the device is turned on. The MOSFET is fully turned on when applying the battery voltage and the $\overline{IN}$ pin goes negative versus drain. Due to the fact that the source is at high potential, the MOSFET is a high-side switch not referring to ground; a charge pump circuit is needed to boost the gate voltage over the source voltage to turn the MOSFET on.

During reverse polarity of the battery, no voltage supplies the gate of the MOSFET which is automatically switched off. When $\overline{IN}$ is left open, the device is in OFF-state and behaves like a power diode between source and drain pins. The power losses of an N-channel MOSFET for reverse battery protection are determined by the $R_{DS,on}$ of the device and the load current. The diagram reported in *Figure 32* gives information about the safe operating area

as well as the maximum pulsed drain current that the device is able to handle during normal operation.

The VN5R003H-E is robust against “ISO 7637-2 2004 rev E” pulses in the configuration with $\overline{IN}$ pin grounded through a resistance R > 5 Ω.

Figure 32. Maximum current versus duration time of VN5R003H-E

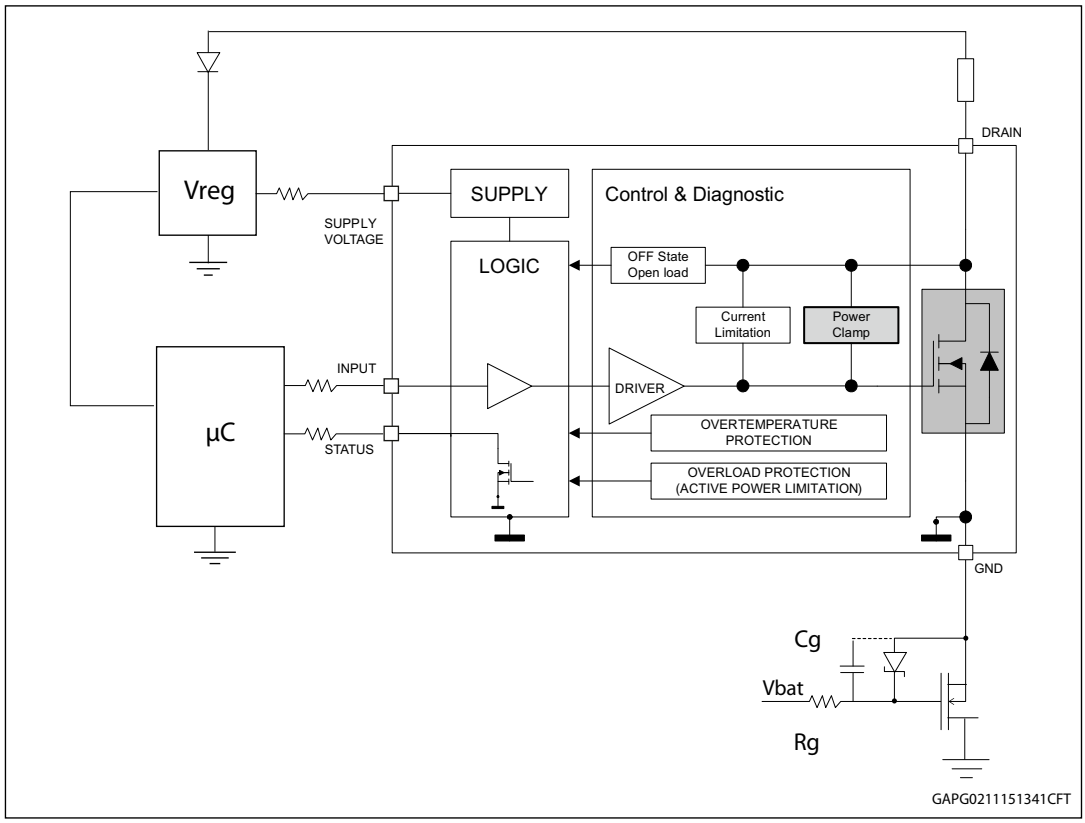


Note: PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: minimum pad lay-out and 2 cm^2

3.2.4 N-channel MOSFET in the ground line

The N-channel MOSFET is connected in a way that its gate is driven directly by the battery voltage and its drain is connected to ground.

Figure 33. Generic schematic and test setup with N-channel Power MOSFET in GND line



In normal conditions it is on, while in case of a reverse battery event it is switched off (because VGS ≤ 0) and it protects the LSD.

A Zener diode is placed between the Power MOSFET source and the gate to prevent gate oxide failure that may be caused when the maximum gate voltage value is exceeded.

The series resistor R_g limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging/discharging current of the gate.

This resistor together with the gate capacitance of the N-channel Power MOSFET determines the turn-off time when the module is exposed to fast negative transients or abrupt reverse polarity according to the LV 124: 2009-10 standards.

A good tentative value could be few tens of kΩ taking in account that a long turn-off time could cause high power dissipation for both the LSD and this N-channel Power MOSFET used as reverse battery.

A capacitor Cg might be placed between the gate and the source of the N-channel Power MOSFET. The RC filter composed by R_g and this C_g can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2011(E) pulse 1 test level IV, keeping the reverse polarity protection circuitry switched on. The time constant (R_g * C_g) must be longer than the pulse length (2 ms).

Either the breakdown voltage BVDSS of the N-channel Power MOSFET should be higher than the maximum negative transient peak voltage of ISO 7637:2-2011(E) or its energy capability in avalanche must be high enough to handle the transient pulse energy.

In normal battery conditions, the load current flows through the LSD and the N-channel Power MOSFET used for reverse battery. An N-channel Power MOSFET with $R_{DS,\ on}$ lower or identical to the LSD $R_{DS,\ o}$n is required to minimize the additional power dissipation caused by the reverse battery protection. Moreover the ground shift due to the reverse battery protection must be low enough to avoid undesired LSD switch off in case of high-current load transients.

3.3 OMNIFET III behavior in case of dynamic reverse battery

Tests have been carried out according to the LV124 specification:

Table 5. Test parameters E-15 reverse polarity - general

Parameter	Value
U	-14.0 V
R_i	< 100 mΩ
t	60 s(1)
Number of cycles	3 (the time between the pulses may be a maximum of 5 minutes)

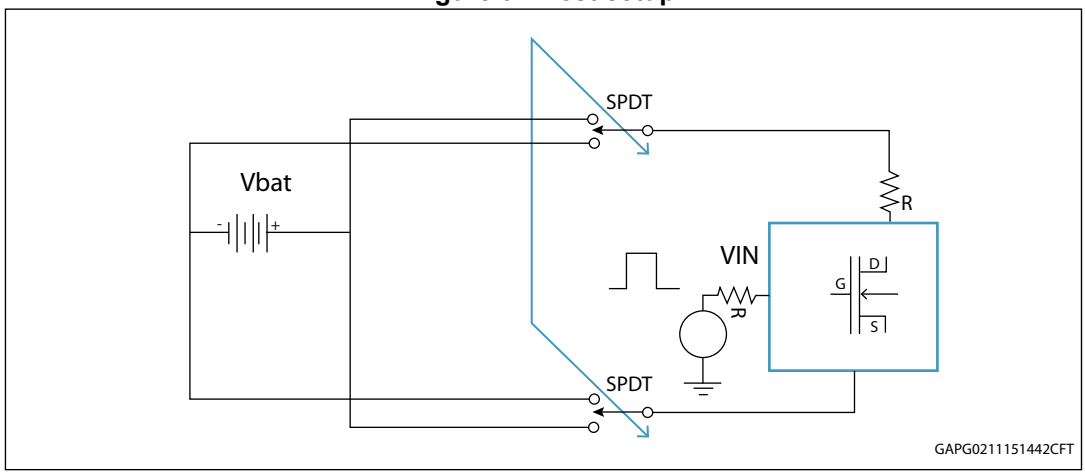
1. For a component in which the operating voltage is switched by means of a relay, the following applies deviating from the value mentioned above is 8 ms.

Test execution

- Device is turned on while drain-source voltage is positive (battery ground equal to device ground).
- Battery is reversed for 60 s; the current flows through the body diode and is limited by the external load.
- Battery is reversed back, device works in normal mode for 5 minutes before reversing the battery again.

Test setup

Figure 34. Test setup



The two switches (SPDT) are coupled. They allow applying reverse voltages across the D.U.T.

Test setup: V_{bat} = 14 V, T_{amb} = T_{room}.

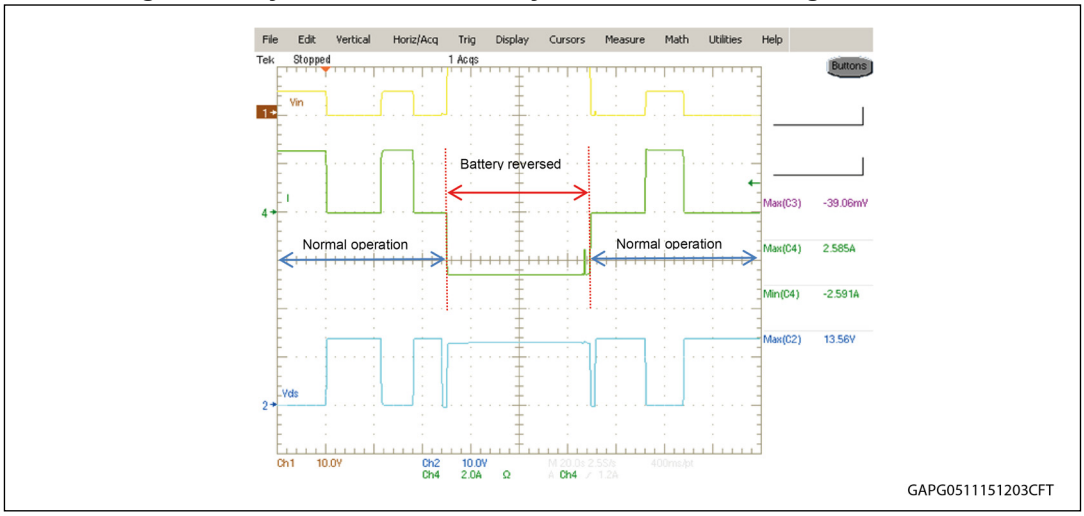
The device is mounted on a PowerSSO-12 PCB with footprint Cu heatsink area

Note: The OMNIFET drain voltage in the plot below is always referred to battery GND.

Example 1

Dynamic reverse battery applied to the VNL5030S5-E driving 21 W+10 W:

Figure 35. Dynamic reverse battery VNL5030S5-E driving 21 W+10 W



Case temperature measured through thermocouple at the end of the three consecutive cycles is around 140 °C. The D.U.T. keeps working normally once the reverse battery is removed.

4 Protection against transients on the battery line

4.1 Introduction on automotive electrical hazards

The automotive environment is a source of many electrical hazards. These hazards, such as electromagnetic interference, electrostatic discharges and other electrical disturbances are generated by various sources like ignition, relay contacts, alternator, injectors, SMPS (i.e. HID front lights) and other accessories. Since electronic modules are sensitive to electromagnetic disturbances (EMI), electrostatic discharges (ESD) and other electrical disturbances, caution must be taken when electronic modules are used in the automotive environment.

These hazards can occur directly in the wiring harness in case of conducted hazards, or can be applied indirectly to the electronic modules by radiation. These generated hazards can impact the electronics in two ways - either on the data lines or on the supply rail wires depending on the environment.

Several standards have been produced to model the electrical hazards that are currently found in automobiles. As a result, manufacturers and suppliers have to consider these standards and have to add protection devices to their modules to fulfill the major obligations imposed by these standards.

This chapter deals with the robustness of OMNIFETs submitted to ISO7637-2:2004 and ISO7637-2:2011 disturbances on the battery line and mounted in the typical application scheme.

4.2 Propagation of electrical hazards on the supply rail

Transients that are generated on the supply rail range mainly concern ISO7637-2 and ISO16750-2 standards.

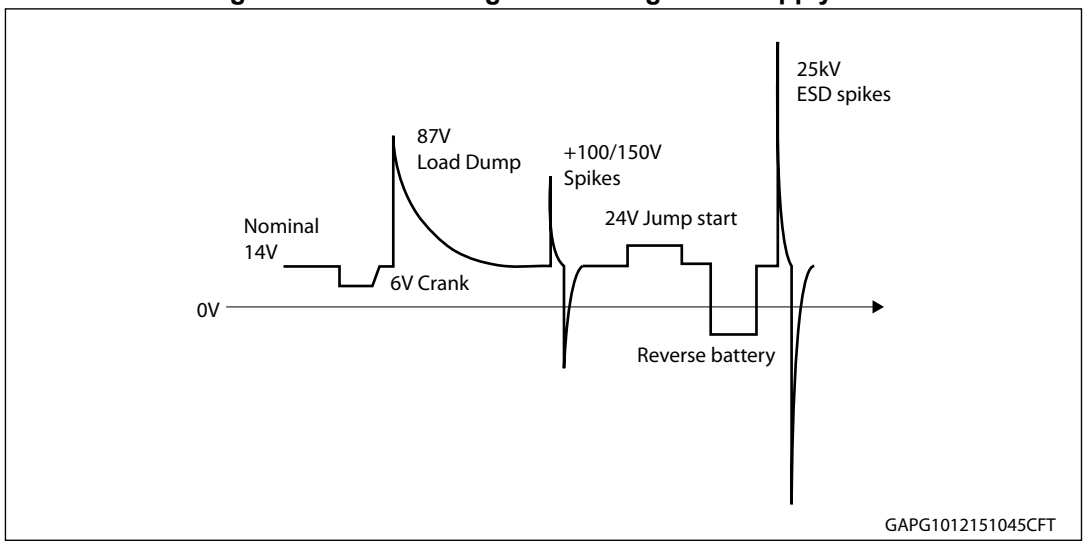
The most energetic transients are those resulting from load-dump and jump-start. But all other hazards may affect the normal operation of electronic modules.

The load-dump is caused when the discharged battery is disconnected from the alternator while the alternator is generating charging current. This transient can last 400 ms and the equivalent generator internal resistance is specified as 0.5 Ω minimum to 4 Ω maximum.

According to the ISO 7637-2 standard, the “+100 spikes” are due to the supply of sudden interruption of currents in a device connected in parallel with the D.U.T. caused by the inductance of the wiring harness, while the “-150 V spikes” are due to a supply disconnection from inductive loads.

This chapter deals with voltage transient pulses, as specified in the ISO 7637-2 standard.

Figure 36. Various surges occurring in the supply rail



4.3 Standard for the protection of automotive electronics

All hazards indicated above are described by several standards bodies such as the Society of automobile engineers (SAE), the Automotive electronic council (AEC) and the International standard organization (ISO).

The tests reported in this document were performed according to the ISO 7637-2 standard, editions 2004 and 2011, which are specified as follows.

Table 6. ISO 7637-2: 2004 (E)

ISO 7637-2: 2004(E) test pulse	Test levels		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and impedance
	III	IV		Min.	Max.	
1	-75 V	-100 V	5000 pulses	0.5s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b	+65 V	+87 V	1 pulse			400 ms, 2 Ω

Table 7. ISO 7637-2: 20011 (E)

Test pulse	Test pulse severity levels U_s			Min. number of pulses or test times	Burst cycle / pulse repetition time	
	IV	III	II/I		Min.	Max.
1	-150 V	-112 V	-75 V	500 pulses	0.5 s	
2a	+112 V	+55 V	+37 V	500 pulses	0.2 s	5 s
2b	+10 V	+10 V	+10 V	10 pulses	0.5 s	5 s
3a	-220 V	-165 V	-112 V	1 h	90 ms	100 ms
3b	+150 V	+112 V	+75 V	1 h	90 ms	100 ms

OMNIFET devices are compliant with the maximum pulses limit since these pulses are indirectly, by the load, transferred to the internal Power MOSFET able to manage the energy content of all pulses up to test pulse severity level IV. In case of load dump, all OMNIFET III are able to manage load dump level up to 40 V (Test pulse 5b).

5 OMNIFET dynamic behavior

5.1 Power loss calculation

The power loss calculation is an important step during the application design as it is a basis for further thermal considerations and PCB design.

This chapter is intended to provide guidelines for the calculation and the estimation of power dissipation in the device in combination with different types of loads (resistive, inductive, capacitive, etc.) and with different modes of operation (steady state, PWM).

All of the following evaluations are focused on power losses occuring in the Power MOSFET of the device. The power dissipation of the control logic, through V_{supply}, is in most cases negligible. If needed, it can be calculated from the external driver output voltage (V_S) and the device I_S.

Device control part power dissipation [W]:

Equation 5:

$$P_{CTRL} = V_{driver,max} \cdot (I_{S(max)} + (V_{driver,max} - V_{SCL(min)} / R_{supply,min}))$$

where V_{driver} is the output voltage of the external circuit that drives the OMNIFET.

This equation is valid for both 5-pin and 3-pin configurations since the power dissipation due to the IN pin is neglected.

5.1.1 Resistive loads

Conduction losses

The conduction losses are given by the power dissipation of the MOSFET switch due to the ON-state resistance (R_{ON}).

ON-state power dissipation [W]:

Equation 6:

$$P_{ON} = R_{ON} \cdot I^2_{OUT,RMS}$$

ON-state energy loss [J]:

Equation 7:

$$E_{ON} = P_{ON} \cdot Ton'$$

where Ton’ = ON-state duration

The R_{ON} parameter is dependent on temperature and on VIN. Relevant graphs are reported in the datasheet in order to extract the $R_{DS,\ on}$ value derating from the typical one (@ 25 °C, V_{IN} = 5 V).

The calculation of conduction losses in the PWM mode is based on a similar consideration as in the case of steady state losses (focusing on R_{ON}, I_{OUT}, t_{on}), however it is important to consider the right PWM on time (corrected with the turn-on/off switching delays and switching times) and right current in ON-state (for instance in case of bulb it depends on actual duty cycle):

Corrected duty cycle [-]:

Equation 8:

$$D_{COR} = D - \frac{t_{dON} - t_{dOFF} + twon}{t_{period}}$$

Where:

Equation 9:

$$D = \frac{t_{IN\_high}}{t_{period}} = \frac{Ton}{T}$$

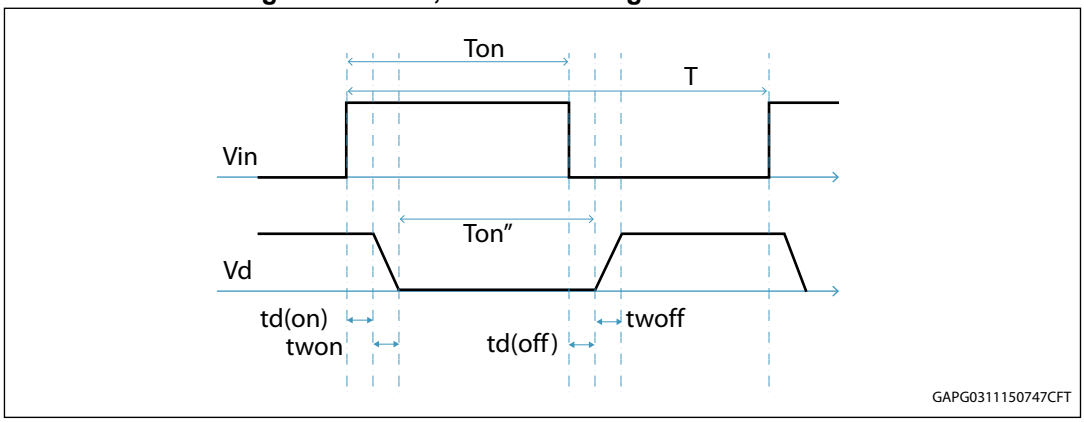
Duty cycle applied on input pin.

Equation 10:

$\frac{t_{dON}}{t_{dOFF}}[s]$: Turn on/off delay time

twon [s], twoff [s] called “Turn on/off switching time” are defined according to the following diagram:

Figure 37. twon, twoff switching times definition



Since the ON-state power dissipation [W] is:

Equation 11:

$$P_{ON} = R_{ON} \cdot I^2_{OUT(ON)}$$

Note: In case of bulb, the load current in ON-state depends on the actual duty cycle.

The average power dissipation [W] is:

Equation 12:

$$P_{AVG} = P_{ON} \cdot D_{COR}$$

Switching losses

The switching losses are important especially in PWM operation. Compared to conduction losses, the calculation depends on many factors like the load characteristics (resistive, capacitive or inductive), the device characteristics (switching times) and the environmental conditions (ambient, temperature, battery voltage).

This section deals with all kinds of resistive loads (such as bulbs, heating elements, etc.). The inductivity of wire harness is neglected (< 5 µH considered). The following calculations are simplified assuming the constant resistance of the load. However, it is applicable also for non-linear resistive loads (bulbs) driven in PWM mode. The PWM frequency is usually high enough (>50 Hz) to minimize the filament temperature (resistance) variation over the PWM period so it can be assumed as constant resistor.

The instantaneous power dissipation in the switch during the switching phase is equal to the drain-to-source voltage (V_{DS}) multiplied by the output (load) current (I_{OUT}). With given switching shapes and resistive load, the instantaneous power dissipation can be approximated by a triangular waveform assuming linear switching times.

Considering the resistive load and ideal linear switching times, the turn-on (turn-off) energy loss [J] is given by the following equation:

Equation 13:

$$E_{sw} = \frac{1}{6} \cdot \frac{V_{bat}^2}{R} \cdot (t_{WON} + t_{WOFF})$$

Then the total switching power dissipation is:

Equation 14:

$$P_{sw} = \frac{1}{6} \cdot \frac{V_{bat}^2}{R} \cdot (t_{WON} + t_{WOFF}) \cdot f$$

where (f) is the switching frequency and t_{WON} and t_{WOFF} are the switching times of the drain voltage calculated from 0% up to 100%, as per the diagram above.

Total power dissipation

The equations above give some information about switching losses; however it is suggested to measure the real power dissipation by checking the device operation in the required application.

The total OMNIFET power dissipation is given by:

Equation 15:

$$P_{diss} = Pd,on + Pd,s + P_{CTRL}$$

Then the junction temperature can be extracted by applying the following formula:

Equation 16:

$$DTj = Tj - Tjstart = Zthj,amb \cdot Pdiss$$

where T_{jstart} is the junction temperature just before the OMNIFET switches on.

The equation above can be used to extract either the average junction temperature or the increase in junction temperature in a given time window where $Z_{thj,amb}$ is chosen for the time of interest.

The thermal fitting model reported in the related datasheet can help to simulate the DTj for power dissipation in a given time window.

OMNIFET load compatibility

In case of resistive loads having a variable resistance such as bulbs whose value depends on the filament temperature, the device must be carefully selected.

Besides the above power dissipation considerations, module designers must verify that in the worst case environmental conditions (T_{amb}, V_{batt}) and in the worst case device (with either minimum or maximum relevant parameters), the device operation does not induce device degradation.

For such a specific case, device degradation can be induced by a DTj caused by a peak of power dissipation above 60 K, where this latter is given by:

Equation 17:

$$DTj = Iinrush \cdot Vds \cdot Zthj,amb(t,inrush)$$

Where Iinrush is the OMNIFET average current during the inrush phase, V_{DS} the following drain-source average voltage and the $Z_{thj,amb}$ is the one extracted for the entire duration of the inrush event (t,inrush). This comes from the integral of the above variables over the inrush time.

Here is the list of extreme cases to be considered and to be verified (12 V system) for the selection of the proper device for a given bulb load:

1. Normal condition:
   - V_{BAT}: 13.5 V
   - T_{case}: 25 °C
   - T_{bulb}: 25 °C
   - Requirement: None of the protection functions must be triggered.
2. Cold condition:
   - V_{BAT}: 16 V
   - T_{case}: 25 °C
   - T_{bulb}: -40 °C
   - Requirement: Max 20 ms of power limitation;
3. Hot condition:
   - V_{BAT}: 16 V
   - T_{case}: 85 °C
   - T_{bulb}: 25 °C
   - Requirement: Thermal shutdown cannot be triggered

Note: In all above conditions both $I_{limH,min}$ and $T_{sd,min}$ are considered.

The wire harness length plays a relevant role in the above calculations and it must be taken in account.

This chapter is intended to suggest drivers that can be used for typical automotive bulb loads or typical combinations of bulbs. The main consideration in case of bulbs, besides the steady state power dissipation, is the handling of the inrush current generated when starting up a cold filament.

A properly selected driver must allow safe turn-on of the bulb without any restrictions under normal conditions (environmental, bulb wattage). Under worst case conditions (high battery, low temperature, bulb tolerances, etc.) the driver should still be able to turn on the bulb even if some protection of the driver may be triggered temporarily. However, the long-term integrity of the drivers must not be jeopardized. Typical combinations of bulbs and M0-5 OMNIFETs (R_{ON} classes) are shown in the following table.

Table 8. Maximum bulbs combinations for given M0-5 R_{ON} class

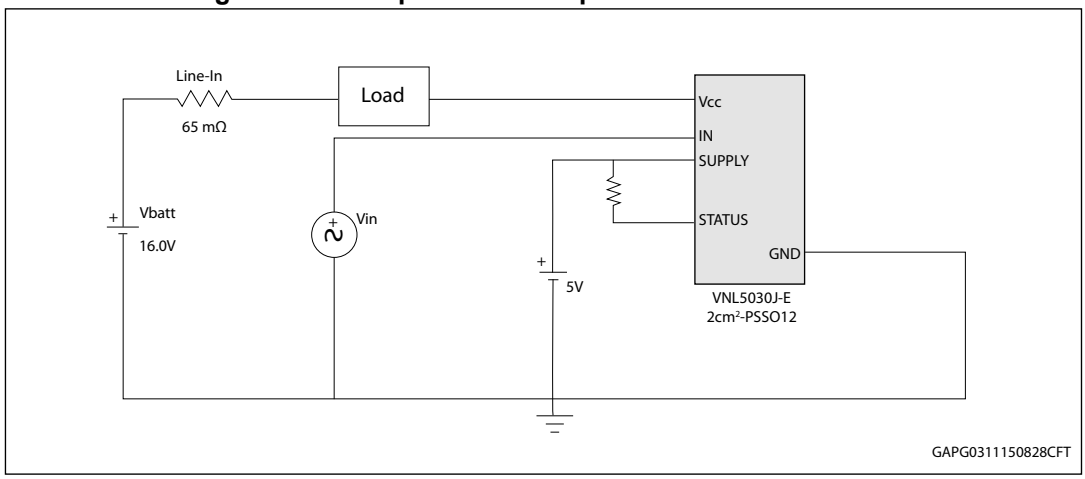
Device R_{DSON} class [mΩ]	Suggested bulb types and combinations (maximum loading)
30	4 x R10W (4 x 10 W)
50	6 x R5W (6 x 5 W)
90	3 x R5W (3 x 5 W)
160	2 x R5W (2 x 5 W)

Simulation example – VNL5030J-E with 4*10 W bulbs (40 W)

A simulation is performed in order to verify if the driver is able to turn on the bulb and matches the requirements under the defined conditions – see steps below.

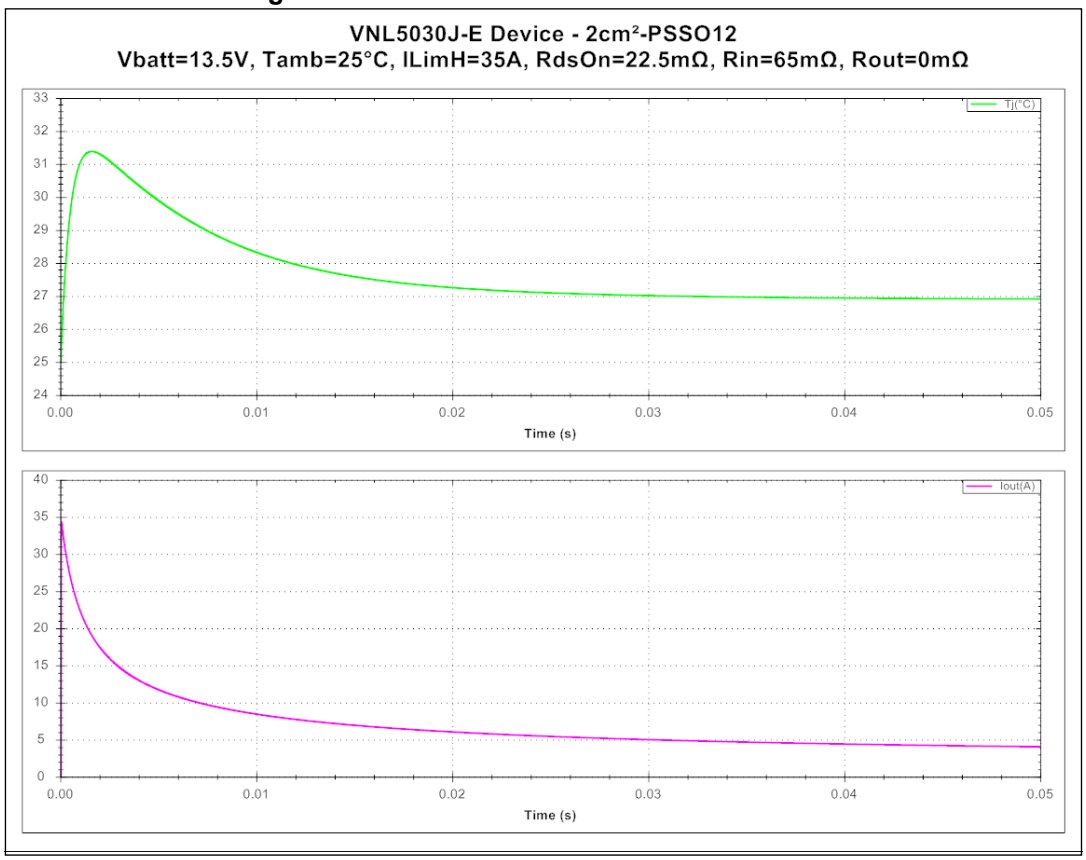
The tool used for this simulation is based on Matlab/Simulink.

Figure 38. Principle of the setup used for the simulation



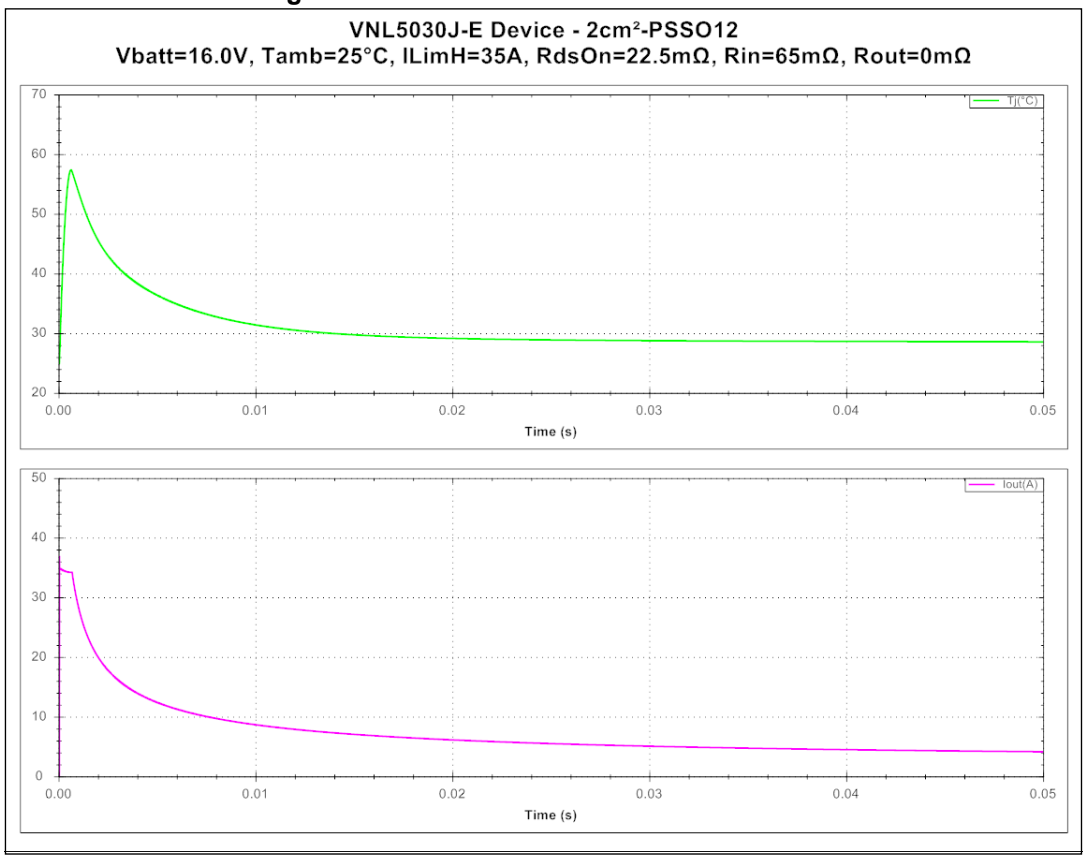
1. Normal condition:
   - V_{BAT}: 13.5 V
   - T_{case}: 25 °C
   - T_{bulb}: 25 °C
   - Requirement: none of the protection functions must be triggered.

Figure 39. Simulation result – Normal condition



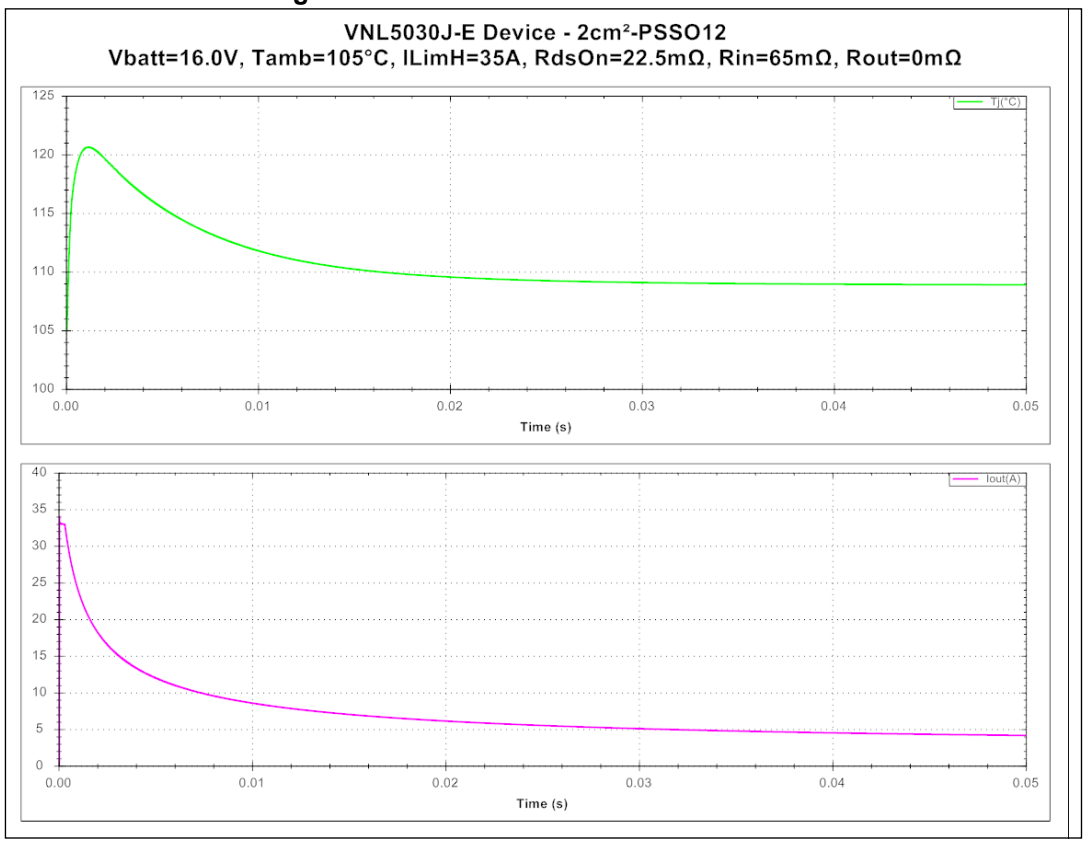
2. Cold condition:
   - V_{BAT}: 16 V
   - T_{case}: 25 °C
   - T_{bulb}: -40 °C
   - Requirement: power limitation allowed for durations of less than 20 ms.

Figure 40. Simulation result – cold condition



3. Hot condition:
   - V_{BAT}: 16 V
   - T_{case}: 105 °C
   - T_{bulb}: 25 °C
   - Requirement: thermal shutdown is allowed for a duration below 20 ms

Figure 41. Simulation result – hot condition



Conclusion**:**

The selected device is able to turn on a 4 x 10 W lamp under the conditions specified above without triggering the device protection functions (power limitation, thermal shutdown).

Note: The simulation example mentioned refers only to the inrush current at the turning on of a cold bulb. The steady state power dissipation and, in case that PWM is applied, the additional switching losses of the driver are still to be considered in order not to exceed the maximum possible power dissipation.

5.1.2 Capacitive loads

This chapter deals with the switching losses in combination with capacitive loads.

The capacitive characteristic of the load creates an inrush current at turn-on. This latter mainly depends on the load capacitance, the driver switching time and the load resistance (i.e. capacitor ESR). A typical requirement for the LSD in such applications is the ability to handle the worst case inrush current without activation of the thermal shutdown protection or with time-limited power limitation phase (< 20 ms).

Besides, the considerations regarding the inrush phase power dissipation which have been already made in case of resistive loads can be applied in case of capacitive loads.

The following measurements were performed on different part numbers (R_{DSON} classes) in order to determine the turn-on switching loss, the slew rate and the maximum possible capacitance value which do not trigger the device protection. The devices were loaded by

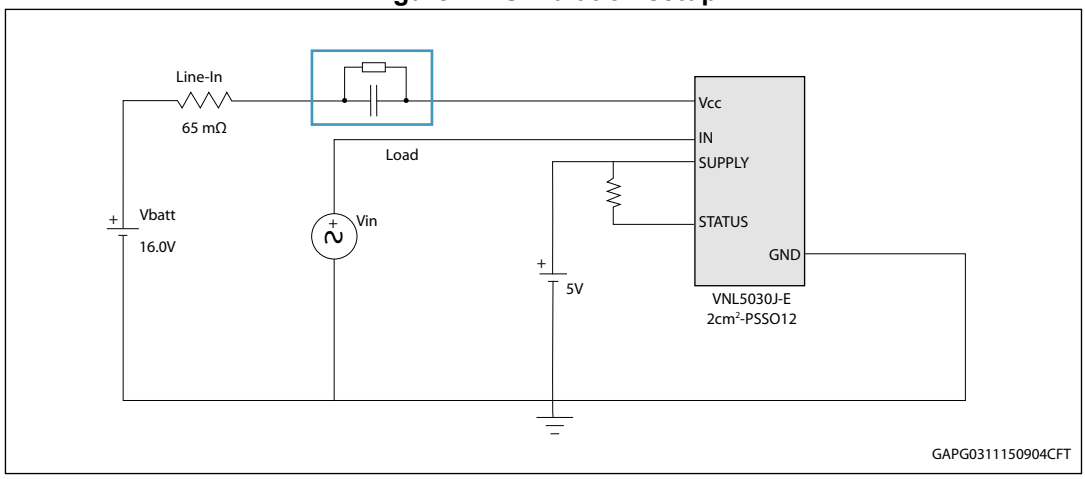
an electrolytic capacitor (or parallel combination of capacitors) and an 1 kΩ resistor in parallel.

Test conditions:

- V_{bat}: 16 V
- Temperature: 23 °C
- Device / Load:
  - VNL5030J-E, VNL5050S5-E, VNL5090S5-E, VNL5160S5-E, VNL5300S5-E
  - Capacitor value is increased until the thermal protection is triggered.

Setup:

Figure 42. Simulation setup



Tests have been performed with increasing capacitance values. The table below reports the first value of capacitance that triggers the device protection.

Example VNL5030J-E:

Figure 43. Example VNL5030J-E

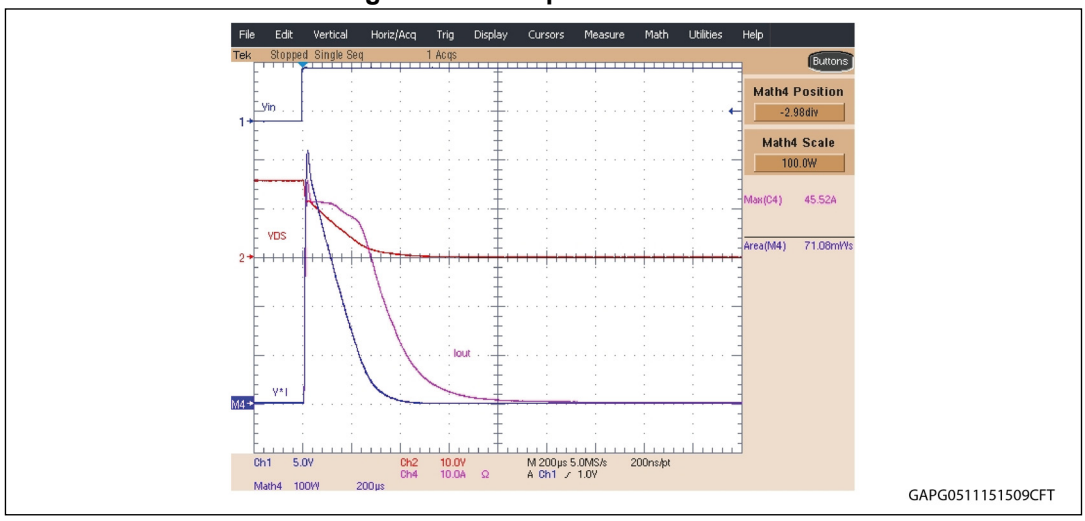


Table 9. Capacitance maximum value

Part number	Max. capacitance [µF] (safety margin applied)	Turn-on loss [mJ]
VNL5300S5-E	47	4.3
VNL5160S5-E	100	10.66
VNL5090S5-E	220	20.7
VNL5050S5-E	470	45.24
VNL5030J-E	1000	71

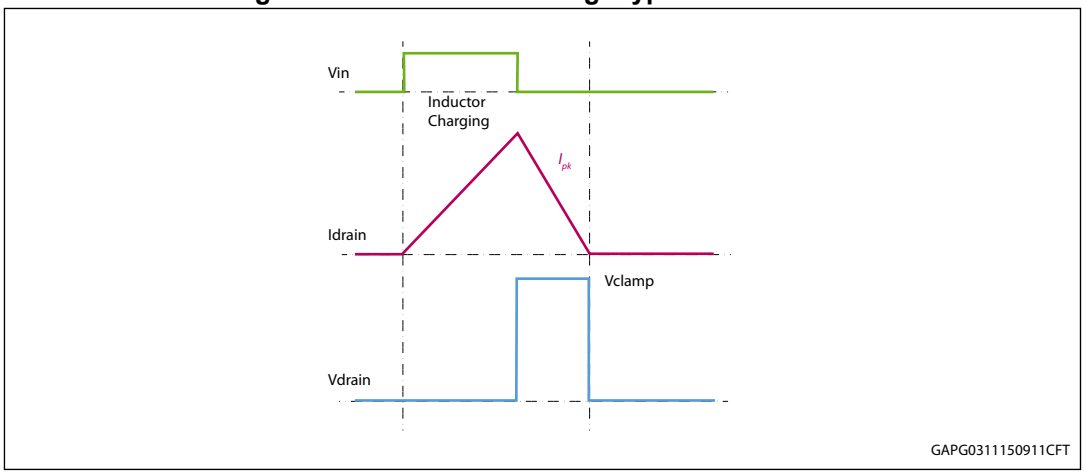
Note: The turn-off switching losses are not measured since they are negligible.

5.1.3 Inductive loads

LSDs have been designed to switch inductive loads such as relays, solenoids, motors, etc. The main design parameter to take in account is the ability of the chosen LSD to dissipate the energy stored in the inductive load.

LSDs have a relatively high output voltage clamping that leads to a fast demagnetization of the inductive load.

Figure 44. Inductive discharge typical waveforms



The aim of this chapter is to have a simple guide on how to check the conditions during demagnetization and how to select a proper LSD (and the external clamping if necessary) according to the given load.

Turn on

When an LSD switches on an inductive load, the current starts increasing with a time constant given by L/R values, so the nominal load current is not reached immediately.

Turn off

The LSD turn-off phase with inductive load is explained by the waveforms in the figure above. The inductance reverses the voltage across it in order to keep the current in the same direction.

The load current decays exponentially (linearly if $R \rightarrow 0$) and reaches zero when all the energy stored in the inductor is dissipated in the LSD and the load resistance.

External clamping circuitry (i.e. a freewheeling diode) could be used to protect the LSD in case the demagnetization energy exceeds the energy capability of the device. By using a standard freewheeling diode, the demagnetization voltage is reduced from V_{clamp} - V_{batt} to approximately 1 V. This has an influence on the demagnetization time (lowering $|V_{DEMAG}|$ $\Rightarrow$ increasing T_{DEMAG}).

Calculation of dissipated energy

As previously mentioned, a typical characteristic of inductive loads is to maintain the direction and value of the actual current flow. Applying nominal voltage on inductive load (turn-on), it takes a certain time (depending on time constant τ = L/R) to reach nominal current.

Removing the voltage source from the inductive load (turn-off), the load inductance tends to continue to drive the current via any available path (i.e. clamp of the LSD) by reversing its voltage (acts as a source) until the stored energy (E_L = 1/2 L I_O^2) is dissipated.

The time needed to dissipate this energy is called demagnetization time (T_{DEMAG}). This time is strongly dependent on the voltage across the load (V_{DEMAG} = V_{clamp} - V_{batt}) at which the demagnetization is performed (higher $|V_{DEMAG}| \Rightarrow$ shorter T_{DEMAG}). A typical V_{CLAMP} for M0-5 OMNIFET is 46 V.

The power dissipated (P_{diss}) by a device that drives an inductive load at given V_{batt}, I_{load} and load characteristics is the following:

Equation 18:

$$Pdiss = Pd,on + Pd,sw$$

in case of external freewheeling when the entire load energy is dissipated outside the OMNIFET.

It becomes:

Equation 19:

$$Pdiss = Pd,on + Pd,demag$$

without freewheeling.

Here below are simple formulas that help to calculate the above terms.

Switching power loss [J]:

Equation 20:

$$Pd,sw = \left(\frac{1}{2}\right) \cdot Vbatt \cdot (tr + tf) \cdot Iload \cdot f$$

This equation is applicable in the case of load current freewheels on external clamp.

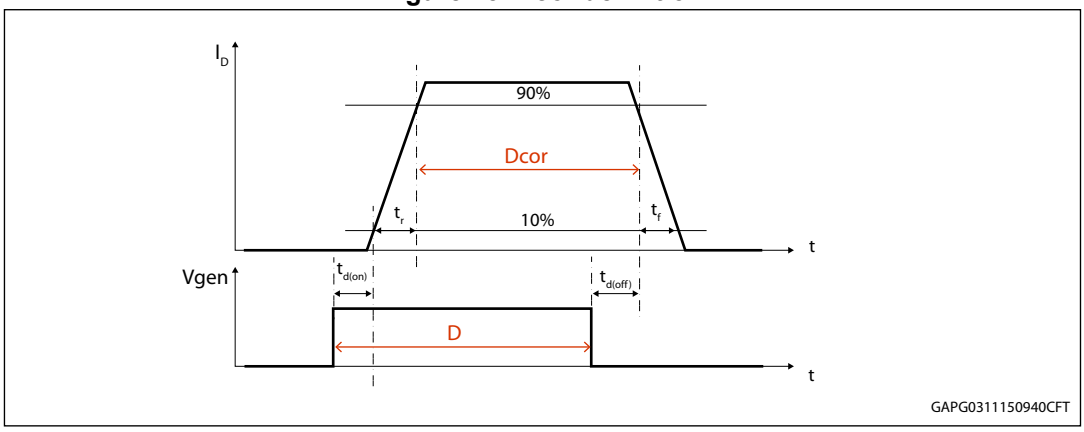
tr, tf are the switching times assumed linear; (f) is the frequency and I_{load} is assumed constant during the entire ON-time. This latter sentence means that current ripple is small with respect to the average load current (I_{load}).

Equation 21:

$$Pd,on = Rds,on \cdot Iload^2 \cdot Dcor$$

where Dcor is the device output duty cycle. This is different from the duty cycle at the IN pin because of the delay and switching times of the device.

Figure 45. Dcor definition



The energy loss during the demagnetization phase [J] is given by:

Equation 22:

$$E_{demag} = \frac{V_{clamp}}{R} \cdot L \cdot I_0 \cdot \left(1 - k \cdot \ln(1 + \frac{1}{k})\right)$$

where

Equation 23:

$k = V_{demag}/(I_0 * R)$

Then

Equation 24:

$P,demag = E_{demag} * f$

The E_{demag} mentioned above comes from the following equation.

The energy dissipated in the low-side driver is given by the integral of the actual power on the MOSFET through the demagnetization time:

Equation 25:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt$$

To integrate the formula above we need to know the current response $i_{OUT}(t)$ and the demagnetization time T_{DEMAG}. The $I_{OUT}(t)$ can be obtained from the well-known formula of R/L circuit current response using the initial current I_0 and the final current V_{DEMAG}/R where $V_{DEMAG} = V_{clamp} - V_{batt}$ considering $i_{OUT} \geq 0$ condition:

Equation 26:

$$i_{OUT}(t) = I_0 - \left(I_0 + \frac{|V_{DEMAG}|}{R}\right) \cdot \left(1 - e^{\frac{-t \cdot R}{L}}\right) \qquad (0 < t < t_{demag} \Rightarrow i_{OUT} \geq 0)$$

Putting i(t) = 0 we can calculate the demagnetization time:

Equation 27:

$$T_{DEMAG} = \frac{L}{R} \cdot \ln\left(1 + \frac{1}{k}\right)$$

where L = load inductance, R = load resistance and I_0 = load current at the beginning of turn off event, $k = V_{DEMAG} / (I_0 * R)$

Equation 28:

$$\lim_{R \to 0} T_{DEMAG} = L \cdot \frac{I_0}{V_{DEMAG}} \qquad (\text{simplified for } R \to 0)$$

Substituting the T_{DEMAG} and $i_{OUT}(t)$ by the formulas above we can calculate the energy dissipated in the LSD**:**

Equation 29:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt = \int_0^{T_{DEMAG}} Vclamp \cdot i_{OUT}(t)dt$$

Equation 30:

$$E_{Demag} = \frac{1}{2} \cdot L \cdot I_0^2 \cdot \frac{V_{clamp}}{V_{clamp} - Vbatt} \qquad (\text{simplified for } R \to 0)$$

Device selection criterion with reference to I-L plot

Even if the device is internally protected against breakdown during the demagnetization phase, the energy capability has to be taken into account during the design of the application.

Two main mechanisms that can lead to premature device failure can be identified:

- Hot spot creation: the temperature during the demagnetization rises quickly (depending on the inductance) and the uneven energy distribution on the power surface can cause a hot spot, leading to device failure.
- Fast thermal fatigue: as in normal operation, the life time of the device is affected by fast thermal variation as described by the Coffin-Manson law. Repetitive demagnetization events with thermal variation exceeding 60 K cause shorter component lifetime due to thermal fatigue.

These considerations lead to two simple design rules:

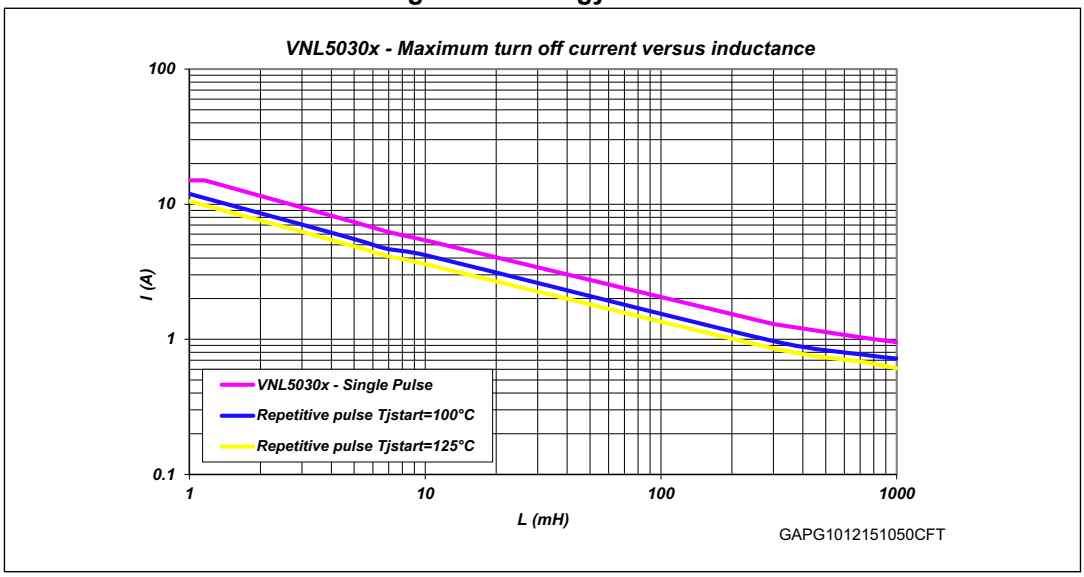
- The demagnetization energy has to be below the energy limit that the device can withstand at a given inductance.
- In case of a repetitive pulse, the average temperature variation of the device should not exceed 60 K at turn-off.

To fulfill these rules the module designer has to calculate the energy dissipated in the LSD at turn-off and then compare this number with the datasheet values.

Here is the suggested procedure in order to check if the chosen device is suitable to drive the required load.

1. Based on the load characteristics and application conditions (I_0) it is possible to calculate: T_{DEMAG}(app), E_{DEMAG}(app) by the above equations
2. Based on the LSD under evaluation, it is possible, at the given required load current I_0, to mark for few points in the repetitive pulse curve (curve c), both $E_{DEMAG,max}$(dev)i and T_{DEMAG}(dev)i thanks to the above equations
3. Then, it is possible to find out the point in the datasheet curve where T_{DEMAG}(app) = T_{DEMAG}(dev)i. On this point, the $E_{DEMAG,max}$(dev)i MUST be above E_{DEMAG}(app).

Figure 46. Energy curves



The energy limit given by the “single pulse” curve is intended for device operation with “rare” energy discharge events, while the “repetitive curve” limits are intended for continuous operation of the device in demagnetization. In other words a “single pulse” energy discharge

could cause the device degradation that could reduce the device lifetime. It is recommended to never exceed this value.

These curves are based on extensive characterization tests and on device thermal modeling. “Repetitive curves” are built based on two constraints:

1. The device temperature increase during the demagnetization phase must be lower than 60 K;
2. The maximum Power MOSFET junction temperature, assuming a uniform junction temperature distribution, during demagnetization phase must be below 160 °C.

6 ESD protection

6.1 EMC requirements for ESD at module level

An electrostatic discharge (ESD) pulse on any ECU connector pin is an expected event during a vehicle life. A transfer of discharge when a person approaches the ECU (for example during maintenance, reparation or installation) is a typical event that could damage the ECU and in particular an IC whose pins are connected to the outside environment.

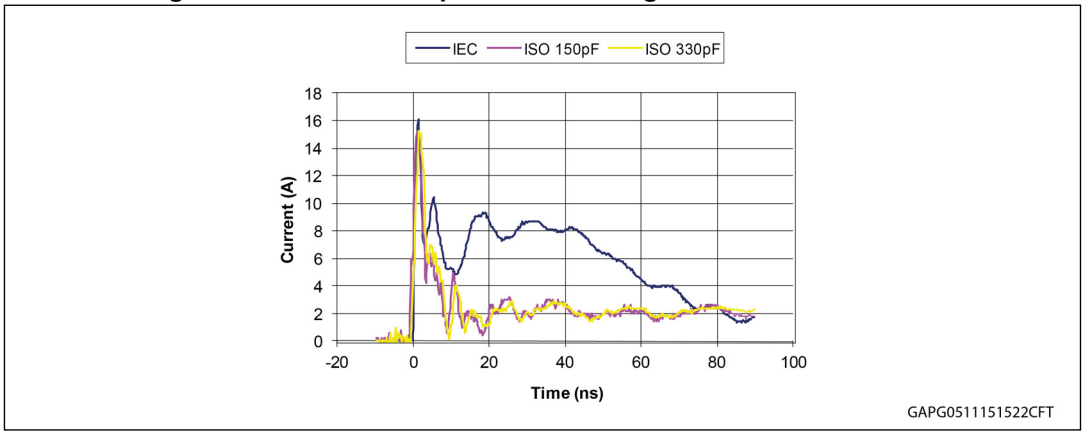
Standards and limits are applied in order to simulate those events. Limits strongly depend on the car manufacturer and on the specific load. Some international standards for testing schemes and requirements have been introduced for the electrical systems such as car modules. They include IEC 61000-4-2 and the automotive standard ISO 10605.

The two standards use different values for the C/R components. IEC 61000-4-2 uses a 330 Ω resistor and a 150 pF capacitor. ISO 10605 uses a 2000 Ω resistor, but different capacitors depending on conditions. A 150 pF capacitor is used to simulate a person reaching an automobile (for example a module load repair or change can be reproduced by this standard). A 330 pF capacitor is used to simulate ESD events for a person sitting in the passenger seat of a vehicle.

ESD pulses consist of two components:

- A capacitive component, characterized by a peak current that lasts a few nanoseconds, which strongly depends on the distributed capacitance of the ESD simulator body.
- A resistive component whose value is defined by the RC content of the standard used (see *Figure 47*).

Figure 47. ESD current pulses according to different standards



The typical ESD requirements of car manufacturers at module level are the following:

1. Module not powered during the test.

   This test simulates any possible handling of the module prior to being assembled in the car.

   Connector pins to test are normally those that go out of the module

   – Supply pins protected and/or filtered as per datasheet
   – Output pins protected and/or filtered as per typical design practice (e.g. ceramic capacitor)

   Standard applied is the ESD HBM Automotive acc. IEC61000-4-2 (150 pF/330 Ω).

   Required acceptance limits are in the range of ±4 kV to ±8 kV (contact discharge).

   Test execution requires a sequence of 3 to 5 ESD pulses applied with fixed delay time (1 s, typically). Pulses are applied either by touching the pin under test with the ESD gun (contact discharge) or without touching it (air discharge).The test is passed if no pin-to-pin I/V characteristic degradation is determined after exposure to the pulses. In some cases extra tests with a modified HBM network (for example 150 pF/2 kΩ) contact discharge are required.

2. Module powered during the test

   This test normally simulates any possible stress that could be applied to the connector pins with module already assembled in car.

   The standard typically applied is the ISO10605 (330 pF/2 kΩ).

   Acceptance limits are in the ± 8 kV range (contact discharge) and ± 15 kV (air discharge).

   In some cases, if higher pulse level is required, the applied network changes in (150 pF/2 kΩ).

   Test execution requires a sequence of 3-5 ESD pulses applied with fixed delay time. A real car battery must be used.

   The module must be inserted in a test environment that simulates the environment inside the car. It is normally ESD tested in real configuration (load on, load off, driver in PWM, etc).

   ESD pulses are applied to the pins that go out of the module such as outputs, transceiver pins, etc.

   The test is passed if no pin-to-pin I/V characteristic degradation is determined after pulse exposure.

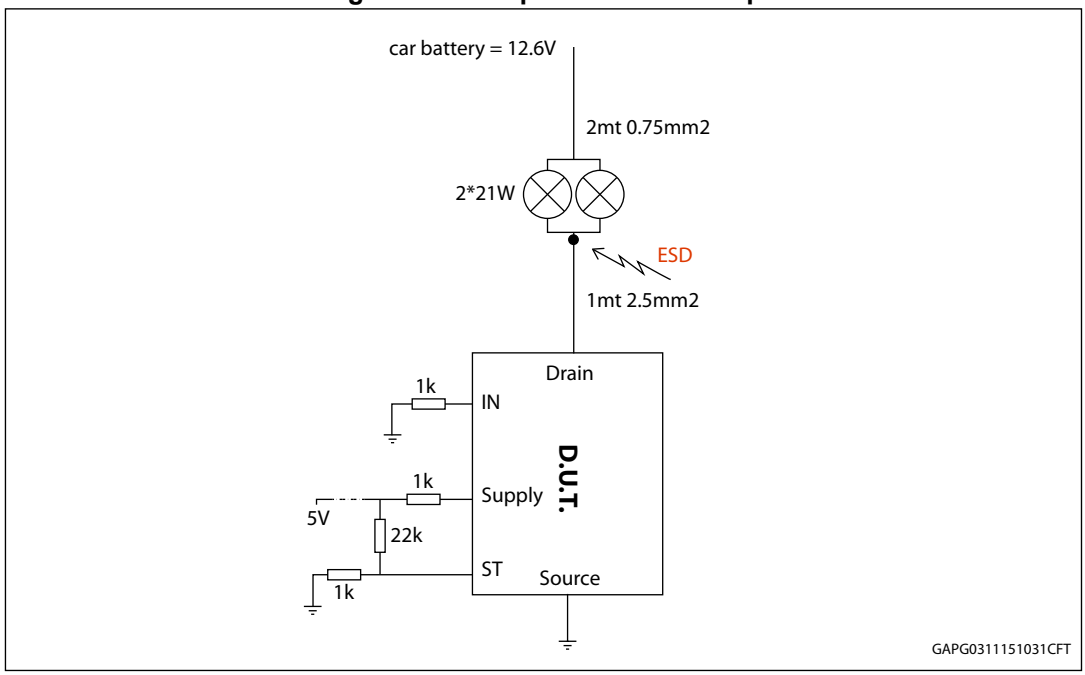
   ESD pulses are applied between the pin under test and module ground connected to the ESD GND plane by a minimum wire.

   Some variability of the ESD has been demonstrated. The main causes of such variability are in general the environmental conditions (mainly humidity), the ESD simulator pulse spread (specifically of the initial current pulse) and the test execution as well.

   The OMNIFET III devices are characterized with powered and unpowered module ESD tests.

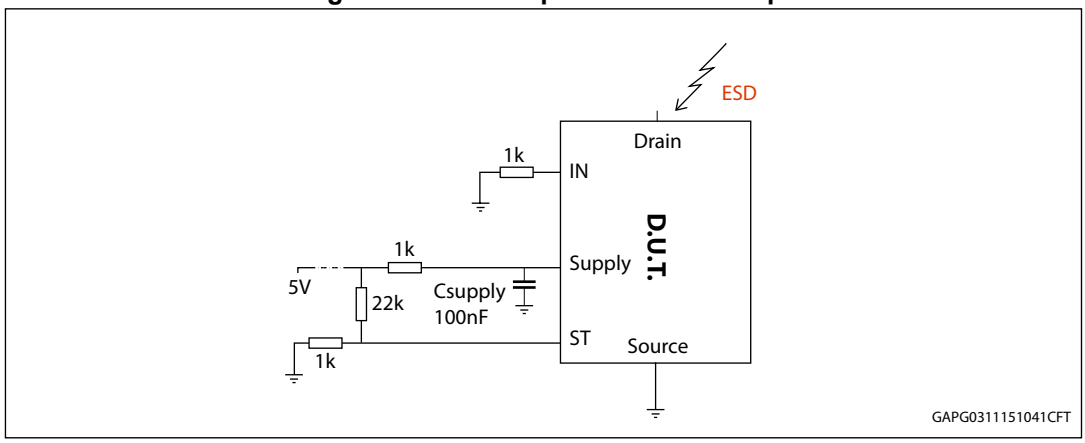
   The powered test setup is shown in *Figure 48*.

Figure 48. ESD powered test setup



The test setup with ESD un-powered is shown in *Figure 49*.

Figure 49. ESD un-powered test setup



The wire length between V_{bat} and DUT V_{CC} and between board GND and ESD ground plane is minimized. ESD simulator ground is identical to battery ground. Both are connected on GND plane.

D.U.T. board is placed above GND plane by means of 50 mm thick insulating support; filtering ceramic (X7R series) capacitors are placed on V_{CC} and on outputs.

D.U.T. outputs not loaded for un-powered test, loaded for powered test; for un-powered module tests, the supply voltage is not present and the device signal pins are connected to GND via the commonly-used protection resistances.

Test conditions:

V_{bat} from real car battery = 12.6 V (for powered module test only);

Room temperature;

Test execution:

Tests are performed on two typical device configurations. For powered module test:

- Device on
- Device off

ESD discharges are applied on output board trace.

Test procedure:

- Incremental discharge voltage levels from 1 kV up to 30 kV are applied with 1 kV voltage step
- 5 discharges on discharge pad OUTx with delay time of 1 s are applied
- Failure test by I/V curve check
- Previous points are repeated until failure (if any)

Device performances are guaranteed by margin to failure reported during characterization.

The test is performed on specific ESD test boards where general ESD layout rules are applied.

The ESD characterization has demonstrated the capability of OMNIFET III devices to pass the ESD levels normally required with a minimum filtering cap (10 nF). This capacitor must be placed as close as possible to the ESD stress injecting point (e.g. the connector). The following results are reported:

Table 10. ESD test results

OMNIFET III ESD results	ESD at module level (powered). Standard ISO10605 (330 pF/2 kΩ	ESD at module level (un-powered) Standard IEC61000-4-2 (150 pF/330 Ω)
Sustained ESD pulse level	> |+/-8 kV|	> |+/-8 kV|

6.2 EMC requirements for ESD at device level

ESD tests for electrical components such as integrated circuits include:

- Human Body Model (HBM)
- Charged Device Model (CDM)

Those ESD test methods for integrated circuits are intended to ensure that the circuits can be safely handled in an ESD-controlled environment during manufacture.

HBM

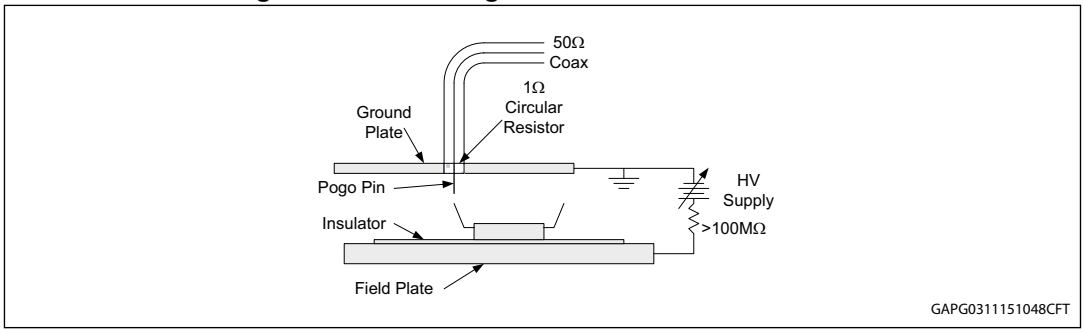
This is intended to simulate a charged person touching an integrated circuit. A person has approximately 100 pF of capacitance; skin and body resistance limit the current during a discharge. HBM tests results, according to JEDEC 22A-114F and CDM-AEC-Q100-011, are reported in the M0-5 OMNIFET datasheet “*Absolute maximum ratings”* section.

CDM

This test (CDM-AEC-Q100-011) emulates an integrated circuit which becomes charged and then discharges when touching a grounded metal surface. There is no fixed value of a capacitor to discharge; the capacitance to be charged is the capacitance of the integrated circuit to its surroundings. The discharge path, consisting only of the circuit's pin and the arc formed between pin and the metal surface, has very little impedance to limit current.

In the field induced CDM, the most popular implementation, the integrated circuit is placed pins up, on top of a field plate, with only a thin insulator between the circuit and the field plate. The thin space between the circuit and the field plate creates a capacitance whose value depends on the size of the integrated circuit and the package geometry. A ground plane is positioned by a pogo pin over the field plate as shown in *Figure 50*.

Figure 50. ESD charge device model test scheme



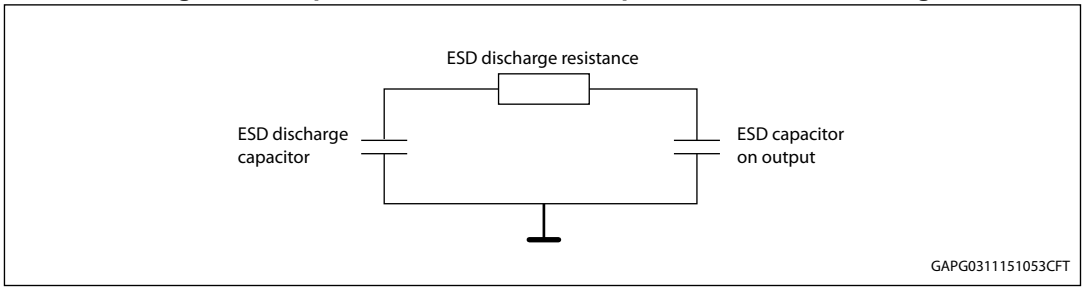
To perform the CDM test, an uncharged circuit is placed on the field plate. The field plate is charged to a high voltage and the circuit's potential tracks the field plate. The ground plane is then moved so that the pogo pin touches the integrated circuit, grounding it. The result is a very fast redistribution of charge between the field plate to ground plate capacitance and the integrated circuit to field plate capacitances. 500 V is the commonly used value.

Results relevant to CDM-AEC-Q100-011 are reported in M0-5 OMNIFET datasheet "*Absolute maximum ratings*" section.

6.3 Design and layout basic suggestions to increase ESD failure point level

When the ESD pulse level required to be passed exceeds the standalone device capability, the device needs external protection. The easiest design practice is the use of a ceramic capacitor on the output. The purpose of the capacitor is to limit the voltage and then the energy discharged into the device. This external capacitor is in parallel with the internal ESD pulse one (see below).

Figure 51. Equivalent circuit for ESD protection dimensioning



A preliminary estimation of the capacitor value can be obtained by applying the following formula:

Equation 31:

$$V_{Final} = V_{ESD} \times \left(\frac{C_{ESD}}{(C_{ESD} + C_{EXT})} \right)$$

Where V_{ESD} is the ESD pulse level required, C_{ESD} is the ESD simulator capacitor value and V_{Final} is the maximum allowed voltage across the device (typically around 45 V).

It is in any case necessary to verify the choice of the external capacitor, given by the formula above, by means of a real test. The main reason for this is the behavior of the capacitor impedance over the frequency. More specifically, since an ESD pulse has frequency content in the range of hundreds of MHz the capacitive value of a real capacitor is lower than a theoretical one.

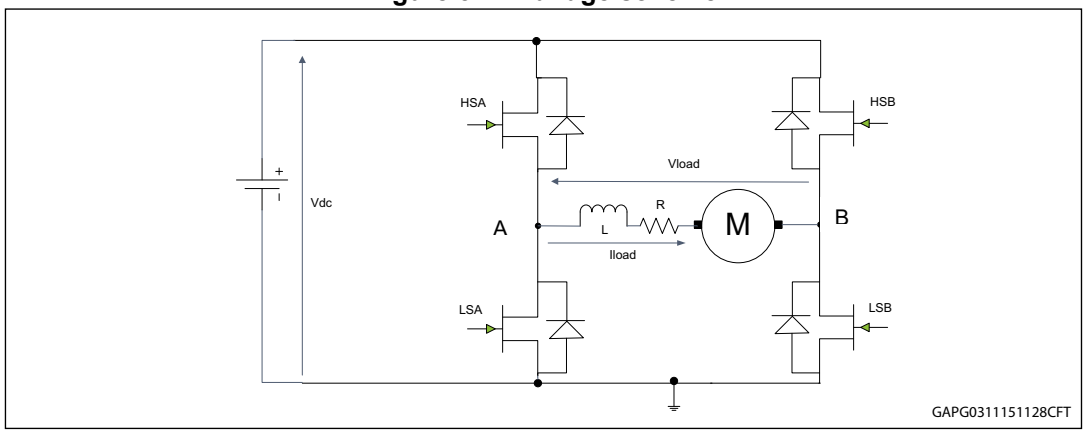
The ESD pulse destruction point strongly depends on the module layout. In order to make the module pass the required stress level, it is recommended to add a ceramic capacitor to the output close to the connector whose value should be in the range of tens of nF. This capacitor decreases both the applied voltage gradient and the maximum output voltage seen by the LSD.

7 Usage in “H-bridge” configurations

7.1 Introduction

The term H-bridge refers to the typical graphical representation of such a circuit. An H-bridge is built with four switches (solid-state or mechanical). Two of them are connected between the battery and the load (high-side switches), the other two between the load and the ground (low-side switches). When the HSA and LSB switches (see *Figure 52*, which shows an H-bridge circuit with four MOSFETs driving a bidirectional DC motor) are closed (and HSB and LSA are open) a positive voltage is applied across the motor. By opening the HSA and LSB switches and closing the HSB and LSA switches, this voltage is reversed, allowing reverse operation of the motor.

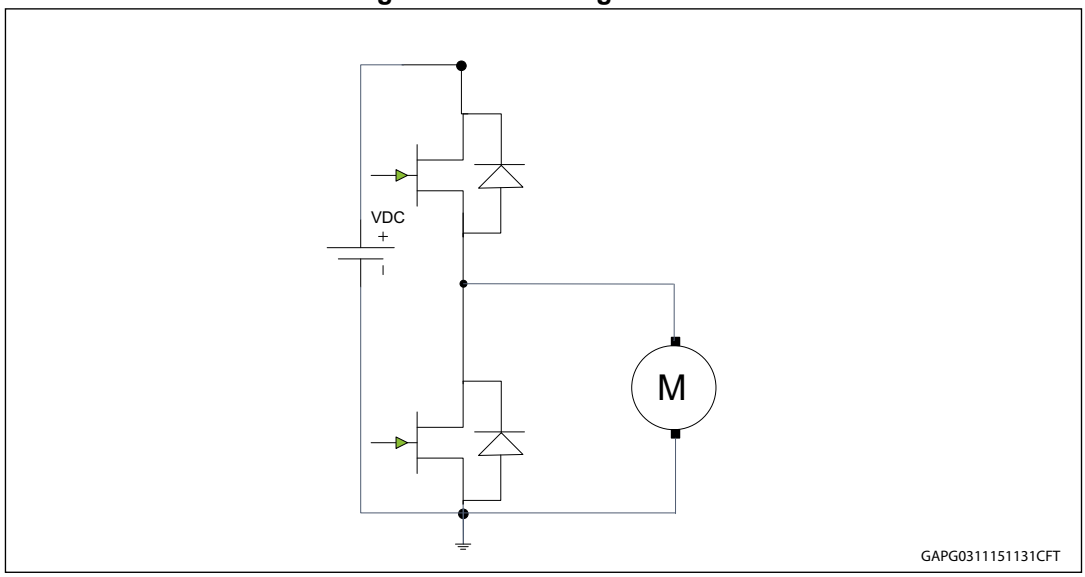
Figure 52. H-bridge scheme



Using the above nomenclature, the HSA and LSA switches, or HSB and LSB, must never be closed at the same time, because this creates a short-circuit via the so-called cross-conduction.

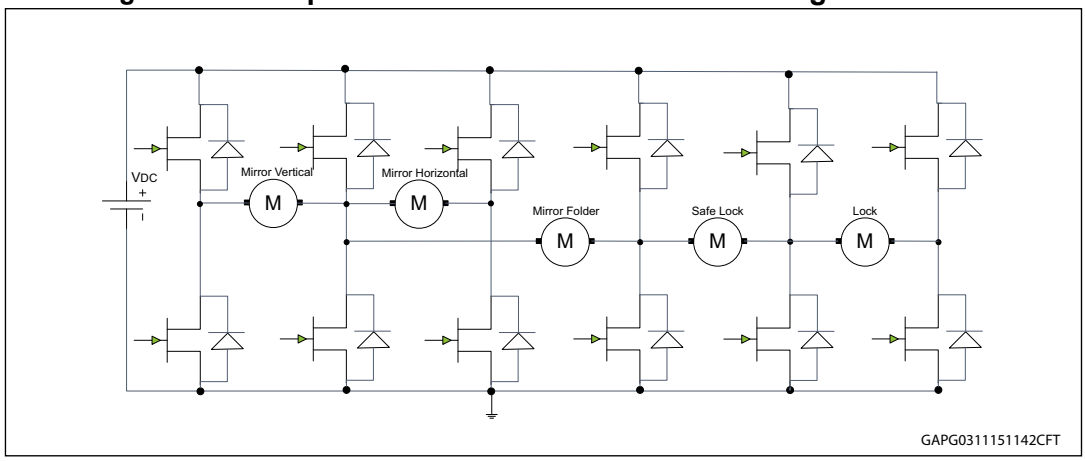
A simpler configuration, called half-bridge, consists of a single high-side driver which supplies or disconnects the battery, the load itself which is directly grounded and a low-side driver in parallel to the load (normally inductive), which is activated only to connect the load to ground. The low-side driver in this way absorbs the inductive energy which otherwise would be completely discharged through the high-side driver, by a consequent fast discharge which does not allow a peak and hold load control. In case of a DC-motor, the low-side driver, when turned on after having turned the high-side driver off, brakes the motor safely to ground and stops its rotation.

Figure 53. Half-bridge scheme



Several half-bridges can be connected together in order to drive many loads in cascaded configurations (see *Figure 54*, which describes an example of an automobile front door system with a total of five motors).

Figure 54. Example of automobile multi-motor driving connection



7.2 M0-5 low-side drivers in “H-bridges”: specific considerations

The M0-5 low-side drivers can be used to drive various bidirectional loads in H-bridge configuration. Some general guidelines must be followed for proper usage. An overview of some potential issues is given in the following paragraphs.

7.2.1 Short-circuit event to ground and to battery

In case of short-circuit of one output of the H-bridges (for instance, “A” as per *Figure 52*) to battery, the M0-5 OMNIFET protects the H-bridge thanks to its protection features (current limitation, power limitation and thermal shutdown). The status pin is pulled low to signal the overtemperature condition.

In case of short of one of the H-bridge legs, either A or B, to GND, the H-bridge needs either a fully protected high-side driver (for example M0-7 high-side driver) or drain-source monitoring of the high-side driver by a microcontroller to prevent failure of the Power MOSFET.

7.2.2 Cross current events

Cross conduction due to MOS delay times

A common issue which can affect one leg, either A or B, of an H-bridge occurs when both HSD and LSD are turned on at the same time. This condition, called cross-conduction, causes significant extra power dissipation in both switches which can become critical especially during PWM operation.

For instance, when the HSD is turned off and the LSD is turned on (e.g. in order to change motor direction), propagation delays and the time required to discharge and charge respectively the HSD and LSD gate capacitances can cause the HSD to remain partially on when the LSD is already turned on.

Here is a practical example where a VND7012AY (12 mΩ, M0-7 high-side driver) is used in combination with two VNL5030S5-E to build an H-bridge. For the sake of simplicity, a resistive load of 4.5 Ω is driven. The HSD_0 and LSD_0 on the left leg are driven complementary with a PWM signal and with different delay times between switching off of the HSD_0 and switching on of the LSD_0. In order to see the effect of the cross-conduction and how it can be attenuated or eliminated, a delay has to be introduced. Current in LSD_0 is plotted.

Figure 55. H-Bridge configuration

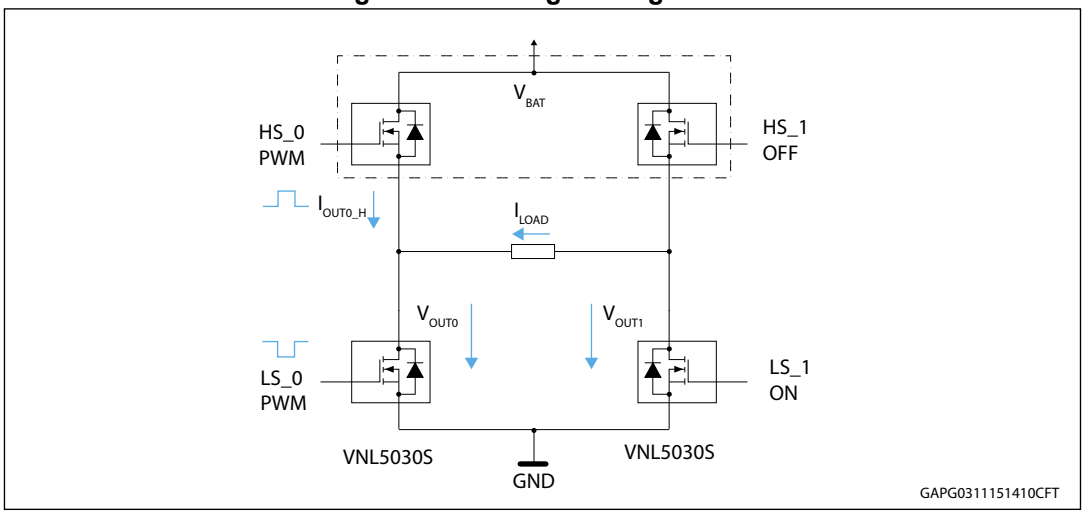


Figure 56. 50 µs delay between HS0 off and LS0 on

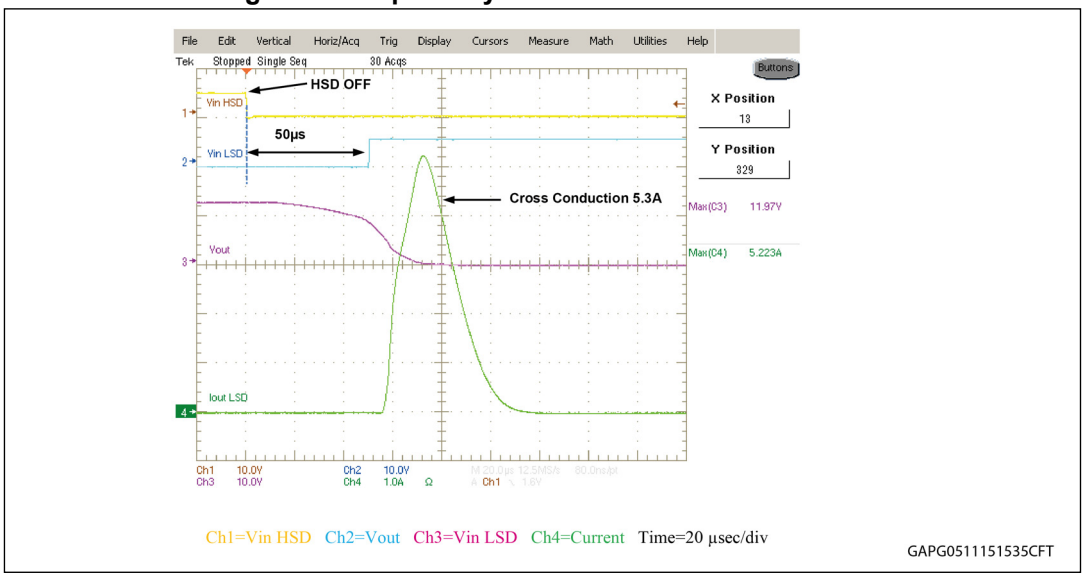
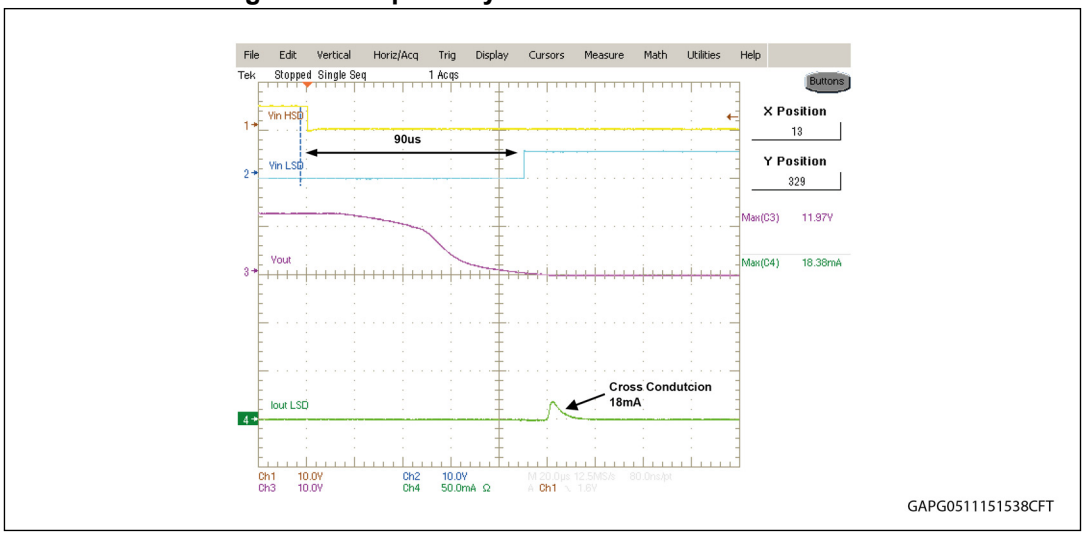


Figure 57. 90 µs delay between HS0 off and LS0 on

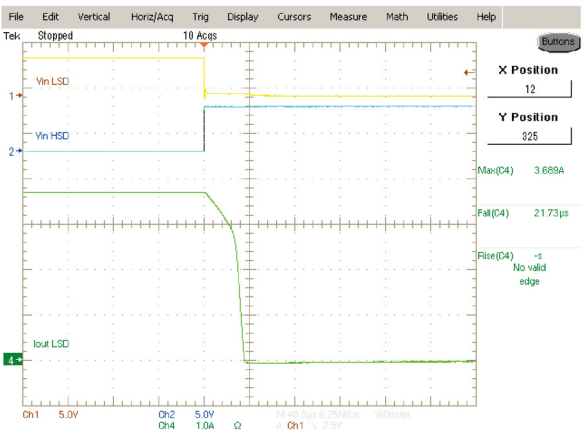


In *Figure 56* a delay of 50 µs causes heavy cross current while a delay of 90 µs as per *Figure 57* causes marginal cross current.

In conclusion, in order to avoid cross-conduction, the low-side drivers must be driven with delay times, so-called “dead times”. As a general rule for monolithic M0-7 HSD in combination with OMNIFET III, the minimum dead time for a low-side driver switch-on is about 250 µs.

Similar considerations can be applied when the HSD must be switched on after the LSD is switched off. In this case, the switching off time of the OMNIFET III is shorter than that of the HSD, so in this case the cross-conduction does not take place even with no delay between LSD and HSD commands. In the figure below, a brake to V_{bat} event in an H-bridge is highlighted.

Figure 58. No delay between LS0 off and HS0 on

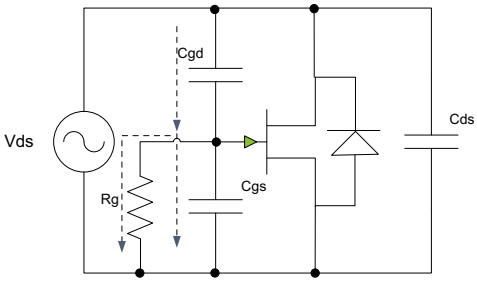


Cross conduction due to Power MOSFET capacitances

Another event causing cross-conduction is related to dynamic effects inside HSD and LSD and precisely to high voltage gradient (dVds/dt) which occurs at each switching.

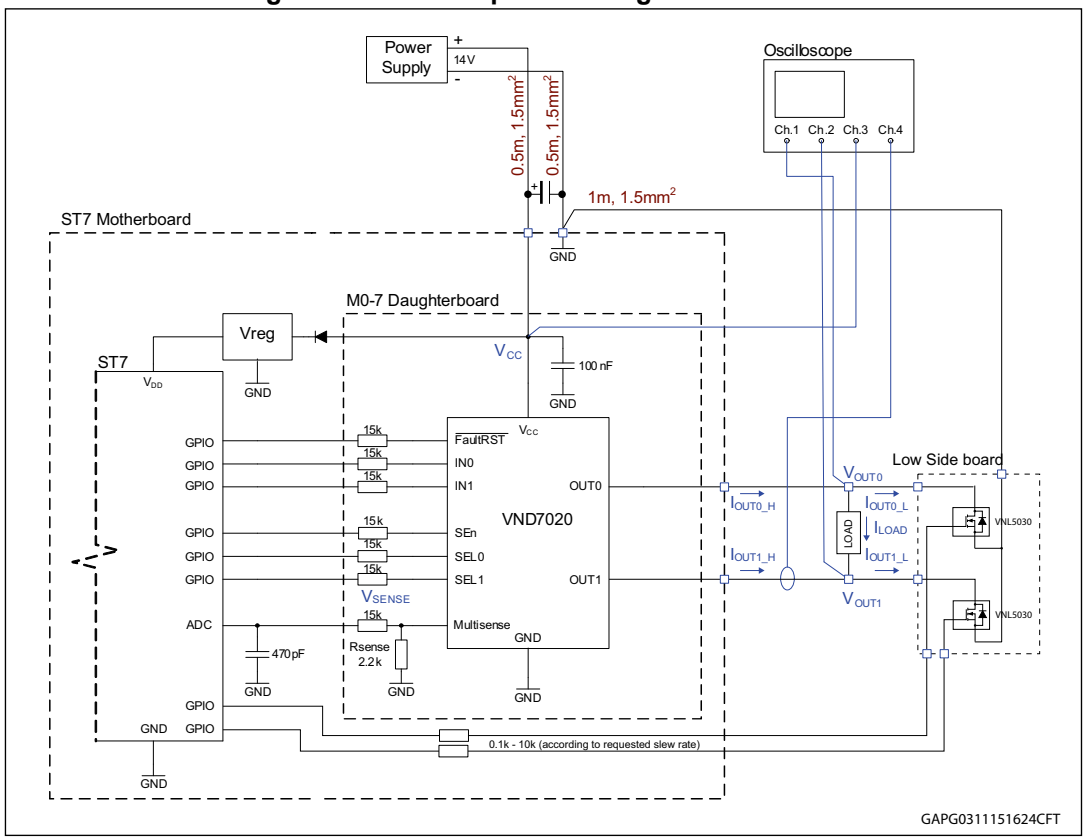
Let us consider an H-bridge in which the high-side driver of a leg (e.g. HS_1) is completely off and the LS_1 is switched on. During the LSD switch-on, the drain-source voltage of HS_1 is submitted to fast dVds/dt. According to the simplified equivalent model of the MOSFET as per *Figure 59* below, this voltage gradient injects a current in the gate-drain capacitance and the gate-source capacitance. The current flowing on the C_{gs} raises the gate voltage, and if the gate voltage reaches the Power MOSFET threshold a consequent turn-on of the Power MOSFET HS_1 takes place. Once this event occurs, HS_1 and LS_1 conduct current simultaneously for a limited time; this causes a cross-conduction event, the so-called “shoot-through”.

Figure 59. Power MOSFET capacitance effect during high dVds/dt



A practical example follows (see *Figure 60*), in which a test setup with two VNL5030S5-E and one VND7020AJ (VIPower M0-7 high-side driver) connected in H-bridge configuration is aimed to reproduce the shoot-through.

Figure 60. Test setup for H-bridge cross current



In this test HSDs and LSDs are driven by a microcontroller. A 4.5 Ω resistance is supplied by turning HS_0 and LS_1, this latter works in PWM at 100 Hz.

Shoot-through could occur because of the parasitic switch on of HS_1 (always off). The OMNIFETIII dVds/dt are low enough (typ. 3 V/µs) to avoid such event. As per *Figure 62*, no shoot through current on V_{bat} (I_{CC}) is reported.

Figure 61. Typical Turn-on/off time for the VNL5030S5-E at 25°C with V_{IN} = 5 V & 10 V

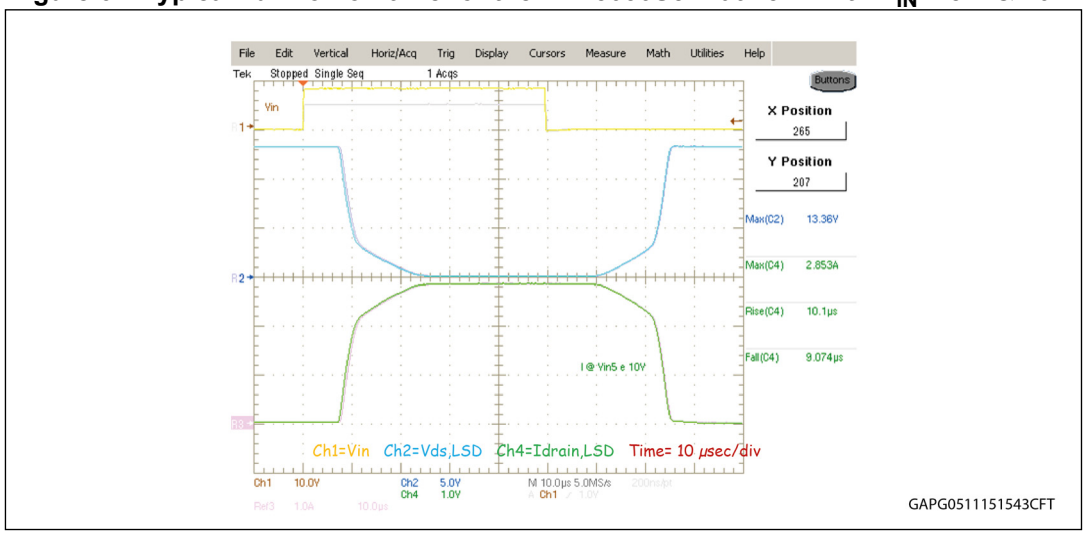
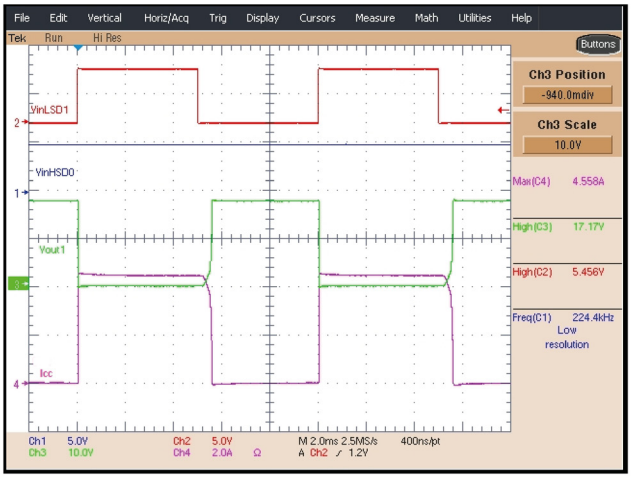


Figure 62. H-bridge - shoot-through ch1 (not present)



Conclusion:

OMNIFET III low-side drivers can be used in H-bridge configuration along with M0-7 HSDs with the limitation to introduce a minimum dead time in the transition HSD on/off and LSD off/on of the same leg.

Freewheeling current of inductive loads

Driving inductive loads in PWM is a common technique to control the average load power according to application requirements (acting as speed control, for example, for DC motors).

If the PWM signal is applied to the HSD0, during its OFF-state the inductive load current re-circulates in the body diode of the LSD0. If, during this phase, the LSD0 input is driven on, the current keeps flowing through the body diode while the LSD remains turned off (therefore no active freewheeling is possible). During freewheeling, the parasitic associated to the supply pin (see *Figure 18*) is on and V_{supply} is forced to 0 V. This prevents OMNIFET switch-on.

Figure 63 shows an example with VND7020AJ combined with 2x VNL5030S5-E driving an inductance that explains this behavior (the current in HS_0 output is plotted as well).

Figure 63. H-bridge configuration: VND7020AJ and 2x VNL5030S5-E

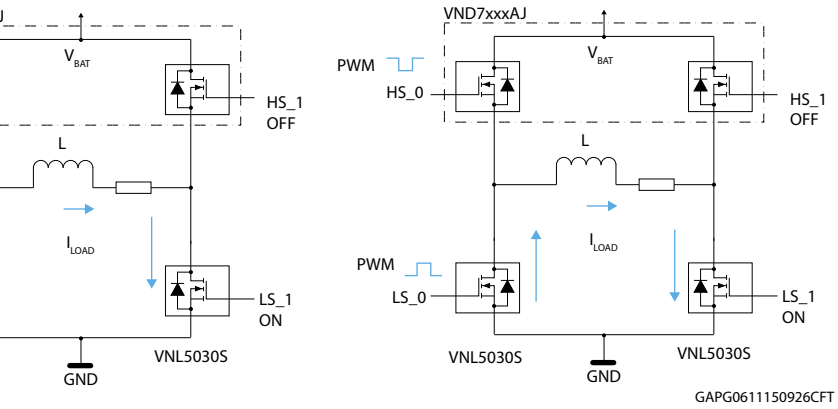
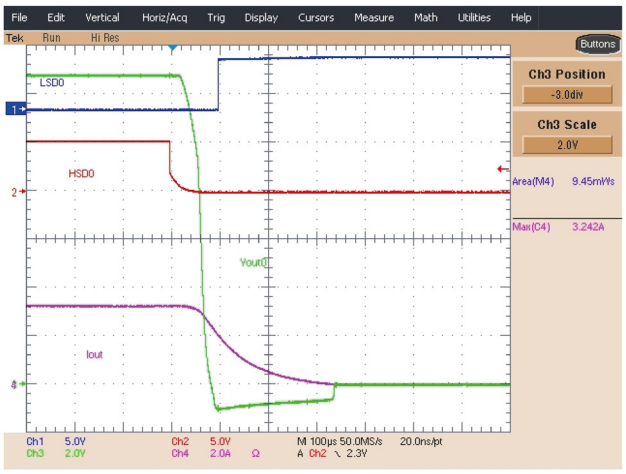


Figure 64. Freewheeling current on HS_0



8 Revision history

Table 11. Document revision history

Date	Revision	Changes
06-Jul-2016	1	Initial release.
27-Nov-2018	2	Updated B value in *Figure 12: (VNL5050x) Static drain source on-resistance vs. input voltage*. Minor text changes.