AN4732
Application note

STCOMET smart meter and power line communication system-on-chip development kit

Patrick Guyard, Riccardo Fiorelli, and Johann Houee

Introduction

The EVLKSTCOMET10-1 is a development kit for the STCOMET platform, exploiting the performance capability of the full-feature STCOMET10 device. The STCOMET10 is a single device integrating a flexible power line communication (PLC) modem with a fully embedded analog front end (AFE) and a line driver, a high performance 3-channel metrology function and a Cortex ™ -M4 application core.
The kit is made of three modules: the STCOMET main board, the LCD module and the power supply board based on the VIPER26H.
With this development kit, it is possible to evaluate a complete single phase smart meter with PLC connectivity. The performance of the metering and application functions could be evaluated along with the PLC transmitting and receiving performance.
The PLC line coupling interface is designed to allow the STCOMET device to transmit and receive on the AC mains line using any narrow-band PLC modulation (single carrier or OFDM) up to 500 kHz, mainly for automatic meter reading (AMR) applications.
The default configuration of the PLC line coupling targets the G3-PLC (ITU G.9903) and PRIME (ITU G.9904) CENELEC A-band protocol standards. With a few BOM modifications, the STCOMET development kit can be adjusted to fit other narrow-band PLC protocols in CENELEC A-band or FCC band (e. g.: S-FSK IEC61334-5-1, IEEE 1901.2, G3-PLC FCC, METERS AND MORE®).
If necessary, a specific customer's module can be designed and placed instead of the LCD module, for a different peripherals configuration.
As it can be seen from the EVLKSTCOMET10-1 picture, a special effort has been made to create the development kit compact and optimized to fit the size of a real meter.
The EVLKSTCOMET10-1 is suitable for the evaluation of the complete STCOMET platform. Featuring the full set STCOMET10 chip, the EVLKSTCOMET10-1 demonstrates at the same time all the functions and performance of the STCOM chips.
Please check for the EVLKSTCOMET10-1 hardware documentation, evaluation software and firmware libraries at st.com/powerline. For specific software or firmware releases, you may need to contact directly the STMicroelectronics sales office.

Figure 1. STCOMET10 development kit (EVLKSTCOMET10-1)

Contents

List of tables

List of figures

1 Safety recommendations

The STCOMET development kit must be used by expert technicians only. Due to the high voltage (85 - 265 V ac) present on the non-isolated parts, special care must be taken in order to avoid electric risks for people safety.

There are no protections against high voltage accidental human contact.

After disconnection of the board from the mains all the live part must not be touched immediately because of the energized capacitors.

It is mandatory to use a mains insulation transformer to perform any tests on the high voltage sections, using test instruments like, for instance, spectrum analyzers or oscilloscopes.

Do not connect any probe to high voltage sections if the board is not isolated from the mains supply, in order to avoid damaging instruments and demonstration tools.

When configured for metering evaluation, the STCOMET development kit is not isolated and ground will be tied to the line. Do NOT connect instrument probes that can bring the earth connection to the line, thus potentially damaging the STCOMET development kit and the instruments and creating electrical risk.

STMicroelectronics assumes no responsibility for the consequences of any improper use of this development tool.

2 STCOMET smart meter and power line communication system-on-chip description

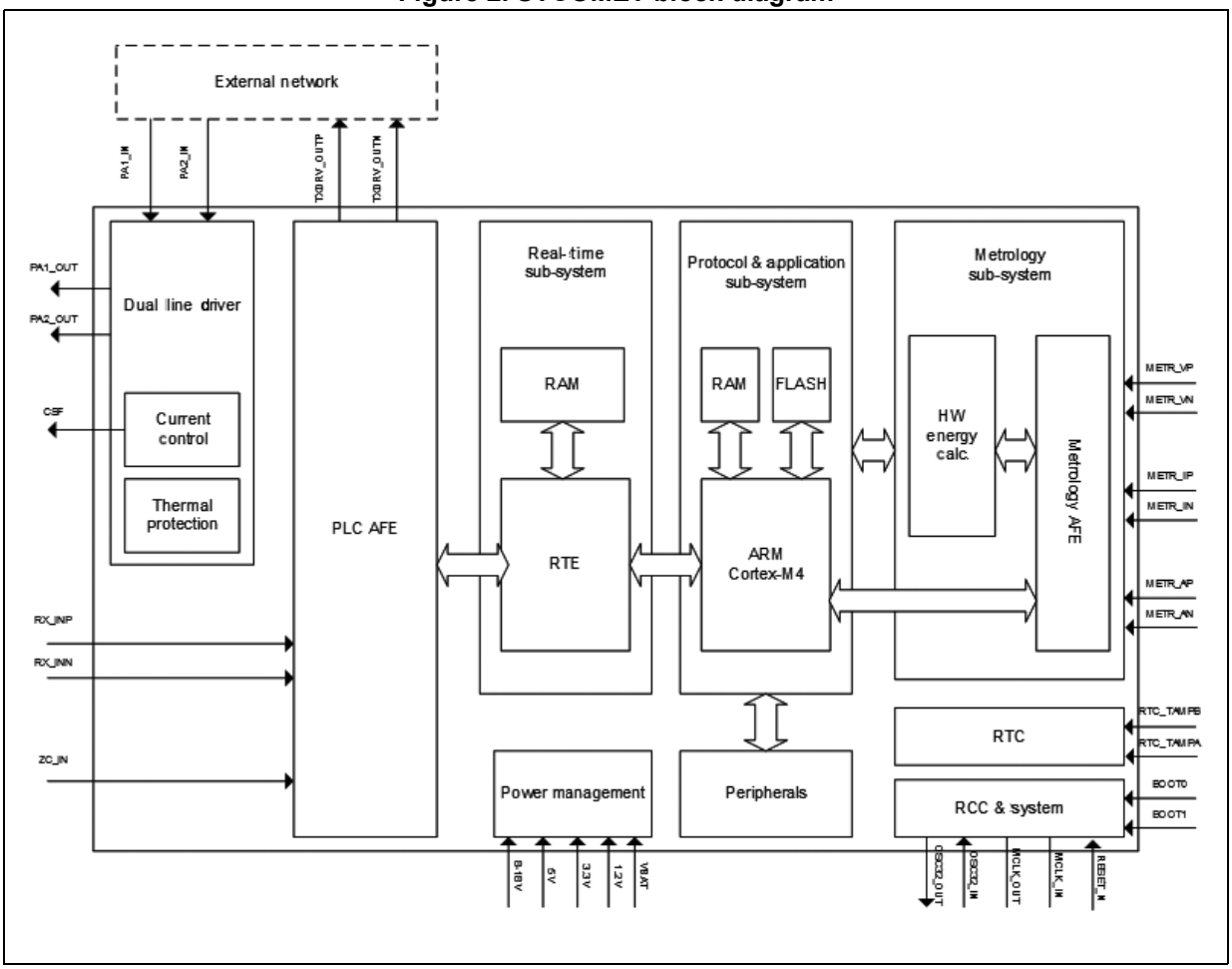
The STCOMET is a device that integrates a narrow-band power line communication (NB-PLC) modem, a high-performance application core and metrology functions.

The PLC modem architecture has been designed to target the EN50065, FCC, ARIB compliant PLC applications. Together with the application core, it enables the STCOMET to support the PRIME, G1, G3, IEEE 1901.2, METERS AND MORE and other narrow-band PLC protocol specifications.

The metrology sub-system is suitable for the EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22 and IEC 62053-23 compliant class1, class0.5 and class0.2 AC metering applications.

For further details, please refer to *1.* in *Section 12 on page 52*.

Figure 2. STCOMET block diagram



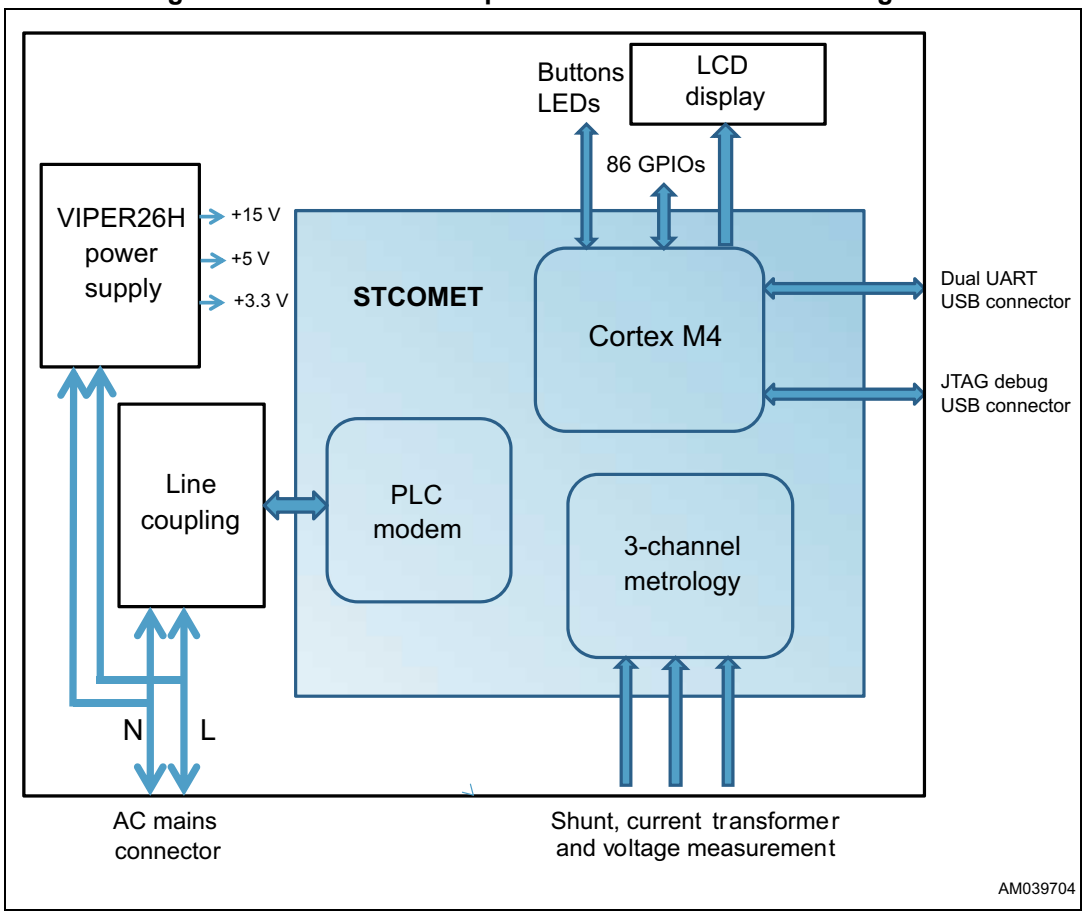
3 STCOMET development kit description

The STCOMET development kit is available as a board set comprising:

- One STCOMET main board
- One LCD module with access to STCOMET GPIOs
- One power supply unit based on VIPER26H

The functional block diagram is depicted in *Figure 3*.

Figure 3. STCOMET development kit - functional block diagram



4 STCOMET development kit electrical characteristics

Table 1. Electrical characteristics

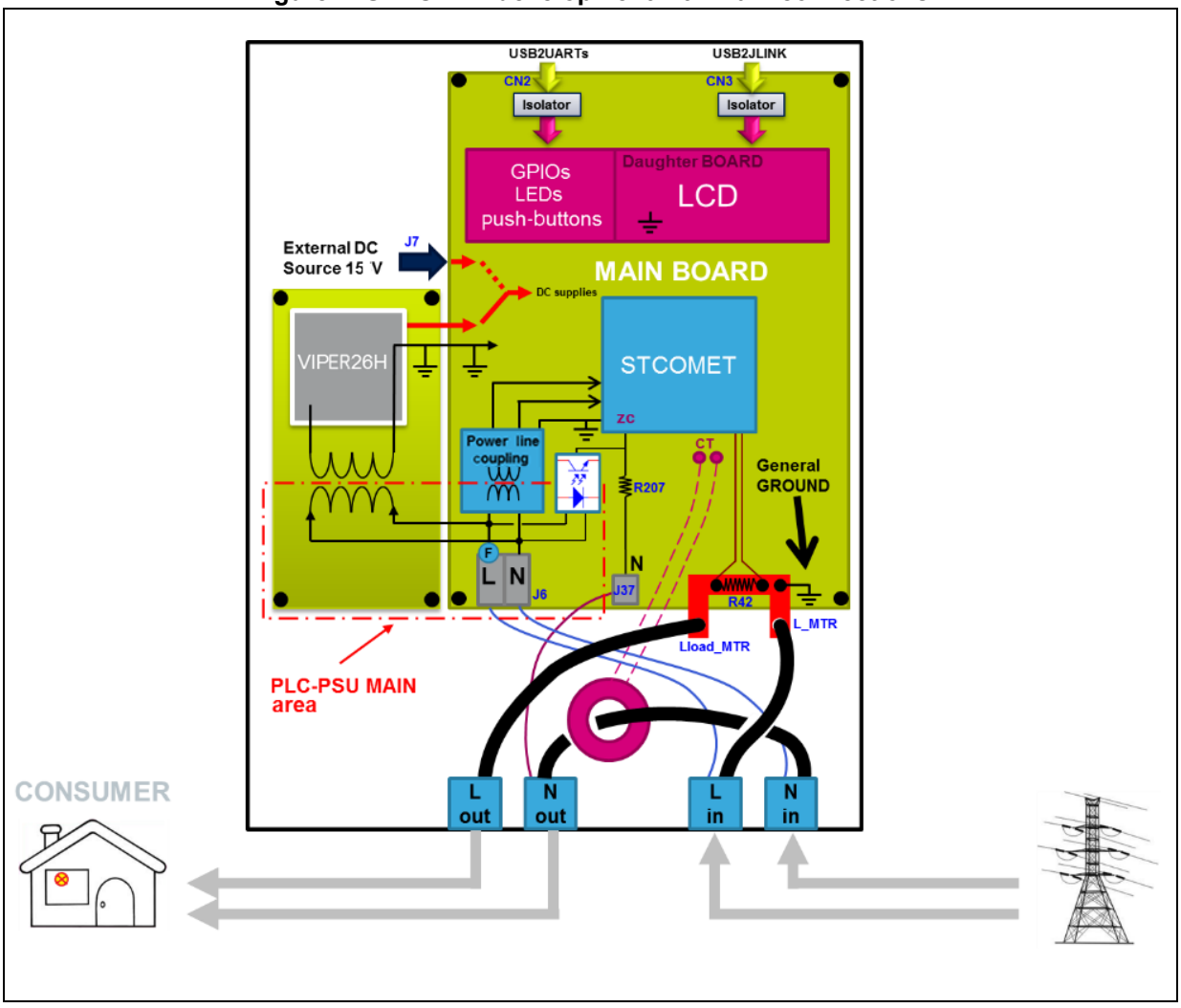
Parameter	Value				Notes
	Min.	Typ.	Max.	Unit	
AC mains input frequency	-	50/60	-	Hz	J6 connector
AC mains input voltage	90	230	440	V rms	J6 connector
Single DC supply mode					
Single DC input voltage	12	15	16	V	J7 connector
Single DC current capability	1	-	-	A	
VIPER26H power supply mode					
VCC DC voltage	14	15	16	V	J13 connector
VCC DC current capability	700	-	-	mA	
5 V DC voltage	4.75	5	5.25	V	
5 V DC current capability	100	-	-	mA	
3.3 V DC voltage	3.1	3.3	3.5	V	
3.3 V DC current capability	200	-	-	mA	

5 IMPORTANT - STCOMET development kit use and safety

There are several ways to use the STCOMET development kit, with different levels of safety. It is very important for the user to understand the related precautions to take for each mode.

Figure 4 gives an overview of the paths used by the line and neutral high voltage on the STCOMET development kit.

Figure 4. STCOMET development kit - main connections



5.1 USB connectors CN2 and CN3

Whatever the connection mode selected by the user, the USB connections at the CN2 and CN3 remain isolated, allowing usage of the user's computer also in non-isolated configuration.

5.2 Low voltage connection mode

For this configuration, no mains voltage is present. The STCOMET development kit must be supplied through the J7 connector, using an isolated DC supply (15 V typ.) (see *Section 7.1 on page 16*).

The HW configuration will be as follows:

- The VIPER26H power supply is OFF and can be removed
- PLC communication can be done through the J6 connector without mains presence
- The zero crossing for PLC can be provided only by the 50 Hz low voltage signal applied to the STCOMET ZC_IN pin (ZC test point on main board)
- Metrology tests can be done only with low voltage/current signals applied to the metrology input pins.

This mode is recommended for SW-FW development or any activity outside of a safe laboratory.

5.3 Isolated mains connection mode

Mains voltage is applied to the J6 only.

In this configuration, line and neutral voltages are present only in the “PLC-PSU main area” highlighted in *Figure 4*, limited to the primary sides with respect to the PLC and PSU transformers.

The rest of the STCOMET development kit remains isolated.

In this mode:

- PLC communication can be done with presence of the mains voltage
- Zero crossing for PLC can be provided through the isolated zero crossing coupling (see *Section 7.2.4 on page 22*)
- Metrology tests can be done only with low voltage/current signals applied to the metrology input pins.

5.4 Non-isolated mains connection mode

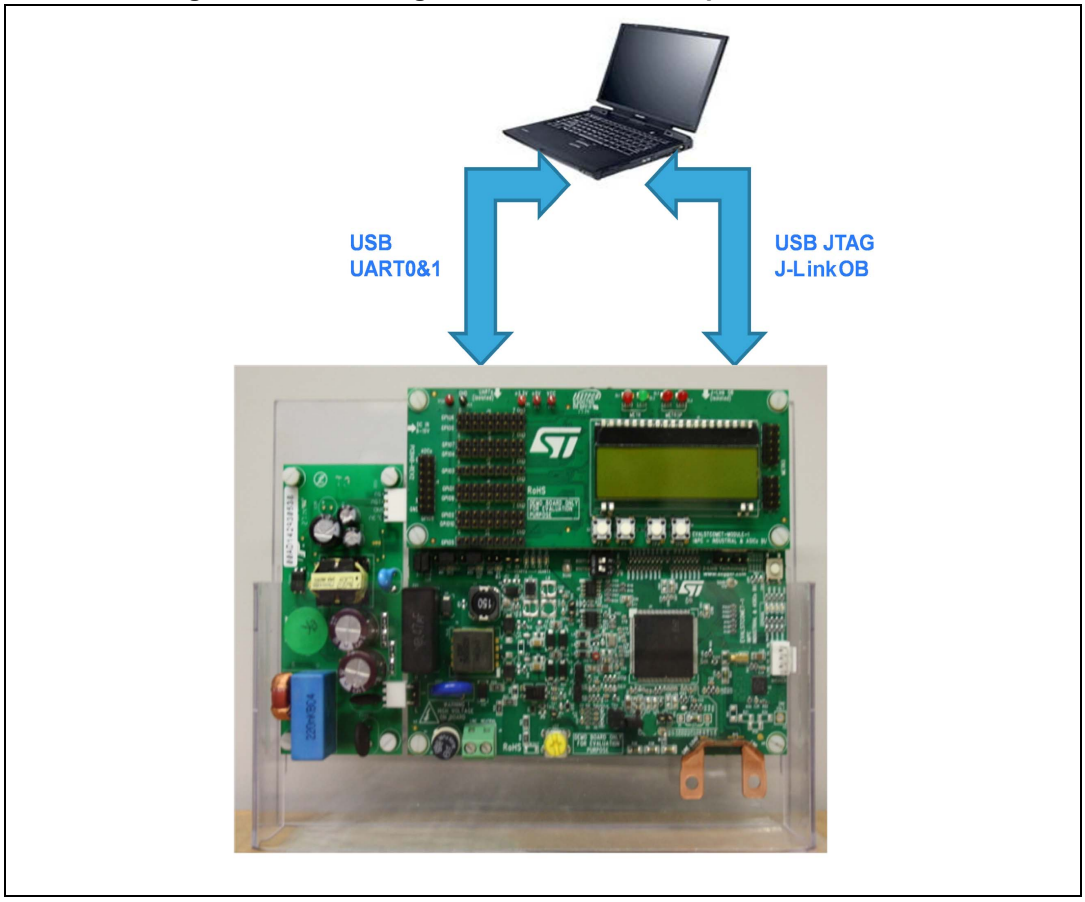
Apply the mains line and neutral voltages to the J6, plus line to the R42 pin 3 (L_MTR) and neutral to the J37.

In this mode:

- The ground will be directly connected to line voltage
- PLC communication can be done with presence of the mains voltage
- Zero crossing for PLC can be provided through the isolated or non-isolated zero crossing coupling circuits (see *Section 7.2.4*)
- Full metrology tests can be performed. The mains load will be connected between the R42 pin 1 (Lload_MTR) and neutral.

6 Using the STCOMET development kit

Figure 5. Connecting the STCOMET development kit to a PC



6.1 Silabs CP2105 driver installation

In order to connect an STCOMET development kit to the PC, install Virtual COM Port drivers for the SiLabs CP2105 device (which converts data between the PC USB port and STCOMET UART0 and UART1).

The latest drivers are available at:

http://www.silabs.com/products/mcu/Pages/SoftwareDownloads.aspx

The LEDs DL5 to DL8 show the UART TX and RX activity.

6.2 Segger J-Link driver installation

For FW JTAG development, a Segger J-Link on-board debugger has been included, with an isolated USB interface to the PC for safe connection even when connecting to the mains.

The latest drivers are available at:

http://www.segger.com/jlink-software.html

6.3 Connection procedure

The following procedure is required for every node to be connected to the PC:

1. Verify that the mini USB cable for the UART (and optionally the one for JTAG access) is connected to the PC
2. Power up the STCOMET development kit
3. Verify that the Virtual COM Ports (and J-Link driver if connected) have been installed.

6.4 Development tool usage

The STCOMET development kit has been conceived as a development platform to develop and test any customer's solution based on the STCOMET device.

The STCOMET main board is widely configurable and allows different HW configurations, for the GPIOs, PLC line coupling and metrology sensors.

6.5 Evaluation tool usage

In addition to use as a development platform, the STCOMET development kit can be used in an application oriented evaluation environment. To do so, isolated USB connections to the PC must be used.

6.5.1 Evaluating with PLC GUI

A typical PLC evaluation environment is composed by two or more STCOMET development kits connected to one or more PCs running a protocol-related GUI which manages the communication services offered by the STCOMET PLC FW.

6.5.2 Evaluating metrology features

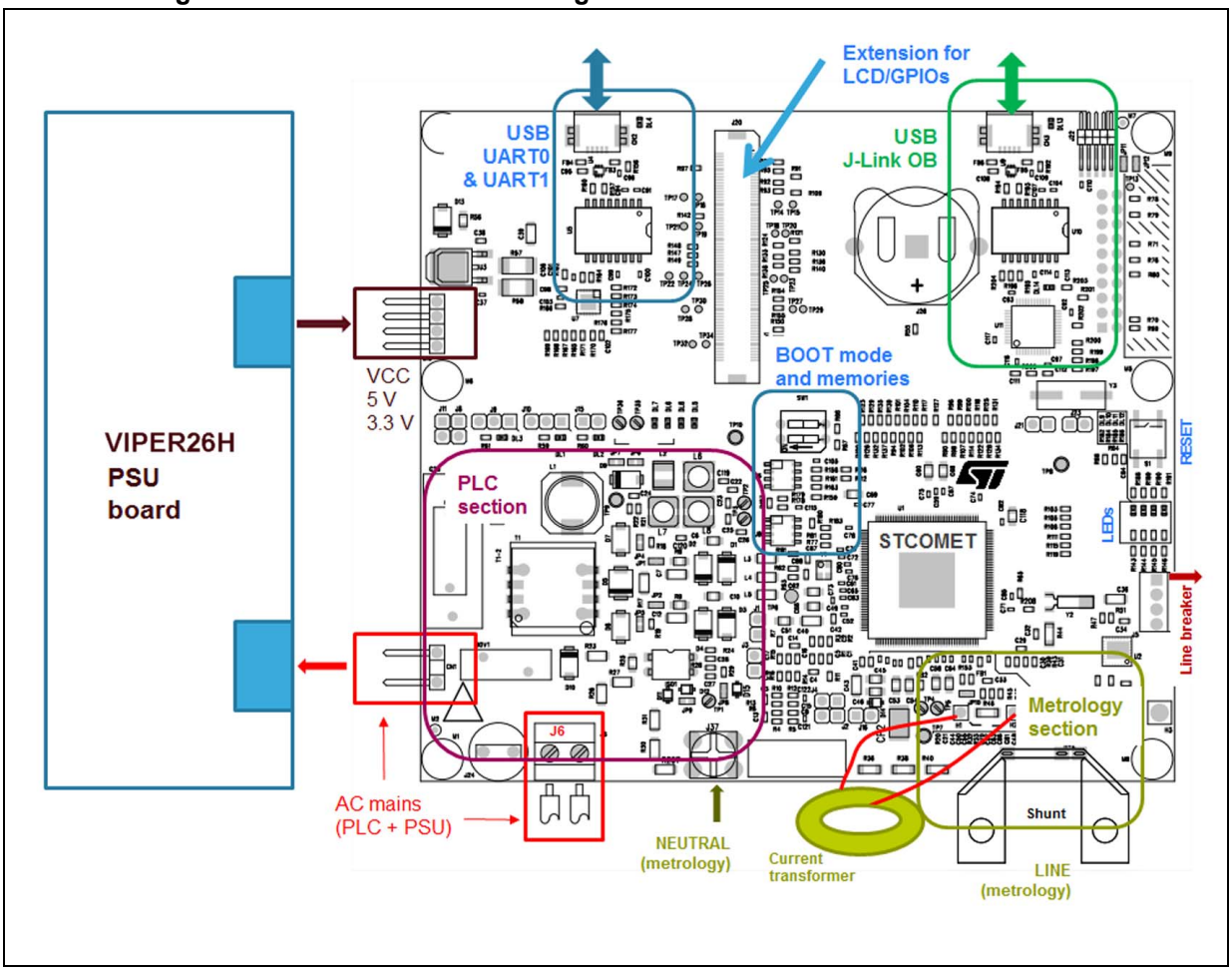
In addition to the PLC evaluation, the user can control the metrology section of the STCOMET through a dedicated GUI accessing the STCOMET registers for configuration and measurement data reading.

7 STCOMET main board description

The STCOMET main board is composed of the following sections:

- STCOMET device section
  - Serial non-volatile memories
  - Boot mode configuration via DIP switches
  - 24 MHz and 32 kHz oscillators
  - Decoupling capacitors
- RTC backup battery
- Line coupling section, including four subsections:
  - Configuration network for the integrated line driver
  - Reception filter
  - Power line coupling
  - Zero crossing coupling
- Metrology section
  - Shunt connection on the line
  - Current transformer (CT) for the neutral
  - Voltage measurement (line - neutral)
- Line breaker driver section
- On-board power supply:
  - Configuration jumpers
  - Embedded regulator for single DC supply mode
- JTAG debug section
  - J-Link on-board accessible via isolated USB
- 2 UARTs over isolated USB
  - Enhanced and standard COM ports
- Module interface connector.

Figure 6. STCOMET board drawing with indication of the various sections



The board has also the following external connections or control:

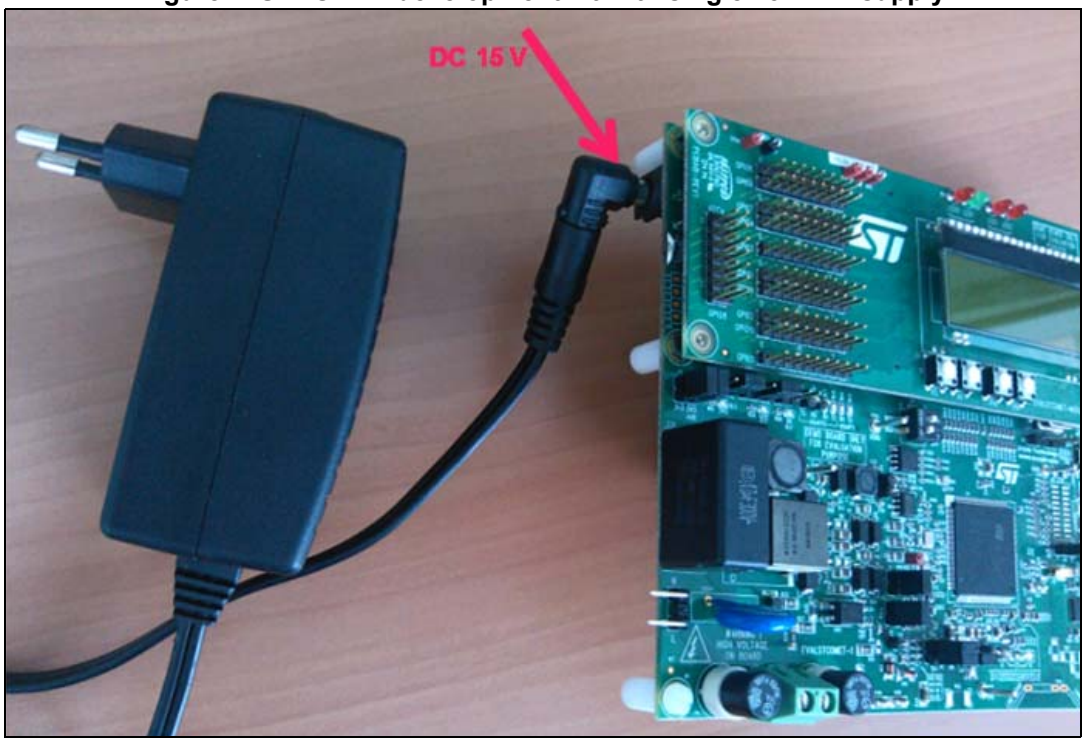
- AC mains (line and neutral) on J6 connector
- Line breaker connector J5 to control external relay
- Reset button and LEDs
- Configuration jumpers.

7.1 Power supply configuration

The STCOMET development kit includes the VIPER26H power supply board. However, for convenient use without applying the mains voltage (mainly for software development) the STCOMET main board could be used without the VIPER26H power supply. In that case, the STCOMET main board can be supplied with an external 15 V DC source (see *Figure 7*).

Note that the external supply jack connector shall have 15 V on the internal contact and GND on the external shield.

Figure 7. STCOMET development kit with single 15 V DC supply

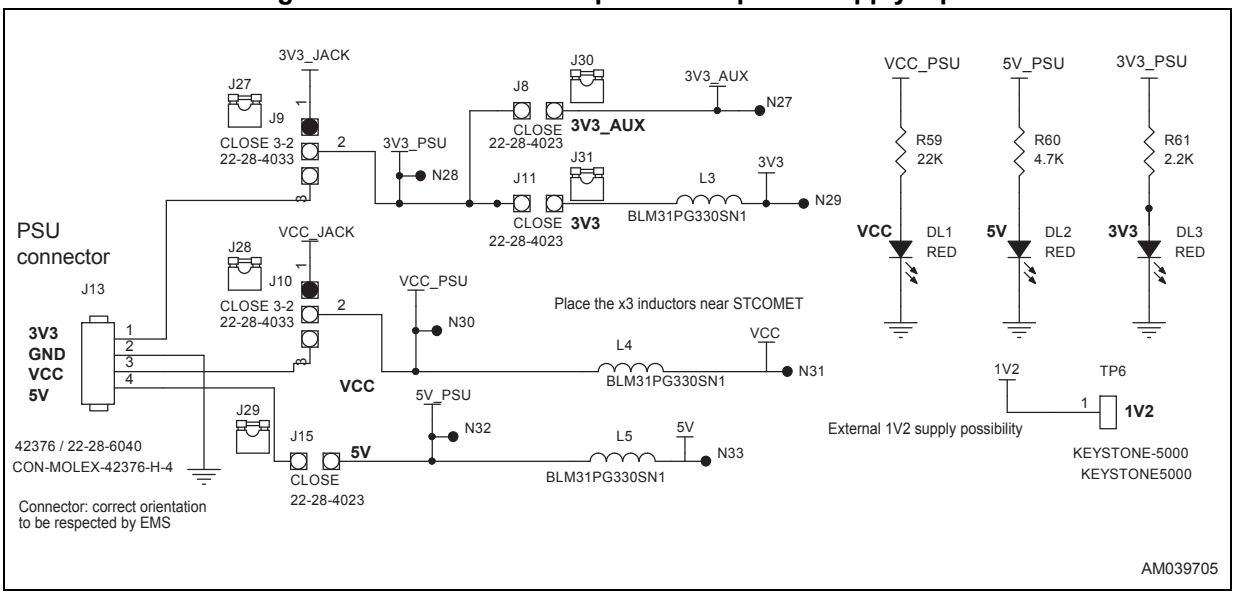


Specific jumper configuration has to be set properly as shown in *Table 2* and *Figure 8*.

Table 2. Power supply configuration

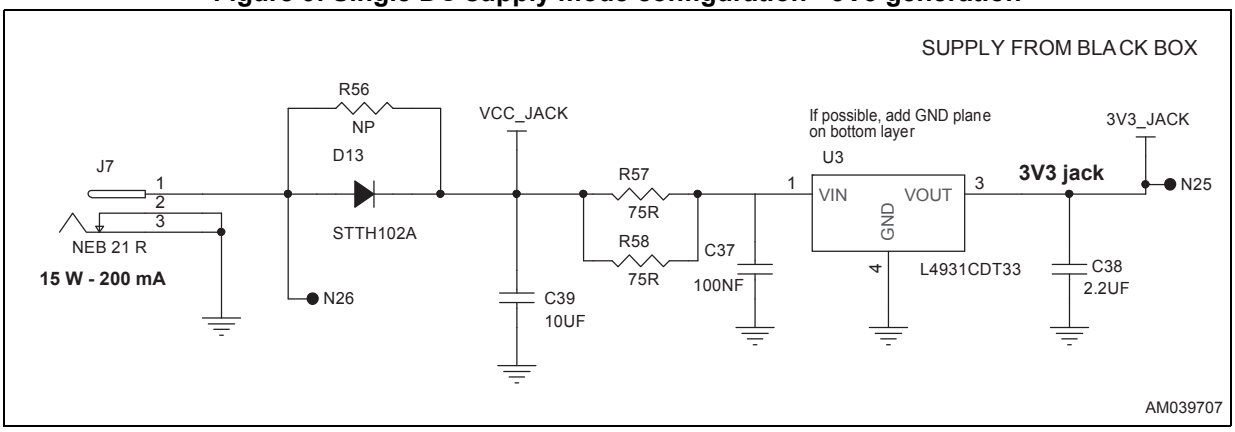
Jumper reference	Configuration	
	VIPER26H power supply mode	Single DC supply mode
J9	Close 2 - 3	Close 1 - 2
J10	Close 2 - 3	Close 1 - 2
J15	Close	Open
J16	Open	Close

Figure 8. STCOMET development kit - power supply input



In the single DC supply mode configuration, the whole STCOMET main board and LCD module are supplied from the single 15 V DC supply using the following circuitry:

Figure 9. Single DC supply mode configuration - 3V3 generation



The diode D13 prevents from revert voltage applied at the J7 level by mistake. VCC_JACK is then the voltage applied to the STCOMET VCC.

The STCOMET 3.3 V is generated with the LDO U3. The 2 resistors R57 and R58 allow to dissipate a portion of the power in order to relieve U3.

The STCOMET 5 V is generated by the 5 V regulator integrated in the STCOMET (pin 53), using the jumper J16 closed.

This is absolutely not an optimized power scheme but it allows generating the necessary supply voltages for safe SW development with low cost components and a reduced PCB size.

7.2 Power line interface section

The line coupling section is composed of four different sub-sections: the line driver (*Figure 10*), the line coupling, the reception filter (*Figure 11*), and the zero crossing coupling (*Figure 12*).

Both transmission and reception paths are fully differential, allowing for the higher dynamic range and noise immunity.

The frequency response of this section is usually sensitive to tolerance of component values. Actual components used in the STCOMET development kit have the following tolerances: ± 20% for the X1 capacitor and the coils, ± 10% for SMD ceramic X7R capacitors, and ± 1% for SMD resistors.

For the line driver, C0G/NPO type capacitors are required to guarantee linearity and stability against signal amplitude and frequency.

Figure 10. STCOMET development kit - line driver section

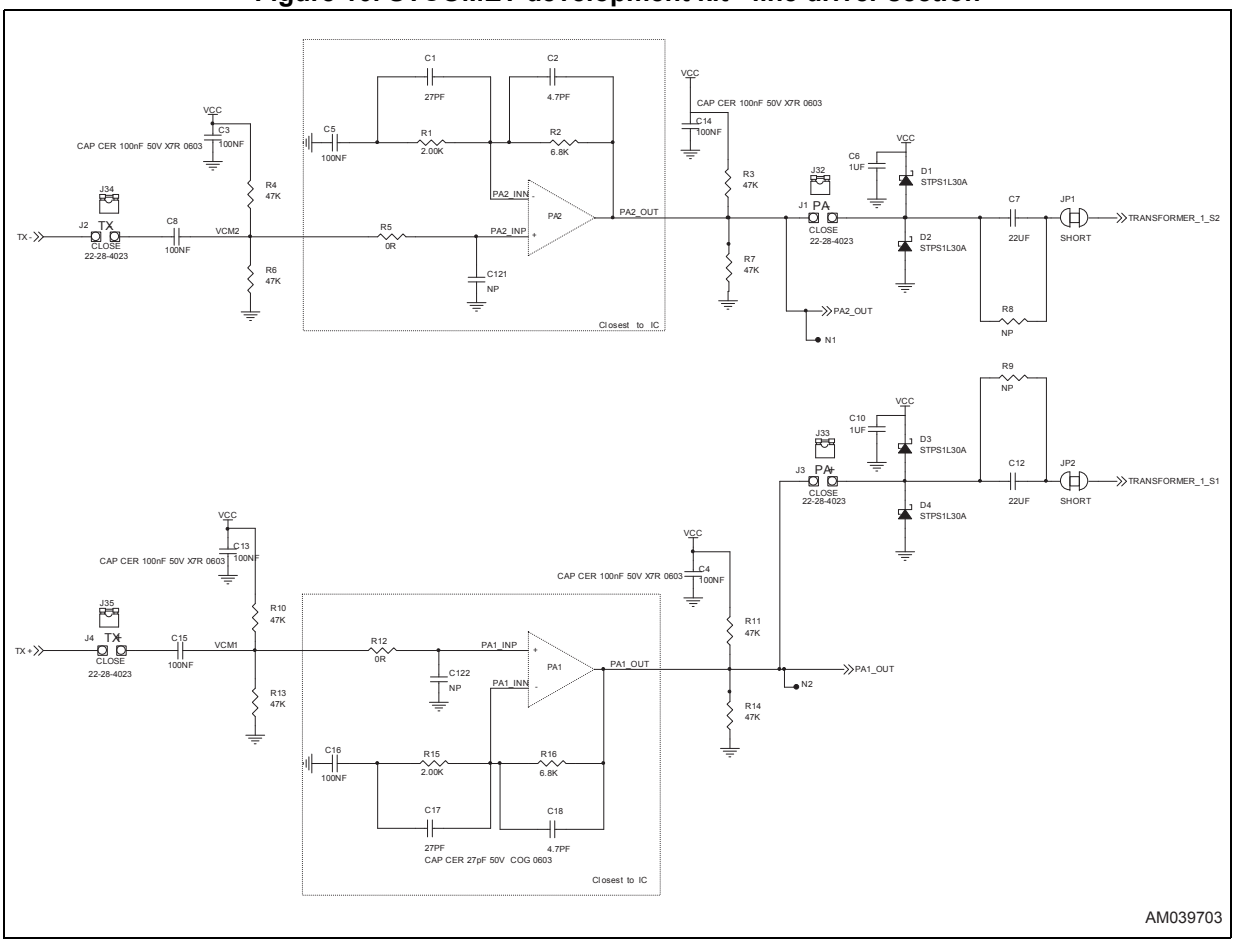


Figure 11. STCOMET development kit - line coupling and reception filter section

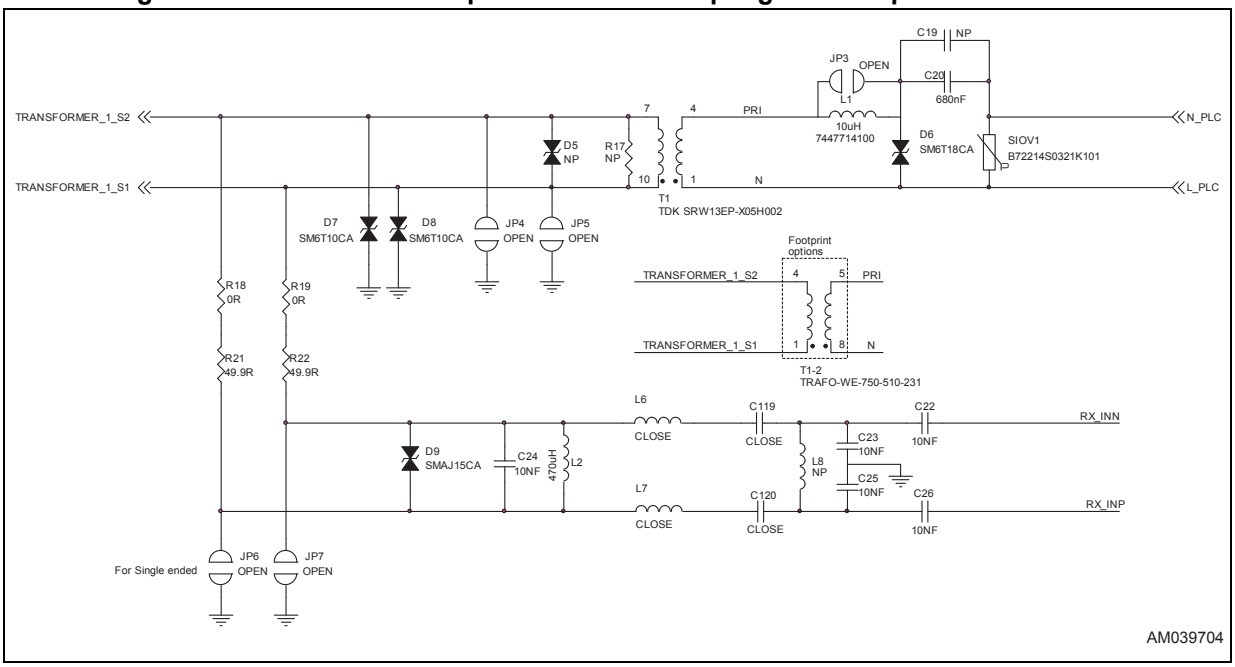
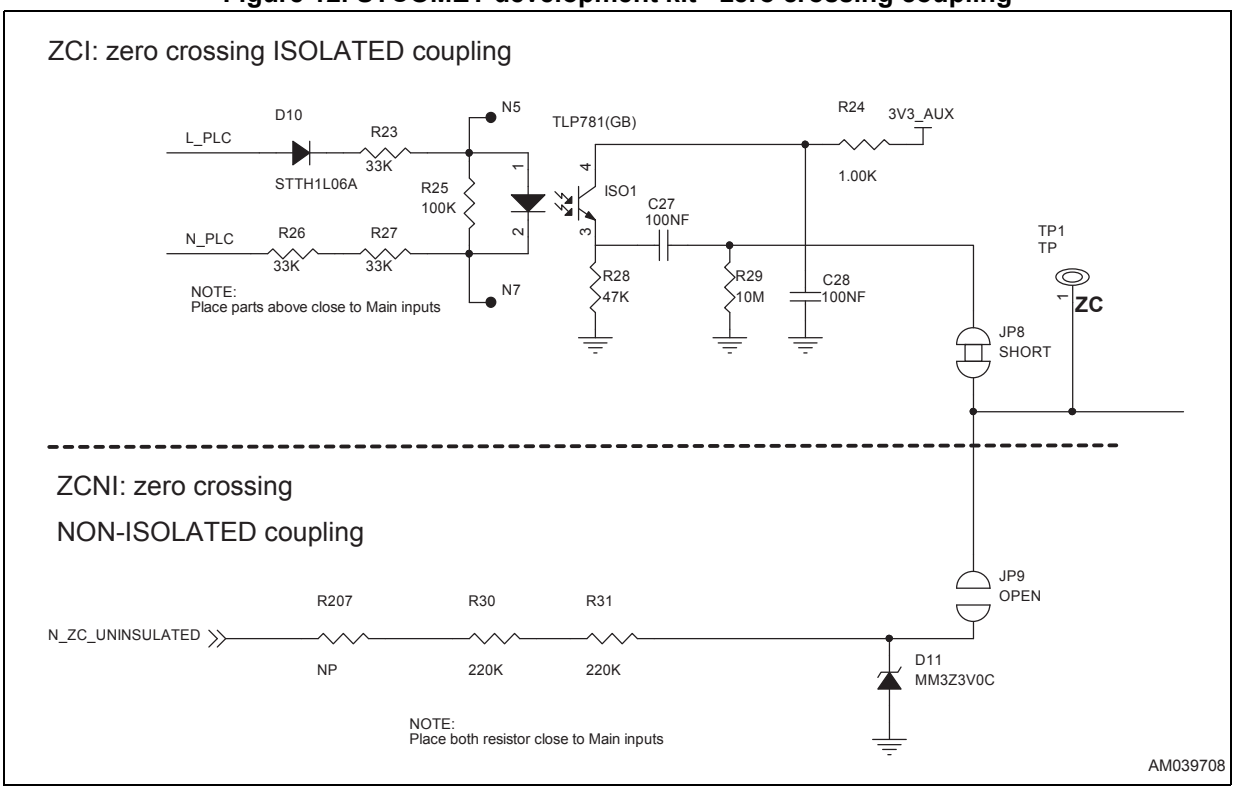


Figure 12. STCOMET development kit - zero crossing coupling



7.2.1 Line driver network

The line driver sub-section is based on the STCOMET internal dual power amplifier (PA), whose input and output pins are externally available to allow configurability of the circuit.

The line driver amplifies the differential transmitted signal generated by the STCOMET through the integrated current DAC and pre-driver.

The STCOMET line driver has very high linearity, so in this development kit it has been used in all-pass configuration.

In the frequencies of interest, the capacitors C1, C2 and C5 have negligible impedance with respect to the R1 and R2, so the in-band amplifier gain can be calculated as:

Equation 1

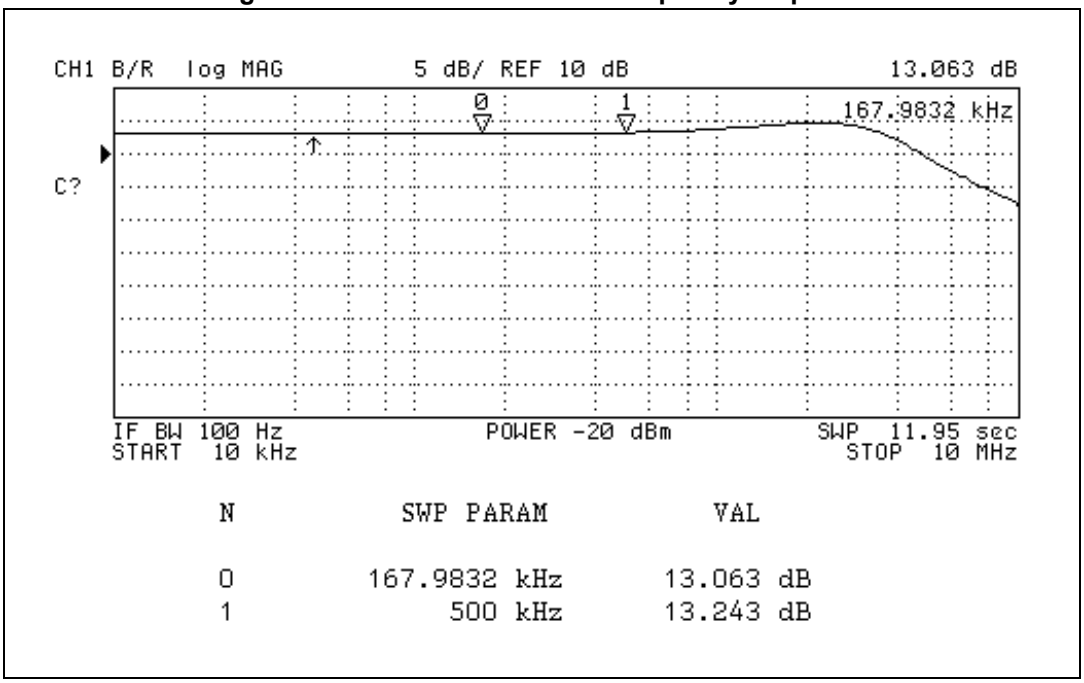
$$|G_{TX}| = 1 + \frac{R_2}{R1} = 4.4 = 13 \text{ dB}$$

The C5 is used to set the DC gain of the filter to 0 dB (input bias and output bias voltages must be both VCC/2), while the C1 and C2 provide gain compensation by reducing the gain at high frequencies.

Table 3. Line driver parameters

Symbol	Parameter	Value [typ]	Unit
|GTX|	In-band voltage gain	13	dB
BW3dB	Low-pass 3-dB bandwidth	5	MHz

Figure 13. Measured line driver frequency response



7.2.2 Line coupling

The coupling to the power line requires a few passive components. In particular, it includes the DC decoupling capacitors C7 and C12, the line transformer T1, the power inductor L1 and the X1 safety capacitor C20.

The L1 has been accurately chosen to have a high saturation current (> 2 A) and very low equivalents series resistance (< 0.1 Ω), to limit distortion and insertion losses even with a heavy line load.

Center frequency for the series resonance can be calculated at first approximation as:

Equation 2

$$fc = \frac{1}{2\pi\sqrt{L_1' \cdot C_{20}}}$$

where L_1 is the series of the L1 and the leakage inductance of the coupling transformer T1, adding about 1 µH to L1.

The Q factor of this coupling circuit is driven by the mains line impedance: the choice of the L1 and C20 values, anyway, leads to limited attenuation due to either parasitic impedance or resonance selectivity.

Particular attention has been paid in choosing the line transformer. The required characteristics are listed in *Table 4*. In order to have a good signal transfer and minimize the insertion losses, it is recommended to choose a transformer with a primary (shunt) inductance of 0.5 mH or greater, a leakage inductance much smaller than L1 and total DC resistance lower than 0.5 Ω.

Table 4. Line coupling transformer specifications

Parameter	Value
Turn ratio	1:1
Shunt inductance	≥ 0.5 mH
Leakage inductance	≤ 1.5 µH
DC total resistance	≤ 0.5 Ω
DC saturation current	≥ 15 mA
Inter-winding capacitance	< 30 pF
Withstanding voltage	≥ 4 kV for double insulation ≥ 1.5 kV for functional insulation

7.2.3 Reception filter

The reception filter in its default configuration is a simple band-pass filter made of resistance in series with a parallel L-C resonant. The center frequency and the quality factor of the filter can be expressed as:

Equation 3

$$f_C = \frac{1}{2\pi}\omega_C \sim \frac{1}{2\pi\sqrt{L_2 C'}}$$

$$Q = \frac{(R_{21+}R_{22})L_2 C'}{(R_{21+}R_{22})R_L C' + L_2}\omega_C$$

where:

$$C' = C_{24} + \frac{C_{23}C_{25}}{C_{23} + C_{25}}$$

R_L is the DC series resistance of the inductor (for example, with L2 = 744045471, R_L = 14.2 Ω max).

The quality factor and the filter selectivity depend mainly on the value of (R21 + R22). Lower value leads to lower steepness of the resonance, while higher value gives higher selectivity.

R_L value may impact insertion losses. To evaluate the relationship between the RL and the received signal loss, the following simplified expression can be used:

Equation 4

$$|R(j\omega_C)| = Q\frac{\omega_C L_2}{R_{21} + R_{22}} = \frac{1}{1 + R_L(R_{21+}R_{22})\frac{C'}{L_2}}$$

With actual values of the components, the transfer gain is almost unitary at center frequency.

By looking to the transfer function formula, it can be noticed that a higher Q can help keeping the losses small, but a high Q would also bring a higher sensitivity of the filter to components tolerance.

7.2.4 Zero crossing coupling

The zero crossing coupling circuit is aimed at providing a bipolar (AC) signal synchronous with the mains network voltage to the ZC_IN pin. This signal must be centered on AGND and limited to less than 10 V pp.

Two ZC mode options are possible on the PLC side: isolated or non-isolated. The selection is made through a few components, as indicated in *Table 5*.

Table 5. Zero crossing coupling configuration

Reference	Isolated configuration (default)	Non-isolated configuration
R207	Open	0 Ω
R26	33 kΩ	Open
JP8	Close	Open
JP9	Open	Close

The isolated zero crossing circuit is realized through an optocoupler in non-inverting configuration. Neutral and phase lines are brought to the optocoupler through 3 x 33 kΩ resistors in series, as represented in *Figure 12 on page 19*. The STTH1L06A diode blocks the negative half-wave, thus reducing the circuit power consumption by half. The 3 x 33 kΩ resistors limit the photodiode input current to nearly 2 mA rms at 230 V AC. Having several resistors helps preventing short-circuits in case of resistor degradation.

The timing characteristics of this circuit, according to the oscilloscope screenshots reported below, are listed in *Table 6*.

Table 6. Zero crossing isolated coupling - measured timing characteristics

Edge	ZC delay	ZC jitter
Positive	232 µs	4 µs
Negative	4.8 µs	3 µs

Figure 14. Isolated zero crossing coupling - positive edge delay

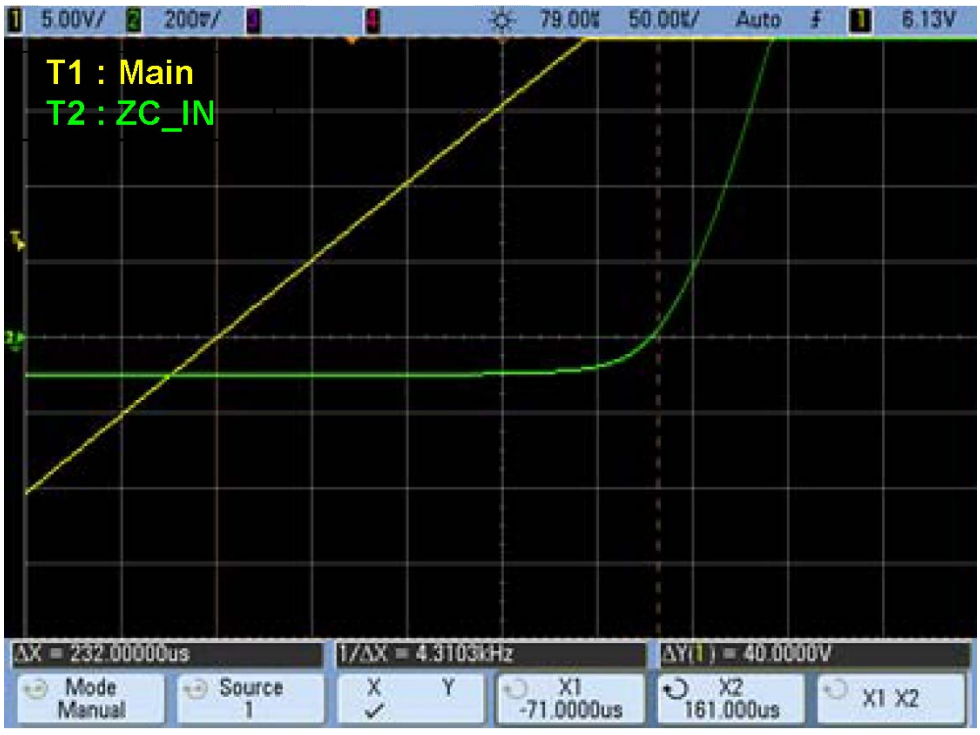
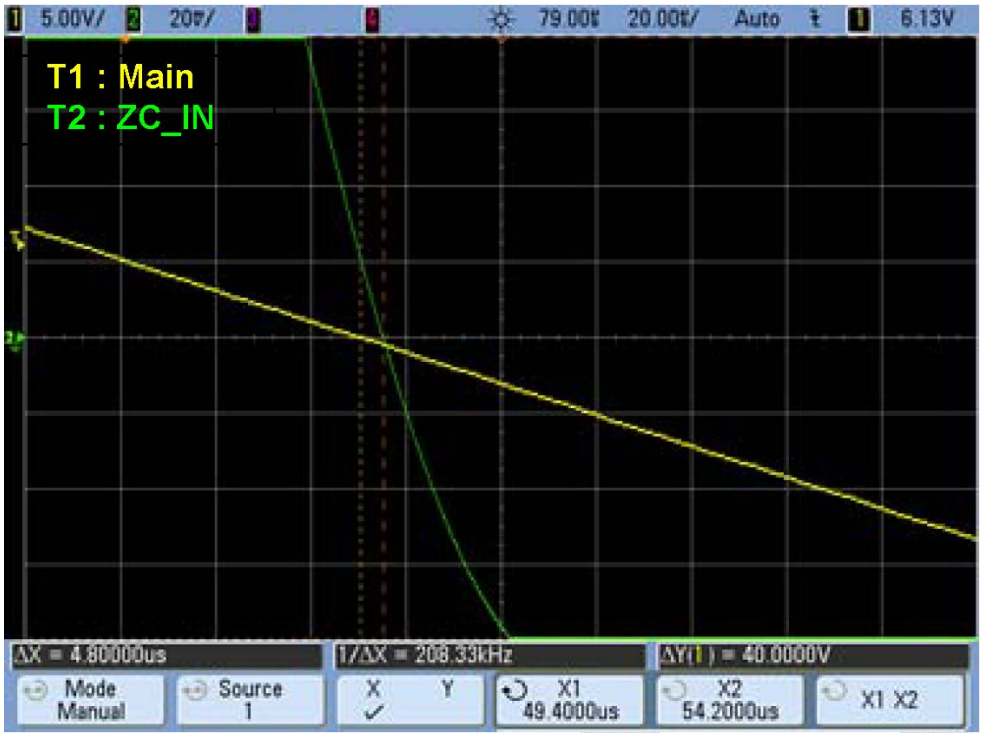


Figure 15. Isolated zero crossing coupling - negative edge delay



A second option is to use non-isolated zero crossing, for BOM cost reduction. In the circuit implemented in the STCOMET development kit, the MM3Z3V0C Zener diode clamps the input mains voltage to +3.0 and -0.7 V, while the two 220 kΩ series resistors limit the Zener current during conduction.

The timing characteristics of this circuit, according to the oscilloscope screenshots reported below, are listed in *Table 7*.

Table 7. Zero crossing non-isolated coupling - measured timing characteristics

Edge	ZC delay	ZC jitter
Positive	2.8 µs	3.3 µs
Negative	18 µs	2.5 µs

Figure 16. Non-isolated zero crossing coupling - positive edge delay

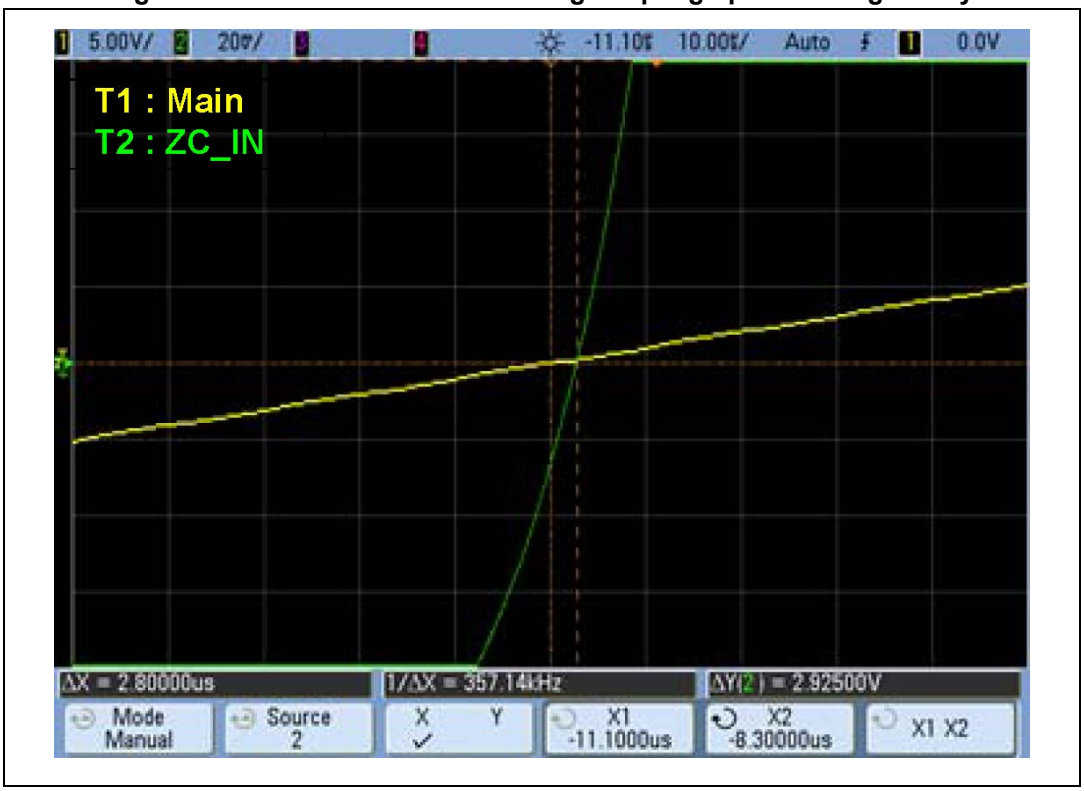


Figure 17. Non-isolated zero crossing coupling - negative edge delay

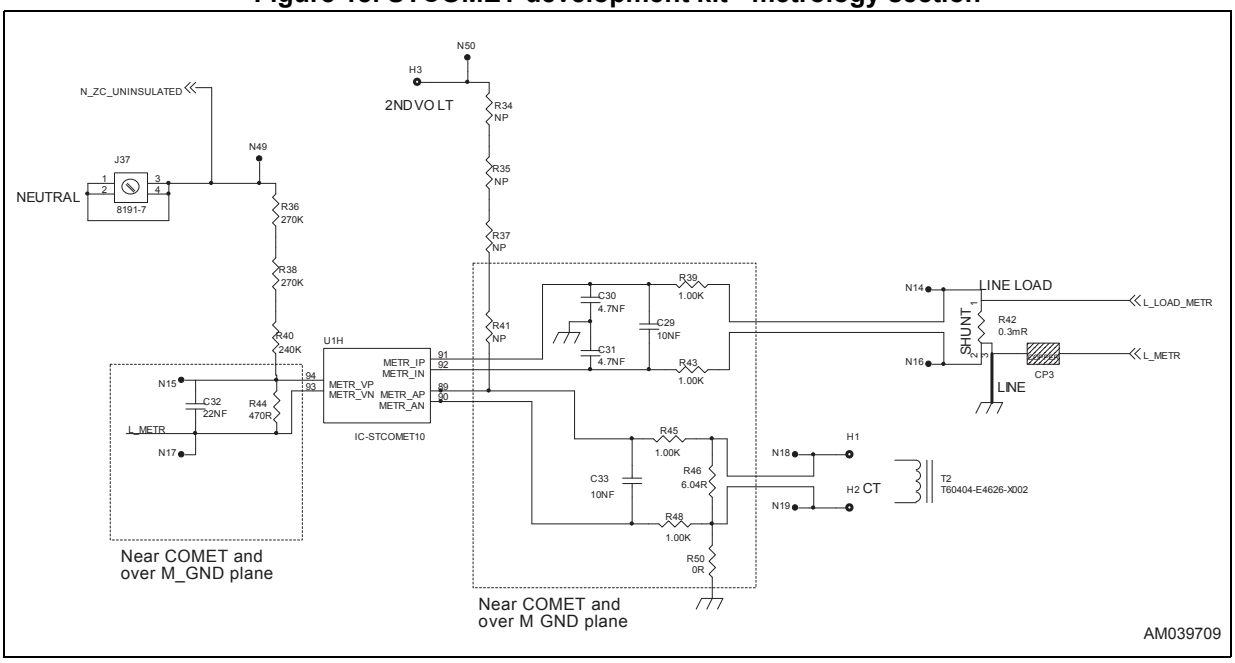
7.3 Metrology section

The STCOMET integrates the metrology function, which includes a 3-channel AFE with 24-bit sigma-delta converters and a dedicated DSP. The STCOMET implements all the features needed for a single-phase energy meter, providing effective measurement of the active and reactive energy, V rms, I rms, instantaneous voltage and current.

In the STCOMET development kit, the three metrology input channels are mapped as follows (see *Figure 18*):

- Channel METR_VP / METR_VN for measuring the mains voltage
- Channel METR_IP / METR_IN for measuring the current through a shunt sensor
- Channel METR_AP / METR_AN for measuring the current through a current transformer sensor.

Figure 18. STCOMET development kit - metrology section



Mains connections are illustrated in *Figure 4 on page 10*.

The metrology LED0 and LED1 on the LCD module (*Figure 23 on page 35*) are blinking according respectively to the cumulative active power and reactive power.

The STCOMET metrology features can be evaluated by using a dedicated GUI.

7.3.1 Metrology circuit description

Current measurement

Anti-aliasing filters are implemented between the shunt, current transformer and the STCOMET for distortion reduction caused by sampling.

Voltage measurement

A resistor divider is used as a voltage sensor. The 780 kΩ resistor is separated into four in series 1% resistors (270 kΩ, 270 kΩ, 240 kΩ, 470 Ω), which ensure robustness against a high voltage transient. This also reduces the potential across the resistors, thereby decreasing the possibility of arcing.

The STCOMET kit also allows to use the channel METR_AP / METR_AN for a second voltage measurement if necessary, for example to monitor the mains voltage after the line breaker. The following BOM modifications must be applied in that case:

- R34 = 620 kΩ
- R35 = R37 = 470 kΩ
- R41 = R45 = R48 = 0 Ω
- R50 = 470 Ω
- C33 = 22 nF.

Metrology zero crossing

The metrology section is including a built-in metrology zero crossing, independent from PLC zero crossing information. This zero crossing signal is based on voltage applied at METR_VP / METR_VN inputs, and can be made available on the STCOMET GPIO06_7 or GPIO09_5 pin.

In principle, it is possible to connect the metrology zero crossing output to ZC_IN input for the PLC section, by adding a 1 µF series capacitor to the ZC_IN and a 1 MΩ resistor (not present on the board) between the ZC_IN pin and AGND, with the JP8 = JP9 = open in this case. Please note that in this use case the delay on PLC zero crossing information is much higher, reaching about a quarter of the mains period.

The timing characteristics of the metrology zero crossing signal, according to the oscilloscope measurements on GPIO09_5 reported below, are listed in *Table 8*.

Table 8. Zero crossing through metrology coupling - measured timing characteristics

Edge	ZC delay	ZC jitter
Positive	4.95 ms	27 µs
Negative	4.94 ms	31 µs

Figure 19. Zero crossing through metrology coupling - positive edge delay

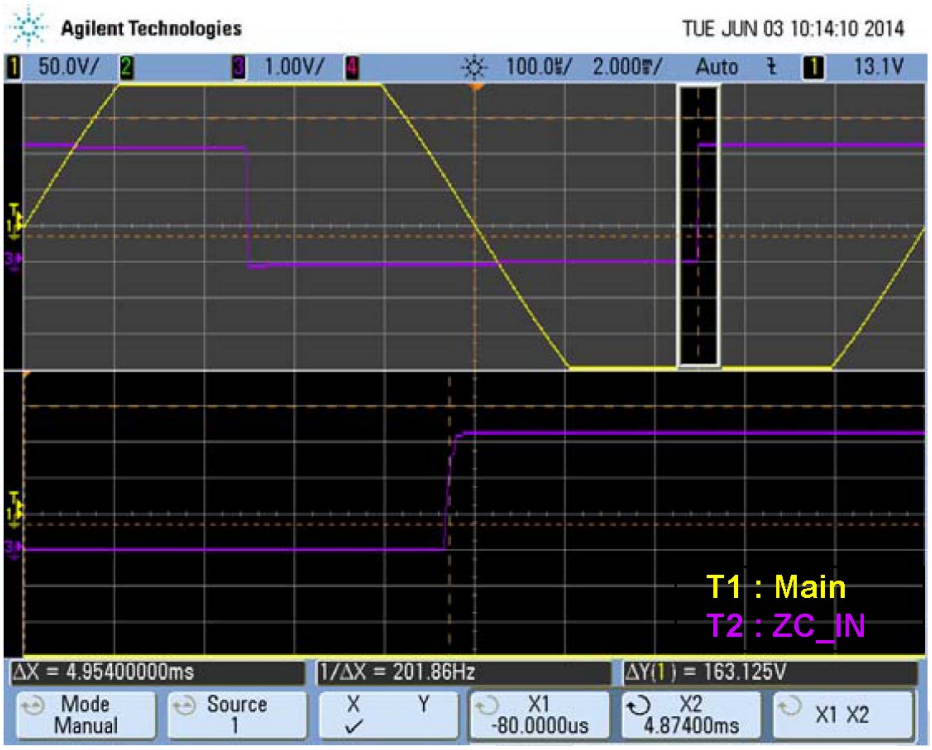
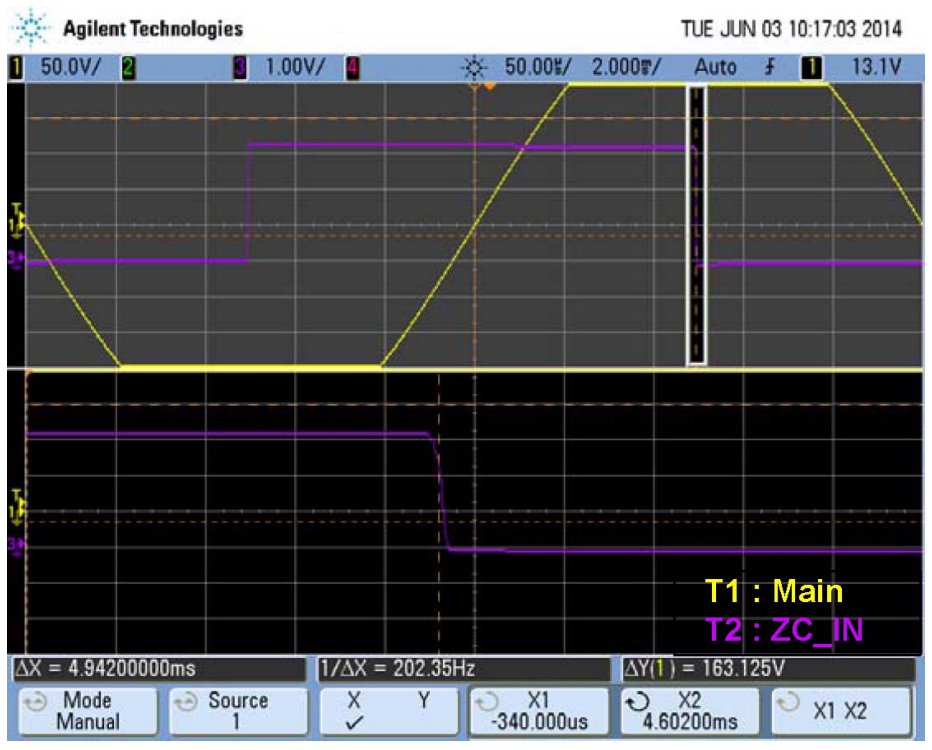


Figure 20. Zero crossing through metrology coupling - negative edge delay



7.3.2 Three-phase metrology evaluation

The STCOMET development kit provides an SPI/UART interface (J2 connector) and general purpose signals (J3 connector) on the LCD module (*Figure 23*) to connect STPMxx metrology boards in order to build a three-phase meter development kit.

Figure 21 reports the J2 and J3 pinout plus the configuration jumpers to select between the UART and SPI connection to the external STPMxx board. *Table 9* describes the jumper configuration to select SPI or UART configuration.

Figure 21. Three-phase metrology evaluation - digital connections to STPMxx evaluation boards

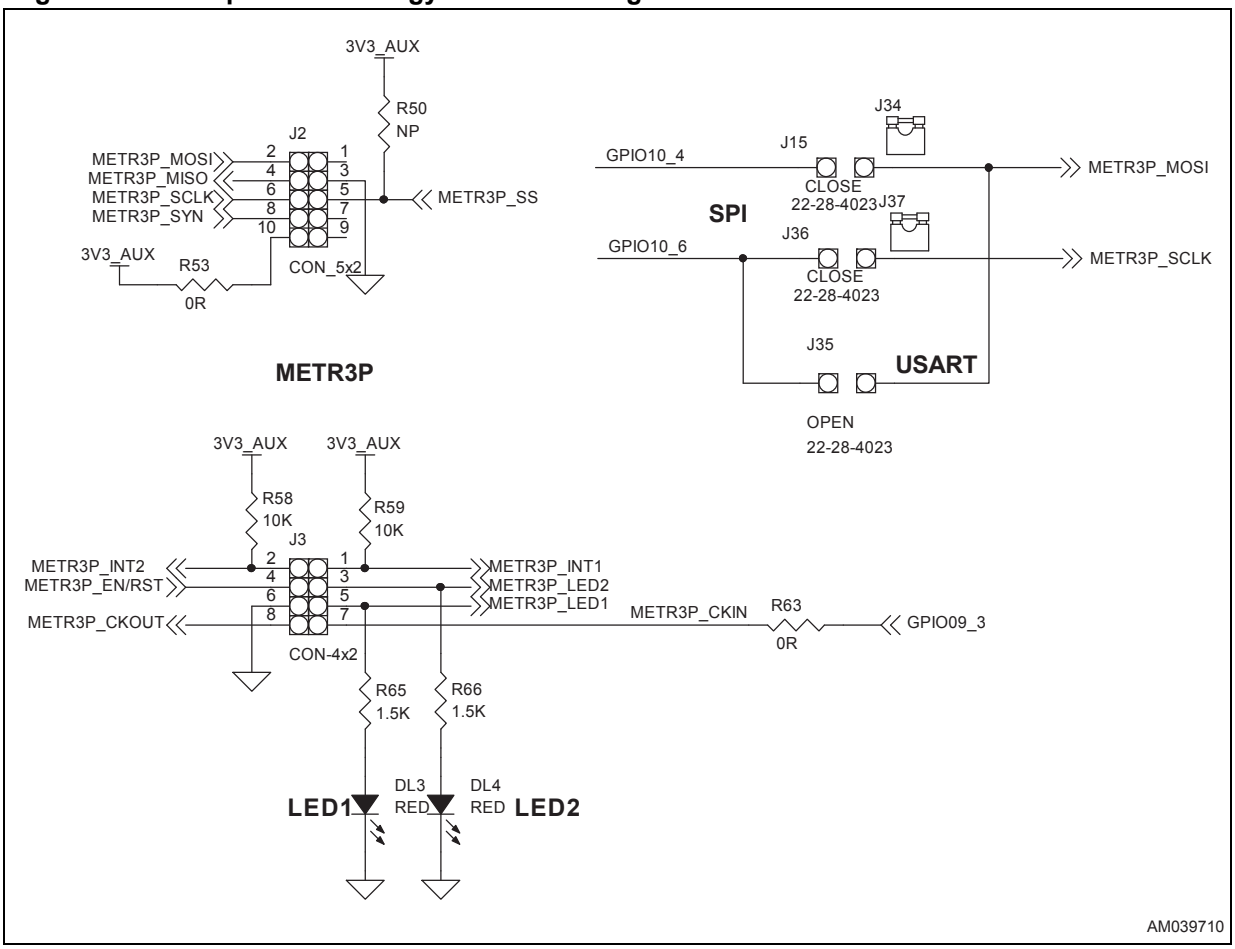


Table 9. Three-phase metrology evaluation - SPI/UART configuration

Jumper	SPI configuration	UART configuration
J15	Close	Open
J35	Open	Close
J36	Close	Open
R50	NP	1 kΩ

7.4 Line breaker section

The STCOMET development kit allows controlling a line breaker relay for remote electrical disconnection. The circuit is based on the ST L2293Q driver, see the datasheet for additional information.

An external voltage supply VR (0 - 36 V max.) must be applied between the J5 pin 4 (GND) and J5 pin 3 (+) as coil driving voltage. The value of the VR must be in agreement with the coil rating.

The line breaker coil must be connected between J5 pins 1 and 2.

The STCOMET GPIOs GPIO00_0 and GPIO00_1 allow to control the voltage applied to the relay coil according to *Table 10*.

Table 10. Line breaker driver - GPIO control

GPIO00_0	GPIO00_1	VRA (J5 pin 2)	VRB (J5 pin 1)	Function
H	L	VR	GND	Turn ON
L	H	GND	VR	Turn OFF
L	L	GND	GND	Keep state (zero current)
H	H	VR	VR	Keep state (zero current)

The J5 is a MOLEX male connector, P/N 22-27-2041. It is designed to be plugged with the female connector MOLEX P/N 22-01-2045.

7.5 STCOMET I/O section

On the STCOMET main board, the I/O section provides the following features:

- External access through several interface types: USB, SPI, I^2C, USART, JTAG, CAN
- Use up to 86 GPIOs
- Control LCD display
- Use up to 6 ADC channels
- Control STPMxx extension boards for three-phase metering
- Manage tamper events
- Manage metrology LEDs

7.5.1 STCOMET system

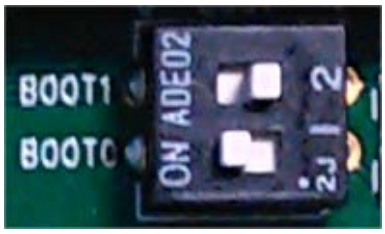
Basic system control of the STCOMET device is listed in *Table 11*.

Table 11. STCOMET main board - system

Connection	Connection type	STCOMET pins	Notes
Reset	Digital	74	Complete reset of the system (push button for reset)
JTAG	Digital	18, 20, 21, 19, 22	Connected to the Segger J-Link OB section (see *Section 6.2 on page 12*)
BOOT MODE	Digital	BOOT0 pin 15 BOOT1 pin 17	Define boot mode as specified in *1.* of *Section 12 on page 52* Configured via DIP switches

The default boot configuration is the normal boot mode (BOOT1 = 1, BOOT0 = 0), as depicted in *Figure 22*.

Figure 22. Default boot switch configuration (normal boot mode)



7.5.2 STCOMET GPIOs mapping

The STCOMET has 86 GPIOs assigned to specific function, as listed below. All GPIOs are connected to the strip connectors on the LCD module and clearly identified on the PCB silkscreen.

Table 12. GPIO assignment table for the STCOMET development kit

GPIO	Description	Connection
GPIO00_0	RELAY_A external relay command	L2293Q on main board
GPIO00_1	RELAY_B external relay command	L2293Q on main board
GPIO00_2	Not used	-
GPIO00_3	Not used	-
GPIO00_4	Not used	-
GPIO00_5	Not used	-
GPIO00_6	I2C0_SDA EEPROM data	EEPROM on main board
GPIO00_7	I2C0_SCL EEPROM clock	EEPROM on EVBSTCOMET

Table 12. GPIO assignment table for the STCOMET development kit (continued)

GPIO	Description	Connection
GPIO01_0	Not used	-
GPIO01_1	UART1_TXD	CP2105 on main board
GPIO01_2	UART1_RXD	CP2105 on main board
GPIO01_3	UART1_RTS	CP2105 on main board
GPIO01_4	UART1_CTS	CP2105 on main board
GPIO01_5	Not used	-
GPIO01_6	Not used	-
GPIO01_7	Not used	-
GPIO02_0	Not used	-
GPIO02_1	Not used	-
GPIO02_2	Not used	-
GPIO02_3	Not used	-
GPIO02_4	Not used	-
GPIO02_5	Not used	-
GPIO02_6	Not used	-
GPIO02_7	Not used	-
GPIO03_0	Backlight LCD on LCD module	LCD on LCD module
GPIO03_1	Not used	-
GPIO03_2	LCD_R/Wn	LCD on LCD module
GPIO03_3	LCD_EN	LCD on LCD module
GPIO03_4	LCD_SPI3_MOSI	LCD on LCD module
GPIO03_5	LCD_RS	LCD on LCD module
GPIO03_6	LCD_SPI3_SCLK	LCD on LCD module
GPIO03_7	LCD_SPI3_SS	LCD on LCD module
GPIO04_0	LCD_D0	LCD on LCD module
GPIO04_1	LCD_D1	LCD on LCD module
GPIO04_2	LCD_D2	LCD on LCD module
GPIO04_3	LCD_D3	LCD on LCD module
GPIO04_4	LCD_D4	LCD on LCD module
GPIO04_5	LCD_D5	LCD on LCD module
GPIO04_6	METR_CMD1	Button on LCD module
GPIO04_7	METR_CMD2	Button on LCD module
GPIO05_0	Not used	-
GPIO05_1	Not used	-
GPIO05_2	Not used	-

Table 12. GPIO assignment table for the STCOMET development kit (continued)

GPIO	Description	Connection
GPIO05_3	Not used	-
GPIO05_4	Not used	-
GPIO05_5	UART0_RTS	CP2105 on main board
GPIO05_6	UART0_CTS	CP2105 on main board
GPIO05_7	IRDA_SD	IrDA on LCD module
GPIO06_0	UART3_TXD	IrDA on LCD module
GPIO06_1	UART3_RXD	IrDA on LCD module
GPIO06_2	Not used	-
GPIO06_3	Not used	-
GPIO06_4	Not used	-
GPIO06_5	Not used	-
GPIO06_6	Not used	-
GPIO06_7	Not used	-
GPIO07_0	Not used	-
GPIO07_1	Not used	-
GPIO07_2	Not used	-
GPIO07_3	Not used	-
GPIO07_4	Not used	-
GPIO07_5	Not used	-
GPIO07_6	Not used	-
GPIO07_7	Not used	-
GPIO08_0	LED0_debug	LED0 on the main board
GPI08_1	LED1_debug	LED1 on the main board
GPIO08_2	LED2_debug	LED2 on the main board
GPIO08_3	LD3_debug	LED3 on the main board
GPIO08_4	Not used	-
GPIO08_5	Not used	-
GPIO09_0	METR3P_INT1	J3 METR3P on LCD module
GPIO09_1	METR3P_INT2	J3 METR3P on LCD module
GPIO09_2	METR3P_EN/RST	J3 METR3P on LCD module
GPIO09_3	METR_LED0	LED0 METR on LCD module
GPIO09_4	METR_LED1	LED1 METR on LCD module
GPIO09_5	Not used	-
GPIO09_6	METR3P_LED1	LED1 METR3P on LCD module
GPIO09_7	METR3P_LED2	LED2 METR3P on LCD module

Table 12. GPIO assignment table for the STCOMET development kit (continued)

GPIO	Description	Connection
GPIO10_0	METR3P_CKOUT	J3 METR3P on LCD module
GPIO10_1	Not used	-
GPIO10_2	METR3P_SYN	J2 METR3P on LCD module
GPIO10_3	METR3P_MOSI	J2 METR3P on LCD module
GPIO10_4	METR3P_MISO	J2 METR3P on LCD module
GPIO10_5	METR3P_SCLK	J2 METR3P on LCD module
GPIO10_6	METR3P_SS	J2 METR3P on LCD module
GPIO10_7	Not used	-

7.5.3 STCOMET Flash SPI0 and EEPROM interfaces

The STCOMET SPI0 interface is connected to an external M25P16 16-Mbit SPI Flash for the FW upgrade.

The I2C0 interface allows storing metrology or other application data into the M24512 EEPROM memory.

7.5.4 STCOMET UART0 and UART1

The STCOMET development kit provides two UARTs over the same isolated USB port connector CN2:

- UART0 corresponds to the Silabs CP2105 enhanced COM port
- UART1 corresponds to the Silabs CP2105 standard COM port.

7.5.5 STCOMET tamper inputs

Two push buttons TPA and TPB, connected respectively to RTC_TAMPA and RTC_TAMPB, are present on the LCD module to simulate tamper events.

7.5.6 STCOMET JTAG interface

The STCOMET development kit provides a debug JTAG interface via the J-Link on-board over an isolated USB port connector CN3.

7.5.7 General purpose push buttons and LEDs

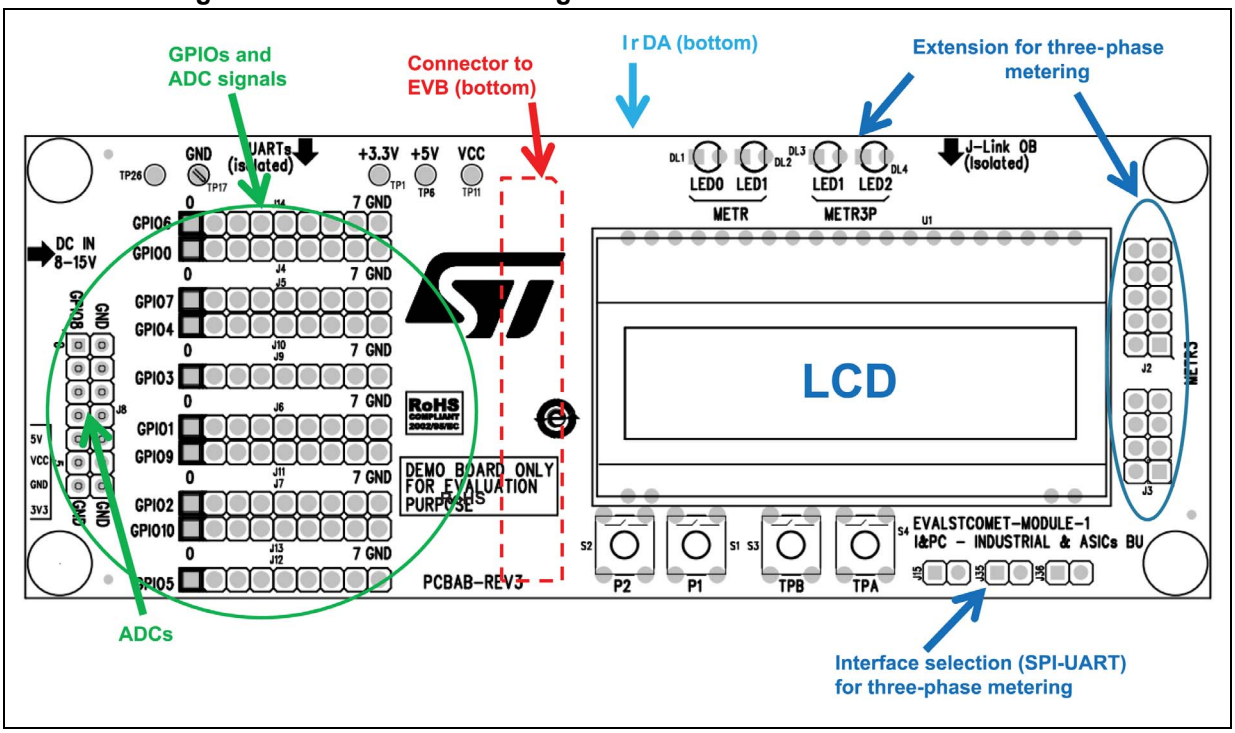
The STCOMET development kit provides a LCD display that could be used to develop a meter application example. Two push-buttons P1 and P2 on the LCD module could be used as inputs for a software application purpose (*Figure 23*).

8 LCD module description

On the top of the STCOMET main board, the LCD module provides:

- LCD display for metering and application information
- LED0 and LED1 for energy measurement
- TPA and TPB buttons to simulate tamper events
- P1 and P1 buttons for any application menu (on LCD)
- All GPIOs and ADC signals accessible thanks to strip connectors
- Extension connectors plus 2 metering LEDs for three-phase metering configuration
- IrDA interface

Figure 23. LCD module drawing with indication of the various sections



9 EN50065 compliance tests

Table 13 lists all the EMC/EMI compliance tests required by the European standard EN50065 for smart metering PLC applications on the low voltage network (which have the highest EMC test levels).

All applicable tests have been carried out on the STCOMET development kit. Full EMC compliance to the EN50065 part 1, 2 - 3 and 7 has been officially achieved with PRIME A-band implementation, while successful pre-compliance tests have been carried out for other PLC implementations.

All immunity tests require a communication link to be established between the equipment under test (EUT) and a stimulus device. During such tests, the presence of a communication is monitored to verify the acceptance criteria according to the specific test.

Table 13. List of standard tests required for EMC compliance to EN50065 - A-band PLC applications

Type	Basic standard	Test	Result
PLC transmission: Conducted measurement	EN 50065-1	Bandwidth measurements	PASS(1)
	EN 50065-1	Maximum output levels	PASS(1)
Conducted disturbance measurements	EN 50065-1, EN 55022	Conducted emissions (9 kHz - 30 MHz)	PASS(1), (2)
Radiated disturbance measurements	EN 50065-1, EN 55022	Radiated emissions (30 MHz - 1 GHz)	PASS(2)
Radiated immunity	EN 61000-4-3	RF radiated fields immunity test (80 - 1000 MHz, 10 V/m)	PASS
	EN 61000-4-8	Magnetic 50 Hz field immunity test (100 A/m, 300 A/m)	Not applicable
Contact/radiated immunity	EN 61000-4-2	Electrostatic discharges immunity test (8 kV contact and air mode)	PASS(3)
Conducted immunity	EN 61000-4-6	RF conducted signals immunity test (150 kHz - 80 MHz, 10 V rms)	PASS(3)
	EN 50065-2-3	Narrow-band signals immunity test (95 kHz-150 kHz; 150 kHz - 30 MHz)	PASS(3)
	EN 61000-4-4	Fast transients immunity test (2 kV, 5 kHz)	PASS(3)
	EN 61000-4-5	Surge immunity test (4 kV, common mode and differential mode)	PASS(3)
	EN 61000-4-11	Power voltage dips and interruption (30% - 10 ms; 60% - 100 ms; 100% - 5 s)	PASS(2), (3)
Input impedance measurement	EN50065-7	RX impedance	PASS(1)
		TX impedance	PASS(1)

1. Related to specific PLC protocol implementation.
2. Results impacted by the VIPER26H power supply module.
3. In case of non-metering applications, communicating outside the CENELEC A-band, please refer to the immunity requirements listed in the EN50065-2-1 document, which may set lower limits for some tests.

10 Design guidelines

10.1 PCB layout guidelines

10.1.1 PCB structure

The STCOMET main board PCB data are listed in *Table 14*.

Table 14. STCOMET main board PCB data

Parameter	Value
Number of layers	4
Laminate type or IPC-4101 categorization	FR4
Board thickness	1.60 mm
Base copper thickness (inner layers)	18 /1 8 µm
Finished copper thickness (outer layers)	35 / 35 µm
Size of PCB unit	115 x 128 mm

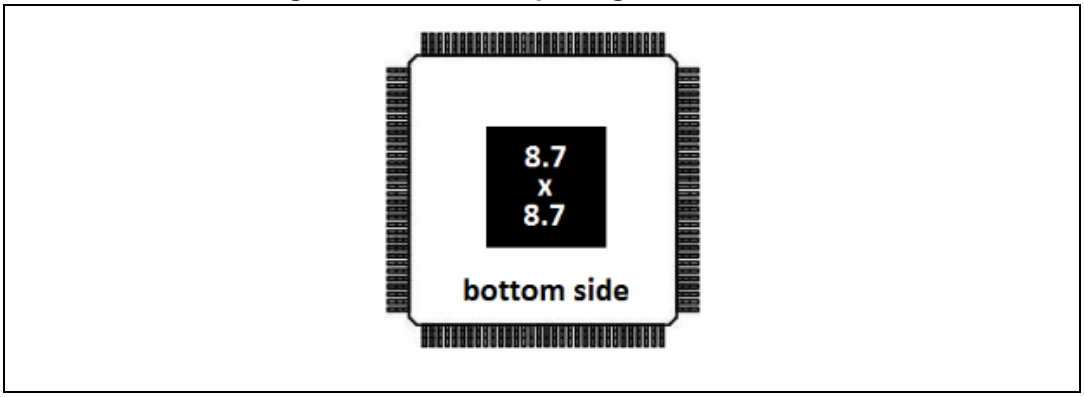
10.1.2 Design for thermal performance

The STCOMET device can operate within the standard industrial temperature range, from -40 to 85 °C ambient temperature. Especially in high ambient temperature conditions, the effect of the power dissipation of the device must be considered to keep it operating in safe conditions.

Even if the STCOMET features thermal protection, the role of the PCB design to ensure proper dissipation is the most important.

A TQFP176 package with an exposed pad (internally connected to DGND) has been chosen for the STCOMET device to have a very good thermal performance. To take full advantage from this, the PCB must be designed to effectively conduct heat away from the package.

Figure 24. STCOMET package - bottom view



To get a low impedance thermal path to the PCB, a 9.5 x 9.5 mm thermal pad has been realized on the top layer under the device. In order to effectively remove the heat, the exposed pad must be well soldered to the PCB thermal pad.

In order to have an effective heat transfer from the top layer of the PCB to the bottom layer, thermal vias need to be included within the thermal pad area. If properly designed, thermal vias are the most efficient paths for removing heat from the device.

The layout recommendations are therefore:

For the top layer:

- Top layer function is to transmit heat from the package to the bottom layer
- The DGND copper area must be placed under the exposed pad, extending as much as possible around the device
- An array of 9 x 9 thermal vias (top to bottom layer) at the 1.0 mm pitch, diameter 0.3 mm, shall be incorporated under the exposed pad, plus enough vias from the DGND top plane to the bottom layer plane
- Any unused area outside of the package must be filled with copper tied to the dissipating DGND plane on the bottom layer.

For the bottom layer:

- The bottom layer acts as the real radiator
- The solid DGND area of copper on this layer must be as large as possible to minimize the thermal impedance
- To minimize solder wicking effect due to open vias, possibly leading to poor soldering of the TQFP176 exposed pad, the via encroaching technique can be adopted. The bottom side solder resist shall have small openings (nearly 0.2 mm larger than the via drill diameter) around the vias; the reduced area of exposed copper on the bottom reduces the amount of solder paste flowing down the vias
- Traces on the bottom side must run as far as possible from the device area.

Figure 25. PCB dissipating area on top layer for the STCOMET development kit board

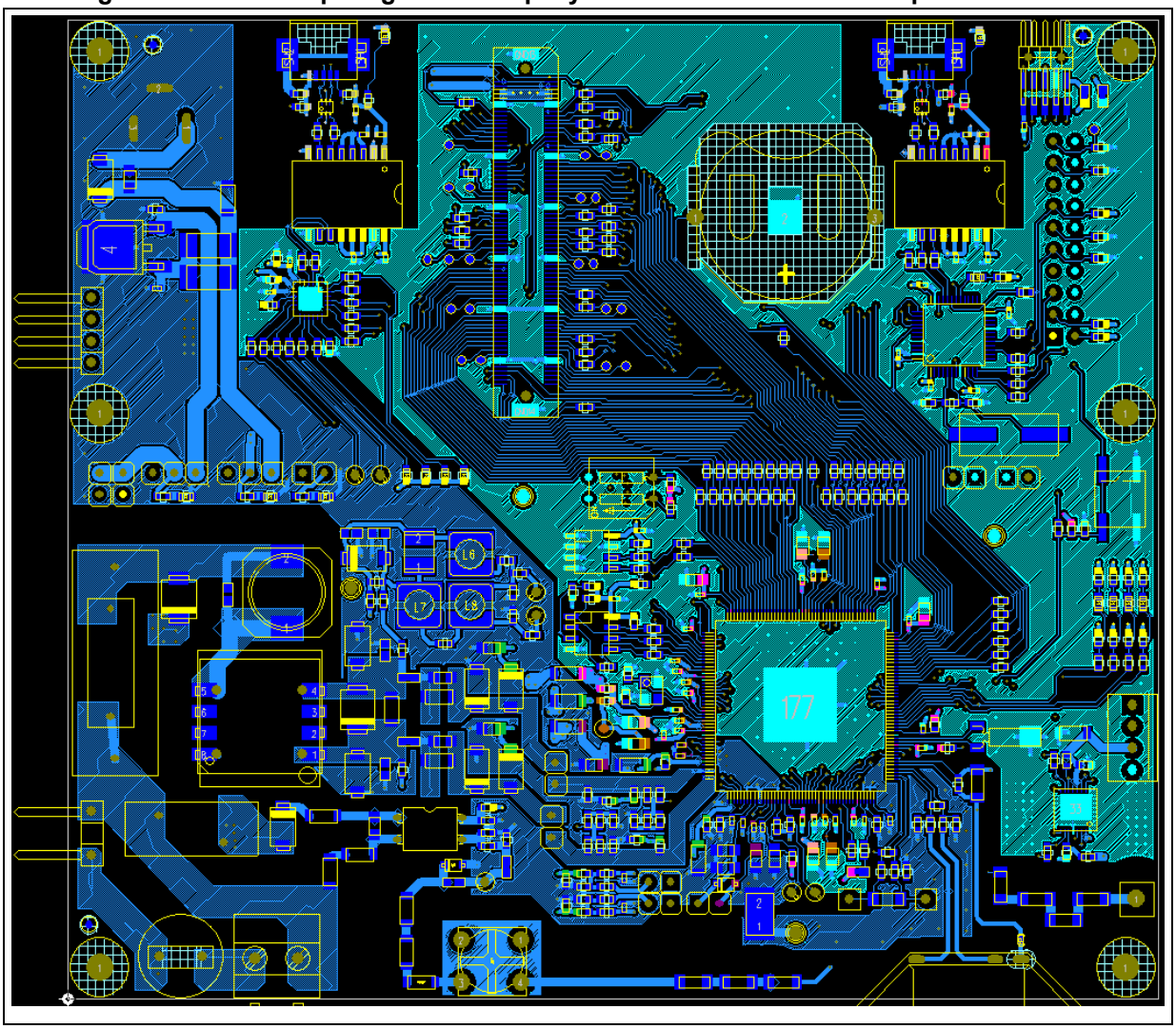
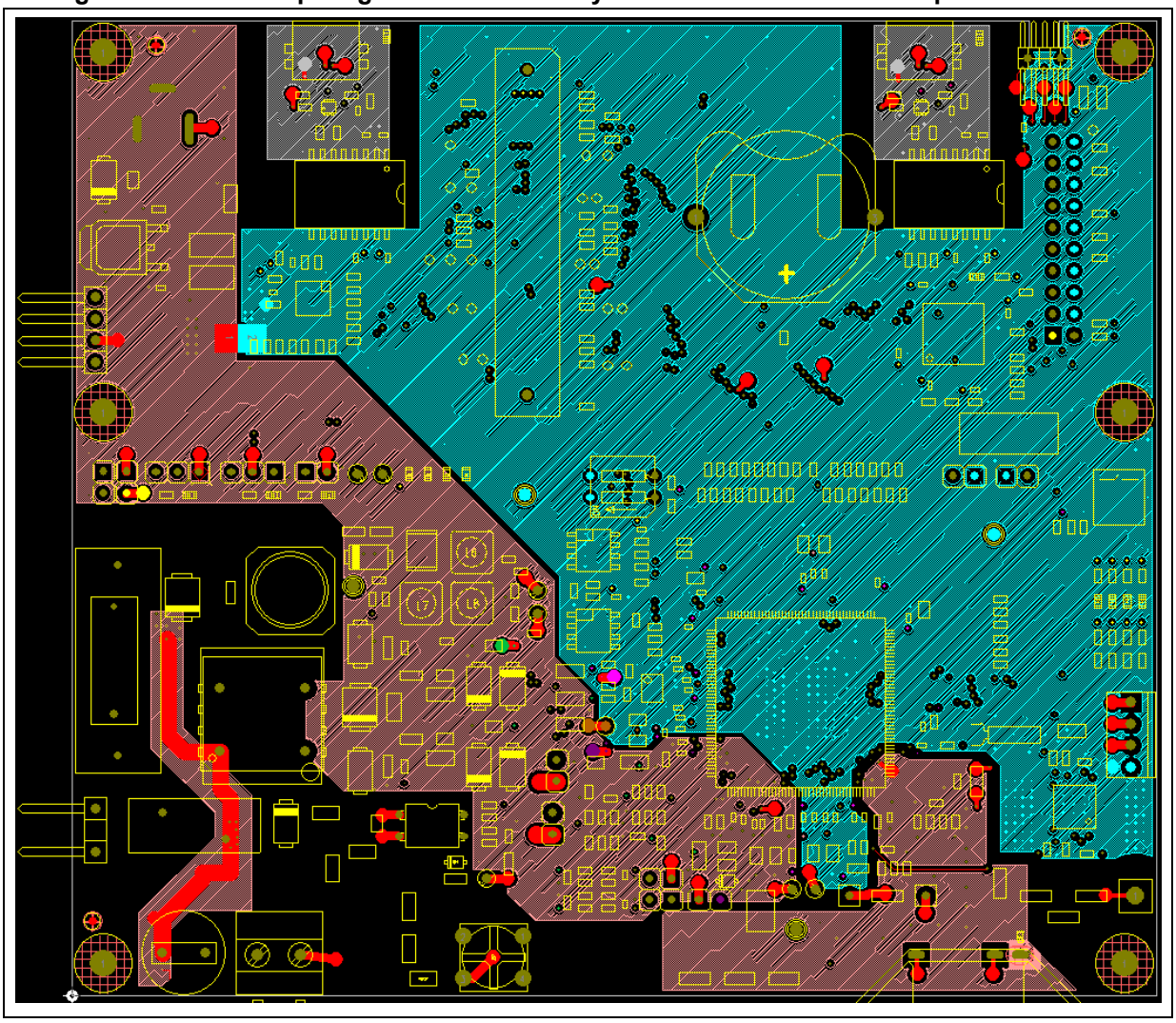


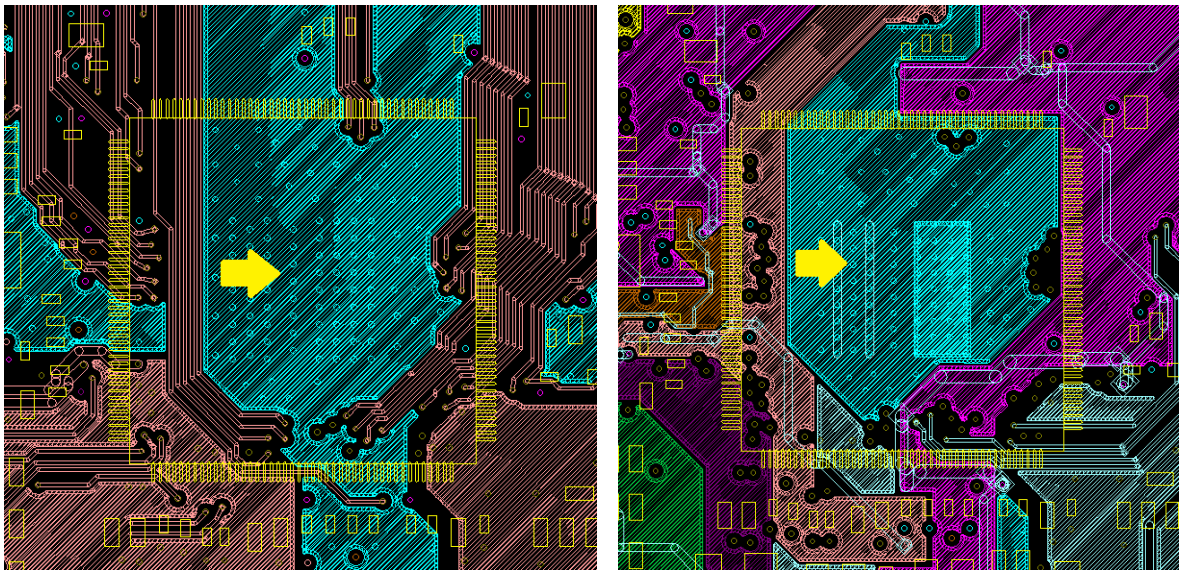
Figure 26. PCB dissipating area on bottom layer for the STCOMET development kit board



On internal layers:

A large area under the STCOMET package must be dedicated to DGND, in order to allow vias making the connection between top and bottom layers.

Figure 27. Internal layers under STCOMET package (L2 = left, L3 = right) for thermal dissipation on STCOMET development kit board



10.1.3 Ground connections

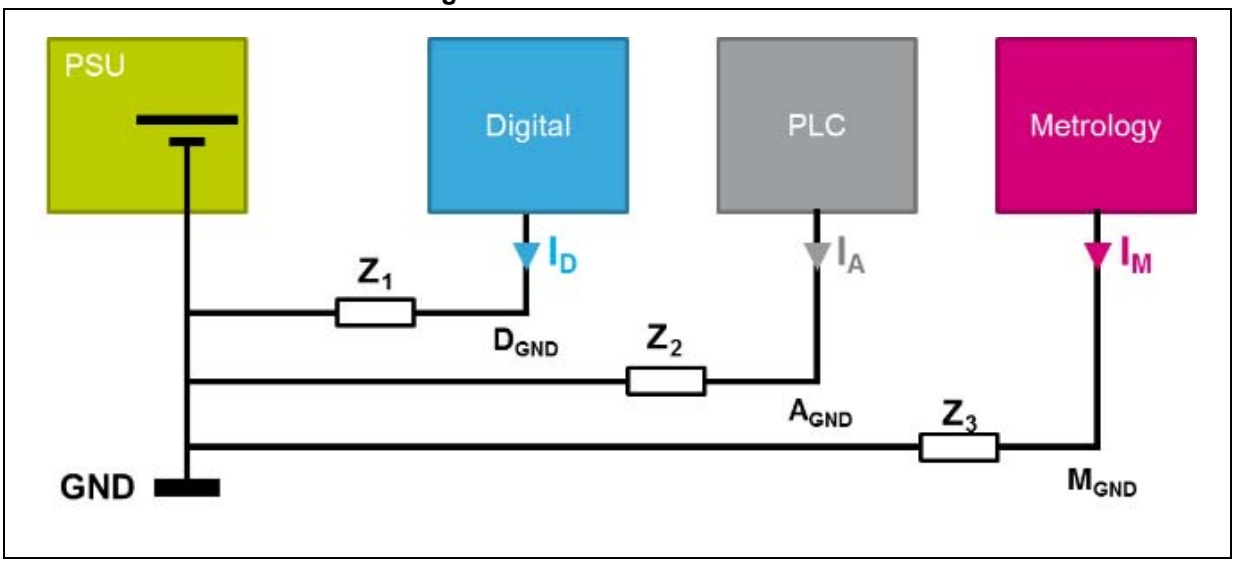
The STCOMET system has 3 distinct ground references: analog (AGND) mainly for PLC, metrology (MGND), and digital (DGND).

It is very important to filter each supply pin to its respective ground. Please refer to the STCOMET datasheet for the association between each supply rail and the correct ground. Good soldering of the STCOMET exposed pad (DGND) is also required to minimize ground noise.

In addition, it is recommended to realize a star connection of the 3 ground planes at the PCB level in order to guarantee good signal integrity. *Figure 28* and *Figure 29* illustrate what are the benefits of such star topology.

Let's consider that GND tracks have not a null impedance but Z1, Z2, and Z3.

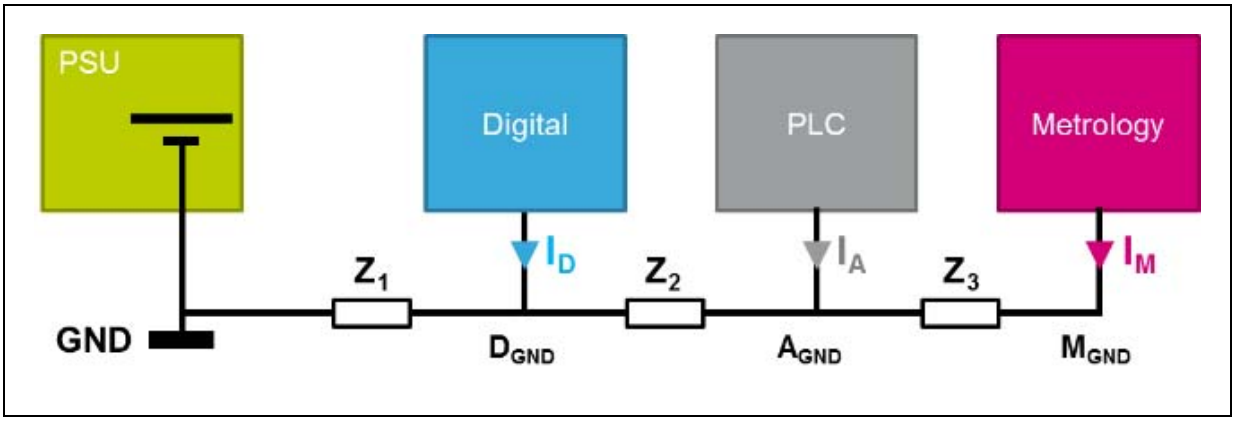
Figure 28. Star GND connection



In *Figure 28*, the voltage offsets are limited to the following values:

- $D_{GND} = GND + Z_1 \times I_D$
- $A_{GND} = GND + Z_2 \times I_A$
- $M_{GND} = GND + Z_3 \times I_M$

Figure 29. Serial GND connection



In *Figure 29*, we can see that each ground reference is shifted with the following voltage offsets:

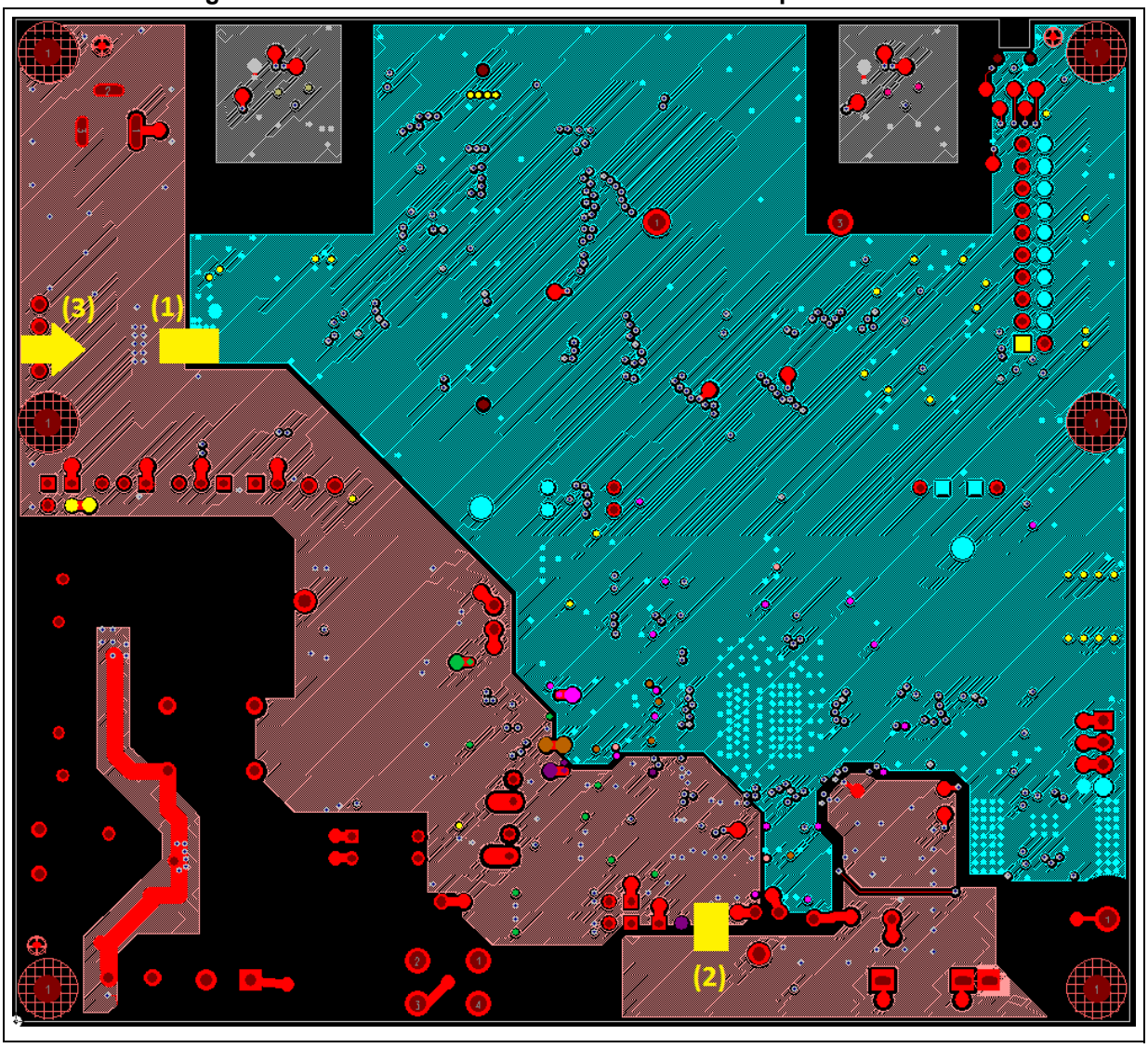
- $D_{GND} = GND + Z_1 \times (I_D + I_A + I_M)$
- $A_{GND} = GND + Z_1 \times (I_D + I_A + I_M) + Z_2 \times (I_A + I_M)$
- $M_{GND} = GND + Z_1 \times (I_D + I_A + I_M) + Z_2 \times (I_A + I_M) + Z_3 \times I_M$

The STCOMET development kit has been designed with respect of a GND star connection, especially between the digital and analog section as shown in *Figure 30*.

The PSU GND “(3)” is split between the AGND (green) and DGND (blue), at the position “(1)”.

The MGND (green area bottom right) is connected to the AGND at the position “(2)”. Due to distance between the MGND area and PSU GND, it was not possible to realize a full star connection, unless having a long dedicated track that would increase the PCB size.

Figure 30. GNDs connections on STCOMET development kit board



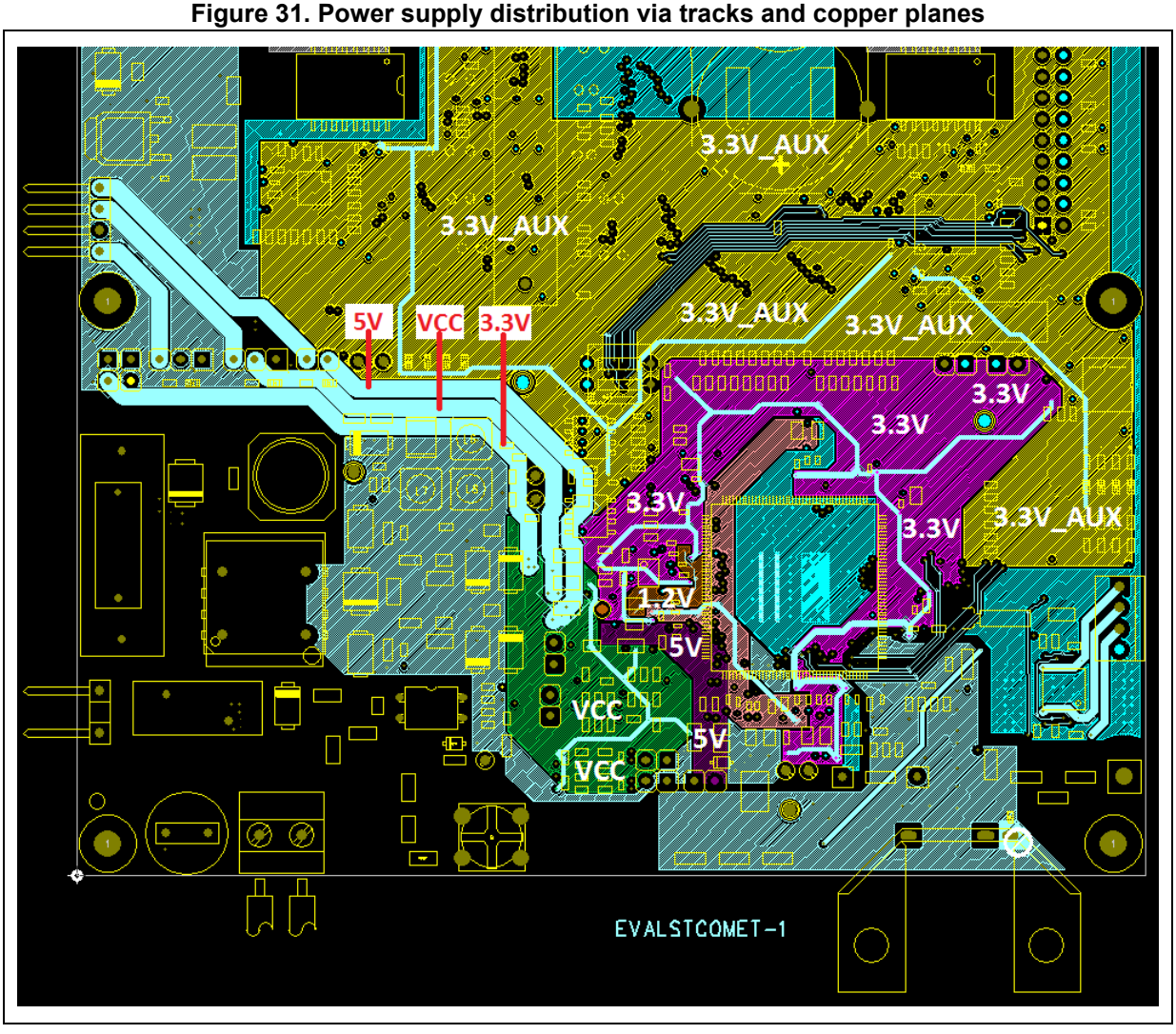
10.1.4 Power supply connections

Best practice rules must be applied to connection of STCOMET power supplies 3.3 V, 5 V and VCC.

Decoupling capacitors must be placed as close as possible to their dedicated pins, the smallest capacitor value being placed first. The associated capacitors/pins can be easily identified on the schematic thanks to dedicated wires: for instance, the C29 and C30 are dedicated to the pin 39, the C58 to the pin 83 and so on.

Wide tracks must be used for power supplies as much as possible. 2 mm wide tracks have been used to carry VCC, 5 V and 3.3 V from PSU input (J13) to ferrite beads L3, L4 and L5. Then, power has been deployed to the STCOMET using planes filling, as illustrated in *Figure 31*.

Figure 31. Power supply distribution via tracks and copper planes

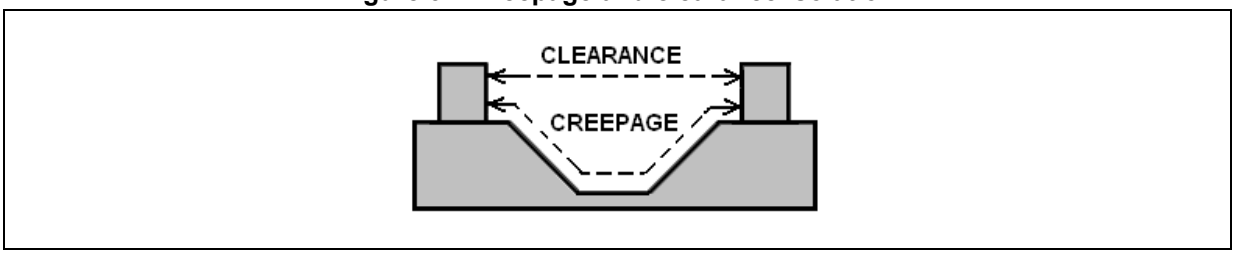


10.1.5 Mains voltage routing

The STCOMET development kit is connected to mains and as a consequence, special care has been taken when routing the high voltage signals (line and neutral) on the board.

Especially, a minimum isolation distance has been applied on the PCB between tracks connected to mains, considering both creepage and clearance.

Figure 32. Creepage and clearance isolation



The following extracts from schematics highlight the signals impacted by the isolation.

Figure 33. Tracks subject to specific isolation (1)

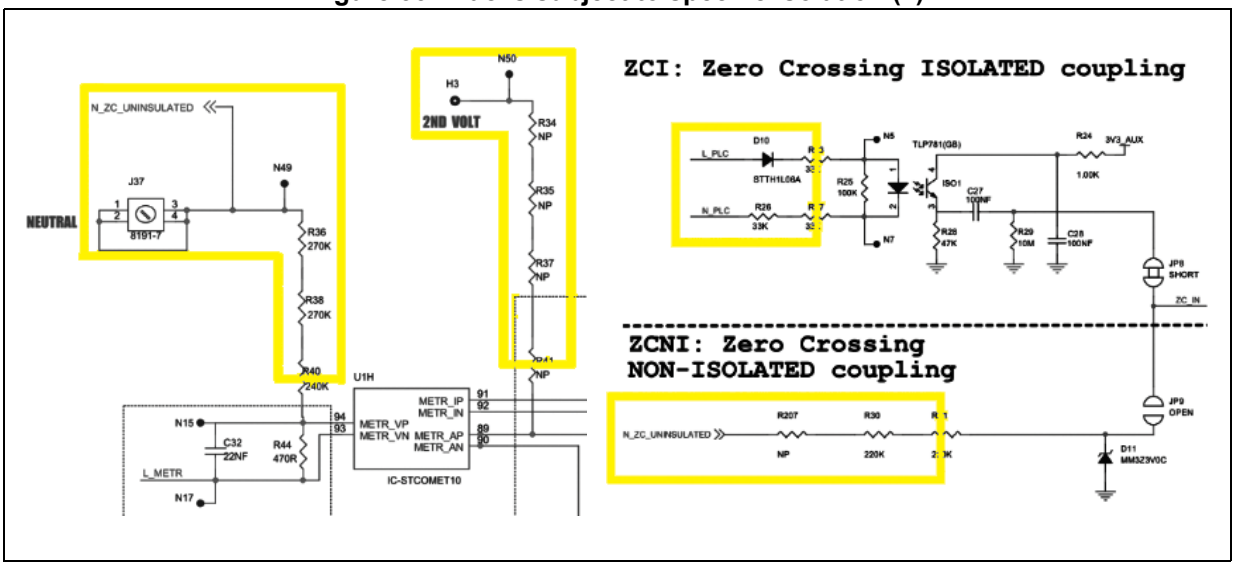
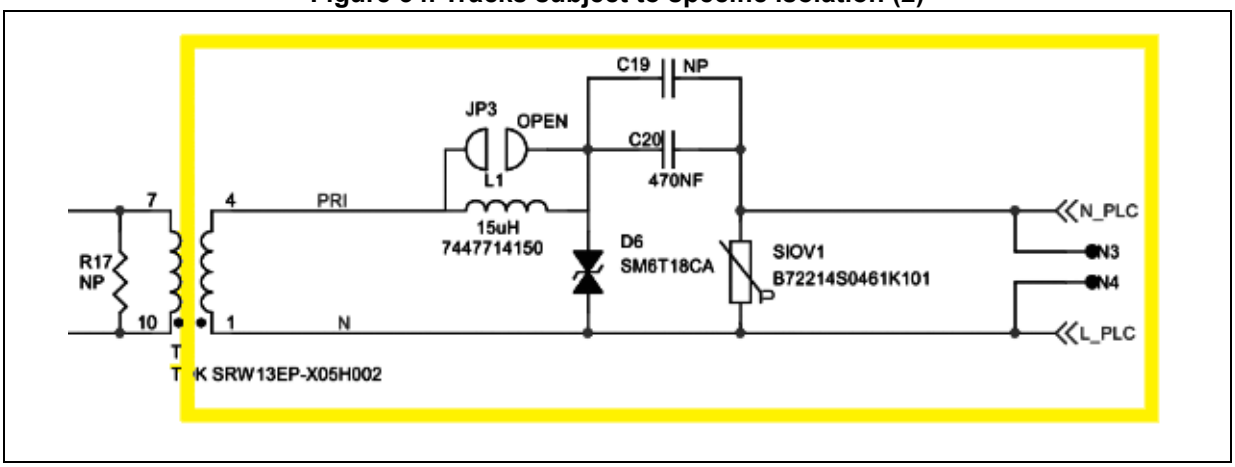


Figure 34. Tracks subject to specific isolation (2)



There are several industry and safety standards that describe different spacing requirements based on the voltage, application and other parameters.

The trace isolation on the STCOMET development kit has been set to 3.5 mm. This isolation corresponds (with 0.3 mm additional margin) to the UL 60950-1 standard, with the specific input data:

- RMS working voltage = 250 V
- Pollution degree = 3
- Material group = I

Please notice also that, in case high voltage tracks would be placed on the PCB edge and on the opposite layer, taking into account the creepage illustration in *Figure 32*, and considering a PCB thickness = 1.6 mm, as a consequence the minimal distance between the tracks and the PCB edge must be [3.5 mm - 1.6 mm] ÷ 2 = 0.95 mm.

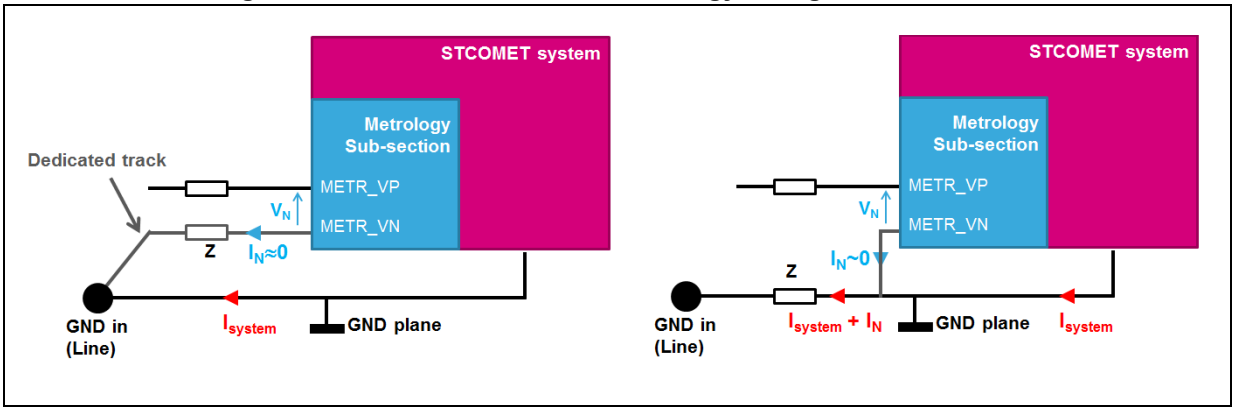
10.1.6 Metrology connections

Voltage measurement connection

The STCOMET METR_VP and METR_VN inputs are dedicated to the mains voltage measurement, through a resistor divider composed by R36 - R38 - R40 - R44. Dedicated tracks have be designed from the line (L) to METR_VN and from neutral (N) to the R36 for an accurate voltage measurement.

Particularly, the METR_VN input must not be tied directly to the GND ground plane at the pin level, as shown in *Figure 35*:

Figure 35. GND connection for metrology voltage measurement

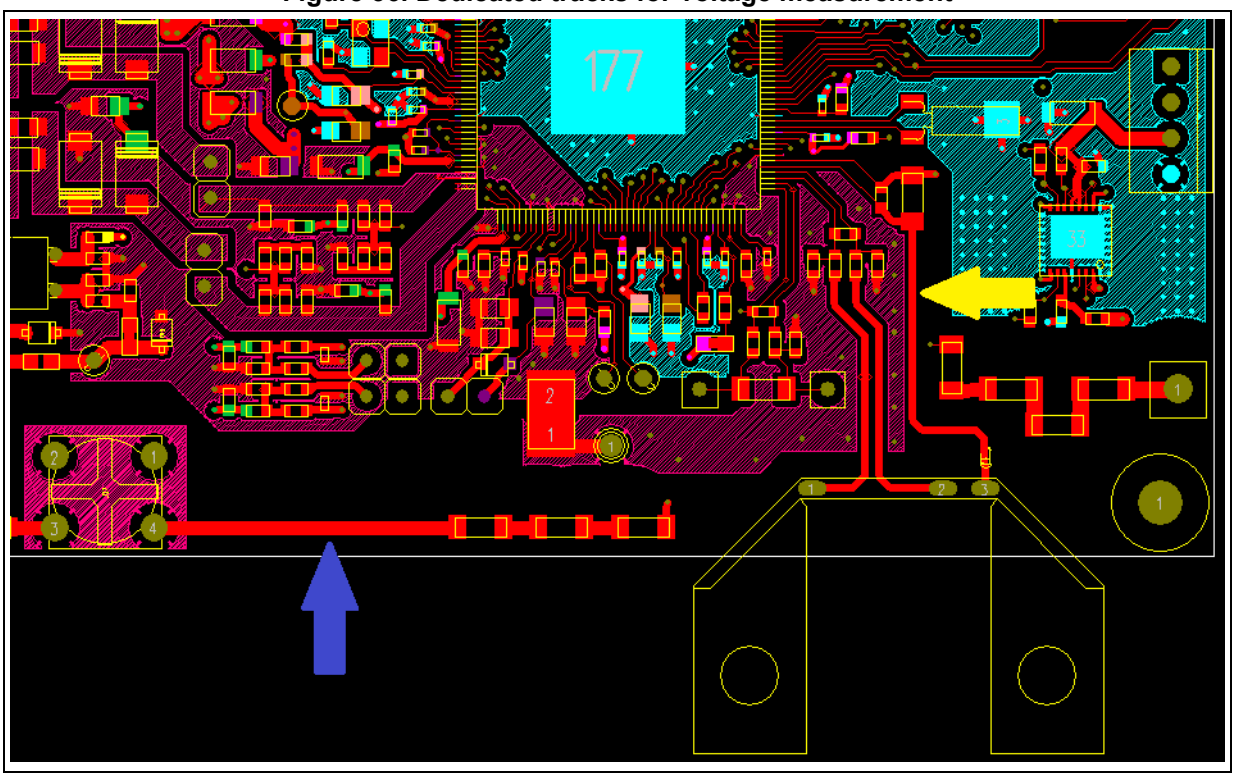


The mains voltage measurement is done between N and L (= GND). We can easily understand in *Figure 35* that if the METR_VN pin is directly tied to the GND plane (right configuration), the voltage VN present at COMET inputs will be shifted by Z x (I_{system} + I_N) compared to the real mains voltage, and this will introduce an error in the measurement. This error cannot be compensated by metrology calibration since I_{system} is not constant but depends on the STCOMET activity (e.g.: PLC transmission). However, if a dedicated track is used from the GND entrance to the METR_VN (left configuration), the error will be minimized due to low value of I_N and compensated by calibration.

The same recommendation can be applied to the neutral connection: use a dedicated track going from the J37 to R36.

The application of those recommendations on the STCOMET development kit is illustrated in *Figure 36* by the blue and yellow arrows.

Figure 36. Dedicated tracks for voltage measurement



10.2 Oscillator section

The STCOMET requires two quartz crystals connected to the internal oscillators:

- A 24 MHz oscillator for the main system clock and a quad frequency synthesizer (QFS)
- A 32.768 kHz oscillator for the real-time clock (RTC) function.

It is very important to keep the crystal oscillators as close as possible to the STCOMET device.

The resonant circuits must be far away from noise sources such as:

- Power supply switching circuitry
- Burst and surge protections
- Line coupling circuits
- Any PCB track or via carrying an RF switching signal

To properly shield and separate the oscillator section from the rest of the board, it is recommended to use a ground plane, on both sides of the PCB, filling all the area below the crystal oscillator. No tracks or vias, except for the crystal connections, should cross the ground plane.

Connecting the case to ground could be a good practice to reduce the effect of radiated signals on the oscillator.

The load capacitors C87 - C88 have been selected in order to center the 24 MHz oscillator, taking into account the additional capacitive load by the STCOMET pins and PCB. Those values may have to be changed for any design using a different PCB layout and crystal.

There is no need to place external load capacitors for the 32.768 kHz oscillator since there are integrated adjustable capacitors in the STCOMET at pins 100 and 101.

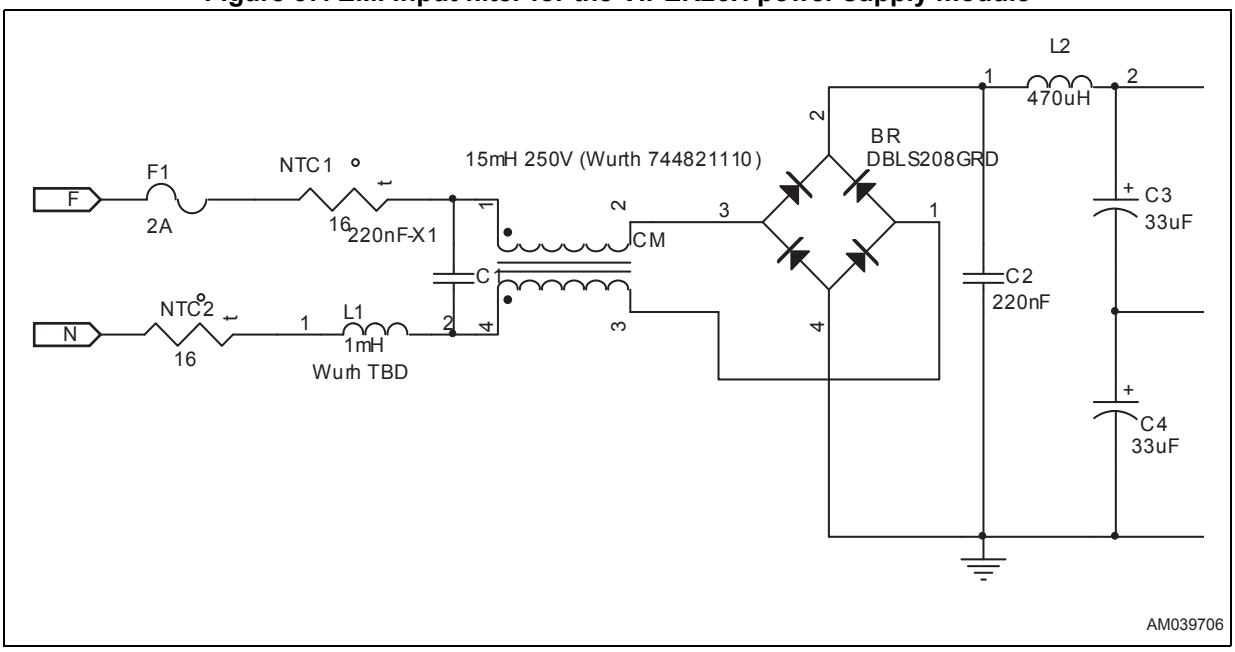
10.3 Power supply

The power supply circuit design is not only relevant in terms of available power. Two points are particularly sensitive for a power line communication application:

- The noise injected on the line
- The input impedance of the power supply unit

Both points involve the EMI input filter design. The circuit of *Figure 37* has been designed to have minimum influence on the STCOMET line coupling circuit, in terms of load impedance and linearity.

Figure 37. EMI input filter for the VIPER26H power supply module



It is recommended to have clamping protections placed on STCOMET DC supply voltages (one per rail) in case the external power supply is subject to voltage transients that can exceed the AMR of the device.

11 FAQ and troubleshooting

In this section the most frequently asked questions and the solution to common STCOMET development kit usage problems are described.

11.1 FAQ

Q: Is it possible to use the STCOMET on a medium or high voltage AC line?

A: Yes. A similar circuit solution as for the low voltage AC line can be used, provided that the coupling interface (and particularly line transformer, power inductor and X1 capacitor) guarantees adequate and safe isolation from the AC line.

Q: Is it possible to use the STCOMET on a DC or de-energized line?

A: Yes, the STCOMET can communicate over any wired connection, given that a suitable coupling circuit is used to connect the device to the line.

Q: Why with the power line communication cannot get I 100% reachability even though the range is few meters?

A: Probability lower than 100% to reach a PLC node within such a small distance can depend on two main factors:

- Attenuation or losses on the power line (for example because of some heavy capacitive load connected close to the transmitter)
- Noise coming from electric or electronic equipment connected on the power line (for example SMPS, ballasts, motors).

It can be useful to measure the signal level at the transmitter and receiver to understand if there are undesired losses. It is also important to measure the noise level and spectral distribution to find whether the PLC channel is somehow “jammed” by noise.

Q: Will the power line communication work if a power distribution transformer is present between two nodes?

A: The communication could work, but the transformer impedance at the signal frequency must be taken into account, since it could introduce strong attenuation in the signal level. A signal coupler (for example, a capacitive coupling) between the two sides of the distribution transformers could be required.

Q: What method of the coupling is preferred for the medium voltage and low voltage mains line: capacitive or inductive?

A: For the MV line, the capacitive coupling is preferable for the narrow-band PLC. In the case of a LV line, being the actual line impedance unpredictable because of the number of electrical devices connected on it, the solution should be an L-C series resonant circuit tuned at channel frequency, designed to have low Q even with very low line impedance (5 Ω and below).

Q: Why to use zero crossing synchronization?

A: The zero crossing synchronization is not mandatory for the power line communication, however it has several advantages.
For instance, it can improve the communication immunity against line noise, since most of the electric equipment generate noise on the power line in correspondence of the mains

voltage peak. Zero crossing synchronization allows establishing the link between the transmitter and receiver during the time with the minimum time-dependent noise.

Zero crossing synchronization is also needed for three-phase communication. In case that one node must communicate with nodes that are connected on other phases of the mains network, zero crossing synchronization allows understanding in which phase a certain message is coming from via delta-phase calculation.

Q: What could be the main sources of harmonic distortion in the STCOMET transmitted signal?

A: Generally, harmonics can rise up because of

- The high output current, due to low line impedance
- Saturation of magnetic components in the line coupling circuit, due to either poor dimensioning of the saturation current or to residual current at mains frequency
- The capacitive load applied to the line driver output
- The insufficient margin to the supply rails (low VCC or high output voltage).

11.2 Troubleshooting

1. **PROBLEM:** the STCOMET development kit doesn't work at all.

What to check:

a) Check that the AC mains supply cable is well connected.

b) Check the voltage on VCC, +5 V, +3.3 V, 1.2 V. All those voltages must be present for the STCOMET operation.

c) Check the jumper and switch configuration according to the selected power supply mode (*Table 2 on page 16*).

2. **PROBLEM:** the STCOMET development kit is not responding.

What to check:

a) Check if some activity is there when trying to communicate via the USB with the board.

b) Try disconnecting and reconnecting the USB cable; sometimes the USB driver fails during the COM port opening or installing.

3. **PROBLEM**: the STCOMET development kit board does not transmit.

What to check:

a) Check the bias voltage on the line driver output (on J1 and J3) with the oscilloscope probe referred to AGND. A DC voltage of VCC/2 must be measured.

b) Check the presence of the output signal on the line driver, TX pre-driver and DAC outputs while transmitting.

4. **PROBLEM:** the STCOMET development kit board transmits only for a short while; the transmission is interrupted.

What to check:

a) Verify the temperature of the STCOMET.

b) Check if there is the short-circuit (i.e.: capacitive) impedance on the mains at the carrier frequency. It could lead to device overheating and the line driver thermal shutdown.

5. **PROBLEM:** the STCOMET development kit board does not receive.

What to check:

Check if the transmitted signal reaches the STCOMET device by measuring the RX_IN voltage (TP2 and TP3) by the oscilloscope probe referred to AGND.

12 References

1. STCOMET datasheet
2. STCOMET development kit schematics and PCB layout
3. L2293Q datasheet

13 Normative references

EN50065: Signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz

- Part 1: General requirements, frequency bands and electromagnetic disturbances
- Part 2-3: Immunity requirements
- Part 4-2: Low voltage decoupling filters - Safety requirements
- Part 7: Equipment impedance

14 Revision history

Table 15. Document revision history

Date	Revision	Changes
01-Sep-2015	1	Initial release.
22-Oct-2015	2	Updated *Section : Introduction on page 1* (updated whole *Introduction*, replaced STCOMET by EVLKSTCOMET10-1, updated PLC protocols, added description, updated title of *Figure 1*). Minor modifications throughout document.
13-Sep-2017	3	Updated *Section 10.3 on page 48* (added text). Minor modifications throughout document.