AN4721
Application note

Hw recommendations for SPC570Sx device family

Introduction

SPC570Sx devices are members of a new family of microcontrollers designed for chassis and safety applications such as ABS and airbag which are Safety Integrity Level (SIL3) and Automotive SIL D (ASIL D) compliant.

The SPC570Sx is built on Power Architecture® technology and integrates technologies that are important for today's and tomorrow's automotive applications.

All the electrical characteristics of the SPC570Sx, including the absolute maximum ratings and recommended operating conditions (such as threshold voltages, maximum and minimum supply voltages), as well as the package mechanical drawings and pin assignments, can be found in the device datasheet (see *A.1: Reference documents*).

This application note complements the information provided in the device datasheet by describing the requirements for the implementation of the development board such as power supply, reset control, clock management, debug management and I/O settings.

It shows how to use the product and defines the minimum hardware resources required to start application development.

Sections of this document give brief descriptions of certain device features without describing the device blocks in detail.

This application note applies to SPC570Sx devices in accordance with *Table 1*.

Table 1. Device summary

Part number	Package
SPC570S40E1	eTQFP64
SPC570S40E3	eTQFP100
SPC570S50E1	eTQFP64
SPC570S50E3	eTQFP100

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It is intended that this application note is read along with the SPC570Sx reference manual, the SPC570Sx datasheet and the errata sheet(s), that can be obtained from the STMicroelectronics website at http://www.st.com (see *A.1: Reference documents*).

Contents

List of tables

List of figures

1 Supply pins and decoupling

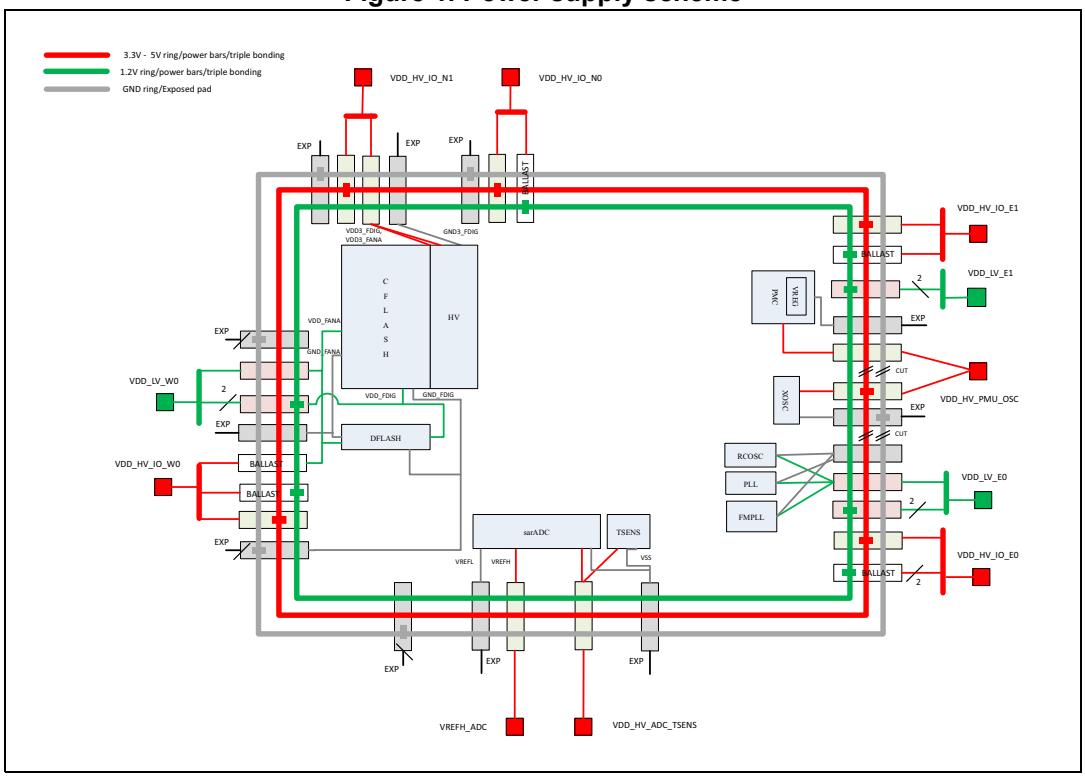
1.1 Power Management

The SPC570Sx provides two dedicated supplies at the package pin level:

- VDD_HV: high voltage external power supply for I/Os, JTAG, and most analog modules
- VDD_HV_ADC: high voltage external power supply for the ADC module

The internal LV supply, which is used to power all the digital macrocells, is generated (from VDD_HV) by an internal voltage regulator (see *Figure 1: Power supply scheme*).

Figure 1. Power supply scheme



Note: The user must configure the 3p3V_5V field (Main segment indicator) of the UTEST Miscellaneous DCF client according to the desired power supply voltage (3.3 V or 5 V).

By default this field is configured for a 3.3 V power supply (UTEST Misc bit 20 = 0).

Table 2. Power pads

Supply	Pad	SPC570SxE1 (eTQFP64)	SPC570SxE3 (eTQFP100)
1.2 V	VDD_LV_W0	12	19
1.2 V	VDD_LV_E0	34	52
1.2 V	VDD_LV_E1	45	68
3.3 V - 5 V	VDD_HV_IO_W0	13	20

Table 2. Power pads (continued)

Supply	Pad	SPC570SxE1 (eTQFP64)	SPC570SxE3 (eTQFP100)
3.3 V - 5 V	VREFH_ADC	19	29
3.3 V - 5 V	VDD_HV_ADC_TSENS	25	39
3.3 V - 5 V	VDD_HV_IO_E0	33	51
3.3 V - 5 V	VDD_HV_PMU_OSC	37	55
3.3 V - 5 V	VDD_HV_IO_E1	46	51
3.3 V - 5 V	VDD_HV_IO_N0	54	85
3.3 V - 5 V	VDD_HV_IO_N1	61	95

1.2 Decoupling capacitors

This section provides the suggested configurations and the values of the different capacitors.

Please refer to the device datasheet (see *A.1: Reference documents*) for the minimum recommended configuration.

Hardware designers must pay particular attention to place the decoupling capacitors beside the respective pins (see *Table 2: Power pads*).

Figure 2. VDD_HV_IO decoupling capacitors recommendation

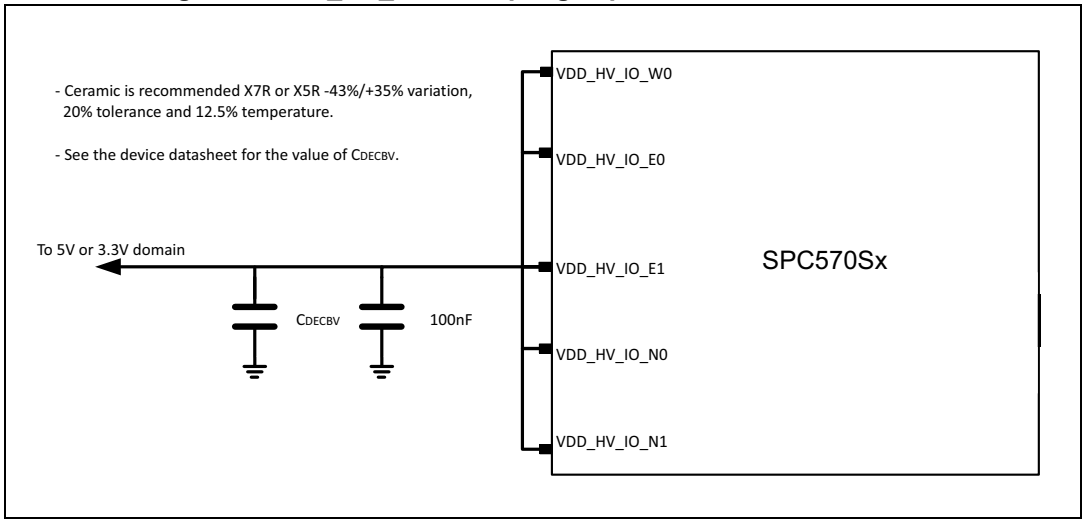
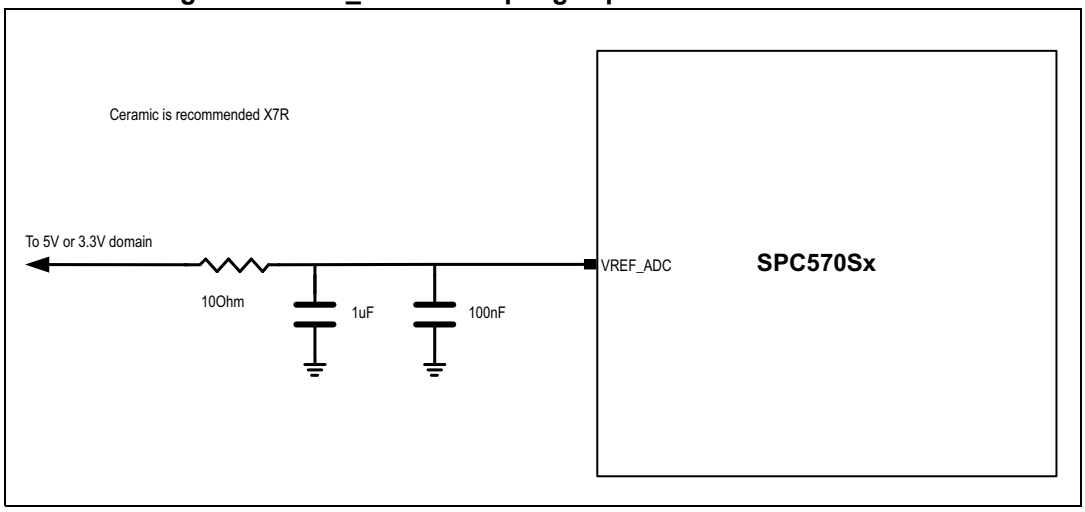


Figure 3. VREF_ADC decoupling capacitors recommendation



If RC filtering is used on the reference voltage then the value of the filter resistance, R_{ref}, should be less than 10 Ω.

Figure 4. VDD_HV_ADC_TSENS decoupling capacitors recommendation

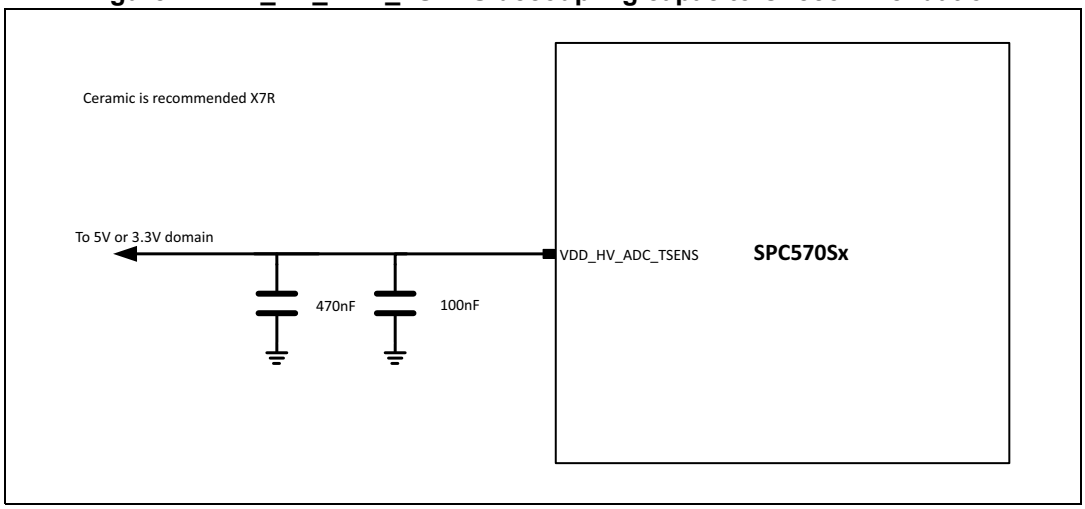


Figure 5. VDD_HV_OSC_PMC decoupling capacitors recommendation

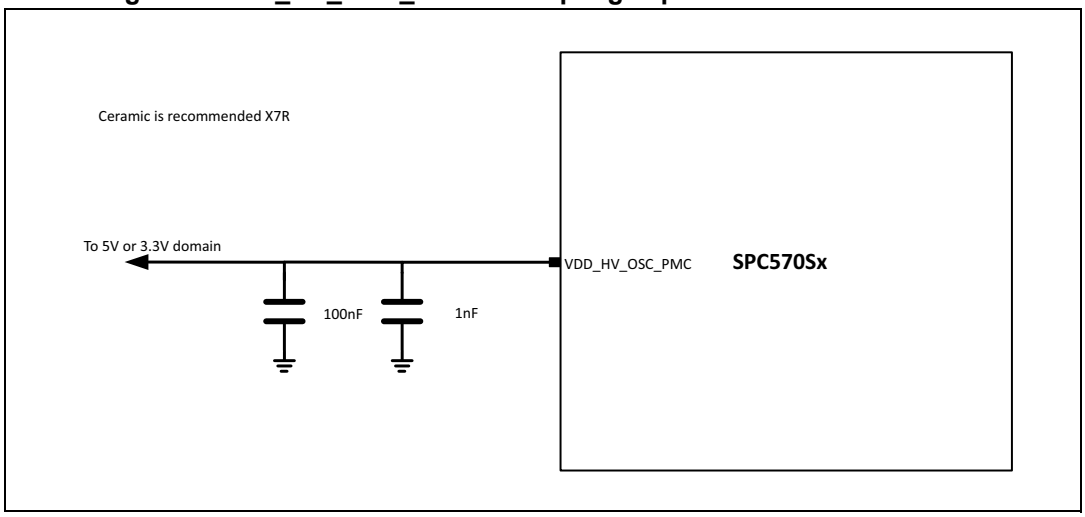
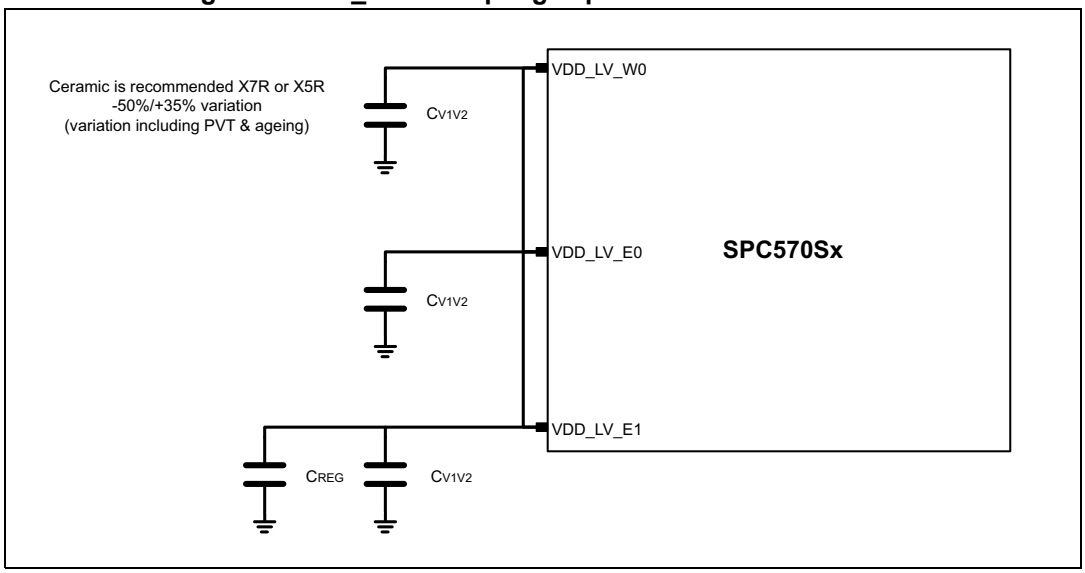


Figure 6. VDD_LV decoupling capacitors recommendation



All 1.2 V pins should be shorted externally on board with minimum resistance and minimum inductance. It is recommended to use a 1.2 V plane on which all 1.2 V pins are shorted to keep resistance and inductance negligible. Recommended capacitors should be placed very close to the device pins such that parasitic resistance can be reduced. Connection from VDD_LV pin to capacitor top plate should not exceed more than 5 mΩ in resistance and 0.5 nH in inductance. Similarly connection from bottom plate of capacitor to PCB ground should not have more than 5 mΩ resistance and 0.5 nH inductance.

1.3 Layout recommendations

The basic rule in the decoupling layout is to minimize the inductance associated with the loop device pin/decoupling capacitor and the total inductance of the connection to the power supply.

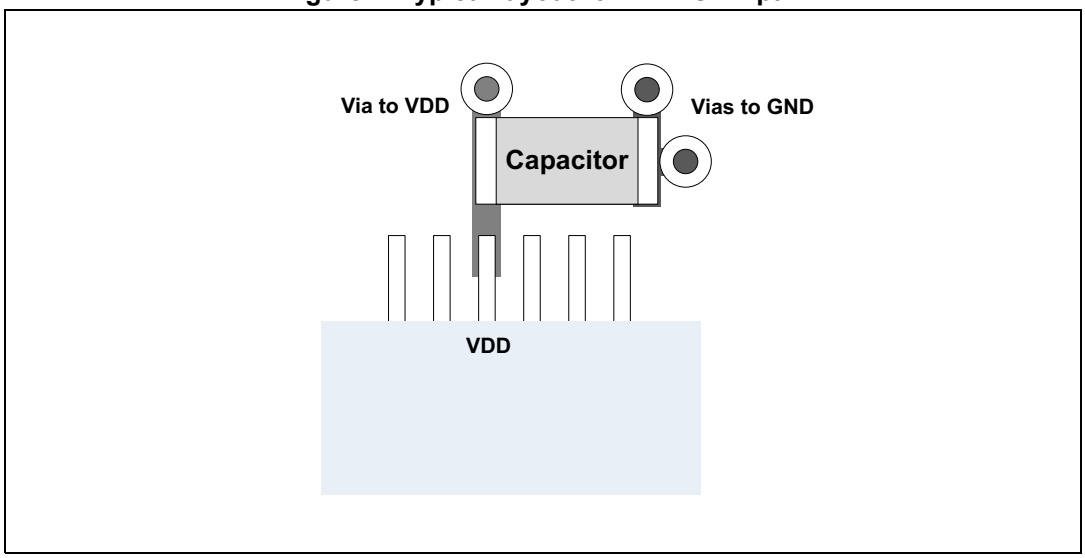
All the supply connections, including pads, tracks and vias, must have as low an impedance as possible (less than 5 nH). This is typically achieved by using copper areas, rather than tracks, and a dedicated power supply plane is preferable in multilayer PCBs.

Moreover, it is recommended to use both low Equivalent Series Resistors (ESR) and low Equivalent Series Inductance (ESL) capacitors.

The capacitors must be placed as close as possible to, or below, the corresponding pins on the underside of the PCB.

Figure 7 shows the typical layout of such a VDD/GND pair.

Figure 7. Typical layout for VDD/GND pair



2 External Oscillator

The external oscillator (XOSC) is provided as a reference for the on-chip PLLs. It can be used as a clock source for the ADCs, timers, serial interfaces as well as a system clock source.

It is available for observation on the CLKOUT pin (see *A.1: Reference documents*) and is used as a reference to calibrate the IRCOSC frequency.

The external oscillator allows a crystal or external clock to be used as the reference clock for the microcontroller.

The XOSC has the following features:

- Oscillator power-down control and status[a].
- Oscillator startup delay.
- Oscillator clock available interrupt.
- Oscillator bypass mode control.
- Internal load capacitors for 20 MHz/40 MHz crystal oscillators.
- Automatic Loop Control (ALC) to remove the need for an external series resistor.
- Gain selection for <= 20 MHz and 40 MHz crystals oscillators to allow for optimal startup margin without overdrive issues.
- Reference clock to PLL0 and to PLL1.
- Reference clock to CMU_0 (IRCOSC trimming).
- Option to drive the CAN protocol clock directly from the XOSC.

The XOSC provides support for 8 – 40 MHz crystal oscillator inputs and has integrated load capacitors.

2.1 XOSC startup

The oscillator is enabled at startup via the XOSC EN field of the UTEST Miscellaneous DCF client. By default the external oscillator is disabled (UTEST Misc bit 24 = 0).

If enabled, the oscillator starts in phase 3 of the reset sequence after negation of the internal POR circuits, but while the external PORST input is asserted. This speeds up the application start-up while accounting for the settling time of the power regulators.

The selection of internal or external load capacitors on the XTAL/EXTAL pins is determined by the XOSC EXT CLOAD bit in the UTEST Miscellaneous DCF client. By default external load capacitors are selected (UTEST Misc bit 25 = 1).

Load capacitor values are determined from the crystal manufacturer data sheet requirements, while taking into account stray PCB and on-chip capacitance. Refer to the device data sheet (see *A.1: Reference documents*) for on-chip capacitance values. When

a. Enabling and disabling of the oscillator is done in the Mode Entry (MC_ME) module.
The ME_<mode>_MC[XOSCON] controls the power-down of oscillator based on the current device mode.
The status of the XOSC is shown in the MC_ME_GS[S_XOSC].
The XOSC can also be enabled by standalone control in the XOSC_CTL register. The XOSC_CTL[OSCON] bit controls power-down while the S_OSC bit provides the oscillator clock available status.

using the internal load capacitors for the oscillator, the startup value of the capacitors is stored in the XOSC LOAD CAP SEL field in the UTEST Miscellaneous DCF client: During phase 3 of the device reset sequence, the oscillator UTEST values are read and driven to the oscillator.

Note: In order to allow the oscillator to reach full amplitude before use, the internal counter (OSCCNT) is started when the device exits reset. The counter is driven by the oscillator output clock. When the counter reaches XOSC_CTL[EOCV] × 512, a signal is sent to the MC_ME module, allowing a mode switch to the oscillator (when used as a system clock or an input to PLL0). The default value for this field after reset depends on implementation and can be found in the XOSC Device Configuration. After reset, software can clear or change the EOCV field in order to shorten or lengthen the delay until the oscillator is ready. It is advised that if the EOCV value is modified it should be done as early as possible in user code. This will ensure that the new value will be used before OSCCNT reaches the count value.

The enable/disable state of the oscillator is captured in the MC_ME module at this time. After reset, the oscillator can be enabled/disabled by software in the MC_ME module. Internal load capacitor selection is maintained by the oscillator if disabled after reset.

The default reset value for the XOSC trimming capacitors does not trim the internal capacitor values (UTEST Misc bit 26:30 = 00000b (XOSC LOAD CAP SEL)).

The internal load capacitor values stored in UTEST flash memory row have triple-voting flip-flop (TVF) implementation to prevent an incorrect value, and thus an undetectable error in the system.

The XOSC has the ability to be started with either an 8 MHz to 20 MHz, or 40 MHz crystal.

The XOSC EN_40 MHz bit in the UTEST Miscellaneous DCF client selects which crystal source will be used: The default value of this field is for an 8 MHz to 20 MHz crystal (UTEST Misc bit 21 = 0).

Note: The user must configure the XOSC EN_40MHz field in the UTEST Miscellaneous DCF client *according to the external crystal used.*

Note: The user must take care when using 16 MHz crystals or lower, because the S_XOSC flag in the ME_GS register will not be set if the CMU_PLL (CMU 0) default configuration is used. Indeed CMU_PLL (CMU 0) is programmed by default to use crystal frequencies greater than IRC (16 MHz) + 0.5 MHz and this condition is no longer valid with XOSC <= 16 MHz.

In this case, to use an XOSC frequency less than or equal to 16 MHz, an RCDIV value (CMU_0.CSR register) that respects the previous formula (CMU_CSR.B.RCDIV = 3) must be used.

This setting has to be done before enabling XOSC in the user code.

2.2 Oscillator bypass mode

The oscillator circuit can be bypassed by setting XOSC_CTL[OSCBYP]. This field can only be set by software, and is only cleared by a system reset. In bypass mode, the oscillator is disabled, and the input clock on the EXTAL pins is level-shifted and driven to the logic on the device. The bypass configuration is independent of the power-down mode of the oscillator.

Note: The external oscillator must be running before the XOSC is turned off. If XOSC is being turned on, the status will be updated only after the clock starts toggling.

2.3 XOSC Pins and Configurations

Table 3. XOSC pins functionality

Pad	Description	Direction	Pin No.	
			eTQFP64	eTQFP100
XTAL	Analog output of the oscillator amplifier circuit—to be grounded if oscillator is used in bypass mode.	Output	36	54
EXTAL	– Analog input of the oscillator amplifier circuit when oscillator is not in bypass mode – Analog input for the clock generator when oscillator is in bypass mode	Input	35	53

Table 4. XOSC configurations

OSC EN	XOSC_CTL[OSCBYP]	XTAL	EXTAL	XOSC Output	XOSC MODE
0	0	No crystal, high-impedance	No crystal, high-impedance	0	Power down, IDDQ
0	1	x	external clock	undefined	Reserved, OSC Disabled
1	1	x	external clock	XTALOUT	Bypass, OSC Enabled
1	0	crystal	crystal	XTALOUT	Normal, OSC Enabled
		ground	external clock	XTALOUT	Normal, OSC Enabled

2.4 Recommended crystals

The following quartzes have been characterized:

- NDK NX5032GA 40MHz with $C_L = C_1 = C_2 = 8$ pF in case internal caps are disabled.
- NDK NX3225GB 20MHz with $C_L = C_1 = C_2 = 8$ pF in case internal caps are disabled.

Note: See crystal manufacturer's specification for recommended load capacitor (C_L) values.

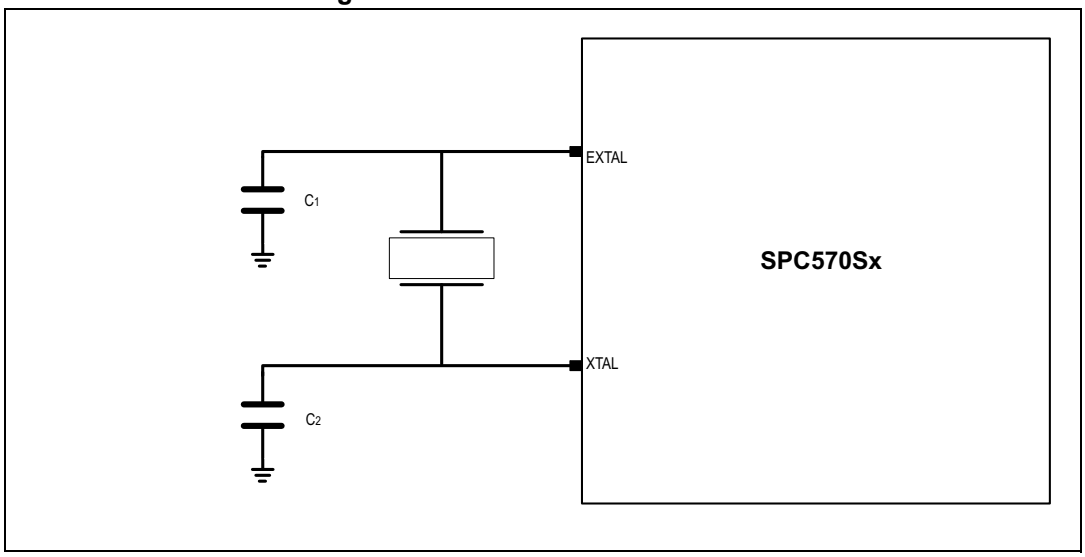
The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (CS_EXTAL/CS_XTAL) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.

2.5 Reference Oscillator Circuit

The oscillator circuit consists of the following components:

- Crystal
- Two capacitors

Figure 8. Reference oscillator circuit

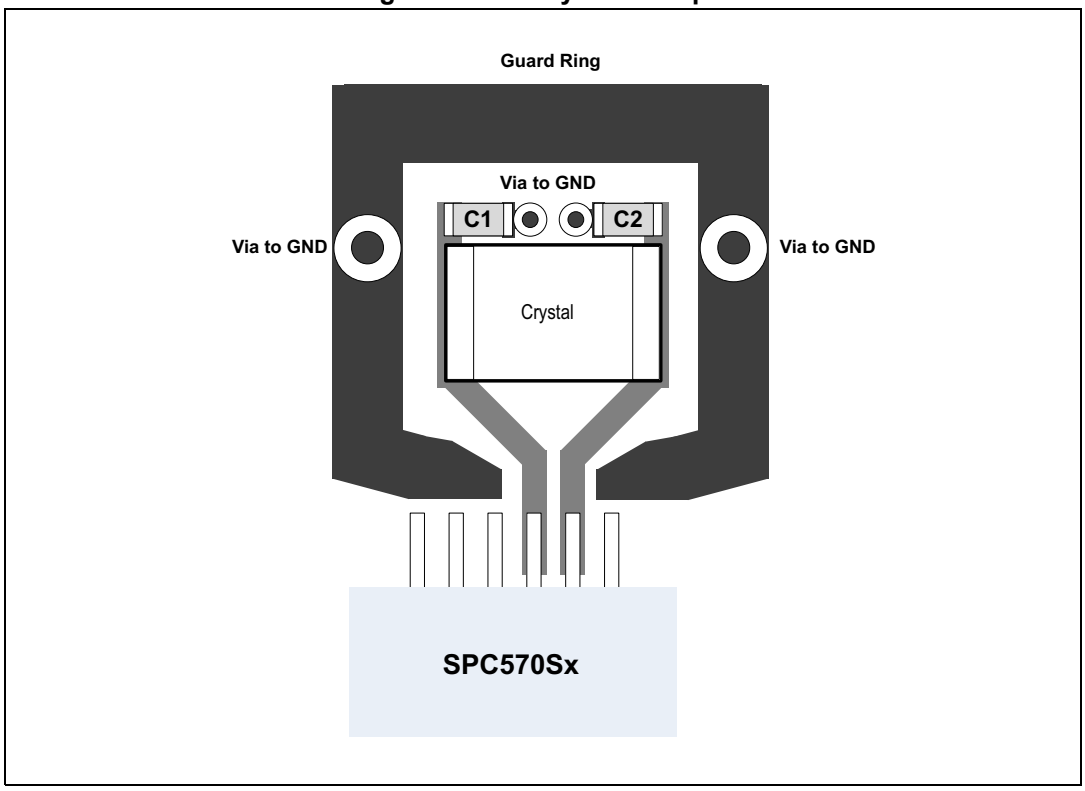


2.6 Layout recommendations

To optimize performance and minimize EMC (electromagnetic compatibility) susceptibility the following recommendations should be observed for designing the oscillator circuitry layout:

- A current flow at the crystal fundamental frequency runs through the oscillator circuit. If the oscillator is clipped, then the high order harmonics are present. To minimize the emissions generated by these currents and enhance the electromagnetic immunity, the oscillator circuits should be kept as compact as possible.
- Avoid other high frequency signals near the oscillator circuitry.
- Configure the GND supply at low impedance.
- Do not place sensitive signals near the oscillator. Analyze cross-talk between different layers.
- Shield the crystal with an additional ground plane underneath the crystal. This has an impact on the oscillation margin of the oscillator: the layout must be carefully characterized.
- Open all inner layers in correspondence of the oscillator to reduce capacitance.
- If the crystal package is metallic, it should be connected directly to GND.
- To isolate the noise to or from the oscillator, it is possible to put a “guard ring” around the oscillator. This ring must be as small as possible.
- Capacitors should be placed between both ends of the crystal and GND (solid plane).

Figure 9. PCB layout example



3 Analog Input pins

Careful decoupling must be implemented so that external component or self induced ripples and noise do not degrade the performance of ADC dedicated supply and reference pins.

The user must be aware that all the performances specified are granted if the figures indicated in this section are respected at device pin level.

The reference voltage pins are the most sensitive for the ADC performance (see *Section 1.2: Decoupling capacitors*) for capacitors to be used on V_{REF} and supply[b].

Note: In case RC filtering is used on the reference then the value of filter resistance R_{ref} should be less than 10 ohms.

External filtering (RC or active) should be done on the ADC input to avoid the high frequency noise being aliased into the baseband spectrum.

Apart from this, an external capacitor with a certain minimum value (see *Equation 2*) is also needed on the ADC input to reduce the drop on the ADC input pin due to charge sharing between the external capacitor and the ADC sampling capacitor.

This capacitor should be a ceramic capacitor with excellent high frequency properties. It should be placed close to the device pin to which the input is connected.

The value of the Input source resistance (R_s) and the anti-alias filter resistance (R_f) should respect the following equation:

Equation 1

$$(R_s + R_f) < \frac{(20 \times 10^6)}{f_c}$$

where f_c is the rate at which the input voltage is converted by a single ADC.

Note: If the given input channel is converted by two ADCs simultaneously then the value of f_c should be twice the actual conversion rate.

Example 1

If the input voltage is sampled and converted every 1.5 µs, then f_c = 1/1.5 µs and (R_s+R_f) must be below 30 Ω.

The minimum limit on the value of the filter capacitance, C_f (in Farads), is given by the following equation:

b. This cap should be placed as close as possible to the device pins but without degrading the placement of reference decoupling capacitors.

Equation 2

$$(C_f) > (N \times 50 \times 10^{-9})$$

where N is the number of ADCs simultaneously converting the given input channel.

Note: No more than two ADCs should simultaneously convert the given input channel.

Example 2

A given input channel is converted simultaneously by two ADCs then minimum 100 nF should be used as filter capacitance.

The current limiting resistor R_L should obey to the following equation:

Equation 3

$$(R_L) < \frac{(T_{sample})}{(10 \times (C_p + N \times 6 \times 10^{-12}))}$$

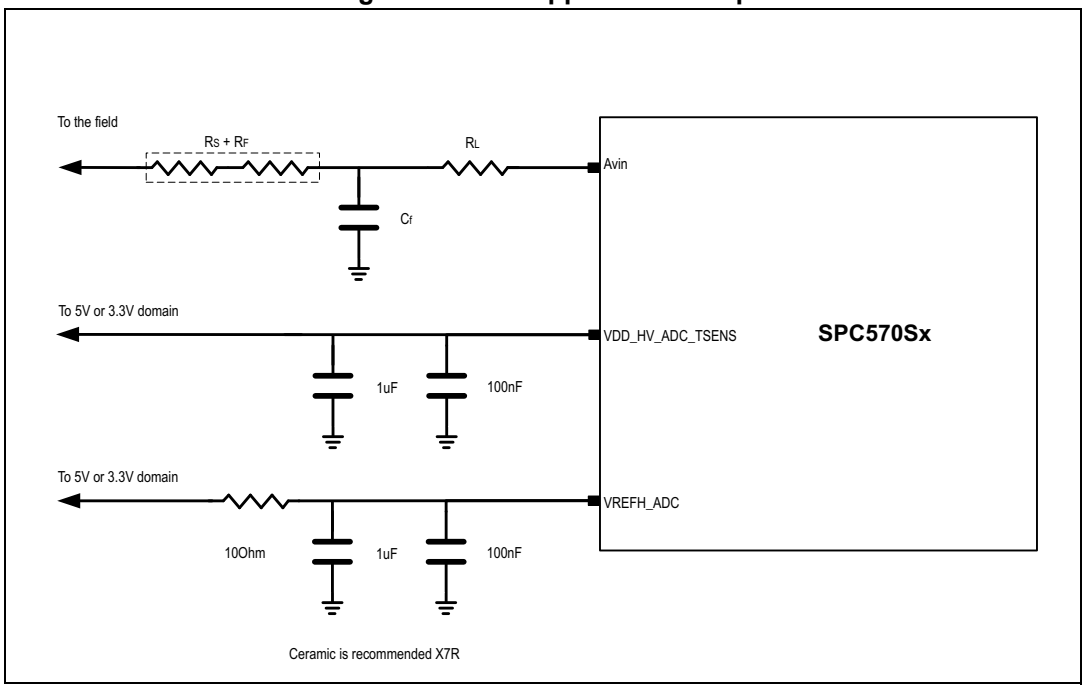
where:

- C_p is the parasitic cap on the ADC input pin inside the SoC
- T_{sample} is the sampling time used by the ADC for conversion
- N is the number of ADCs simultaneously converting the given input channel

If the SoC parasitic capacitance on the ADC input pin is 14 pF and the sampling time is programmed to be 0.5 µs, then the value of R_L should be less than 2500 Ω.

Note: While deciding the value of R_L, consider that the leakage current on the ADC input pin will create a voltage error across the R_L, thereby leading to a conversion error.

Figure 10. ADC application setup



4 Configuration of pins and unused IOs

4.1 I/O pad types

The device features several I/O types with different drive strength:

Table 5. I/O pad specification descriptions

Pad type	Description
Slow configuration	Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω
Fast configuration	Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω
Very fast configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω
Input only pads	These pads are associated to ADC channels and the external 8-40 MHz crystal oscillator (XOSC) providing low input leakage

In order to reduce the noise generated on the I/O power, it is recommended to select the slowest configuration compatible with the functionality required. A series resistor in the range of few tenths of an ohm can be effective as filter, combined with the parasitic capacitance of the connection.

High toggling rates and signals used as clocks for external devices or peripherals could require reinforced decoupling and filtering.

4.2 Pad configuration

This product contains safety mechanisms to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (VDD or VSS).

This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins (see *A.1: Reference documents* for further details).

Table 6. Pin startup and reset states

Pin	Startup state(1)	State during Reset	State after reset
I/O pins	Weak pull-up	Input, weak pull-up	Input, weak pull-up
Analog Inputs	High-impedance	High-impedance	High-impedance
F0 (ERROR0)	Weak pull-up	Input, weak pull-up	Input, weak pull-up

Table 6. Pin startup and reset states (continued)

Pin	Startup state(1)	State during Reset	State after reset
F1 (ERROR1)	Weak pull-up	Input, weak pull-up	Input, weak pull-up
PORST	Weak pull-down	Input, weak pull-down	Input, weak pull-down
TESTMODE	Weak pull-down	Input, weak pull-down	Input, weak pull-down
TDI	High-impedance	Input, weak pull-up	Input, weak pull-up
TDO	High-impedance	High-impedance	High-impedance
TMS	High-impedance	Input, weak pull-up	Input, weak pull-up
TCK	High-impedance	Input, weak pull-down	Input, weak pull-down
XTAL/EXTAL	High-impedance	High-impedance	High-impedance

1. Startup state is exited when the core and high-voltage supplies reach minimum levels as defined in the Power Management chapter (see *A.1: Reference documents* for further details).

5 Reset

Table 7. Reset Pins

Pad	Description	Direction	Pin No.	
			eTQFP64	eTQFP100
PORST	Power on reset with Schmitt trigger characteristics and noise filter. PORST is active low and acts as Destructive reset.	Bidirectional	44	66
ESR0	Reset Monitor (on Port C[15])	Output	41	62

5.1 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional reset pin (PORST).

The PORST pin acts as an input to initialize the device to a known start-up state.

The detection of a falling edge on PORST will start the reset sequence.

For safety reasons, a weak pull-down is always connected to the PORST pin.

PORST pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence: Recommended value is 4.7 KΩ.

Figure 11. Start-up reset requirements

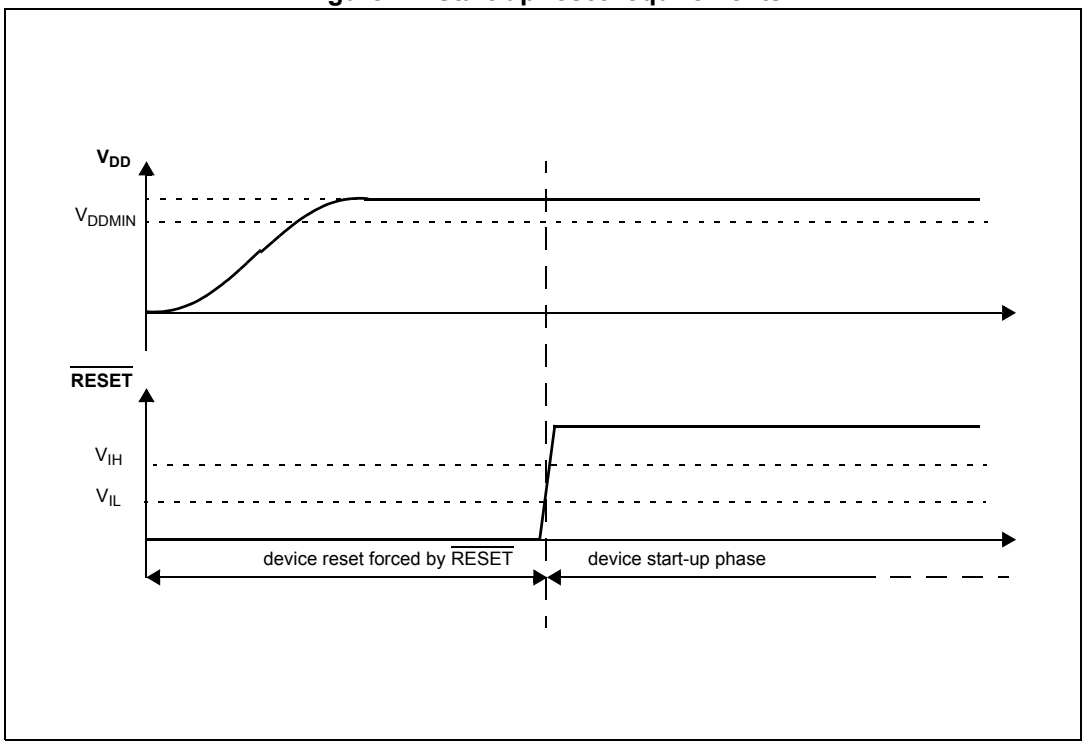
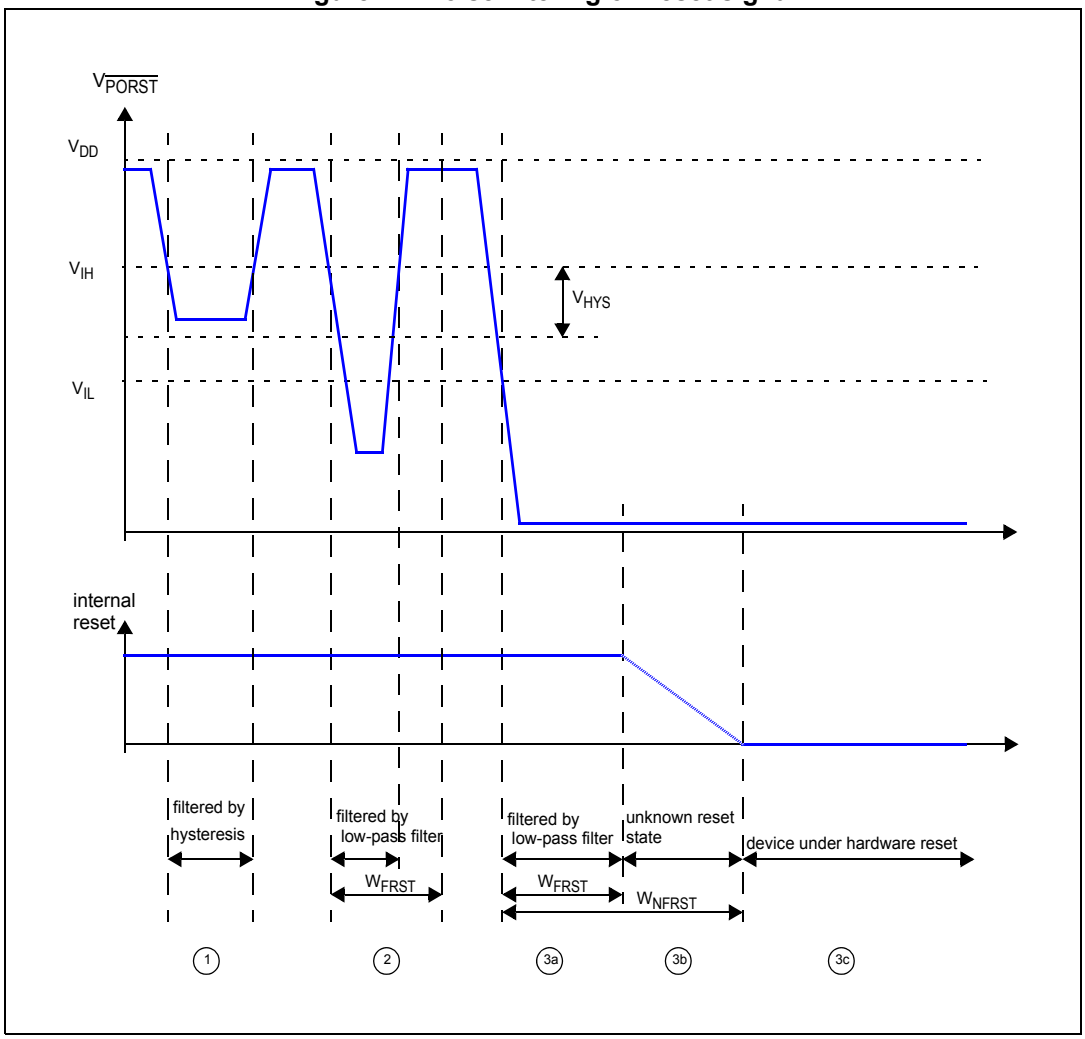


Figure 12 describes device behavior depending on supply signal on $\overline{\text{PORST}}$ (see *A.1: Reference documents* for further details):

1. $\overline{\text{PORST}}$ does not go low enough: it is filtered by input buffer hysteresis. The device remains in the current state.
2. $\overline{\text{PORST}}$ goes low enough, but not for long enough: it is filtered by a low pass filter. The device remains in the current state.
3. $\overline{\text{PORST}}$ generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown. It may either be reset or remains in the current state depending on extra conditions (PVT — process, voltage, temperature).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. The device is under hardware reset.

Figure 12. Noise filtering on reset signal



The external reset signal (pulse) of PORST pin must be greater than W_{NFRST} (2000 ns) to generate an internal reset. Pulses less than W_{FRST} (500 ns) will not generate an internal

reset. An internal reset may, or may not, be generated for pulses between W_{FRST} and W_{NFRST}.

To prevent noise on the reset signal from wrongly generating a reset, the PORST pad includes an analog filter.

To enhance EM immunity, the reset circuitry must be compact and close to the PORST pin, keeping connections short and providing local decoupling.

5.2 ESR0 pin functionality

This device does not implement a dedicated pin to output a reset signal. Nevertheless, it is possible to statically configure one pin to act as an output reset. The operation is done by reading a specific DCF record, which can be written one time only and it is assigned to a triple-voting set of flip-flops. The DCF is read during the reset phase 3 Destructive and the read value is maintained till the next power on reset.

Following list summarizes the static pin configuration:

1. PAD 47 (see *Table 7: Reset Pins*) can have a double function (see *A.1: Reference documents* for further details):
   a) ESR0 reset output only
   b) GPIO/AF
2. The choice between *a)* or *b)* is done via DCF reading at every reset.
3. The DCF is write-once and stored into a triple-voting set of flip-flops.
4. The value read via DCF shall be available to the SW via a register read-only status bit, so that the application can always monitor the correct configuration.
5. The value uploaded via DCF is maintained throughout the next Power-On-Reset.
6. After a Power-On-Reset the default value is GPIO.
7. After a Destructive or Functional reset, the default value is the last one being uploaded via DCF.
8. In case the pin is configured as GPIO, during a reset phase the pin shall maintain the same under-reset safe configuration as for all the other GPIOs.
9. In case the pin is configured as ESR0, during a reset phase the pin is driven to ‘0’ by the RGM module, while out of reset, the pin is not driven.

Note: ESR0 pin characteristics: ESR0 is strongly driven during reset and it is weakly pulled up out of reset. So, out of reset, the rise of this pin will depend on the output load.

Internal pull up resistance is 75 KΩ (worst case), so outside resistance should be at least 10 times of this to have a output signal rising to max value of IO supply.

6 Debug

SPC570Sx microcontrollers have a comprehensive feature set to assist debug and trace (see *A.1: Reference documents* for further details).

6.1 Interfaces

Two interfaces are used to support debug and trace functionality. These are the JTAG port and the Nexus Auxiliary Port (NAP). The JTAG is port is used for debug and test purposes while the NAP is used to transfer trace data streams.

6.1.1 JTAG Port

The SPC570Sx feature a JTAG port with a 4 pin interface. The supported signals are TDI, TDO, TCK and TMS. TRST is not used.

Table 8. JTAG signals

Signal	Description	Direction
TDI	Test Data Input	Input
TDO	Test Data Output	Output
TCK	Test Clock	Input
TMS	Test Mode Select	Input

Table 9. JTAG pads

JTAG Connector Signal	JTAG Connector PAD	eTQFP64	eTQFP100
TDI	1	38	59
VSS	2	GND	GND
TDO	3	40	61
VSS	4	GND	GND
TCLK	5	42	63
VSS	6	GND	GND
EVTI	7	64	3
PORST	8	44	66
ESR0(1)	9	41	62
TMS	10	39	60
VREF	11	46	51
VSS	12	GND	GND
EVTO	13	63	4
JCOMP	14	—	—

1. If ESR0 signal is not available (because not configured through DCF), please short ESR0 to PORST pad.

6.1.2 Nexus Auxiliary port

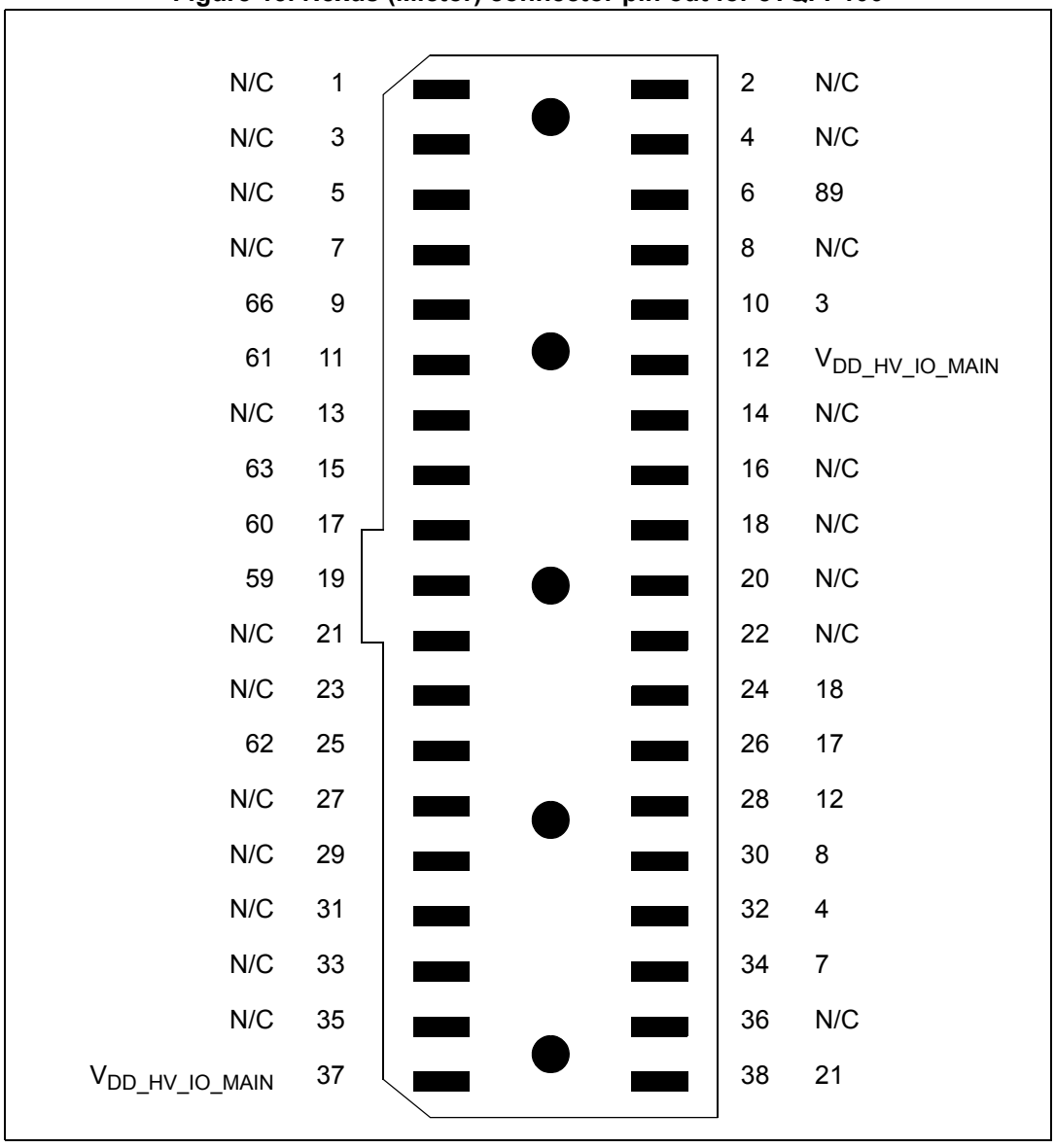
SPC570Sx has Nexus 2+ and can be run in reduced port mode with four MDO signals.

Table 10. Nexus Signals

Signal	Description	Direction
EVTI	Event Trigger Input	Input
EVTO	Event Trigger Output	Output
MSEO	MDO Start/End Output	Output
MCKO	MDO and MSEO signal clock	Output
MDO(0-3)	Trace	Output

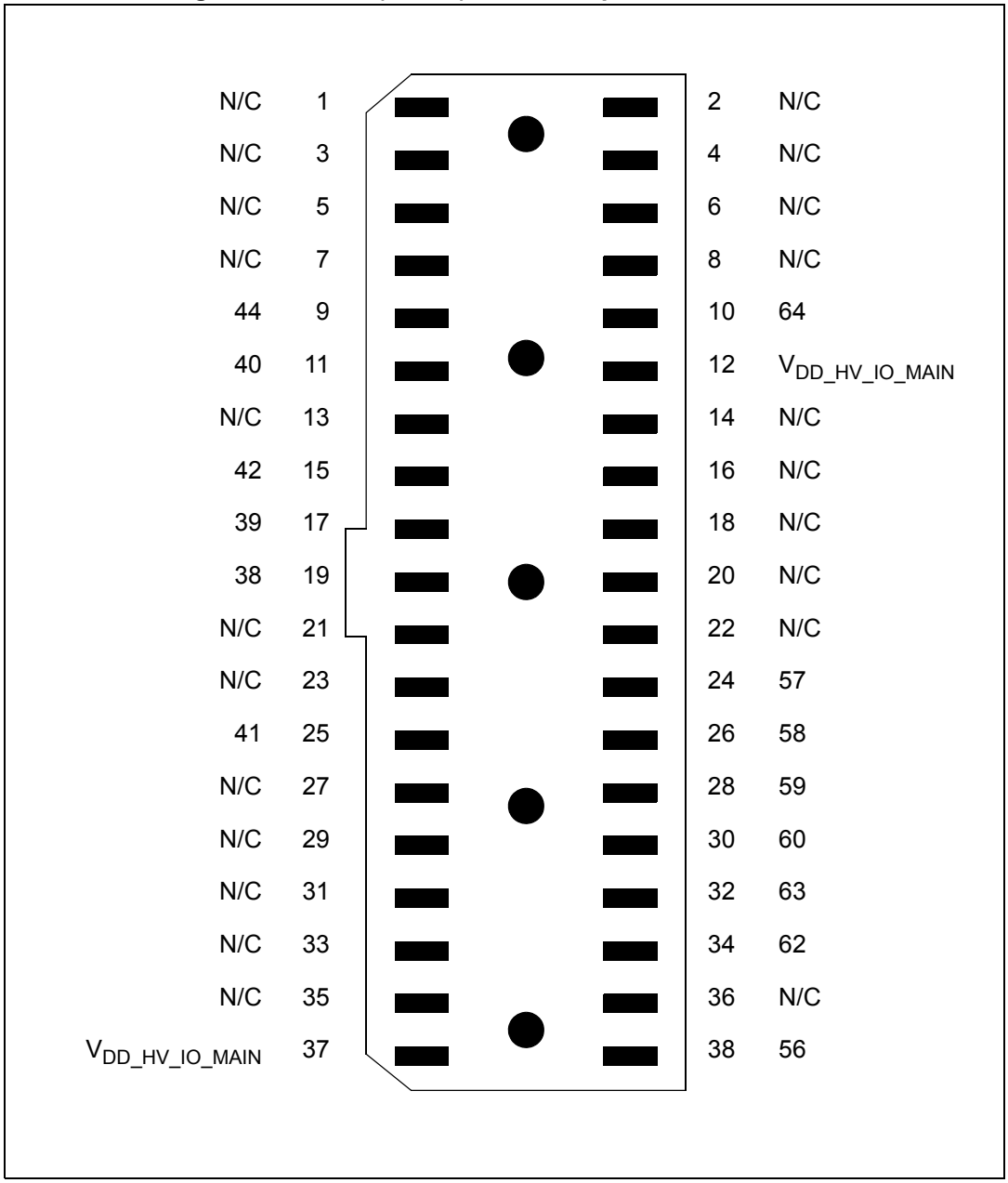
6.1.2.1 Examples of Nexus Connector configuration

Figure 13. Nexus (Mictor) connector pin out for eTQFP100



Note: The NEXUS signals for the eTQFP100 package are on AF3 (see A.1: Reference documents for further details).

Figure 14. Nexus (Mictor) connector pin out for eTQFP64



Note: The CLOCKOUT signal is not available on the Nexus connector for the eTQFP64 package because pin 57 PE[5] shares the functionality of CLKOUT or Nexus - MDO3.

7 Exposed pad

7.1 Introduction

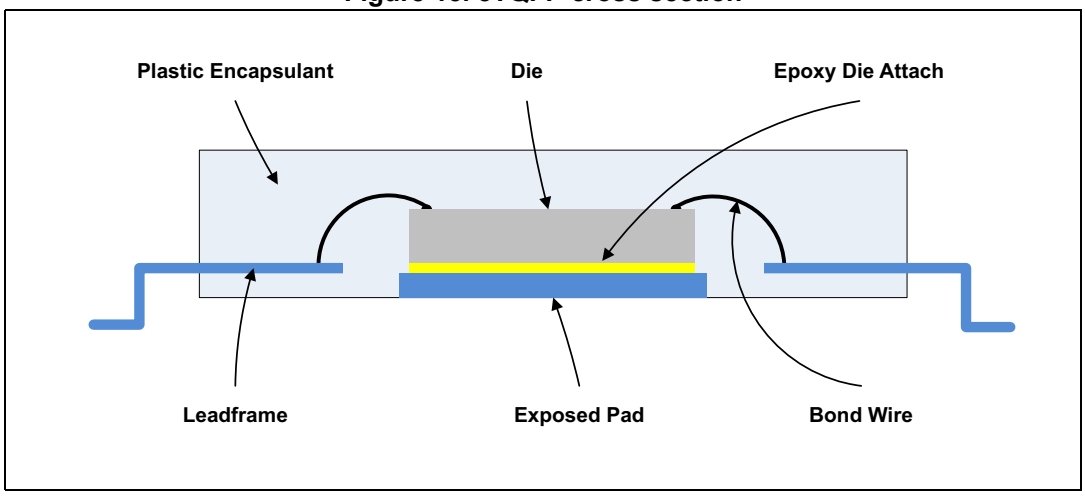
The exposed pad on the bottom of package provides a very efficient heat sink as well as electrical ground to the PCB board (it also provides a reliable mechanical connection for the chip and a reliable ground plane for EMC purposes).

The package structure also provides an extremely low thermal resistance path between the device junction and the exterior of the package (see *Section A.1: Reference documents*).

The exposed pad must be soldered to a PCB land or land pattern that has sufficient connections to heat sinking areas of copper on the PCB. These connections should include thermal vias under the exposed pad to bond the land pattern to the heat sinking copper.

Note: The exposed pad should never be connected to a potential other than MCU ground.

Figure 15. eTQFP cross section



7.2 Design Guidelines

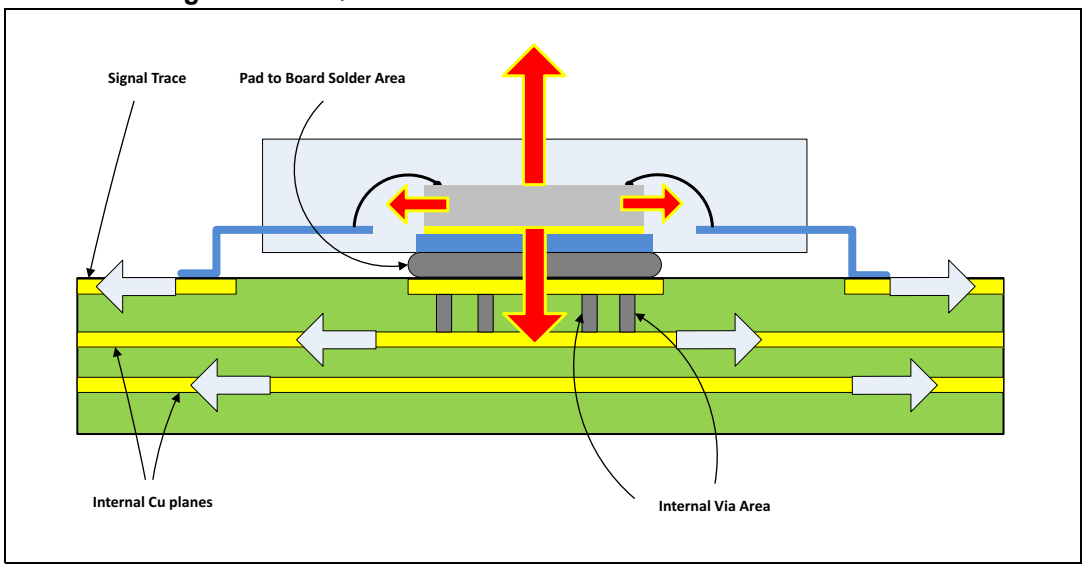
Caution: These recommendations are to be used as a guideline only

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package.

General guidelines for eTQFP packages:

- Lead foot should be approximately centered on the pad with equal pad extension from the toe and the foot.
- Typically, the pad is extended 0.5 mm beyond the eTQFP foot at both the heel and the toe.
- Care should be taken that PCB pads do not extend under the eTQFP body, which can cause issues in assembly.
- Pad width should be approximately 60% of the lead pitch: PCB pad width should be designed at 0.30 mm for this 0.50 mm lead pitch package (see *Section A.1: Reference documents*).

Figure 16. eTQFP cross-section with heat transfer schematic



In order to maximize both heat removal from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package.

It is suggested that the solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance.

The PCB should be designed with a clearance of at least 0.25 mm between the outer edges of the land pattern and the inner edges of lead pads to avoid any shorts.

7.2.1 Thermal Vias

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct heat from the surface of the PCB to the ground plane(s).

The vias act as “heat pipes” and the number required is application specific and dependent upon the package power dissipation as well as the electrical conductivity requirements (see *Section A.1: Reference documents*).

Note: Thermal and electrical analysis and/or testing is recommended to determine the minimum number of vias required.

Typically the maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern based on a 1.2 mm grid.

In order to avoid any solder wicking inside the via during the soldering process (which may result in solder voids between the exposed pad and the thermal land) it is also recommended that the diameter of the vias should be between 0.30 to 0.33 mm with 1.0 oz. copper barrel plating.

If the copper plating does not plug the vias, the thermal vias can be “tented” with a solder mask on the top surface of the PCB to prevent solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

Appendix A Further Information

A.1 Reference documents

1. *32-bit Power Architecture® microcontroller for automotive ASILD Chassis & Safety applications* (RM0349, DocID024507, Rev 6)
2. *32-bit Power Architecture® microcontroller for automotive ASILD Chassis & Safety applications* (DS9607, DocID024492, Rev 6)

A.2 Acronyms and abbreviations

Table 11. Acronyms and abbreviations

Terms	Meaning
ADC	Analog to Digital Converter
ALC	Automatic Loop Control
DCF	Device Configuration Format records
EM	Electromagnetic
EMC	Electromagnetic Compatibility
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
ESR0	External Reset Signal no.0
eTQFP	Thin Quad Flat Pack with exposed pad
HV	High Voltage
Hw	Hardware
IRCOSC	Internal Resistor-Capacitor Oscillator
JTAG	Joint Test Action Group test access port
LV	Low Voltage
NAP	Nexus Port Controller
NEXUS	IEEE-ISTO 5001-2003 a standard debugging interface
PCB	Printed Circuit Board
PORST	Power-On-Reset
SMT	Surface Mount Technology
SoC	System-on-Chip
TSENS	Temperature Sensor
TVF	Triple-Voting Flip-flop
UTEST	User Test Flash
XOSC	External Oscillator

Revision history

Table 12. Revision history

Date	Revision	Changes
22-Jun-2015	1	Initial release.
19-Dec-2016	2	Updated *Figure 6: VDD_LV decoupling capacitors recommendation*. In *Section 1.2: Decoupling capacitors*, added paragraph “All 1.2 V pins should be shorted externally on board with minimum resistance...” In *Section 2.4: Recommended crystals*: – changed “NDK NX5032GA 40MHz with CL=C1=C2=15 pF” to “NDK NX5032GA 40MHz with CL=C1=C2=8 pF” – changed “NDK NX3225GB 20MHz with CL=C1=C2=8 pF” to “NDK NX3225GB 20MHz with CL=C1=C2=8 pF”