AN4587
Application note

Input bias current of a chopper amplifier

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Introduction

Chopper amplifiers are generally considered as the perfect choice in applications where DC precision is mandatory.

This kind of amplifier uses a continuous time modulation technique to exhibit extremely low offset and 1/f noise.

However, despite numerous advantages of the chopper, the switching technique shows some drawbacks that should be taken into consideration for new design.

The TSZ121 is a chopper amplifier with an input offset voltage max of 5 µV at 25 °C.

Due to its switching mode, some injection charge appears on the input pins of this chopper amplifier. This switching effect, generates both voltage and current “noise” transients at the chopping clock frequency and its harmonics. The TSZ121 is a CMOS input, thus, it exhibits a very low input bias current (Iib). This is a very desirable feature if large source impedances are present. However, charge injection produces some unexpected effects on the input bias current behavior.

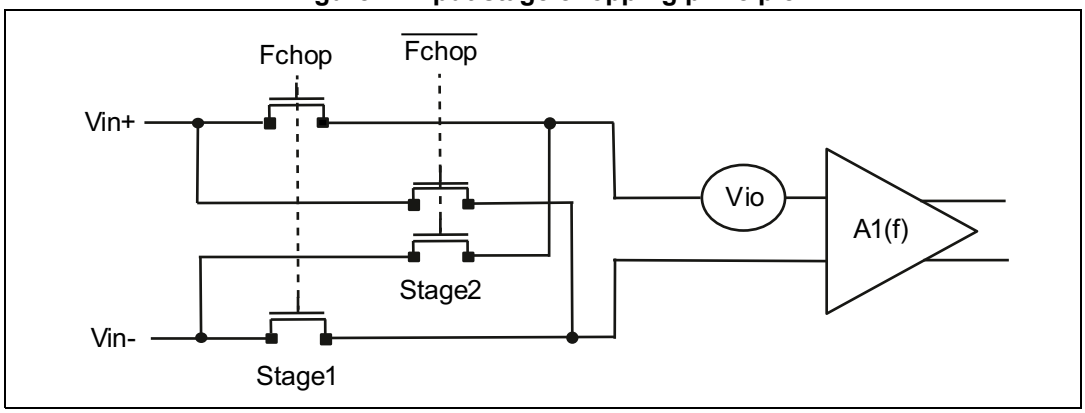
Contents

1 What causes Iib spikes

Figure 1 shows the chopping principle of the TSZ121 input stages. The input voltage passes through a chopper stage driven by a clock at a frequency Fchop. On the first clock cycle (step 1), the first MOS stage is closed and the Vio is amplified in the normal way. On the next clock cycle, the second MOS stage is closed, and in this case, the Vio is amplified in a reverse way compared to step1.

The average equivalent, Vio, of these two cycles is close to zero.

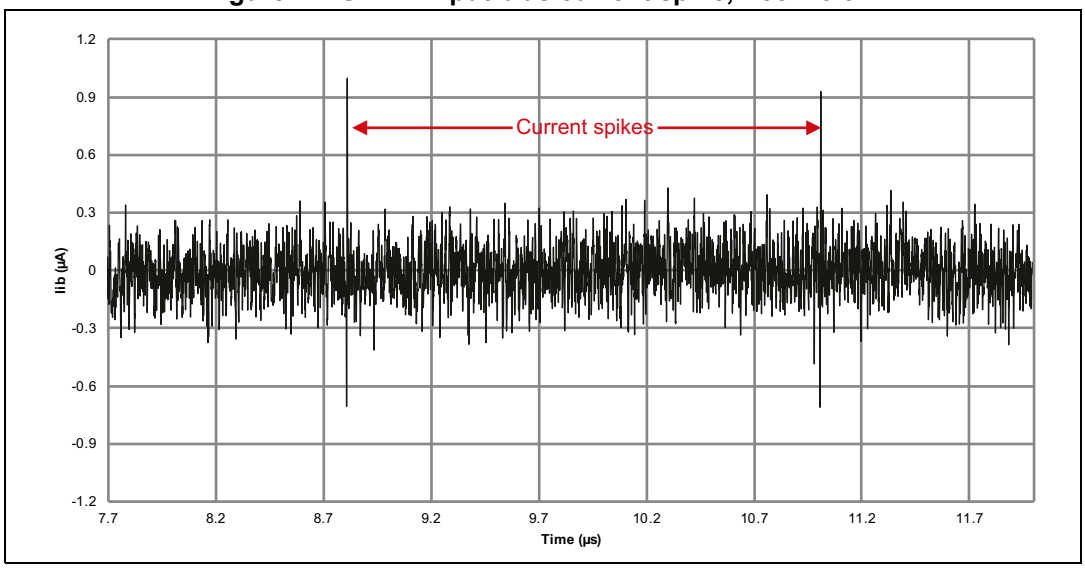
Figure 1. Input stage chopping principle



But, due to the switching MOS, this chopper stage injects some charge directly on the input, resulting in current spikes on the input pins.

Figure 2 shows a snapshot scope of the input bias current measured on the TSZ121.

Figure 2. TSZ121 input bias current spike, Vcc = 5.5 V



Two things cause these current spikes on the inputs:

- Charge injection
- Clock feed through

They are described below.

1.1 Charge injection

Figure 3 shows that when the transistor MOS is ON, the electrons can travel through the channel from the source to the drain (in this example the MOS is a NMOS).

But, when the transistor MOS is OFF, the channel is closed, and all charges are dispersed into the source and drain as shown in *Figure 4*.

Figure 3. MOS ON

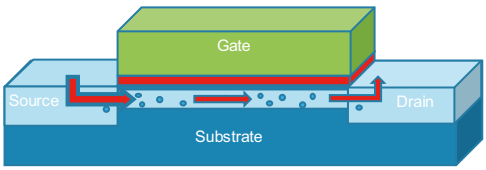
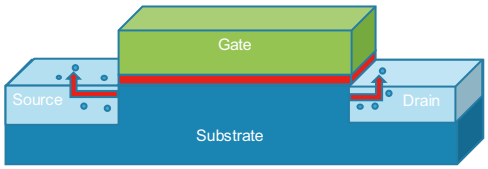


Figure 4. MOS OFF



The total charge in the channel of a MOS switch is given by *Equation 1*.

Equation 1

$$Q = Am \cdot Cox(Vgs - Vth) \quad (1)$$

Where:

- Am is the area of the MOS gate
- Cox is the oxide capacitance per unit area
- Vgs can also be defined as Vcc-Vin where Vcc is directly linked to the power supply of the TSZ121 and Vin is the input common mode voltage (gate voltage is at Vcc when the transistor is ON).

When the transistor is switched OFF the charges are evacuated resulting in a current.

So, the spikes appearing on the input pins of the TSZ121 are also linked to the power supply.

Figure 5 and *6* are a snapshot scope of the current in the input pins of the TSZ121 at different Vcc while *Figure 7* and *8* are simulations of the current in the input pins. Effectively, we can see that when the Vcc is low, the amplitude of the spikes on the input bias current is largely attenuated.

Figure 5. TSZ121 input bias current spike, Vcc = 5.5 V

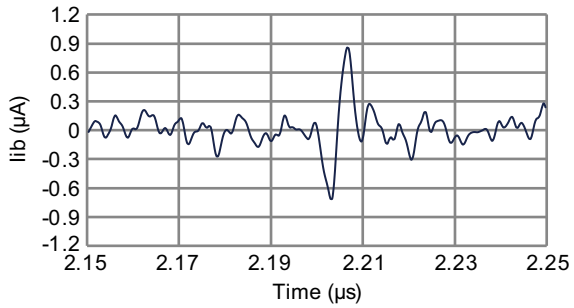


Figure 6. TSZ121 input bias current spike, Vcc = 1.8 V

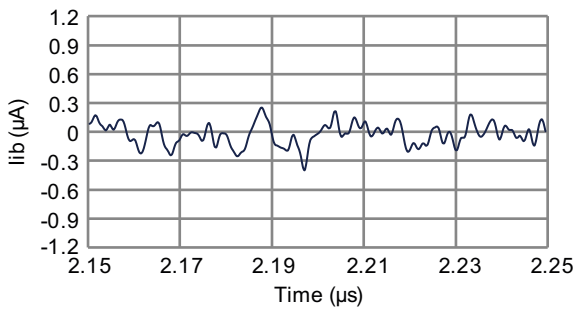


Figure 7. Simulation of input bias current, Vcc = 5.5 V

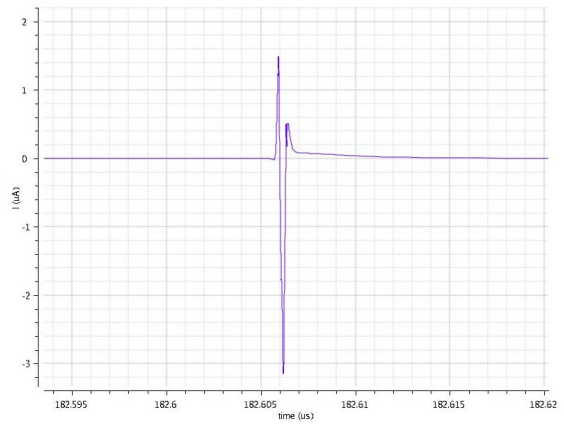
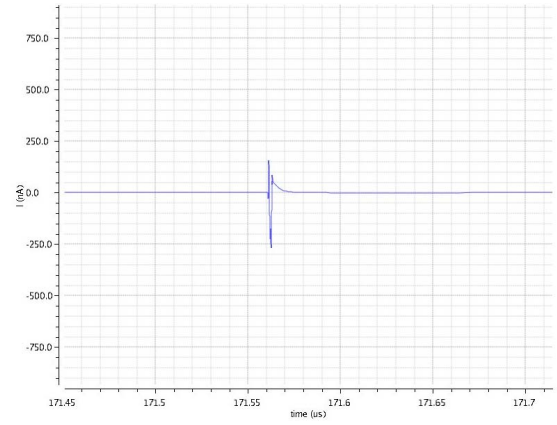


Figure 8. Simulation of input bias current, Vcc = 1.8 V



The input bias current of the TSZ121 datasheet is an average of this current over a long period.

This average DC current can also be expressed mathematically.

We can see in *Figure 1* that there are two stages of MOS, meaning that the charges are injected twice at every clock cycle. So, we can deduce a net DC current on the inputs given by *Equation 2*.

Equation 2

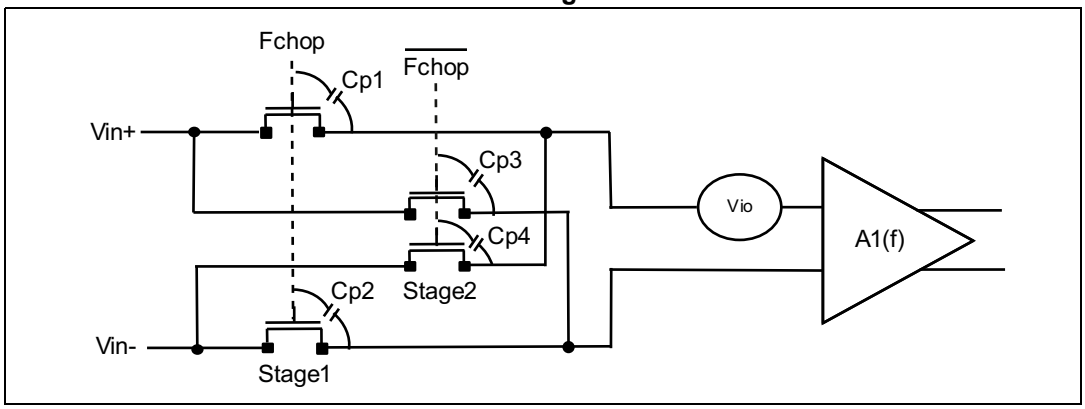
$$Iinj_{DC} = 2 \cdot fchop \cdot Q \qquad (2)$$

Where fchop is the chopping frequency.

1.2 Clock feed through

Current spikes are also due to the imbalanced parasitic capacitance on the input of the chopper which is generally called “clock feed through”. Effectively, as shown in *Figure 9*, the MOS presents a parasitic capacitance, Cp, and an AC spike appears on each clock transition of the chopper stages.

Figure 9. Parasitic capacitance of the chopper architecture causing clock feed through



This AC current can be expressed as a DC current on the input pin of the TSZ121 with an average value given by *Equation 3*.

Equation 3

$$Ioff_{DC} = 2 \cdot fchop \cdot \Delta Cp \cdot Vcc \qquad (3)$$

Where

$$\Delta Cp = (Cp1 - Cp4) - (Cp2 - Cp3)$$

The input bias current expressed in the datasheet of the TSZ121 is represented by the sum of the injection charge and the offset due to the clock feed through. It can be expressed as shown in *Equation 4*.

Equation 4

$$Iib_{average} = Iinj_{DC} + Ioff_{DC} \qquad (4)$$

Due to the chopper architecture using switching MOS, the input bias current of this kind of op amp shows a net DC current slightly higher than a traditional CMOS op amp. As expressed by *Equation 4* the input bias current mainly depends on the Vcc and the input common mode voltage.

Figure 10 and *11* show the variation of the Iib depending on these two parameters. The higher the Vcc, the higher the Inj_{DC} (*Equation 2*) and $Ioff_{DC}$ (*Equation 3*) and so the average value of the Iib increases. However, the higher the input common mode voltage, Vicm, the lower the input bias current (*Equation 2*) because the total charge in the MOS is decreased.

Figure 10. Input bias current vs Vicm

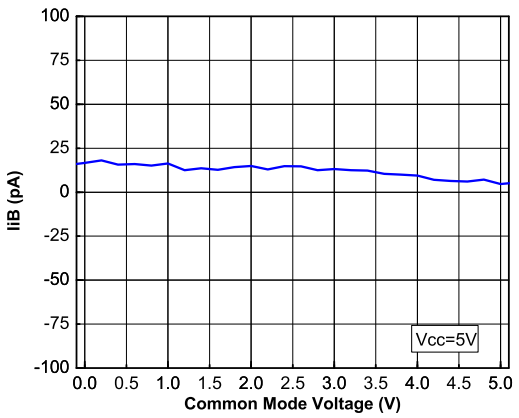
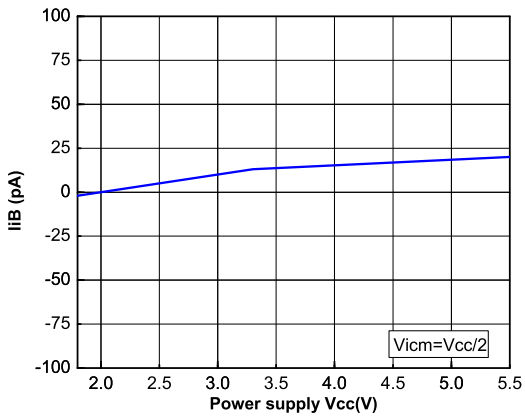


Figure 11. Input bias current vs Vcc



2 Inpact of input current spikes on real applications

The input bias current spikes generated by the chopper architecture, occur at an equivalent high frequency (several GHz) because of their sharp edges. The TSZ121 presents a GBP = 400 kHz. Consequently, these input current spikes are not seen on the output of the TSZ121 when used in closed loop configuration because the device filters them. Nevertheless, the input current spikes might affect what is placed before the TSZ121.

2.1 High impedance input

Generally, special care must be taken with the input current of an op amp when we use a high impedance sensor to limit the error on the input.

In this case, input current spikes might potentially disturb the sensor.

In figures *12* through *16* below, several simulations have been made to emulate a sensor by changing the Rin_load seen by the input of the TSZ121.

Figure 12. Iib spike vs input impedance

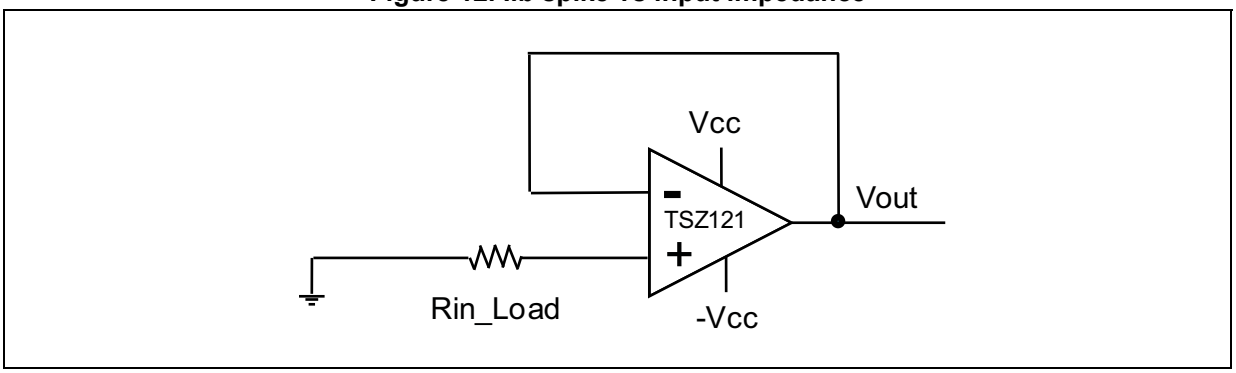


Figure 13. Rin_load = 1 kΩ

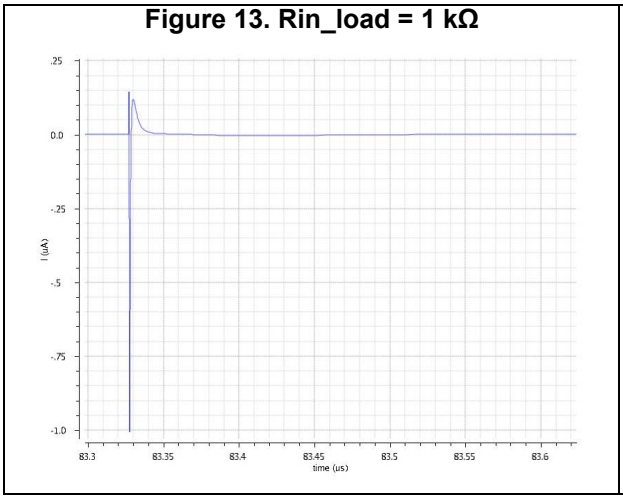


Figure 14. Rin_load = 10 kΩ

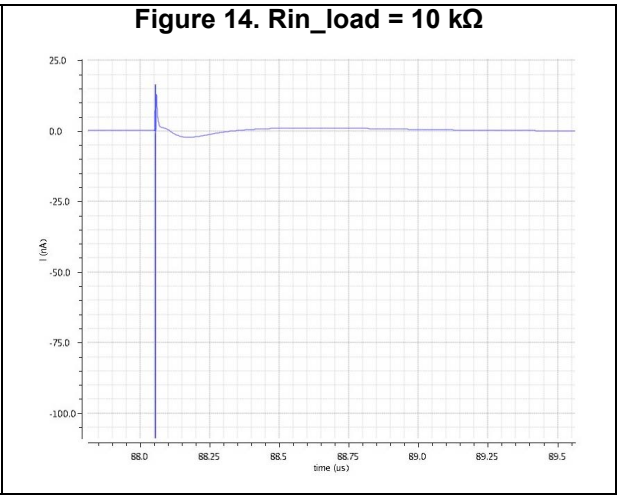


Figure 15. Rin_load = 100 kΩ

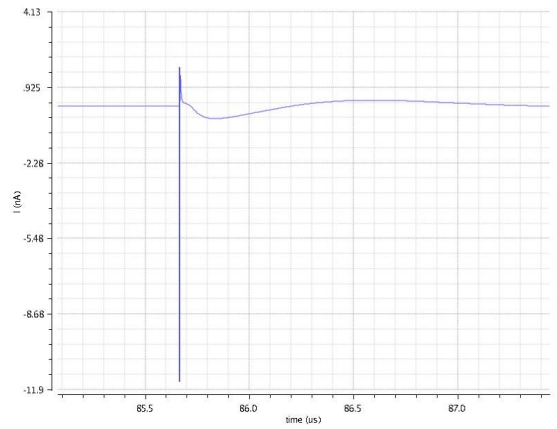


Figure 16. Rin_load = 1 MΩ

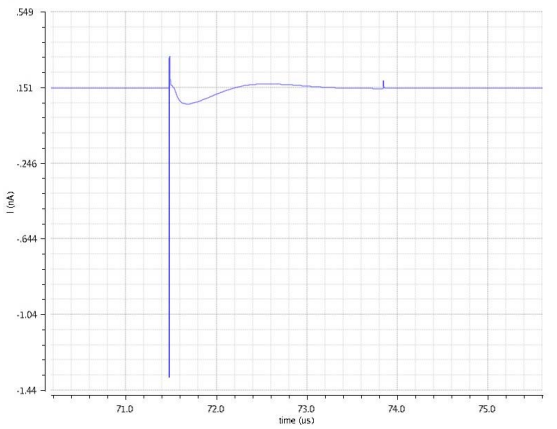


Table 1 summarizes the amplitude of the Iib spikes considering different input impedances seen by the input pin of the TSZ121. These values are calculated from simulations.

Table 1. Iib spike amplitude vs. Rin_load

Rin_load	0 Ω	1 kΩ	10 kΩ	100 kΩ	1 MΩ
Amplitude Iib spike	4.5 µA	1.15 µA	125 nA	13 nA	1.5 nA

We can observe that the higher the impedance on the input pin of the TSZ121, the lower the Iib spikes. Actually, these current spikes follow an internal path with lower impedance.

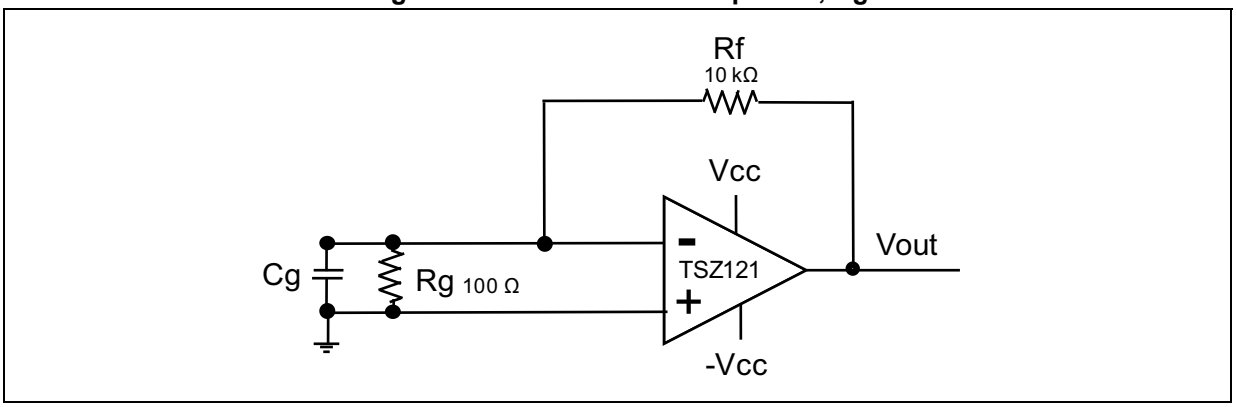
This means that the spikes generated by a chopper op amp should not disturb a high impedance sensor.

2.2 Filter input current spikes thanks to a common mode capacitor

The TSZ121 should not necessarily be used with a high impedance sensor which naturally smooths the Iib spikes.

In the case of a low impedance sensor, it may be interesting to filter the input current spikes by using a common mode capacitor as shown in *Figure 17*.

Figure 17. Common mode capacitor, Cg



At high frequency (current spikes) the common mode capacitor, Cg, shows lower impedance than that of the sensor. In this case, Cg draws the main part of the current as a consequence of filtering the input current spikes.

Figure 18 and *19* are snapshot probes measured on the TSZ121. They show that the Iib spikes have been filtered by adding a common mode capacitor of 10 pF.

Figure 18. TSZ121 input bias current spike, Vcc = 5.5 V

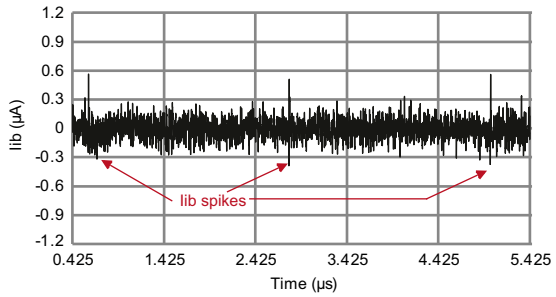
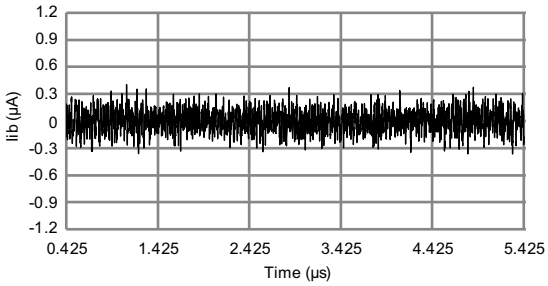


Figure 19. TSZ121 Iib filtered by a common mode capacitor, Cg = 10 pF, Vcc = 5.5 V



Adding a common mode capacitor, helps significantly to filter the Iib spikes generated by the chopper input stage. Obviously, the higher the capacitor, the better the filtering. But we cannot increase the capacitance value too much without risking system instability.

Below, we calculate the maximum value of the Cg capacitor to ensure good stability.

The loop gain is given by *Equation 5*.

Equation 5

$$-A\frac{Rg}{Rg+Rf}\times\frac{1}{1+jw\left(\frac{Rg\cdot Rf}{Rg+Rf}\cdot Cg\right)} \quad (5)$$

Where A is the open loop transfer function of the op amp.

One pole appears as shown in *Equation 6*.

Equation 6

$$fp = \frac{1}{2\pi \cdot \frac{Rf \cdot Rg}{Rf + Rg} \cdot Cg} \quad (6)$$

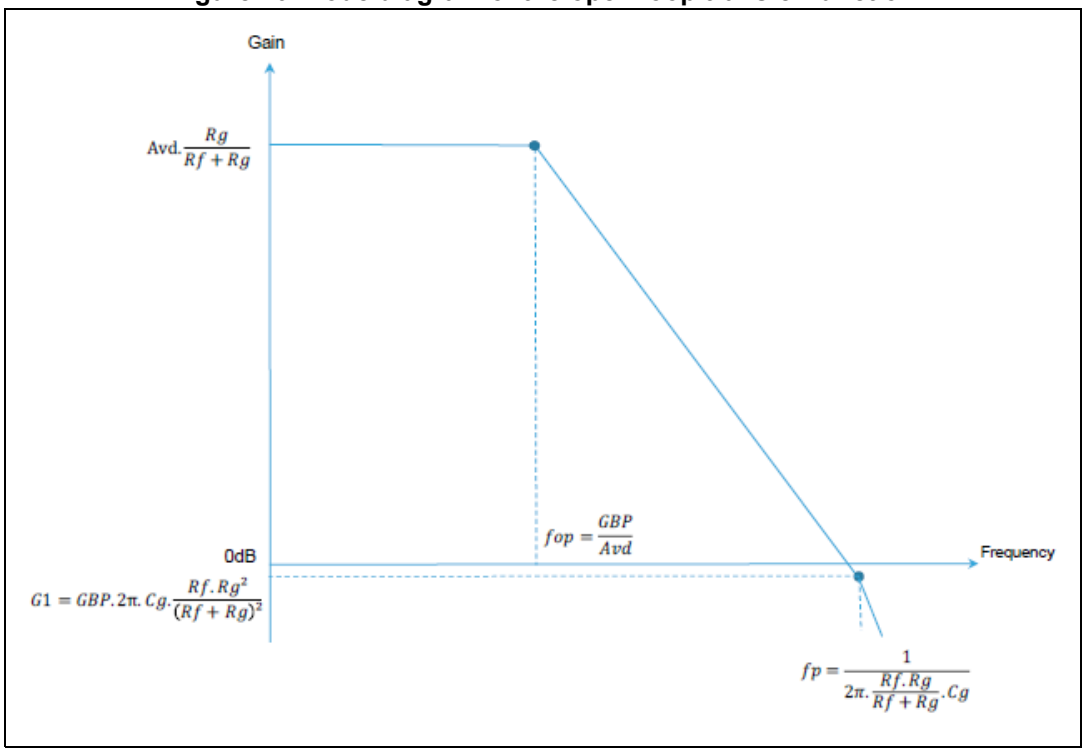
In addition to the pole of *Equation 6*, we have to consider the low frequency pole of the open loop transfer function of the operational amplifier as shown in *Equation 7*.

Equation 7

$$fop = \frac{GBP}{Avd} \quad (7)$$

The bode diagram of this system can be plotted as shown in *Figure 20*.

Figure 20. Bode diagram of the open loop transfer function



To guaranty the stability of the system, the bode diagram must cross the X-axis with a slope of -20 dB/decade.

So, considering *Figure 20* and to ensure stability, the gain at frequency fp, must be lower than 1 (see *Equation 8*).

Equation 8

$$GBP \cdot 2\pi \cdot Cg \cdot \frac{Rf \cdot Rg^2}{(Rf + Rg)^2} < 1 \quad (8)$$

We can deduce the maximum capacitance, Cg, to guarantee the stability of the TSZ121 using *Equation 9*.

Equation 9

$$Cgmax = \frac{(Rf + Rg)^2}{2\pi \cdot GBP \cdot Rf \cdot Rg^2} \quad (9)$$

In this application:

- GBP = 400 kHz
- Rg = 100 Ω
- Rf = 10 kΩ

Therefore, the maximum capacitance does not exceed Cg = 406 nF.

3 Conclusion

The chopper op amp, due to its internal switching architecture, generates current spikes on its input pins. This explains why the average input bias current of a chopper is slightly higher than a traditional op amp.

Depending on the application environment, these input current spikes, of a few µA, might make some designers apprehensive about using a chopper op amp.

However, we have seen in this application note that using a chopper with a high impedance sensor tends to limit the amplitude of these spikes and it should not disturb the sensor.

Moreover, adding a common mode capacitor also helps to filter the input current spikes. The value of this capacitor must be chosen carefully in order to keep the whole system stable.

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
28-Oct-2014	1	Initial release