AN4568
Application note

Differences between SPC56EL70x and SPC56EL60x devices family

Introduction

The SPC56ELx family is developed around the central requirement for functional safety.

This family includes two different devices:

- SPC56EL60x
- SPC56EL70x

These two devices are highly compatible in terms of hardware and software. SPC56EL70x device is considered as a compatible extension of SPC56EL60x devices.

The aim of this document is to highlight which are the differences between these two devices.

A short summary of the enhancement is:

- Flash
  - 2MB of Flash in SPC56EL70x
  - 1MB of Flash in SPC56EL60x
- SRAM
  - 192KB of RAM in SPC56EL70x
  - 128KB of RAM in SPC56EL60x
- FlexCAN
  - 3 modules in SPC56EL70x
  - 2 modules in SPC56EL60x.

This document considers SPC56EL70x devices cut 2.0 and SPC56EL60x devices cut 3.2.

The SPC56EL70 follows a Functional Safety process compliant with ISO26262:2011 ASIL D requirements.

This process has been already used to develop the SPC56EL60, that has been assessed by Exida to have a "Systematic Integrity: ASIL D" according to the ISO 26262:2011.

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1 JTAG ID number and MIDR

The two devices have different JTAG ID and MIDR values as shown in *Table 1*.

Table 1. Differences on JTAG ID and MIDRx

	JTAG_ID	MIDR1.PRTNUM	MIDR2.FLASH_SIZE_1	MIDR2.FLASH_SIZE_2
SPC56EL60x	0x3AEA_3041	0x5653	0x6	0x0
SPC56EL70x	0x0AEA_9041	0x5646	0x7	0x0

2 Flash

SPC56EL70x device embeds a Flash that is twice the size of the one embedded in SPC56EL60x devices.

Flash partitioning is slightly different as shown in *Table 2*.

Table 2. Flash partitioning

Flash partitions	SPC56EL60x	SPC56EL70x
Partition 1	16KB	16KB
Partition 1	48KB	16KB
Partition 1	48KB	16KB
Partition 1	16KB	16KB
Partition 2	64KB	16KB
Partition 2	64KB	16KB
Partition 2	-	16KB
Partition 2	-	16KB
Partition 3	128KB	64KB
Partition 3	128KB	64KB
Partition 4	256KB	128KB
Partition 4	256KB	128KB
Partition 5	-	256KB
Partition 5	-	256KB
Partition 6	-	256KB
Partition 6	-	256KB
Partition 7	-	256KB
Partition 7	-	256KB

During the boot process the device searches multiple predefined Flash locations for a valid boot ID.

The lowest sector that starts with a valid boot ID is used to boot the device (refer to section “Potential boot sectors” from reference manual to have all details about this topic see *B.1: Reference document*).

SPC56EL70x devices implement two additional Flash locations that are searched during the boot process as shown in *Table 3*.

Table 3. Potential boot sectors

Search order	SPC56EL60x devices sectors	SPC56EL70x devices sectors
1	0x0000_0000	0x0000_0000
2	0x0000_4000	0x0000_4000

Table 3. Potential boot sectors (continued)

Search order	SPC56EL60x devices sectors	SPC56EL70x devices sectors
3	0x0001_0000,	0x0001_0000
4	0x0001_C000	0x0001_C000
5	0x0002_0000	0x0002_0000
6	0x0003_0000	0x0003_0000
7	-	0x0000_8000
8	-	0x0000_C000

3 RAM

Differences on RAM integration depend on the selected mode.

Table 4. RAM implementation

SPC56EL60x	SPC56EL70x
Lock-step mode (LSM)	
128KB starting at 0x4000_0000	192KB starting at 0x4000_000
Decoupled parallel mode (DPM)	
64KB starting at 0x4000_0000	96KB starting at 0x4000_0000
64KB starting at 0x5000_0000	96KB starting at 0x5000_0000

4 FlexCAN

SPC56EL70x devices embed an additional FlexCAN with respect to the ones embedded in SPC56EL60x devices, i.e. FlexCAN_2.

Integration and usage of FlexCAN_0 and FlexCAN_1 are identical on both SPC56EL60x and SPC56EL70x devices.

FlexCAN_2 requires some additional interrupts and registers as described in the below tables.

Base address of FlexCAN_2 is 0xFFFC_8000.

Table 5. Additional interrupts related to FlexCAN_2

IRQ#	Offset	Source Signal	Source Module for INTC_0/1
105	0x0690	FLEXCAN_ESR[ERR_INT]	FlexCAN_2
106	0x06A0	FLEXCAN_ESR_BOFF | FLEXCAN_Transmit_Warning | FLEXCAN_Receive_Warning	FlexCAN_2
107	0x06B0	FLEXCAN_ESR_WAK	FlexCAN_2
108	0x06C0	FLEXCAN_BUF_00_03	FlexCAN_2
109	0x06D0	FLEXCAN_BUF_04_07	FlexCAN_2
110	0x06E0	FLEXCAN_BUF_08_11	FlexCAN_2
111	0x06F0	FLEXCAN_BUF_12_15	FlexCAN_2
112	0x0700	FLEXCAN_BUF_16_31	FlexCAN_2

Table 6. Additional registers to configure the FlexCAN_2's behavior

Module	Register	Description
MC_ME	ME_PCTL18	This register select the configurations during run and non-run modes for FlexCAN_2
MC_ME	ME_PS0.S_FlexCAN_2	This register provides the status of the FlexCAN_2
SIUL	PSMI[43]	This register define pads as input to FlexCAN_2

Table 7. FlexCAN_2 pin out

PAD	ALT Mode	Function
A[7]	ALT 2	CAN_2_RX
A[8]	ALT 2	CAN_2_TX
F[14]	ALT 2	CAN_2_RX
F[15]	ALT 2	CAN_2_TX

5 Summary

This document highlights the differences between SPC56EL60x and SPC56EL70x devices.

Considering the small number of differences, it is possible to develop an application that runs on both SPC56EL60x and SPC56EL70x devices.

Typical applications running on SPC56EL60x can be ported on SPC56EL70x without any modification.

Appendix A Documentation comparison

Most of the technical documentation developed for SPC56EL60x devices are also valid for SPC56EL70x devices.

Table 8. Documentation comparison

DOC number	Title	Valid for SPC56EL70x	Comments
AN4429	RPC56xx and SPC56xx C90FL Flash recovery in case of brownout during Flash erase operation	Yes	Additional FlexCAN, bigger RAM and Flash shall be taken into account.
AN3229	Using DMA and CRC for configuration integrity check with SPC56ELx devices	Yes	
AN3121	Getting started tutorial for SPC56EL60	Yes	Additional FlexCAN, bigger RAM and Flash shall be taken into account.
AN3242	Flash ECC logic test for SPC56ELx	Yes	Bigger Flash shall be taken into account.
AN3237	How to configure and service the watchdog timer of SPC56ELx	Yes	
AN3324	Implementing power-on self-tests for SPC56ELx in lock step mode	Yes	Bigger Flash shall be taken into account.
AN4124	Using SPC56EL60x/RPC56EL60x fault collection and control unit (FCCU)	Yes	
AN4253	SPC564Lx device startup flow	Yes	
AN4367	SPC56EL60xx/RPC56EL60xx/SPC56xL70xx/RPC56xL70xx device exception handling	Yes	
AN4371	SPC56ELxx/RPC56ELxx ADC Built-in self-tests ADC working in CPU mode	Yes	
AN4417	SPC564Axx/RPC564Axx/SPC56ELxx/RPC56ELxx devices Exception handling and single/double bit error	Yes	
DS9374	32-bit Power Architecture® microcontroller for automotive SIL3/ASILD chassis and safety applications	-	SPC56EL70x family has a dedicated DS
RM0342	SPC56XL70xx 32-bit MCU family built on the embedded Power Architecture®	-	SPC56EL70x family has a dedicated RM
ES0207	SPC56xL70, SPC56xL64 devices errata JTAG_ID = 0X0AEA_9041	-	SPC56EL70x family has a dedicated Errata sheet. SPC56EL70x family has an additional errata compared with the SPC56EL60x family. This errata is related to the integration of the additional FlexCAN available on SPC56EL70x, i.e. e0063.

Table 8. Documentation comparison (continued)

DOC number	Title	Valid for SPC56EL70x	Comments
	Reference code	Yes	Reference code working on SPC56EL60x devices works also in SPC56EL70x devices. The other way round is not always true due to the larger hardware resources of SPC56EL70x devices.
	SAG	-	SPC56EL70x devices has a dedicated SAG (99% equal to the SPC56EL60x devices)
	SAG addendum	Yes	

Appendix B Further information

B.1 Reference document

1. *SPC56EL60 32-bit MCU family built on the embedded Power Architecture®* (RM0032 Doc ID 15265)
2. *SPC56XL70xx 32-bit MCU family built on the embedded Power Architecture®* (RM0342 Doc ID 023986)

B.2 Acronyms

Table 9. Acronyms

Acronym	Name
RAM	Random Access Memory
IRQ	Interrupt request
MC_ME	Mode Entry Module
SIUL	System Integration Unit Light
DS	Datasheet
RM	Reference Manual

Revision history

Table 10. Document revision history

Date	Revision	Changes
11-Aug-2014	1	Initial release.
06-Nov-2014	2	Updated *Table 8*.
21-Dec-2021	3	Added in the introduction a statement on the ISO26262.