AN4472
Application note

STEVAL-IME008V1 evaluation board based on the STHV749 transmission pulser

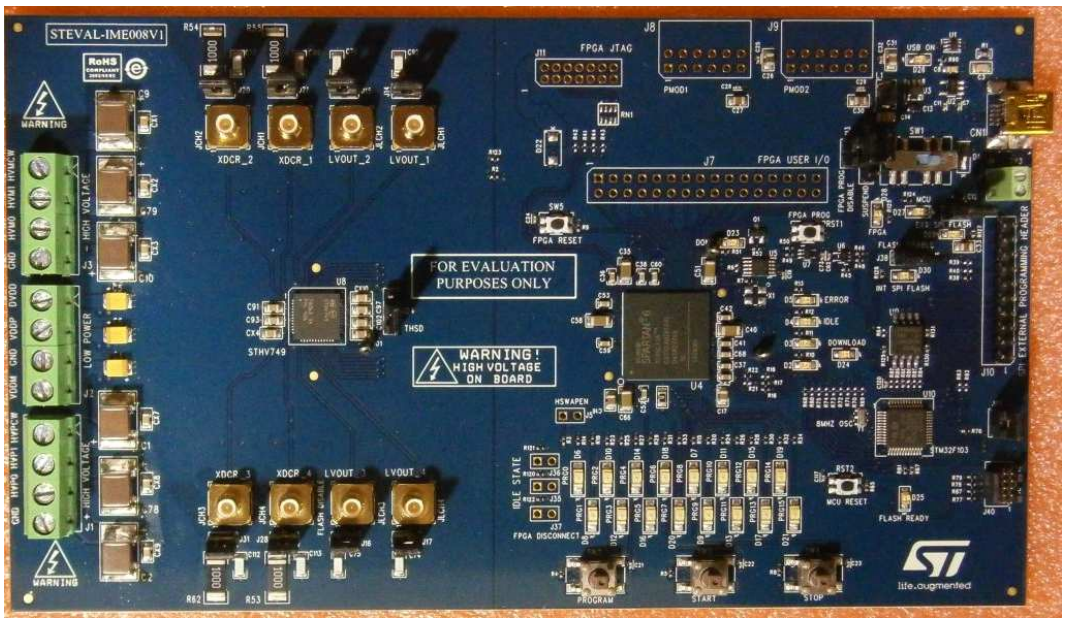
Introduction

The STEVAL-IME008V1 is an evaluation board designed around the STHV749 transmission pulser, a state-of-the-art solution for ultrasound imaging applications.

The system can drive four transducers as 4-channel transmitters and the output waveforms can be displayed directly on an oscilloscope by connecting the scope probe to the relative BNCs.

16 preset waveforms are available to test the HV pulser under different conditions.

Figure 1. Photo of STEVAL-IME008V1



Warning: **Before applying any voltage supply to the STEVAL-IME008V1, please read the instructions contained in this document carefully.**

Contents

1 Board features 3

2 Getting starting 4

3 Hardware layout and configuration 5

3.1 Power supply 6

3.2 MCU 7

3.3 SPI Flash memory 7

3.4 FPGA 8

3.4.1 Stored patterns 11

3.4.2 Pattern program 0 (3-level and 5-level output option) 11

3.4.3 Pattern Program 1 (SEL = 1, 5-level output option) 13

3.4.4 Pattern Program 2 16

3.4.5 Pattern Program 3 17

3.4.6 Pattern Program 4 19

3.4.7 Pattern Program 5 21

3.4.8 Pattern Program 6 23

3.5 STHV749 stage 25

3.6 Operating supply conditions 28

4 Connectors 29

4.1 Power supply 29

4.2 Power-up sequence 30

4.3 MCU 30

4.4 SPI Flash memory 31

4.5 FPGA 32

5 Schematic diagrams 34

6 Revision history 43

1 Board features

- Suitable for ultrasound imaging applications
- 4 monolithic channels, 5-level high voltage pulser
- Integrated T/R switch
- On-board equivalent piezoelectric load implemented by means of an R/C equivalent network
- USB interface for uploading customized output waveforms
- 4 Mb serial Flash memory for storing customized waveforms
- Memory expansion connector for expanding the serial Flash size
- High voltage and low voltage connectors to power the STHV749
- 25 LEDs to check board status and proper operation
- Human machine interface to select, start and stop the stored output waveforms

2 Getting starting

The STEVAL-IME008V1 is shipped by STMicroelectronics, ready to use in Normal mode. The user only needs to:

1. plug the right power supply to the board (see *Section 3.1*)
2. connect the BNC to the oscilloscope
3. check that switch SW1 is set on the FPGA position
4. check that the LED indicator DONE (D23) turns on
5. check that FPGA is in the idle state (LED D4 is on)
6. select the waveform with the Program button – the corresponding program LED (D6-D21) turns on
7. press the START button to run the selected program – the START LED (D2) turns on
8. the selected waveform continuous until the STOP button is pressed, which lights the relative LED (D3) – when the program ends, the FPGA returns to the idle state (LED D4 is on)
9. to run the same program again, restart from step 7; to run another program, restart from step 6

For Programming mode information, please refer to UM1083.

3 Hardware layout and configuration

The hardware block diagram (*Figure 2*) illustrates the main connection between STHV749, the FPGA, the STM32F103C8T6 and the SPI Flash memory. *Figure 3* shows the connectors, LEDs and features on the board.

Figure 2. Hardware block diagram

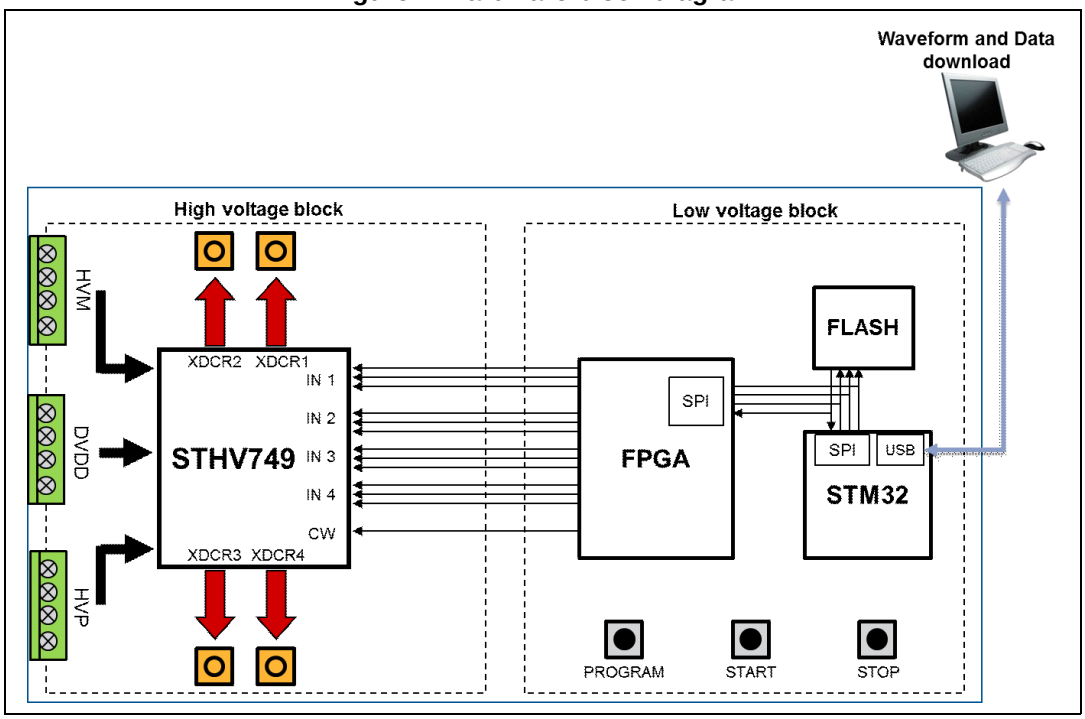
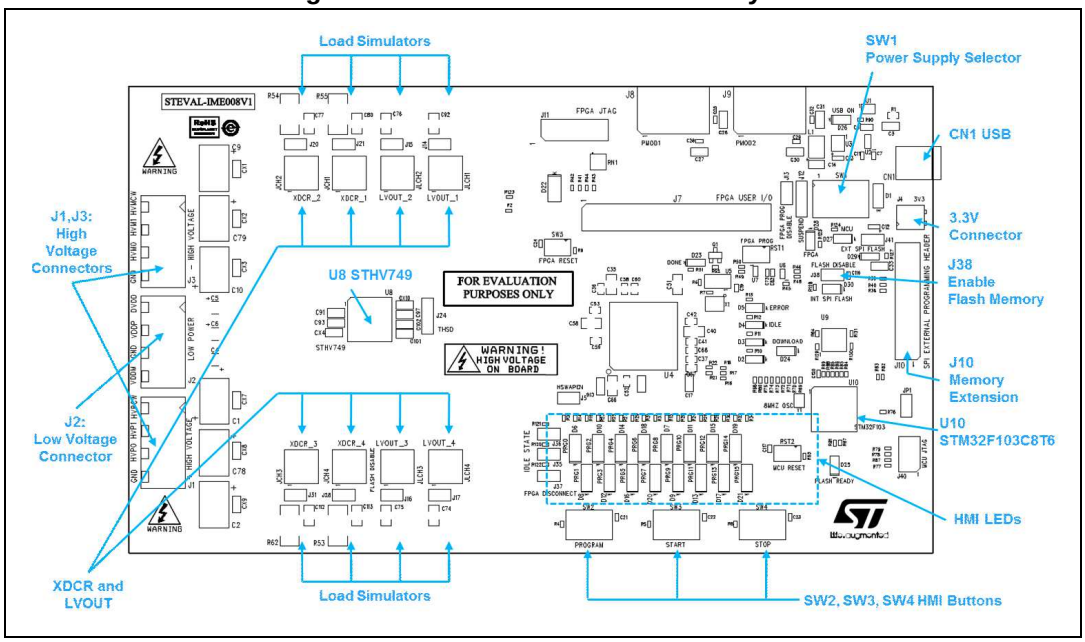


Figure 3. STEVAL-IME008V1 board layout



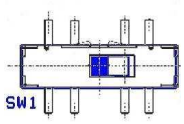
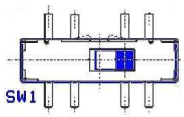
3.1 Power supply

The low voltage block of the STEVAL-IME008V1 board is designed to be powered by:

- 3.3 V DC connected to J4 to supply FPGA and SPI Flash memory in Normal mode
- 5 V DC through the USB Mini B connector to supply the STM32 and the SPI Memory in Programming mode

The power supply is configured by setting SW1 and J41 as described in *Table 1*.

Table 1. Power related Jumpers

	Description	
SW1	 LEFT (1)	For *normal* operation mode, supplying power to FPGA and SPI Flash memory. Default Setting
	 RIGHT (1)	For *update* operation mode, supplying power to STM32F103 and SPI Flash memory
J41	FPGA and SPI Flash memory are powered by DVDD (J2). Default setting: Not Mounted on PCB	

1. Left and Right are conceived by looking the board as depicted in *Figure 1*.

Note: Fitting the J41 jumper can create a voltage mismatch between J4 and J2 when either of these is not 3.3 V.

LED D26, D27 and D28 show the power supply configuration as described in *Table 1*.

Table 2. Power supply LEDs

	Color	Name	Description
D26	Red	USB ON	The USB cable is plugged
D27	Red	MCU	Programming mode, supplying power to STM32F103 and SPI Flash memory
D28	Red	FPGA	Normal mode, supplying power to FPGA and SPI Flash memory

The high voltage block of the STEVAL-IME008V1 is designed to be powered by (see *Table 23* for maximum rating):

- HVPCW: Continuous wave high voltage positive supply (J1 conn.)
- HVP0:TX0 High voltage positive supply (J1 conn.)
- HVP1:TX1 High voltage positive supply (J1 conn.)

- GND: Ground (J1 conn.)
- DVDD: Logic voltage, 3.3 V (J2 conn.)
- VDDP: Positive supply voltage 3.3 V (J2 conn.)
- VDDM: Negative supply voltage -3.3 V to 0 (J2 conn.)
- GND: Ground (J2 conn.)
- HVMCW: Continuous wave high voltage negative supply (J3 conn.)
- HVM0: TX0 high voltage negative supply (J3 conn.)
- HVM1:TX1 high voltage negative supply (J3 conn.)
- GND: Ground (J2 conn.)

Note: Supply high voltage only in Normal mode and not in Programming mode

3.2 MCU

The STM32F103C8T6 is dedicated to updating the waveform and the FPGA bit stream on the SPI Flash memory. It is pre-programmed as a DFU (device firmware upgrade) device, and can upgrade internal and external FLASH memory.

The STM32F103 manages all the DFU operations such as product identifier, vendor identifier and Firmware version authentication as well as the alternate setting number (Target ID), used to upgrade the SPI Flash memory on the STEVAL-IME008V1 and render upgrades more secure.

Note: See AN3156 and UM0412 for further details about the upgrade through DFU.

3.3 SPI Flash memory

The STEVAL-IME008V1 hosts a Micron N25Q032 (U9) 32-Mbit (4 Mb x 8) serial Flash memory bank with advanced write protection mechanisms. It can be accessed by a high speed SPI-compatible bus and can function in XIP ("eXecution in Place") mode.

The N25Q032 also supports high-performance quad I/O instructions; these instructions allow quadrupling of the transfer bandwidth for read and program operations used by the FPGA.

If this memory is insufficient, the user can disable the on-board Flash by disconnecting J38 (see *Table 4*) and connect external Flash memory via the J10 connector (see *Table 27*). When the external Flash is connected, LED D29 is lit (*Table 3*).

Table 3. SPI Flash memory LED

	Color	Name	Description
D29	Green	EXT SPI-FLASH	The external SPI-Flash Module is connected
D30	Red	On-board SPI-FLASH	The on-board SPI-Flash is used

The Flash memory is configured by setting J38 as described in *Table 4*.

Table 4. SPI Flash memory Jumper

	Status	Description
J38	Closed	Connected, supply power to the on-board SPI Flash memory (U9). Default setting: Connected
	Open	Not Connected, the on-board SPI Flash memory will not receive the power supply.

3.4 FPGA

The STEVAL-IME008V1 includes a Xilinx Spartan®-6 XC6SLX16 FPGA, which drives the STHV749 pulser by generating a suitable sequence of digital control signals (called programs). The board can store 16 individually selectable programs.

The main features of waveforms generated by a program are summarized in *Table 5*.

Table 5. Programmable waveforms main features

Feature	Min.	Default	Max.
Programmable Waveforms Number	1	6	16
Pulse Time Resolution	-	5 ns	-
Pulse Pattern Duration (1)	40 ns	-	20.48 µs
Cycle Period (PRF) (2)	40 ns	-	2621.44 µs
Cycles Number	1	-	255
Infinite cycle	defined by the program		

1. Time period of the pulse sequence pattern.
2. Time period of a pulse repetition cycle.

The data required to generate a program is stored in the SPI Flash memory. When the program starts, data is downloaded from Flash memory and stored in FPGA internal RAM blocks where it is manipulated to generate the high-speed STHV749 digital control signals.

SPI Flash also contains FPGA configuration data (bit stream) which is automatically loaded during start-up and after the FPGA reset (SW5) is pressed.

The FPGA is configured by setting jumpers as described in *Table 6*.

Table 6. FPGA Jumper

	Description	
J5	J5 is used to control FPGA I/O pull ups during configuration. It should be connected to enable I/O pull ups during FPGA configuration. Default setting: Not connected.	
J12	Force FPGA into Suspend mode	
	Allow STM32 to control FPGA Suspend mode (default setting)	

Table 6. FPGA Jumper (continued)

	Description	
J13	J13 is used to prevent FPGA programming from configuration source. Connected: disable FPGA programming. Not Connected: enable FPGA programming. (default setting: not connected)	
J35 and J36	Configure J35 and J36 to setup outputs idle state as follows: (default setting: Not connected)	
	High Z	J35 and J36 not connected
	Clamp / HVR_SW	J35 connected, J36 not connected
	High Z	J35 and J36 connected
	Clamp	J35 not connected, J36 connected
J37	Configure J37 to connect FPGA outputs to STHV749 (default setting: Not connected)	
	Connected: disconnect FPGA outputs (High Z)	
	Not Connected: connect FPGA outputs	

Once the FPGA has been configured, the DONE LED (D23) turns on and the FPGA state machine initiates the idle state entry sequence (LED D4 turns on).

Use the program button to select and generate the desired waveform (refer to *Section 3.4.1*), which is highlighted by a corresponding LED (D6-D21 represent Program 0-Program 15 respectively). The selection following the last installed program cycles back to Program 0.

The START button activates the selected program and the START LED (D2) turns on. When the program ends, the FPGA returns to the idle state (LED D4 is on). If a continuous wave program is selected, the STOP button must be pressed to stop program execution; the FPGA returns to the idle state and the STOP LED (D3) turns on. The LEDs associated with FPGA operations are described in *Table 7*.

Table 7. FPGA LED

	Color	Name	Description
D2	Green	START	A program is running after the START button SW5 is pressed.
D3	Green	STOP	The STOP button SW4 has been pressed.
D4	Green	IDLE	The FPGA state machine is in the idle state.

Table 7. FPGA LED (continued)

	Color	Name	Description
D5	Red	ERROR	An error has occurred during FPGA state machine execution.
D23	Green	DONE	The FPGA has been successfully configured.
D6-D21	Yellow	PROG 0-15	The corresponding program is selected

The FPGA state machine can be also controlled by an external digital device through the FPGA USER I/O connector (J7); see *Table 28* for the relative naming and pin-out positioning.

To enable remote control of the board through an external device, the REMOTE_ENABLE pin must be set high. The waveform program can be selected by setting the PROG<3:0> port. If an uninstalled program is selected, the ERROR output signal goes high. Also, the idle state can be selected through the IDLE_SEL<1:0> port. If remote control is enabled, the Program, Start and Stop buttons are disabled.

A waveform program can be started by means of the REMOTE_START signal (active high) and stopped by setting high the REMOTE_STOP signal. Either the FPGA reset (SW5) or REMOTE_RESET signal can be used to reset the FPGA.

Some internal FPGA control signals can be monitored through the FPGA USER I/O connector (regardless of whether remote control is enabled or disabled). *Figure 4* and *Figure 5* show the expected behavior of these timing control signals.

Figure 4. FPGA timing control signals (beginning of cycle n)

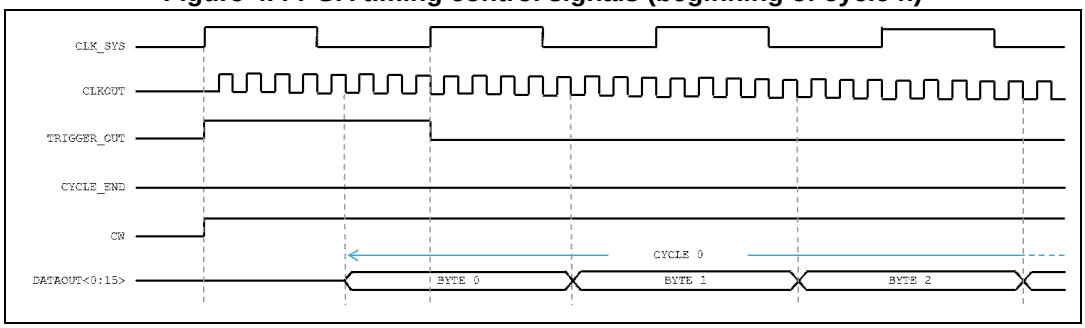
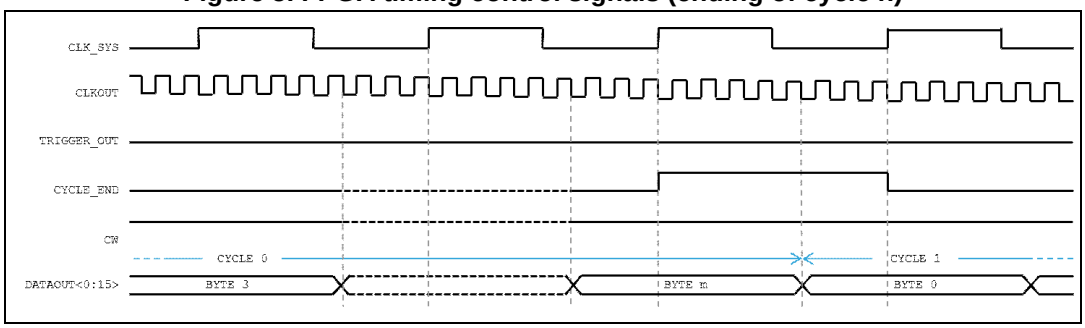


Figure 5. FPGA timing control signals (ending of cycle n)



3.4.1 Stored patterns

The STEVAL-IME008V1 allows up to 16 patterns to be stored in the on-board Flash memory in order to demonstrate the potential performance of the pulser outputs. Listed below are the default patterns already stored in the Flash memory and available for immediate use.

3.4.2 Pattern program 0 (3-level and 5-level output option)

The first pattern stored in the SPI Flash is described in *Table 8*, where the output pulses are in phase. The state sequence is given in *Table 9*.

The test conditions applied to generate the waveforms in *Figure 6* and *Figure 7* are:

- HVP0 = HVP1 = + 80 V
- HVM0 = HVM1 = - 80 V
- Load: 300 pF // 100 Ω

Table 8. Program 0

	Mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PW	5	10	positive	150 µs	TX0, TX0 & 1
XDCR_2	PW	5	10	negative	150 µs	TX0, TX0 & 1
XDCR_3	PW	5	10	positive	150 µs	TX1, TX0 & 1
XDCR_4	PW	5	10	negative	150 µs	TX1, TX0 & 1

Table 9. State sequence Program 0 [SEL=1 (5-level output), SEL=0 (3-level output)]

XDCR_1		XDCR_2		XDCR_3		XDCR_4		SEL
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	“1”
HVP0	100 ns	HVM0	100ns	HVP1	100 ns	HVP1	100 ns	“1”
HVM0	100 ns	HVP0	100ns	HVM1	100 ns	HVM1	100 ns	“1”
HVP0	100 ns	HVM0	100ns	HVP1	100 ns	HVP1	100 ns	“1”
HVM0	100 ns	HVP0	100ns	HVM1	100 ns	HVM1	100 ns	“1”
HVP0	100 ns	HVM0	100ns	HVP1	100 ns	HVP1	100 ns	“1”
HVM0	100 ns	HVP0	100ns	HVM1	100 ns	HVM1	100 ns	“1”
HVP0	100 ns	HVM0	100ns	HVP1	100 ns	HVP1	100 ns	“1”
HVM0	100 ns	HVP0	100ns	HVM1	100 ns	HVM1	100 ns	“1”
HVP0	100 ns	HVM0	100ns	HVP1	100 ns	HVP1	100 ns	“1”
HVM0	100 ns	HVP0	100ns	HVM1	100 ns	HVM1	100 ns	“1”
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	“1”
RX	145 µs	RX	145 µs	RX	145 µs	RX	145us	“1”
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	“0”
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns	“0”
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns	“0”
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns	“0”

Table 9. State sequence Program 0 [SEL=1 (5-level output), SEL=0 (3-level output)] (continued)

XDCR_1		XDCR_2		XDCR_3		XDCR_4		SEL
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns	“0”
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns	“0”
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns	“0”
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns	“0”
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns	“0”
HVP	100 ns	HVM	100 ns	HVP	100 ns	HVP	100 ns	“0”
HVM	100 ns	HVP	100 ns	HVM	100 ns	HVM	100 ns	“0”
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	“0”
RX	145 µs	RX	145 µs	RX	145 µs	RX	145 µs	“0”

Figure 6. Acquisition by Program 0 with SEL=1, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively

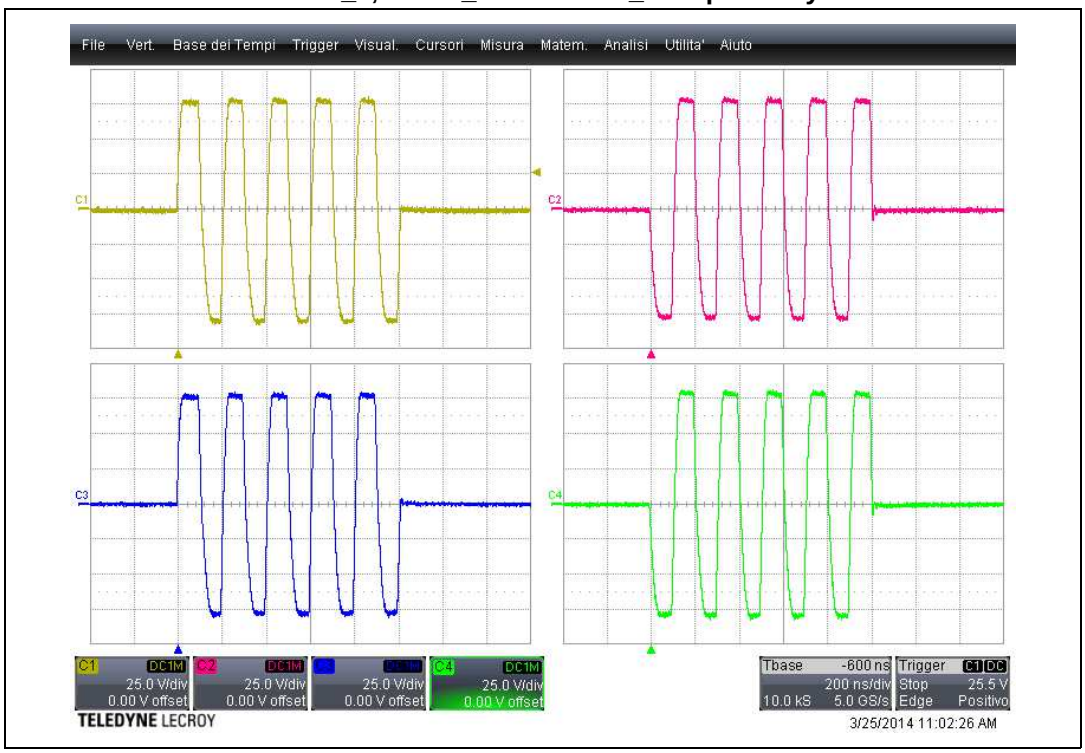
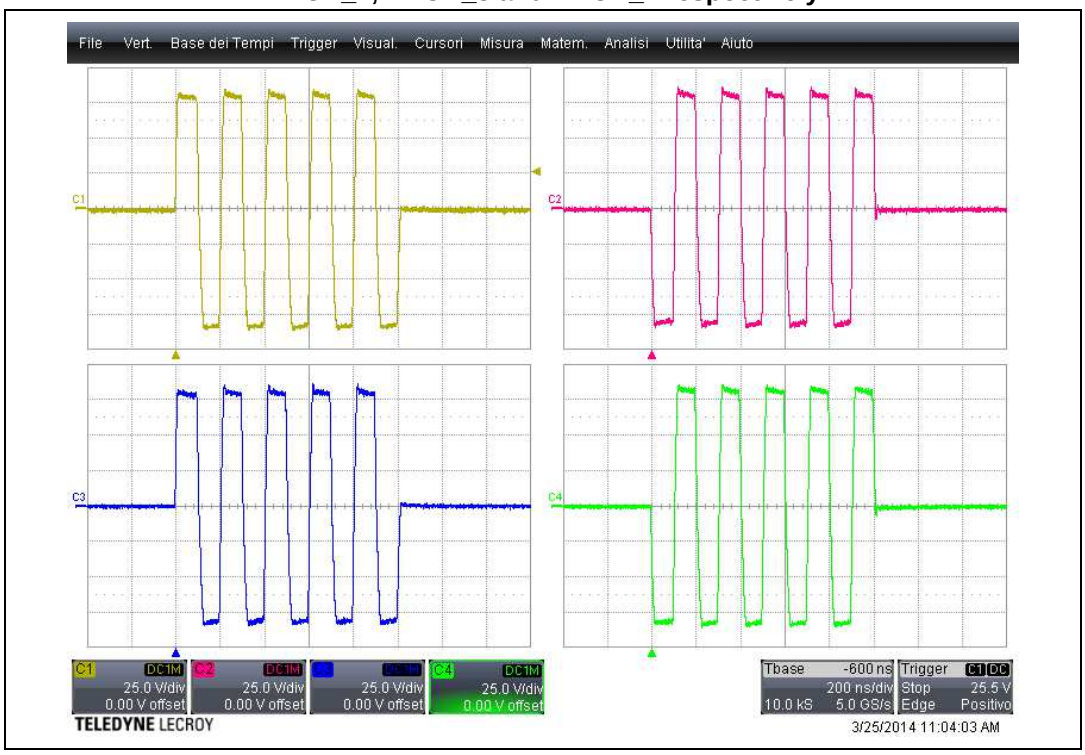


Figure 7. Acquisition by Program 0 with SEL=0, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



3.4.3 Pattern Program 1 (SEL = 1, 5-level output option)

The second pattern stored in the SPI Flash is described in *Table 10*, where the output pulses are delayed by 10 ns each. The state sequence is given in *Table 11*.

The test conditions applied to generate the waveforms in *Figure 8* and *Figure 9* are:

- HVP0 = + 80 V
- HVP1 = + 40 V
- HVM0 = - 80 V
- HVM1 = - 40 V
- Load: 300 pF // 100 Ω

Table 10. Program “1”

	mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PW	5	10	positive	150 µs	TX0, TX1
XDCR_2	PW	5	10	positive	150 µs	TX0, TX1
XDCR_3	PW	5	10	positive	150 µs	TX1, TX1
XDCR_4	PW	5	10	positive	150 µs	TX1, TX1

Table 11. State sequence Program “1”

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
CLAMP	1 µs	CLAMP	1.01 µs	CLAMP	1.02 µs	CLAMP	1.03 µs
HVP0	100 ns	HVP0	100 ns	HVP0	100 ns	HVP0	100 ns
HVM0	100 ns	HVM0	100 ns	HVM0	100 ns	HVM0	100 ns
HVP0	100 ns	HVP0	100 ns	HVP0	100 ns	HVP0	100 ns
HVM0	100 ns	HVM0	100 ns	HVM0	100 ns	HVM0	100 ns
HVP0	100 ns	HVP0	100 ns	HVP0	100 ns	HVP0	100 ns
HVM0	100 ns	HVM0	100 ns	HVM0	100 ns	HVM0	100 ns
HVP0	100 ns	HVP0	100 ns	HVP0	100 ns	HVP0	100 ns
HVM0	100 ns	HVM0	100 ns	HVM0	100 ns	HVM0	100 ns
HVP0	100 ns	HVP0	100 ns	HVP0	100 ns	HVP0	100 ns
HVM0	100 ns	HVM0	100 ns	HVM0	100 ns	HVM0	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	145 µs	RX	145 µs	RX	145 µs	RX	145 µs
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP1	100 ns	HVP1	100 ns	HVP1	100 ns	HVP1	100 ns
HVM1	100 ns	HVM1	100 ns	HVM1	100 ns	HVM1	100 ns
HVP1	100 ns	HVP1	100 ns	HVP1	100 ns	HVP1	100 ns
HVM1	100 ns	HVM1	100 ns	HVM1	100 ns	HVM1	100 ns
HVP1	100 ns	HVP1	100 ns	HVP1	100 ns	HVP1	100 ns
HVM1	100 ns	HVM1	100 ns	HVM1	100 ns	HVM1	100 ns
HVP1	100 ns	HVP1	100 ns	HVP1	100 ns	HVP1	100 ns
HVM1	100 ns	HVM1	100 ns	HVM1	100 ns	HVM1	100 ns
HVP1	100 ns	HVP1	100 ns	HVP1	100 ns	HVP1	100 ns
HVM1	100 ns	HVM1	100 ns	HVM1	100 ns	HVM1	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	145 µs	RX	145 µs	RX	145 µs	RX	145 µs
CLAMP	1 µs	CLAMP	990 ns	CLAMP	980 ns	CLAMP	970 ns

Figure 8. Acquisition by Program "1" with H-Bridge TX0, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively

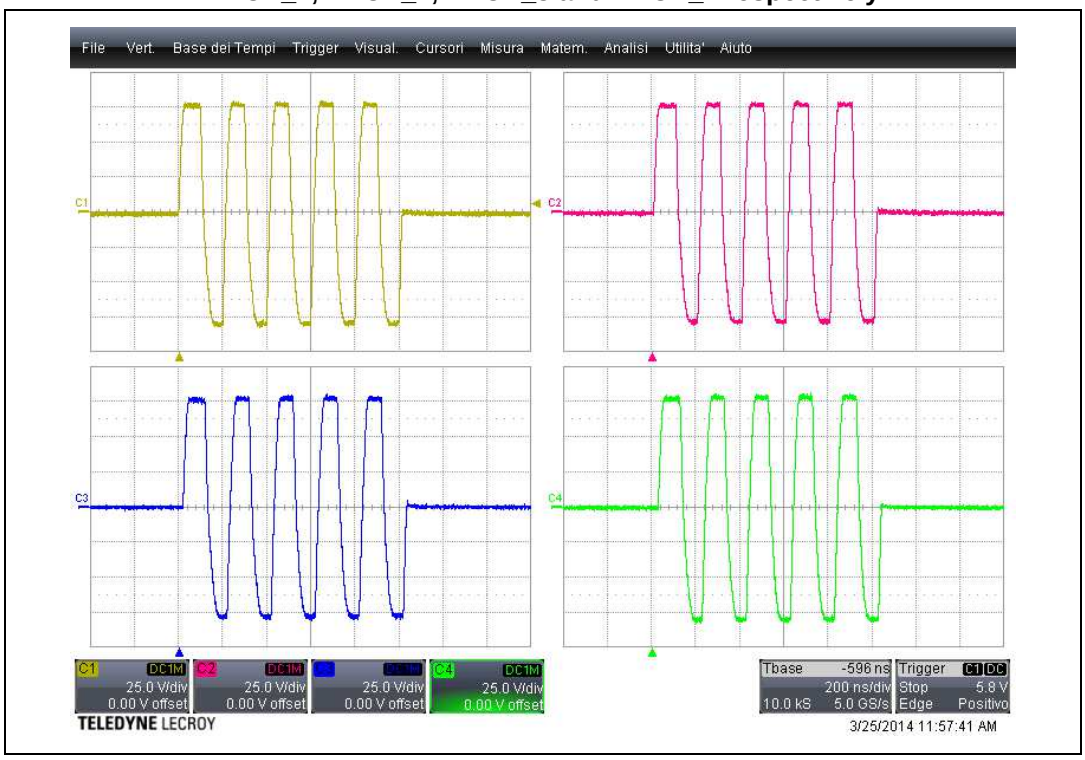
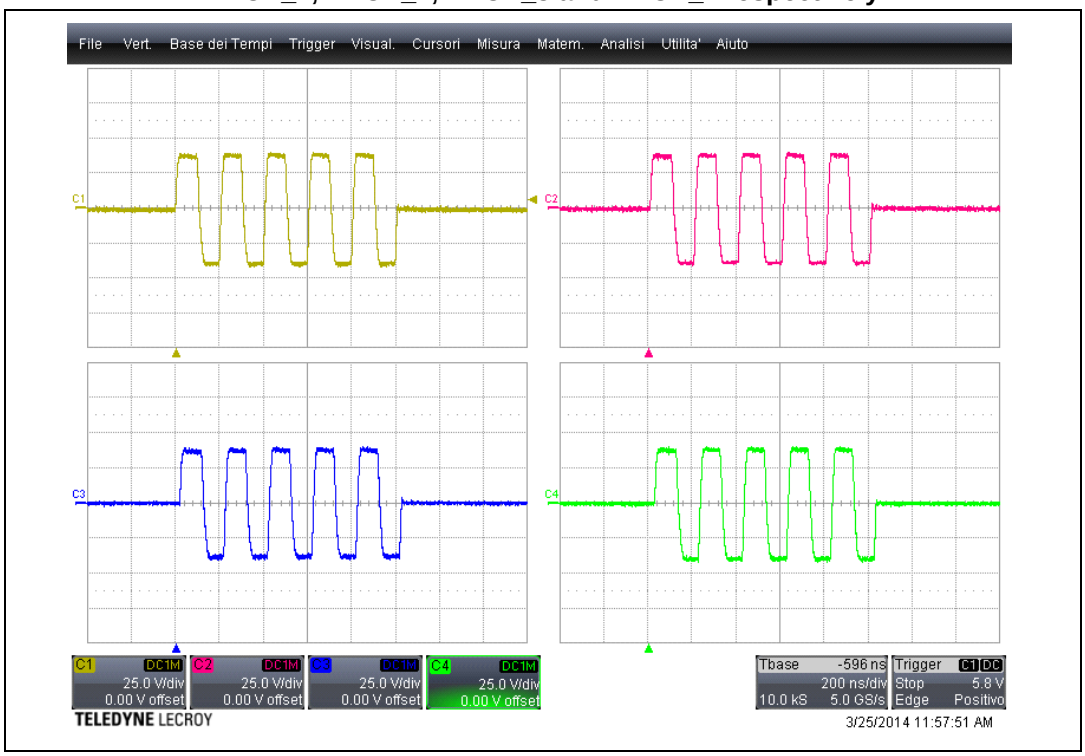


Figure 9. Acquisition by Program "1" with H-Bridge TX1, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



3.4.4 Pattern Program 2

The third pattern stored in the SPI Flash is described in *Table 12*, where the output pulses are in phase. The state sequence is given in *Table 13*.

The test conditions applied to generate the waveforms in *Figure 10* are:

- HVP_CW = + 10 V
- HVM_CW = - 10 V
- Load: 300 pF // 100 Ω

Table 12. Program 2, SEL = don't care

	mode	Frequency [MHz]	Number of pulses	Initial pulse	H-Bridge
XDCR_1	CW	5	continuous wave	positive	HV-CW (0.5 A)
XDCR_2	CW	2.5	continuous wave	positive	HV-CW (0.5 A)
XDCR_3	CW	5	continuous wave	positive	HV-CW (0.5 A)
XDCR_4	CW	2.5	continuous wave	positive	HV-CW (0.5 A)

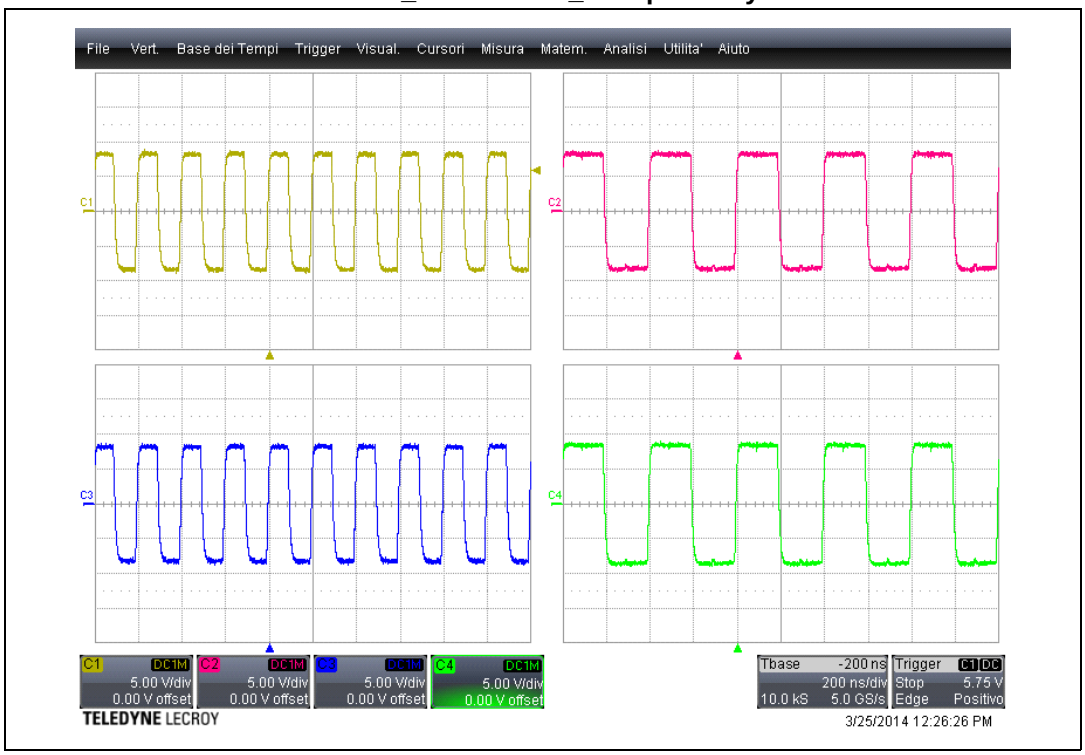
Table 13. State sequence Program 2

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	200 ns	HVP_CW	200 ns
HVM_CW	100 ns	HVM_CW	100 ns	HVM_CW	200 ns	HVM_CW	200 ns
HVP_CW	100 ns	HVP_CW	100 ns	HVP_CW	200 ns	HVP_CW	200 ns

Table 13. State sequence Program 2 (continued)

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns	HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns
HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns	HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns
HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns	HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns
HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns	HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns
HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns	HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns
HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns	HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns
HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns	HVP_CW(.5A)	100 ns	HVP_CW(.5A)	200 ns
HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns	HVM_CW(.5A)	100 ns	HVM_CW(.5A)	200 ns

Figure 10. Acquisition by Program 2, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



3.4.5 Pattern Program 3

The fourth pattern stored in the SPI Flash is described in *Table 14*, where the output pulses are delayed by 10 ns each. The state sequence is given in *Table 15*.

The test conditions applied to generate the waveforms in *Figure 11* and *Figure 12* are:

- HVP_CW = + 10 V
- HVM_CW = - 10 V
- Load: 300 pF // 100 Ω

Table 14. Program 3, SEL = don't care

	mode	Frequency [MHz]	Number of pulses	Initial pulse	H-Bridge
XDCR_1	CW	5	continuous wave	positive	HV-CW (0.25 A)
XDCR_2	CW	5	continuous wave	positive	HV-CW (0.25 A)
XDCR_3	CW	5	continuous wave	positive	HV-CW (0.25 A)
XDCR_4	CW	5	continuous wave	positive	HV-CW (0.25 A)

Table 15. State sequence Program 3

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
HVP_CW (.25 A)	20 ns	HVP_CW (.25 A)	30ns	HVP_CW (.25 A)	40 ns	HVP_CW (.25 A)	50 ns
HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	80 ns	HVP_CW (.25 A)	70ns	HVP_CW (.25 A)	60 ns	HVP_CW (.25 A)	50 ns

Figure 11. Acquisition by Program 3, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively

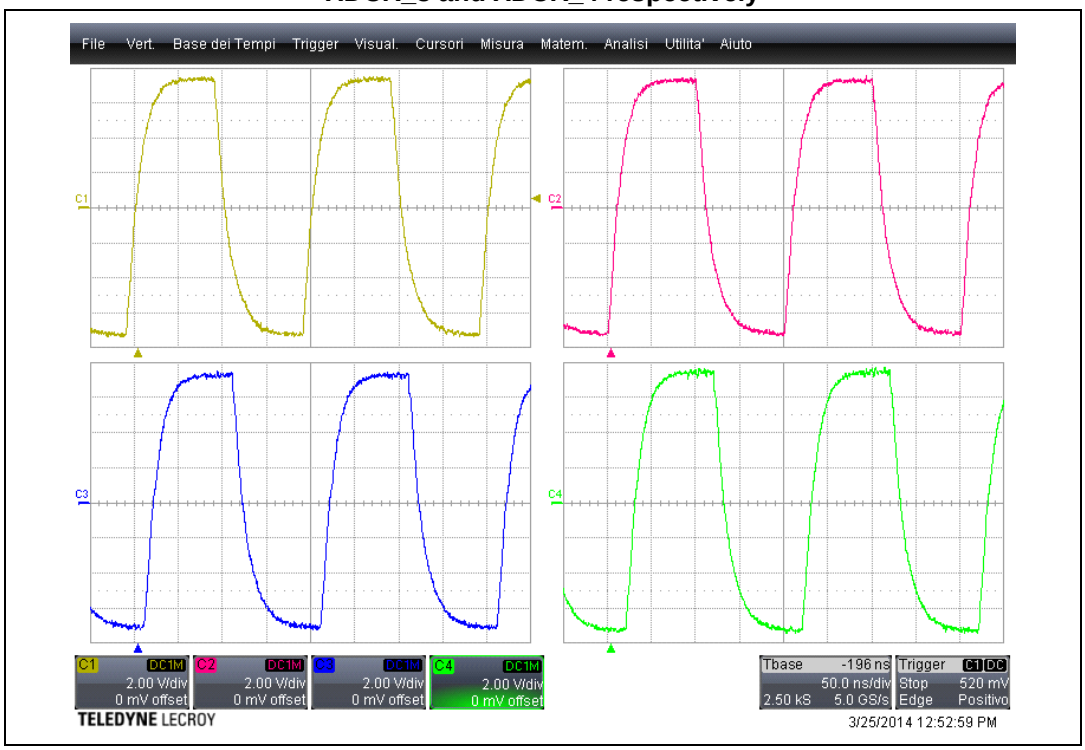
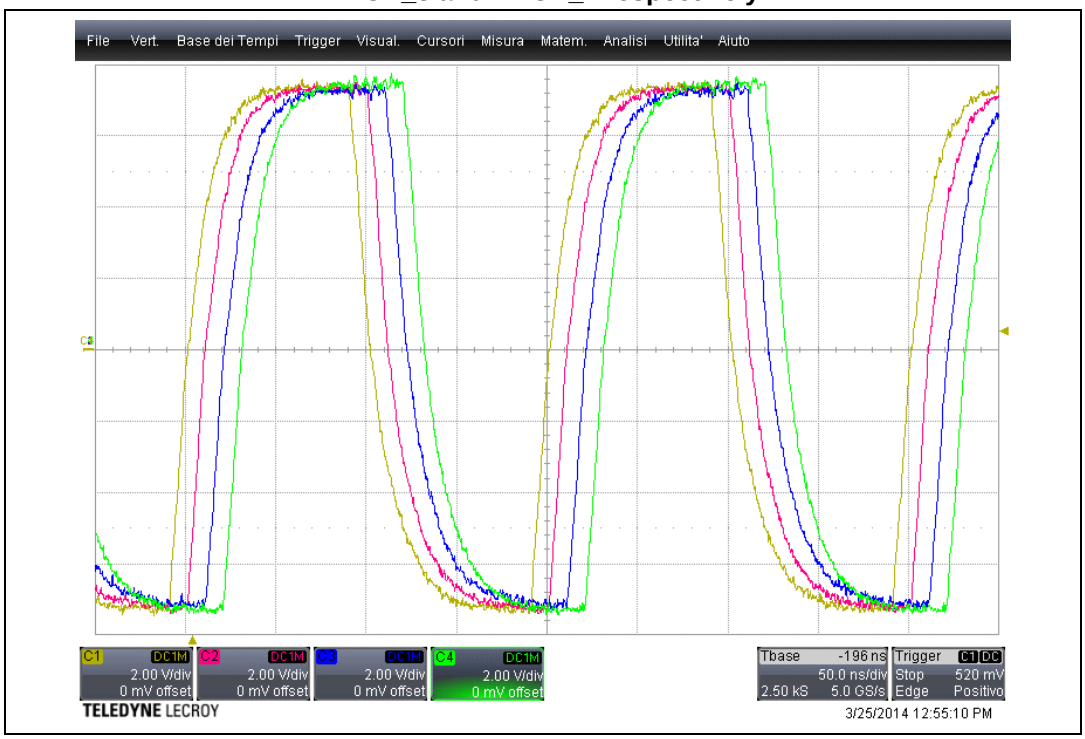


Figure 12. Acquisition by Program 3, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



3.4.6 Pattern Program 4

The fifth pattern stored in the SPI Flash is described in *Table 16*, with the output pulses in phase and SEL is 1 for the 5-level output option. The state sequence is given in *Table 17*.

The test conditions applied to generate the waveforms in *Figure 13* and *Figure 14* are:

- HVP0 = + 80 V
- HVP1 = + 40 V
- HVM0 = - 80 V
- HVM1 = - 40 V
- Load: 300 pF // 100 Ω

Table 16. Program 4, SEL=1

	mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PC	2.5	3	positive	150 µs	TX0, TX1
XDCR_2	PC	2.5	3	negative	150 µs	TX0, TX1
XDCR_3	PC	5	3	positive	150 µs	TX0, TX1
XDCR_4	PC	5	3	negative	150 µs	TX0, TX1

Table 17. State sequence Program 4

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP0	200 ns	HVM0	200 ns	HVP0	100 ns	HVM0	100 ns
HVM0	200 ns	HVP0	200 ns	HVM0	100 ns	HVP0	100 ns
HVP0	200 ns	HVM0	200 ns	HVP0	100 ns	HVM0	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	145.4 µs	RX	145.4 µs	RX	145.7 µs	RX	145.7 µs
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP1	200 ns	HVM1	200 ns	HVP1	100 ns	HVM1	100 ns
HVM1	200 ns	HVP1	200 ns	HVM1	100 ns	HVP1	100 ns
HVP1	200 ns	HVM1	200 ns	HVP1	100 ns	HVM1	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
RX	145.4 µs	RX	145.4 µs	RX	145.7 µs	RX	145.7 µs

Figure 13. Acquisition by Program 4, H-Bridge TX0, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively

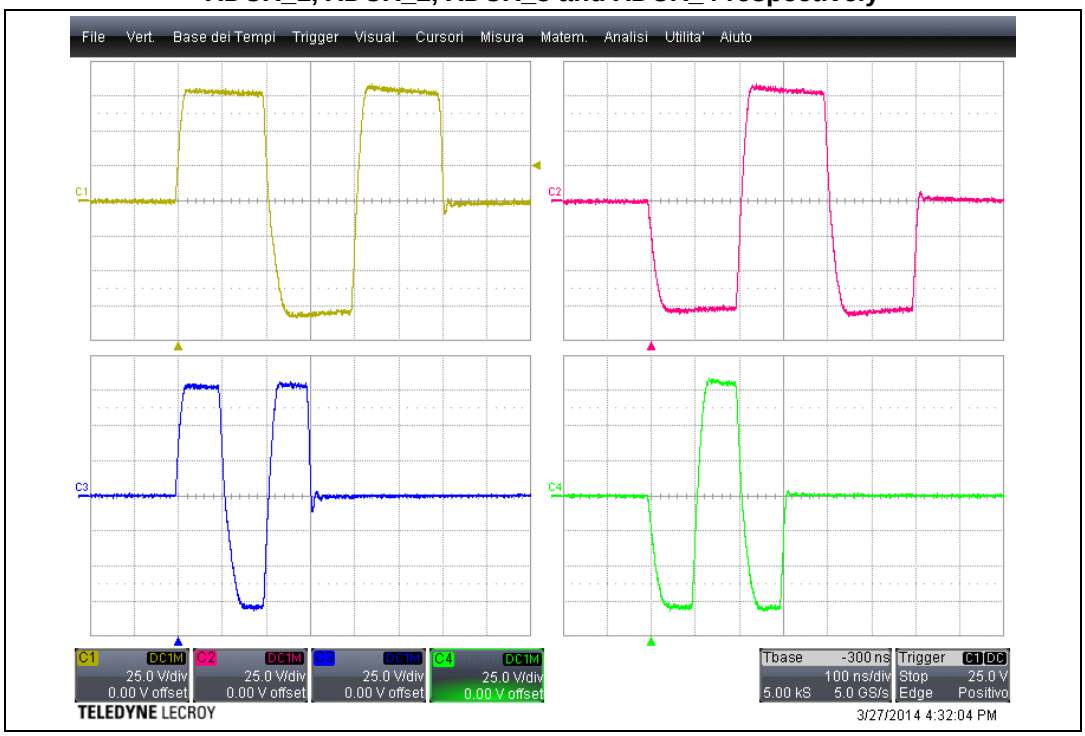
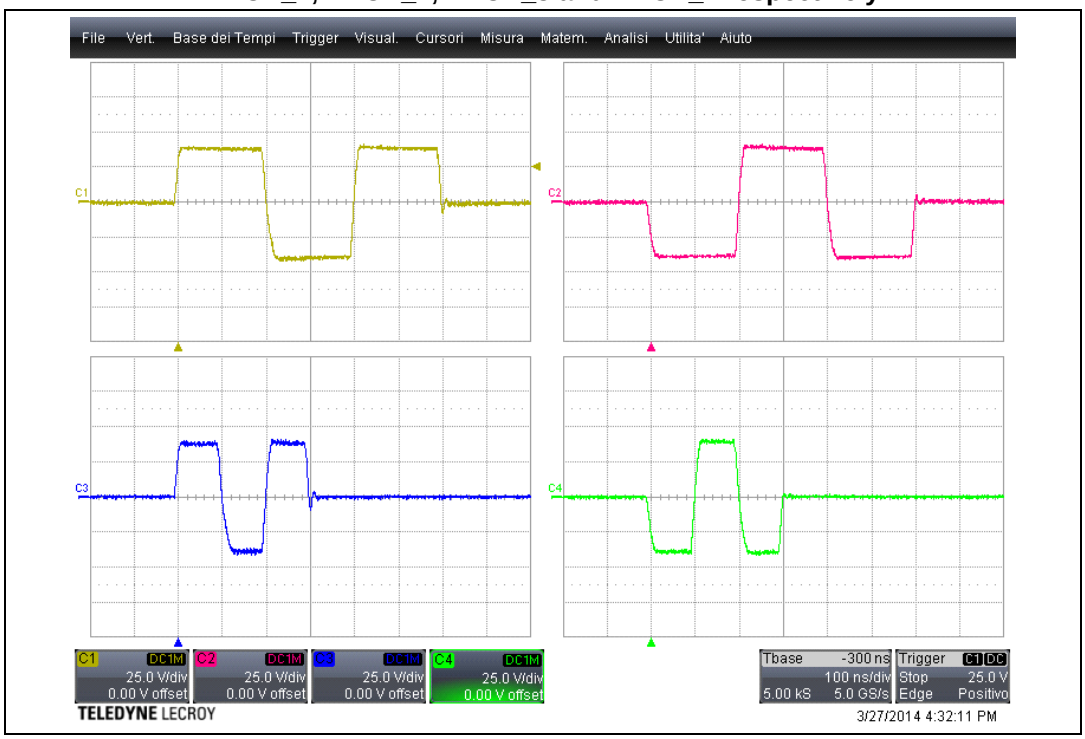


Figure 14. Acquisition by Program 4, H-Bridge TX1, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



3.4.7 Pattern Program 5

The sixth pattern stored in the SPI Flash is described in *Table 18*, where the output pulses are in phase and SEL is 1 for the 5-level output option. The state sequence is given in *Table 18*.

The test conditions applied to generate the waveforms in *Figure 15* and *Figure 16* are:

- HVP0 = + 80 V
- HVP1 = + 40 V
- HVM0 = - 80 V
- HVM1 = - 40 V
- Load: 300 pF // 100 Ω

Table 18. Program 5, SEL=1

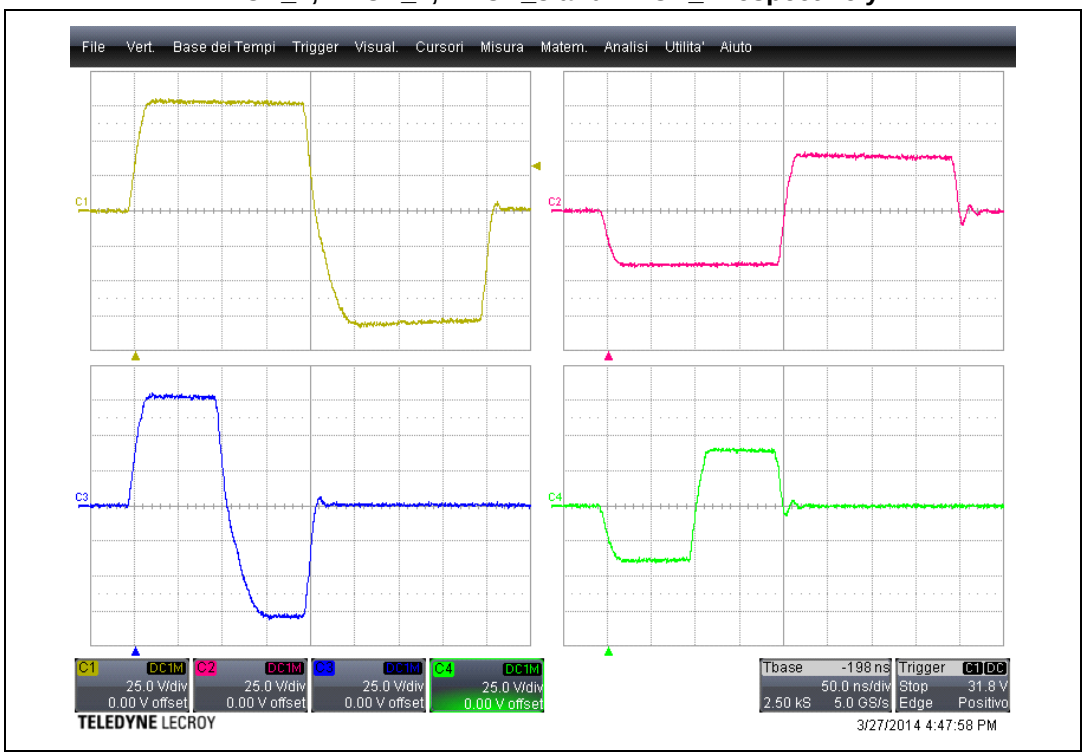
	mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PC	2.5	2	positive	300 µs	TX0
XDCR_2	PC	2.5	2	negative	300 µs	TX1
XDCR_3	PC	5	2	positive	300 µs	TX0
XDCR_4	PC	5	2	negative	300 µs	TX1

Table 19. State sequence Program 5

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP0	200 ns	HVM1	200 ns	HVP0	100 ns	HVM1	100 ns
HVM0	200 ns	HVP1	200 ns	HVM0	100 ns	HVP1	100 ns
CLAMP	6 µs	CLAMP	6 µs	CLAMP	6 µs	CLAMP	6 µs
HVM0	200 ns	HVP1	200 ns	HVM0	100 ns	HVP0	100 ns
HVP0	200 ns	HVM1	200 ns	HVP0	100 ns	HVM0	100 ns
CLAMP	291.2 µs	CLAMP	291.2 µs	CLAMP	291.6 µs	CLAMP	291.6 µs

Figure 15. Acquisition by Program 5, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively

Figure 16. Acquisition by Program 5, zoom of Figure 15, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



3.4.8 Pattern Program 6

The seventh pattern stored in the SPI Flash is described in *Table 20*, with the output pulses in phase and SEL is 0 for the 3-level output option. The state sequence is given in *Table 21*.

The test conditions applied to generate the waveforms in *Figure 17* are:

- HVP0 = HVP1 = + 80 V
- HVP_CW = + 40 V
- HVM0 = HVM1 = - 80 V
- HVM_CW = - 40 V
- Load: 300 pF // 100 Ω

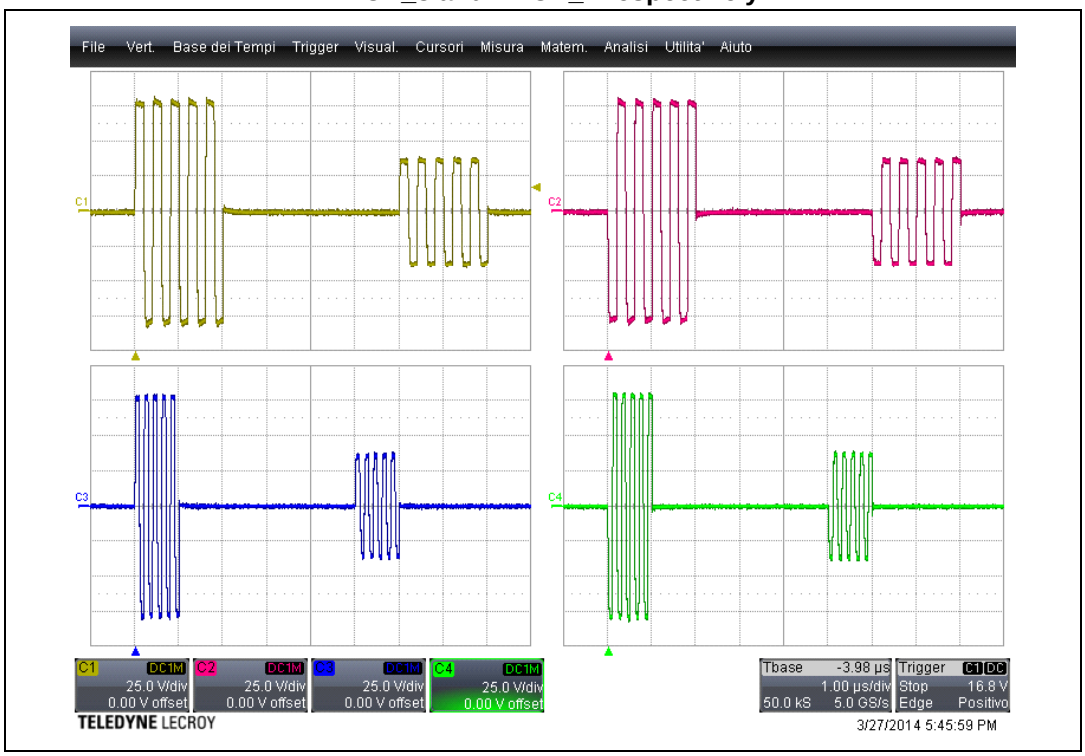
Table 20. Program 6, SEL=0

	mode	Frequency [MHz]	Number of pulses	Initial pulse	PRF	H-Bridge
XDCR_1	PW -CW	2.5	10 (PW) + 10 (CW)	positive	300 µs	TX0 & TX1, CW (0.5 A)
XDCR_2	PW -CW	2.5	10 (PW) + 10 (CW)	negative	300 µs	TX0 & TX1, CW (0.5 A)
XDCR_3	PW -CW	5	10 (PW) + 10 (CW)	positive	300 µs	TX0 & TX1, CW (0.5 A)
XDCR_4	PW -CW	5	10 (PW) + 10 (CW)	negative	300 µs	TX0 & TX1, CW (0.5 A)

Table 21. State sequence Program 6

XDCR_1		XDCR_2		XDCR_3		XDCR_4	
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVP	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVM	100 ns
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVP	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVM	100 ns
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVP	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVM	100 ns
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVP	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVM	100 ns
HVP	200 ns	HVM	200 ns	HVP	100 ns	HVP	100 ns
HVM	200 ns	HVP	200 ns	HVM	100 ns	HVM	100 ns
CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs	CLAMP	2 µs
CLAMP_CW	2 µs	CLAMP_CW	2 µs	CLAMP_CW	2 µs	CLAMP_CW	2 µs
HVP_CW (.25 A)	200 ns	HVP_CW(.25A)	200 ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	200 ns	HVM_CW(.25A)	200 ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	200 ns	HVP_CW(.25A)	200 ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	200 ns	HVM_CW(.25A)	200 ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	200 ns	HVP_CW(.25A)	200 ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	200 ns	HVM_CW(.25A)	200 ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	200 ns	HVP_CW(.25A)	200 ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	200 ns	HVM_CW(.25A)	200 ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
HVP_CW (.25 A)	200 ns	HVP_CW(.25A)	200 ns	HVP_CW (.25 A)	100 ns	HVP_CW (.25 A)	100 ns
HVM_CW (.25 A)	200 ns	HVM_CW(.25A)	200 ns	HVM_CW (.25 A)	100 ns	HVM_CW (.25 A)	100 ns
CLAMP_CW	290 µs	CLAMP_CW	290 µs	CLAMP_CW	292 µs	CLAMP_CW	292 µs

Figure 17. Acquisition by Program 6, where C1, C2, C3 and C4 are XDCR_1, XDCR_2, XDCR_3 and XDCR_4 respectively



Further customized pattern can be uploaded by user into remaining memory slots (thru .dfu file - see UM1083.pdf), where it's tailored in base of the test necessities from final application.

3.5 STHV749 stage

The STHV749 high-voltage, high-speed pulser generator features four independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive, or MEMS transducers.

The device contains a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes, and high-power P-channel and N-channel MOSFETs as output stages for each channel. There is also clamping-to-ground circuitry, anti-leakage, an anti-memory effect block, a thermal sensor, and a HV receiver switch (HVR_SW) to ensure strong decoupling during the transmission phase.

The STHV749 also includes self-biasing and thermal shutdown blocks (see block diagram in *Figure 18*). Each channel can support up to five active output levels with two main half bridges. It consists of three independently supplied output stages: two (TX0 and TX1) used for pulsed wave (PW) and one for continuous wave (CW) operations. TX0 and TX1 are able to provide up to ± 2 A peak output current each while, to reduce power dissipation and jitter in continuous wave mode, the fully optimized CW output stage delivers up to ± 0.3 A. The current capability for CW mode can also be set to 0.6 A.

The device can also be configured to operate as a 3-output-level, ± 4 A, 40 MHz pulser: this mode can be selected via a dedicated input pin (SEL). In this configuration, the TX0 and TX1 half bridges are paralleled in order to provide higher peak current and shorter pulse waveforms, thus providing a higher output frequency.

Note: For further information, please refer to the STHV749 datasheet.

The STEVAL-IME008V1 allows the user to configure special pins on the STHV749 described below:

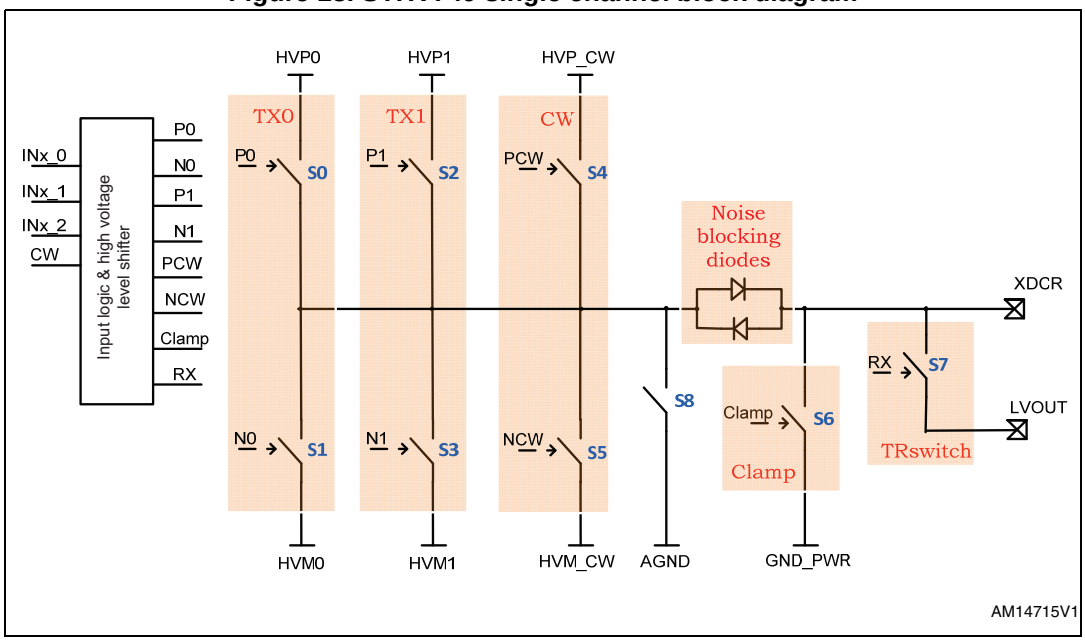
- THSD is a thermal flag. The output stage of the THSD pin is an NMOS channel open-drain, so the external pull-up resistance (R ≥ 10 kΩ) must be connected to the positive low-voltage supply (see *Figure 18*). If the internal temperature exceeds 160 °C, the THSD goes down and puts all the channels into the HZ state. Thermal protection can be disabled by externally forcing THSD to a positive low-voltage supply.
- EXPOSED-PAD is internally connected to the substrate. It can be floating or connected to a 100 V capacitance toward ground, in order to reduce noise during the receiving phase.

The fixed configuration of the THSD pin is described in *Table 22*.

Table 22. STHV749 special pin configuration

Special pins on the PCB demo		
Name	**description**	**Status on board**
THSD (pin 23)	Thermal shutdown flag pin	Active (J24 closed between 1 and 2 - forced to 3 V through R58 = 10 kΩ). the user can also give control to FPGA by shorting J24 between 2 and 3. the user can monitor the THSD status on TP3 (test point).

Figure 18. STHV749 single channel block diagram



The STHV749 output waveforms can be displayed directly for each channel Ch 1/2/3/4 using an oscilloscope by connecting the scope probe to the JCh1, JCh2, JCh3, Jch4 BNC connectors. The user can also select whether or not to connect the on-board equivalent load, a 270 pF 100 V capacitor paralleled with a 100 Ω, 2 W resistor (through J20, J21, J28, J31). A coaxial cable can also be used to easily connect the user transducer, and four low voltage outputs are available to receive the echo traduced signal arriving from the piezo-element through HVR_SW (JLch1, JLch2, JLch3, JLch4).

This PCB design features layer separation, which ensures good filtering and an effective decoupling between the low voltage inputs and the HV switching signals (XDCR, etc.), together with the capacitance values. The user can download the gerber reference file for this board from www.st.com.

3.6 Operating supply conditions

Table 23. DC working supply conditions

Operating supply voltages					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
VDDP	Positive supply voltage	2.7	3.3	3.6	V
VDDM	Negative supply voltage	-2.7	-3.3	-3.6	V
VDD	Positive logic voltage	1.6	3.3	3.6	V
HVP0	TX0 high voltage positive supply			95	V
HVP1	TX1 high voltage positive supply			95	V
HVM0	TX0 high voltage negative supply	-95			V
HVM1	TX1 high voltage negative supply	-95			V
HVP_CW	CW high voltage positive supply			95	V
HVM_CW	CW high voltage negative supply	-95			V

Note: HVM0 / HVM1 /HVM_CW and HVP0 / HVP1 /HVP_CW are fully independent on the board.

Table 24. Current consumption in CW mode, @ 5 MHz, HV_CW = ± 5 V, no-load

Current consumption			
Symbol	**Parameter**	**Value**	**Unit**
IVDDP	Positive supply current	2	mA
IVDDM	Negative supply current	7	mA
HVP_CW	CW high voltage positive supply current	15	mA
HVM_CW	CW high voltage negative supply current	12	mA

4 Connectors

4.1 Power supply

The STEVAL-IME008V1 board must be powered by the J4, J1, J2 and J3 connectors shown in the following figures.

Figure 19. Power supply connector J4

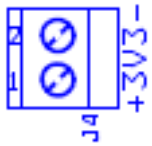


Figure 20. Power supply connector J1

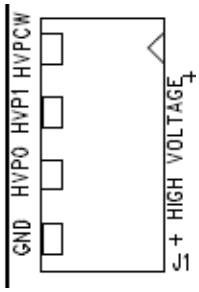


Figure 21. Power supply connector J2

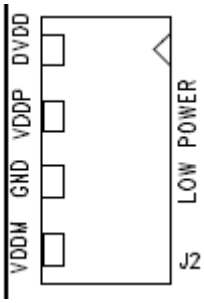
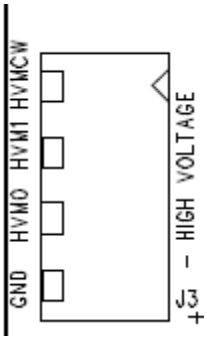


Figure 22. Power supply connector J3



4.2 Power-up sequence

The device is fully power-up/power-down free, meaning that there is no recommended sequence to follow in order to power up/down the STHV749.

4.3 MCU

Figure 23. USB mini-B connector (CN1)

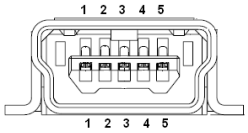


Table 25. USB mini B connector pin out

Pin number	Description
1	Vbus (power)
2	DM (STM32 PA11)
3	DP (STM32 PA12)
4	N.C.
5	Ground

Figure 24. SWD (J40)

Table 26. JTAG/SWD connector pin out

Pin number	Description
1	MCU_3V3
2	JTMS
3	GND
4	JTCK
5	GND
6	JTDO
7	GND
8	JTDI
9	GND
10	RESET#

4.4 SPI Flash memory

Figure 25. Memory expansion connector (J10)

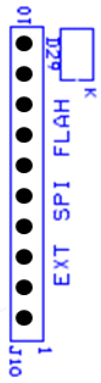


Table 27. Memory expansion connector pin out

Pin number	Description
1	MCU_FPGA_PROG (not used)
2	SPI MISO3
3	SPI MISO2
4	SPI CS
5	SPI MOSI
6	SPI MISO
7	SPI CLK
8	GND
9	3.3 V
10	CHECK

Note: This memory is mutually exclusive with the on-board Flash memory, remove J38 before connecting the expansion memory via J10; the relative LED (D29) turns on.

4.5 FPGA

FPGA USER I/O connector (J7) connector is used for debugging purpose; it allows users to directly interface with FPGA I/Os.

Table 28. FPGA USER I/O connector pin out

Pin number	Description	Pin number	Description	Direction
1	GND	2	CW	OUTPUT
3	GND	4	TRIGGER_OUT	OUTPUT
5	GND	6	CLKOUT	OUTPUT
7	GND	8	CYCLE_END	OUTPUT
9	GND	10	THSD_EN	OUTPUT
11	GND	12	ERROR	OUTPUT
13	GND	14	PROG<0>	IN/OUT
15	GND	16	PROG<1>	IN/OUT
17	GND	18	PROG<2>	IN/OUT
19	GND	20	PROG<3>	IN/OUT
21	GND	22	IDLE_SEL<0>	IN/OUT
23	GND	24	IDLE_SEL<1>	IN/OUT
25	GND	26	REMOTE_ENABLE	INPUT
27	GND	28	REMOTE_START	INPUT
29	GND	30	REMOTE_STOP	INPUT
31	GND	32	REMOTE_RESET	INPUT

Table 29. FPGA PMOD connectors (J8) not mounted on the board

Pin number	Description	Pin number	Description
1	Not used	2	Not used
3	Not used	4	Not used
5	GND	6	3.3 V
7	Not used	8	Not used
9	Not used	10	Not used
11	GND	12	3.3 V

Table 30. FPGA PMOD connectors (J9) not mounted on the board

Pin number	Description	Pin number	Description
1	Not used	2	Not used
3	Not used	4	Not used
5	GND	6	3.3 V
7	Not used	8	Not used
9	Not used	10	Not used
11	GND	12	3.3 V

Two right-angle, 12-pin (2 x 6 female) Peripheral Module (PMOD) headers (J8, J9) are interfaced to the FPGA, with each header providing 3.3 V power, ground and eight I/O's. These headers may be used as general-purpose I/Os or to interface with the PMODs in order to enable additional user customizations. J8 and J9 are placed in close proximity (0'9" - centers) on the PCB in order to support dual PMODs.

Table 31. FPGA JTAG connectors (J11) not mounted on the board

Pin number	Description	Pin number	Description
1	GND	2	3.3 V
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	Not used
13	GND	14	Not used

The STEVAL-IME008V1 evaluation board supports the serial peripheral interface (SPI Flash) method for configuring the FPGA. The default configuration mode (determined by pullup/pulldown resistors R17, R18, R21, and R22) is "Master Serial / SPI" mode, which allows the FPGA to be configured by the SPI Flash device. Spartan-6 devices have a dedicated four-wire JTAG port (always available to the FPGA regardless of the mode pin settings), allowing the Boundary-scan configuration method.

Configuring the FPGA via Boundary-scan requires a JTAG download cable to be attached to the 14-pin 2 mm spaced keyed header J11 (to be mounted) with a ribbon cable. Resistors RN1, R41 to R44 and diode D22 must also be mounted.

Jumper J13 is used to prevent FPGA programming from the configuration source. It must be open (default) to enable FPGA programming. The DONE LED (D23) on the board lights when the FPGA has successfully been configured.

5 Schematic diagrams

Figure 26. STEVAL_IME008V1- Part 1

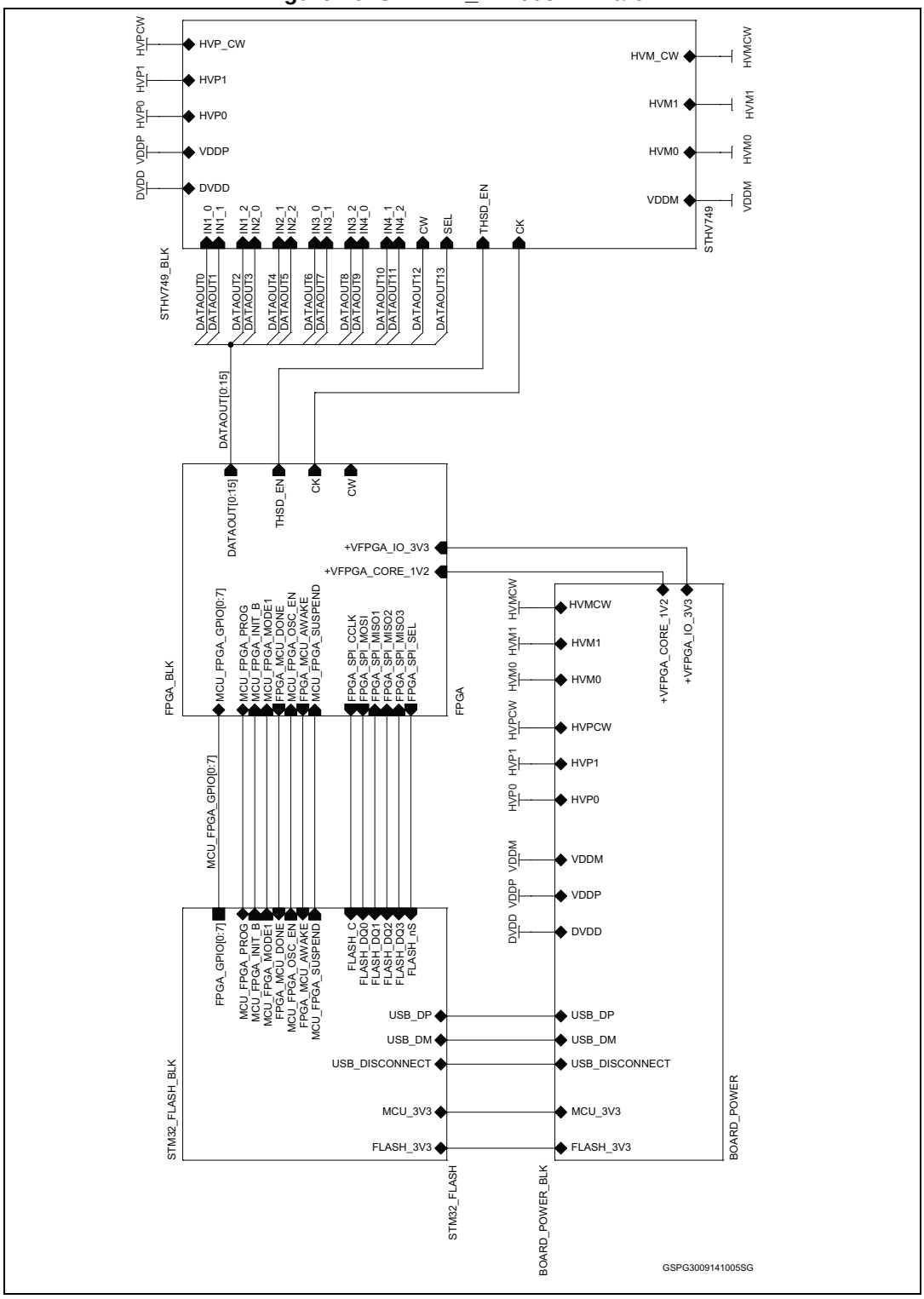


Figure 27. STEVAL_IME008V1- Part 2

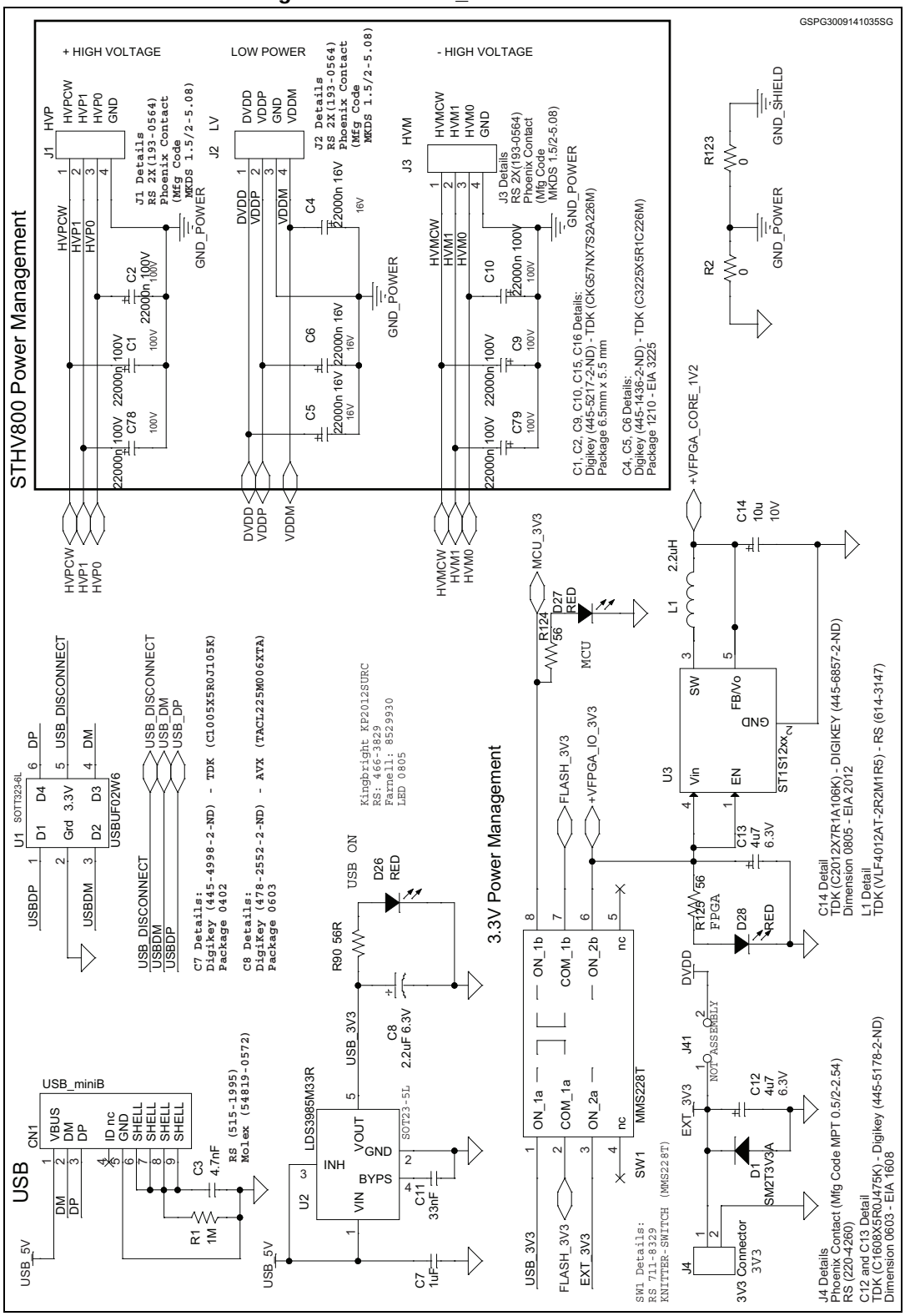


Figure 28. STEVAL_IME008V1- Part 3

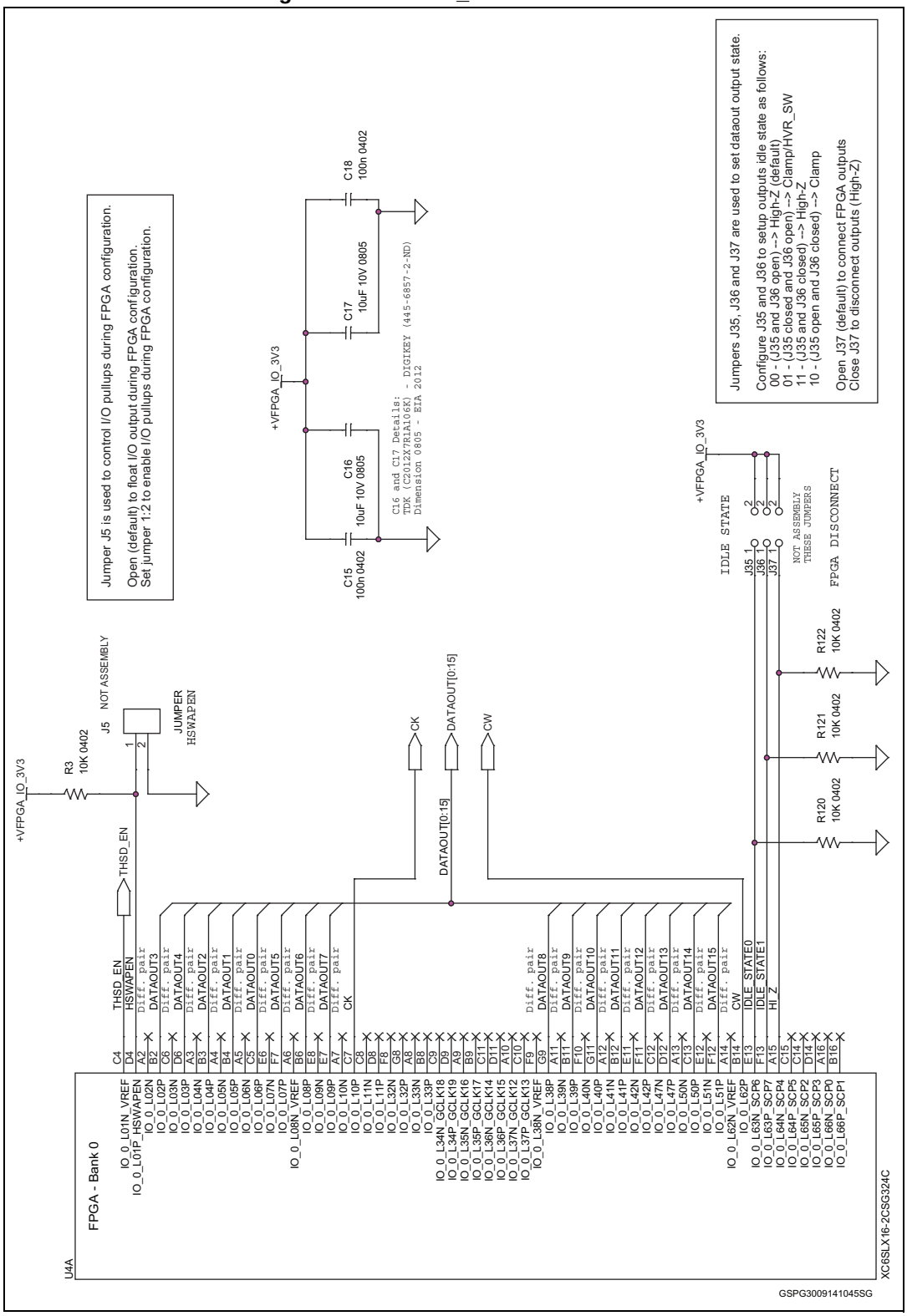


Figure 29. STEVAL_IME008V1- Part 4

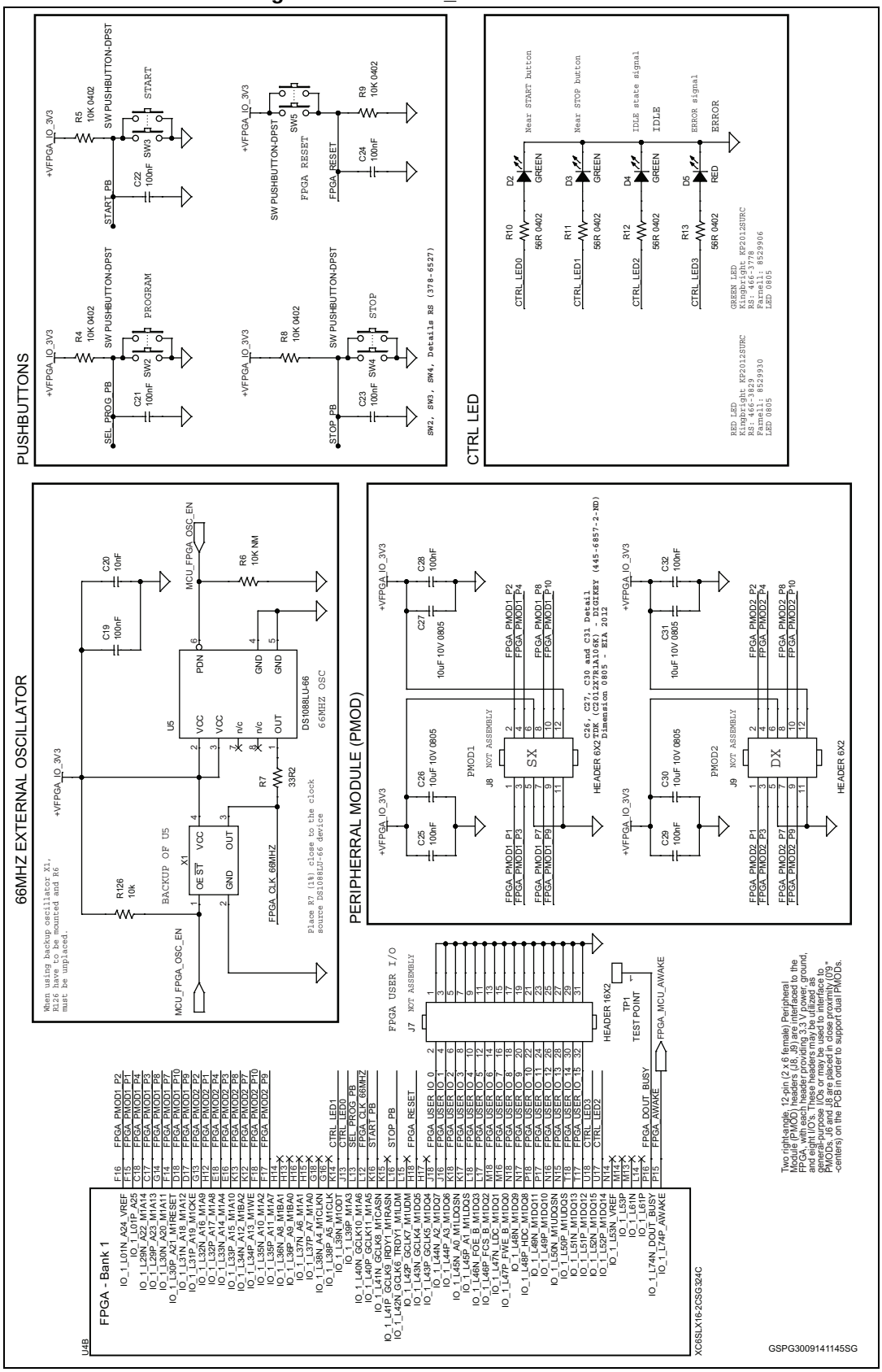


Figure 30. STEVAL_IME008V1- Part 5

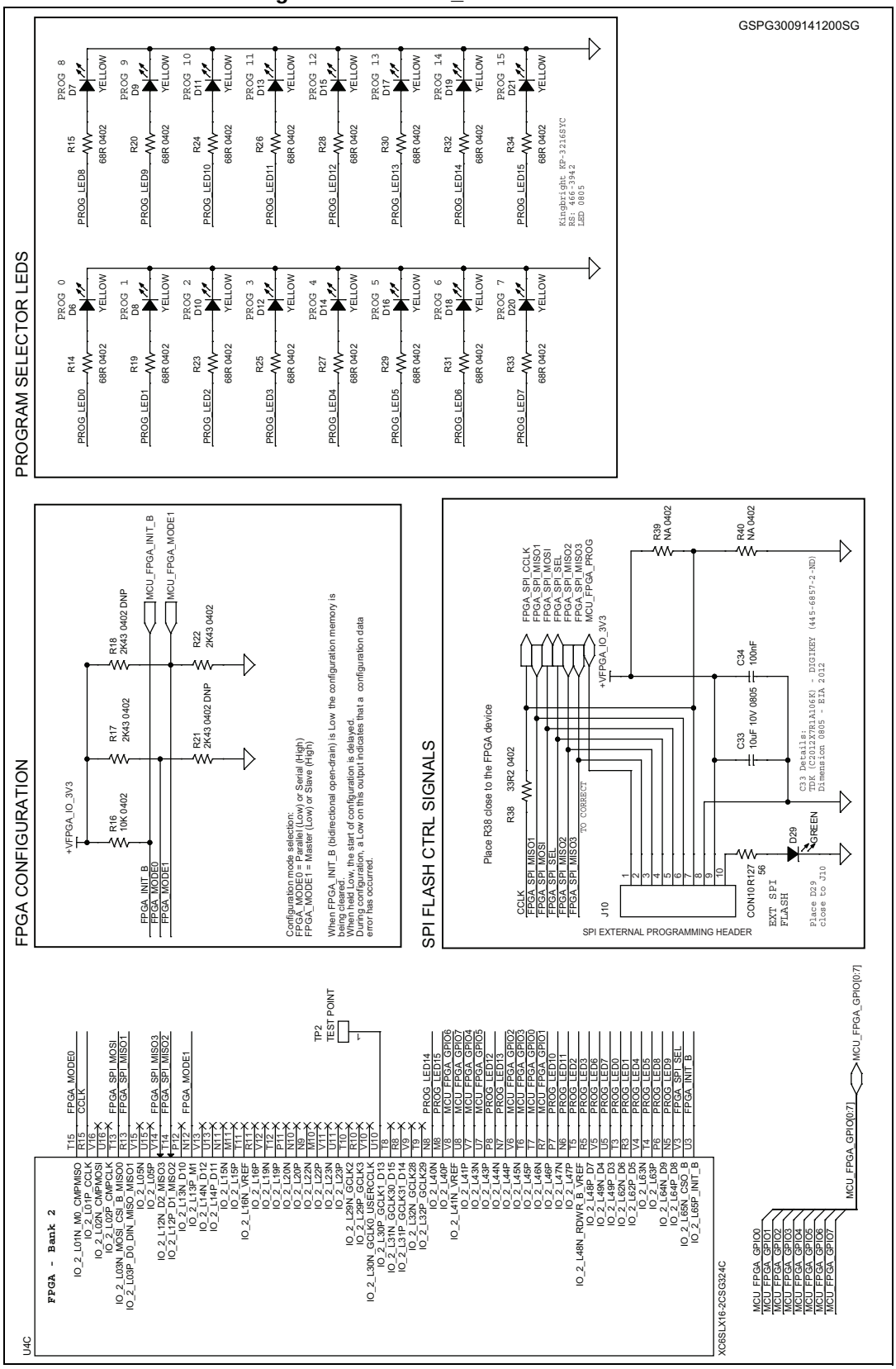


Figure 31. STEVAL_IME008V1- Part 6

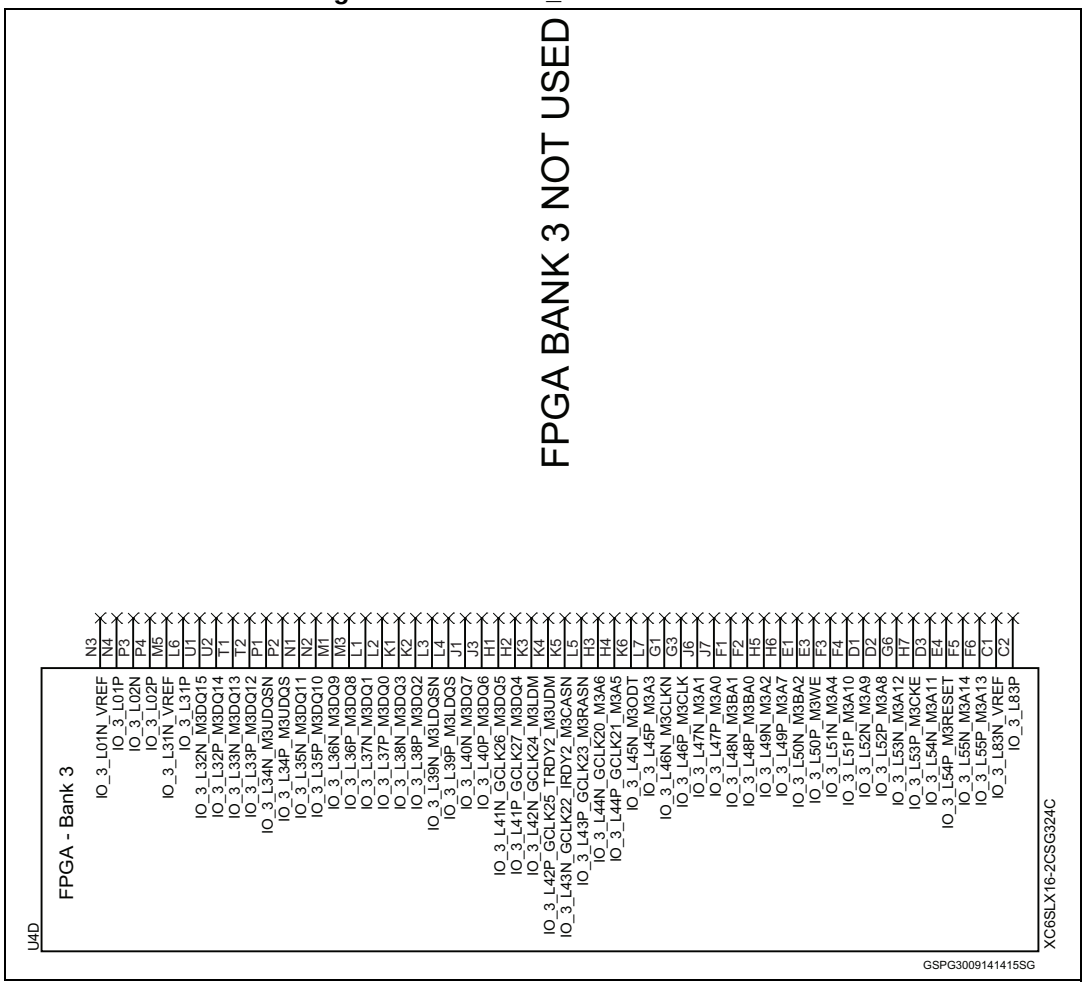


Figure 32. STEVAL_IME008V1- Part 7

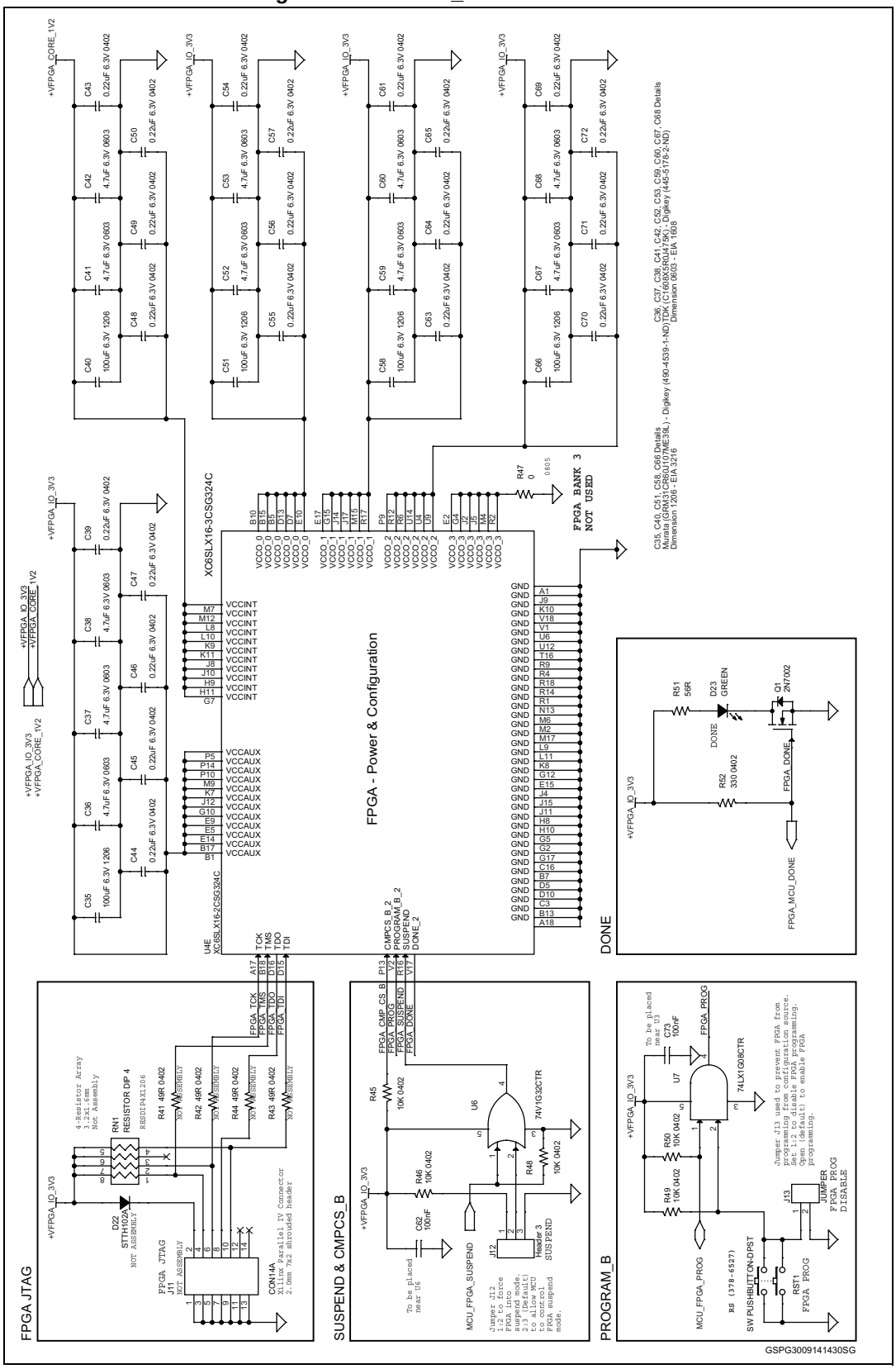


Figure 33. STEVAL_IME008V1- Part 8

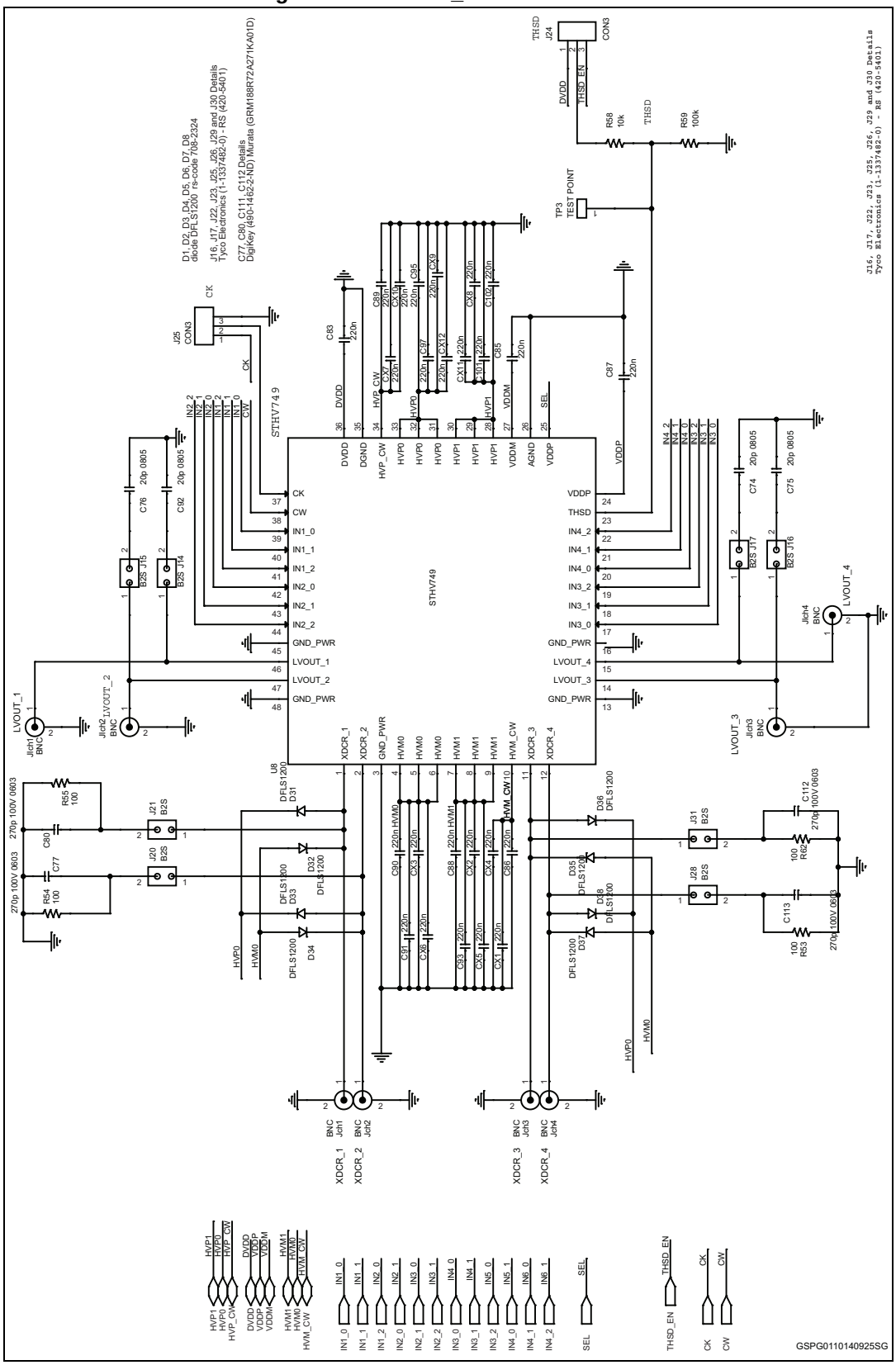
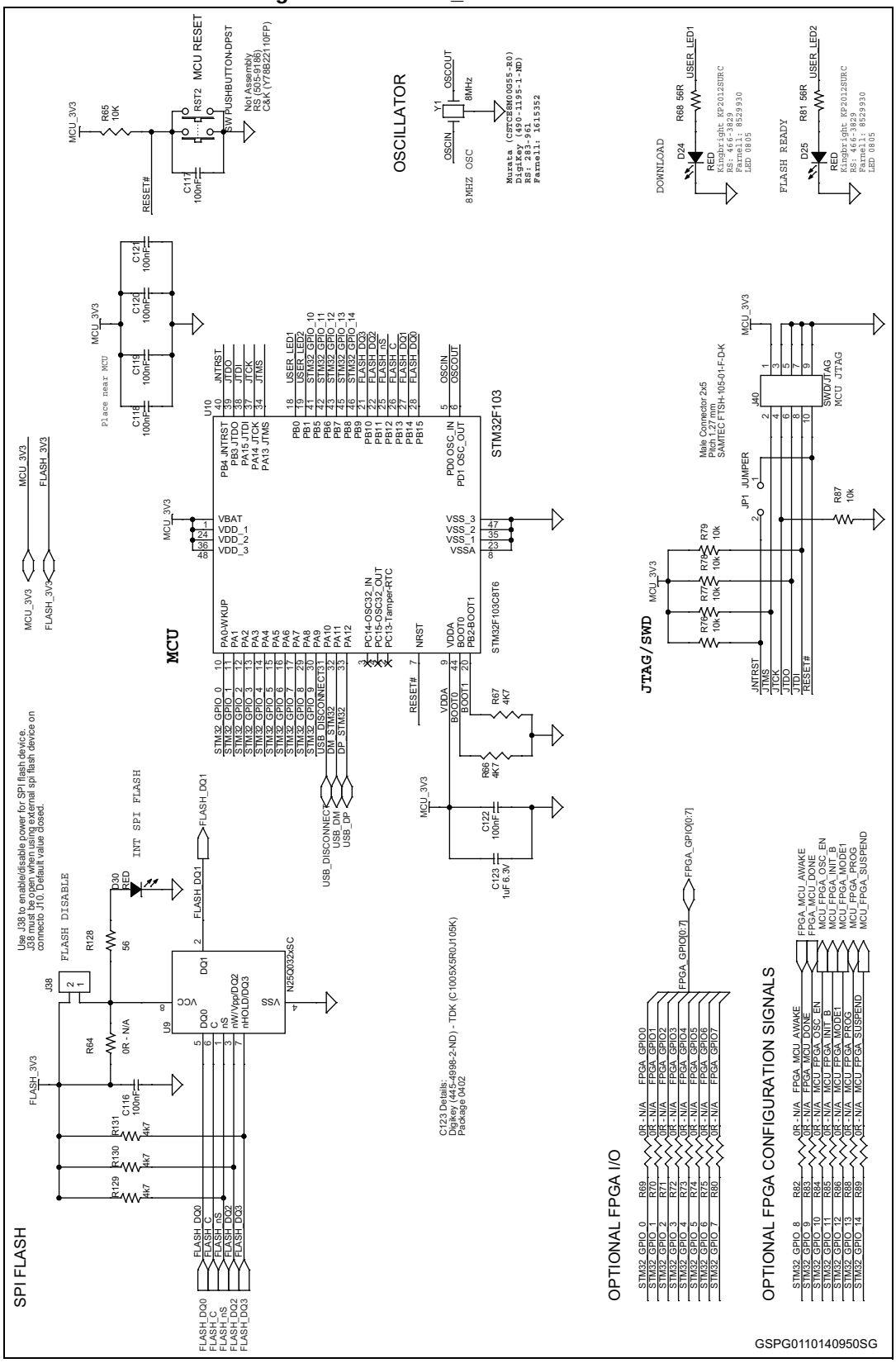


Figure 34. STEVAL_IME008V1- Part 9



6 Revision history

Table 32. Document revision history

Date	Revision	Changes
10-Dec-2014	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved