AN4439
Application note

L99ASC03G current sense amplifier offset adjust

Introduction

The L99ASC03G is a 3 phase BLDC motor controller. This device drives 6 MOSFETs for standard trapezoidal driven BLDC motors using back EMF for rotor position detection. This device has a current sense amplifier that provides an output of 1/2 Vcc (2.5 V) when there is no current sensed. This was done to provide bi-directional current detection. Some applications only need unidirectional current sensing. When this is the case, reducing or eliminating this offset would be advantageous to allow full use of the available microcontroller ADC range.

This application note provides the detailed calculations to provide the proper external resistor selection and tolerances required for optimal current sensing accuracy.

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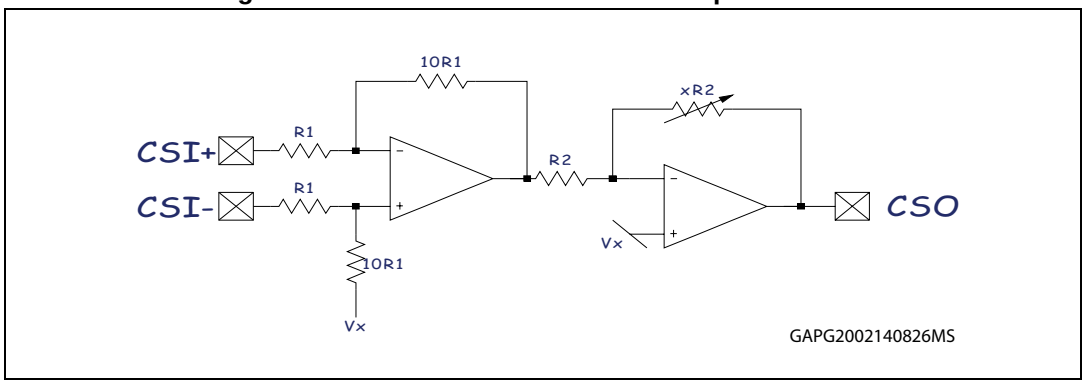
1 The L99ASC03G current sense amplifier circuit

The L99ASC03G current sense amplifier consists of two stages. The first stage is a fixed gain of 10 inverting amplifier. The second stage is a programmable gain inverting amplifier. The second stage programmable voltage gain (A_{V2}) can be programmed for a gain of 2, 3, 7, or 10. This translates to system gain settings of 20, 30, 70 and 100 when considering both op-amps.

Figure 1. L99ASC03G current sense amplifier circuit

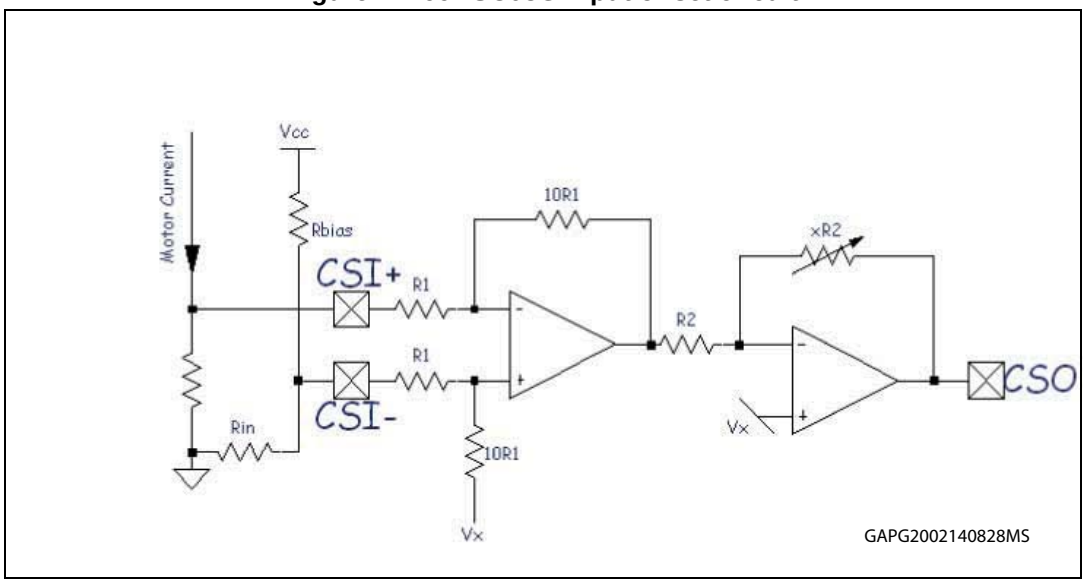


Where:

- R_1=R_2=10 kΩ +45 % / -15 % (semiconductor resistor vary a lot and they vary together. As a result ratios stay fairly tight)
- V_X = 2.5 V +/-2 %

With both the CSI+ and CSI- pins available we can add a few resistors to the CSI- pin to generate an appropriate offset to bring the CSO @ 0 A to close to 0 V.

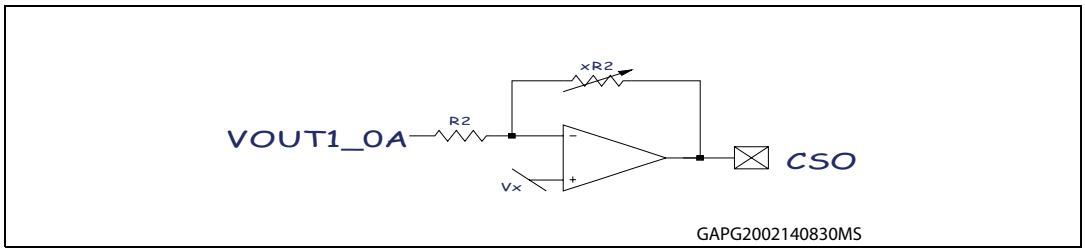
Figure 2. L99ASC03G input offset circuit



2 Calculating the input resistor values

We first calculate the voltages needed at the output of the first stage (V_{OUT1_0A}) at the four different second stage gain settings.

Figure 3. Second stage Op-Amp



A simple KCL equation:

Equation 1

$$\frac{V_{OUT1\_0V} - V_X}{R_2} = \frac{V_X}{xR_2}$$

where xR_2 can be defined by the programmed gain as:

Equation 2

$$xR_2 = A_{V2} \cdot R_2$$

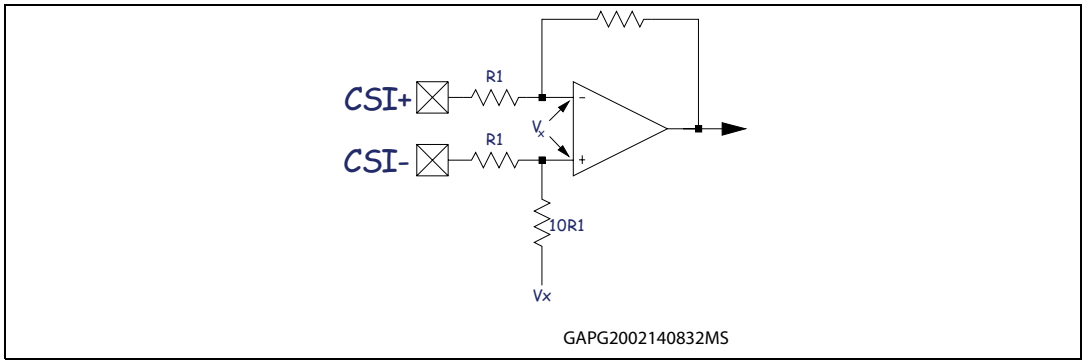
Solving for V_{OUT1_0V} provides:

Equation 3

$$V_{OUT1\_0V} = \frac{R_2 \cdot V_X + V_X \cdot xR_2}{xR_2}$$

Looking at the CSI+ input we determine what the voltage (V_x, *lower case x*) at the Op-Amp pins must be to generate V_{OUT1_0V}. We set CSI+ to 0V to simplify the equation.

Figure 4. First stage Op-Amp



Equation 4

$$\frac{V_X}{R_1} = \frac{V_{OUT1\_0V} - V_X}{10R_1}$$

Solve this for V_X to obtain:

Equation 5

$$V_X = \frac{V_{OUT1\_0V}}{11}$$

Using Kirchoff's current law (KCL) on the negative input (CSI- or in this equation CSN) we have the following two equations:

Equation 6

$$\frac{V_{CC} - V_{CSN}}{R_{Bias}} - \frac{V_{CSN}}{R_{IN}} - \frac{V_{CSN} - V_X}{11 \cdot R_1}$$

Equation 7

$$\frac{V_{CSN} - V_x}{R_1} - \frac{V_x - V_X}{10 \cdot R_1}$$

Then solving *Equation 6* and *Equation 7* for CSN and putting them together obtains:

Equation 8

$$\frac{11 \cdot V_x}{10} - \frac{V_X}{10} = \frac{11 \cdot R_1 \cdot R_{IN} \cdot V_{CC} + R_{IN} \cdot R_{Bias} \cdot V_X}{11 \cdot R_1 \cdot R_{IN} + 11 \cdot R_{IN} \cdot R_{Bias} + R_{IN} \cdot R_{Bias}}$$

Solving for R_{IN}, while including *Equation 2*, *Equation 3* and *Equation 5* and simplifying we obtain:

Equation 9

$$R_{IN} = \frac{11 \cdot R_1 \cdot R_{Bias} \cdot V_X}{11 \cdot R_1 \cdot V_X + R_{Bias} \cdot V_X - (110 \cdot A_{V2} \cdot R_1 \cdot V_{CC}) - (10 \cdot A_{V2} \cdot R_{Bias} \cdot V_}$$

We can now determine a value for R_{IN} for a given R_{Bias} and gain setting.

For R_{Bias}=10 kΩ 1% and rounding to the nearest 1 % resistor value we have:

Table 1. Rin values

Gain	R_{IN} (1%)
20	249Ω
30	162Ω
70	68.1Ω
100	47.5Ω

2.1 Calculating the transfer function from input to CSO

First we rewrite *Equation 4* to include CSI+ (CSP) as a non-zero number:

Equation 10

$$\frac{V_{CSP} - V_x}{R_1} = \frac{V_x - V_{OUT1}}{10 \cdot R_1}$$

We define V_x in terms of R_{IN}, and R_{Bias}:

Equation 11

$$V_x = \frac{V_X}{11} + \frac{10 \cdot \left(\frac{11 \cdot R_1 \cdot R_{IN} \cdot V_{CC} + R_{IN} \cdot R_{Bias} \cdot V_X}{11 \cdot R_1 \cdot R_{IN} + 11 \cdot R_1 \cdot R_{Bias} + R_{IN} \cdot R_{Bias}} \right)}{11}$$

Defining V_{OUT1} in terms of V_{CSO}:

Equation 12

$$V_{OUT1} = \frac{V_X - V_{CSO} + A_{V2} \cdot V_X}{A_{V2}}$$

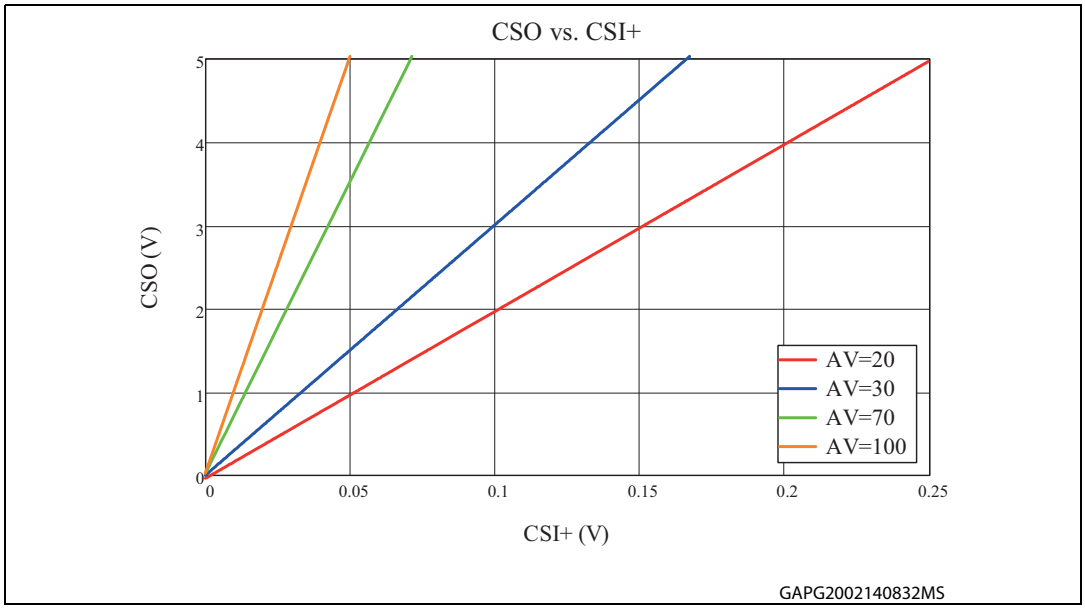
Insert *Equation 11* and *Equation 12* into *Equation 10* and solve for V_{CSO} to obtain:

Equation 13

$$V_{CSO} = A_V \cdot V_{CSP} - \frac{A_V \cdot \left(11 \cdot R_1 \cdot R_{IN} \cdot V_{CC} + R_{IN} \cdot R_{Bias} \cdot V_X\right)}{11 \cdot R_1 \cdot R_{IN} + 11 \cdot R_1 \cdot R_{Bias} + R_{IN} \cdot R_{Bias}} + V_X$$

Where A_V is now the programmable gain value of: 20, 30, 70, and 100.

Figure 5. CSO typical transfer functions at the 4 different gain settings



Tolerance calculations induced by adding external resistors.

The L99ASC03G internal resistors have a large tolerance associated with them. The advantage is that they will track with a very high degree of accuracy. As a result resistor value ratios are maintained regardless of their absolute value variations. This is an advantage as long as external resistors are not involved in the equation. Unfortunately to add offset to our system we added two external resistors.

Some advantages are that these resistors are added to the ground side of the op-amp system. This means that the effect is simply a DC offset. Variations in the internal resistors with respect to the external resistors will then only affect a simple DC offset and not adversely affect gain. As a result, the DC offset can be calibrated any time there is no current in the ground leg of the inverter (i.e. whenever the motor is not being driven or during freewheeling).

Using 1% resistors in *Equation 13* above and inserting the worst case min and max values for the internal resistors the variation is calculated.

Worst case high:

- R_{IN} = min value
- R_{Bias} = max value
- R_1 = min value

Worst case low:

- R_{IN} = min value
- R_{Bias} = max value
- R_1 = min value

The worst case is where the external resistor, R_{IN} is the largest. That is at the lowest gain. As the gain increases the RIN value drops. This reduces the offset error due to resistor tolerances.

Figure 6. Transfer function tolerance at a gain of 20

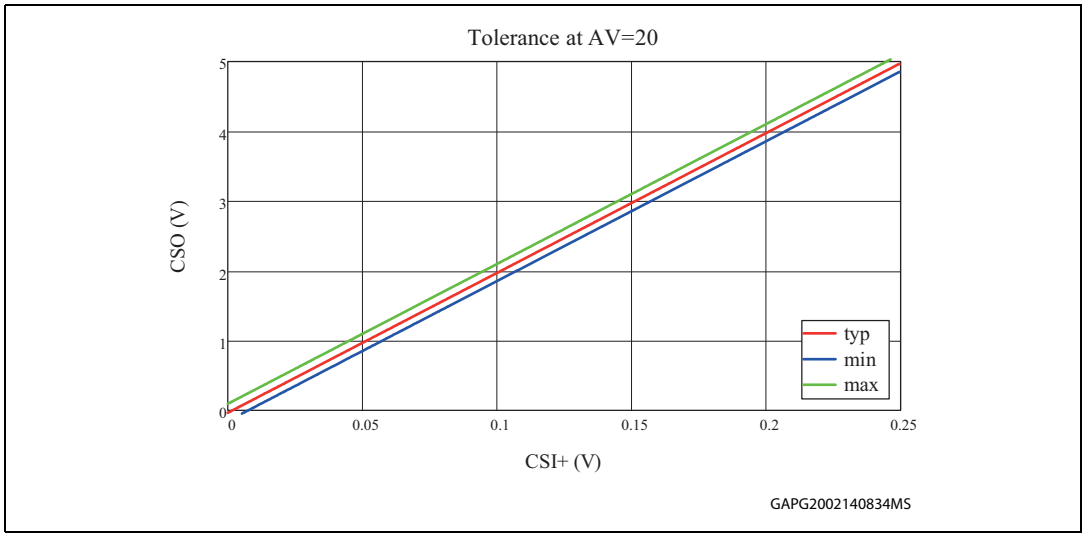
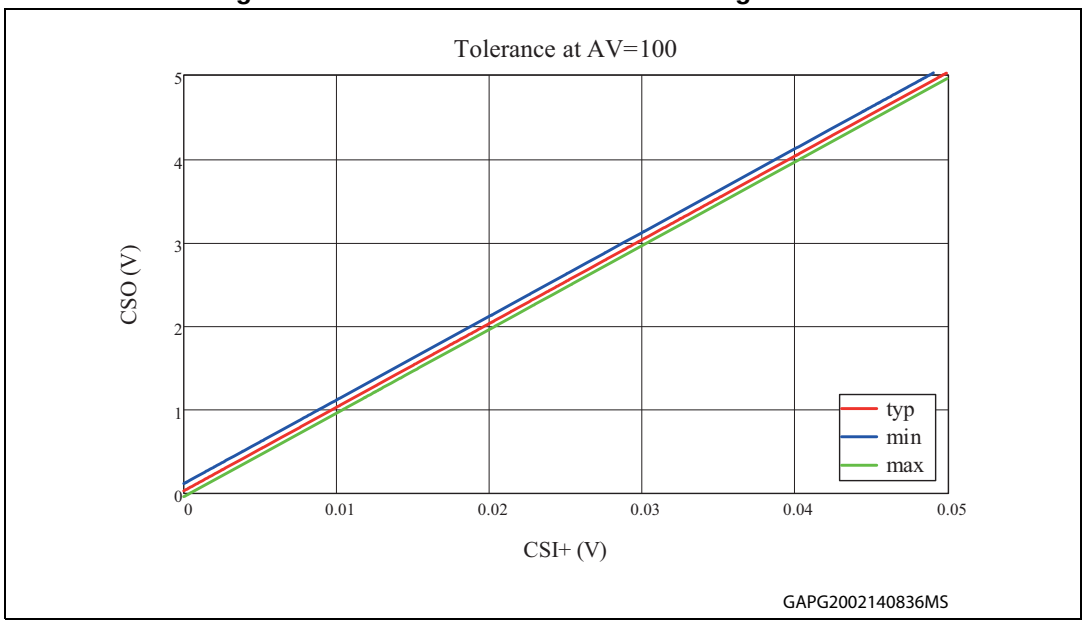
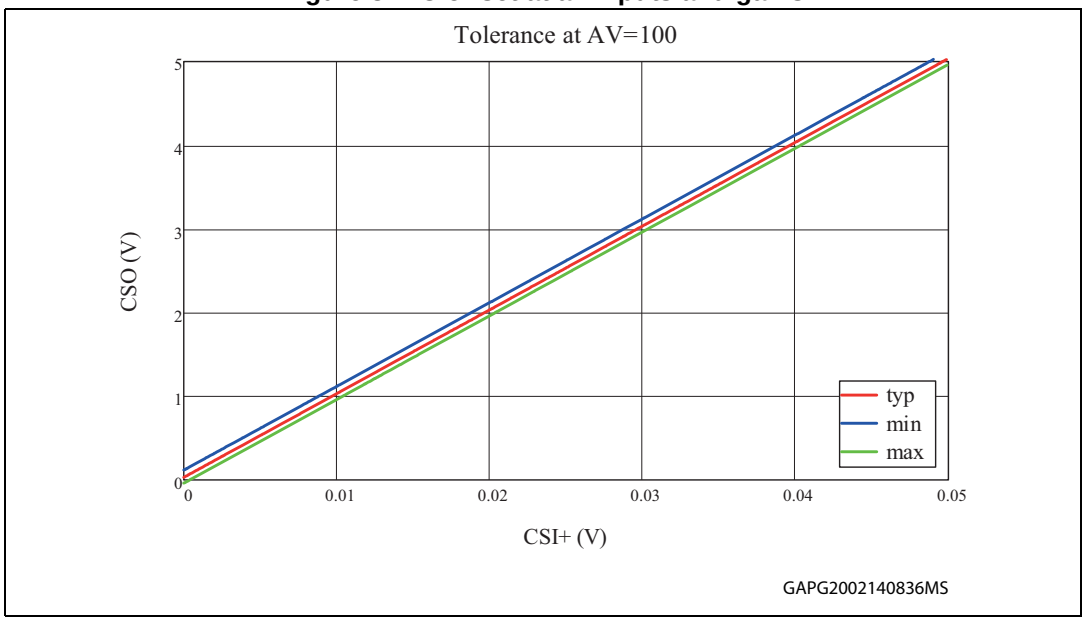


Figure 7. Transfer function tolerance at a gain of 100



When looking at the errors on the same graph (*Figure 8*) we find that the input resistor value when kept low (<300 Ω) has little effect on the tolerance.

Figure 8. DC offset at all inputs and gains



3 Generating a small offset to overcome input resistor tolerance and CSO lower limits

The output of the current sense amplifier (CSO pin) has a minimum specified voltage of 0.2 V. This means that there will have to be some current in the sense resistor to start moving the CSO voltage up. Generating an offset is needed to bring that current lower. This translates to reducing the R_{IN} resistor value or increasing the R_{Bias} value. To know how much that will need to be we look at the transfer equation and set the input voltage (V_{CSI+}) to 0 V and the output voltage (V_{CSO}) to 0.2 V and solve for R_{IN}.

Solving this for R_{IN} provides:

Equation 14

$$V_X + (V_X \cdot A_V) - \left(\left(V_X + 10 \cdot \frac{11 \cdot R_1 \cdot R_{IN} \cdot V_{CC} + R_{IN} \cdot R_{Bias} \cdot V_X}{11 \cdot R_1 \cdot R_{IN} + 11 \cdot R_{IN} \cdot R_{Bias} + R_{IN} \cdot R_{Bias}}\right) \cdot A_V\right) = 0.2V$$

Equation 15

$$R_{IN} = -\frac{1.0 \cdot \left(11.0 \cdot R_1 \cdot R_{Bias} \cdot V - 55.0 \cdot R_1 \cdot R_{Bias} \cdot V_X\right)}{11.0 \cdot R_1 \cdot V + R_{Bias} \cdot V - 55.0 \cdot R_1 \cdot V_X - 5.0 \cdot R_{Bias} \cdot V_X + 550.0 A_{V2} \cdot R_1 \cdot V_{CC} + 50.0 \cdot A_{V2} \cdot R_{Bias} \cdot V_X}$$

For R_{Bias}=10 kΩ 1% and rounding to the nearest 1% resistor and compensating for tolerance we have:

Table 2. 1% Rin values for CSOmin=0.2 V

Gain	R_{IN} (1%)
20	215Ω
30	143Ω
70	60.4Ω
100	42.2Ω

This gives a fixed offset that is above 0.2 V over time and temperature allowing the CSO pin to never be out of range from 0 A to whatever gain and sense resistor size will allow.

Table 3 below provides worst case offset voltages over time and temperature with respect to the above selected resistors.

Table 3. DC offset voltages with given resistor values

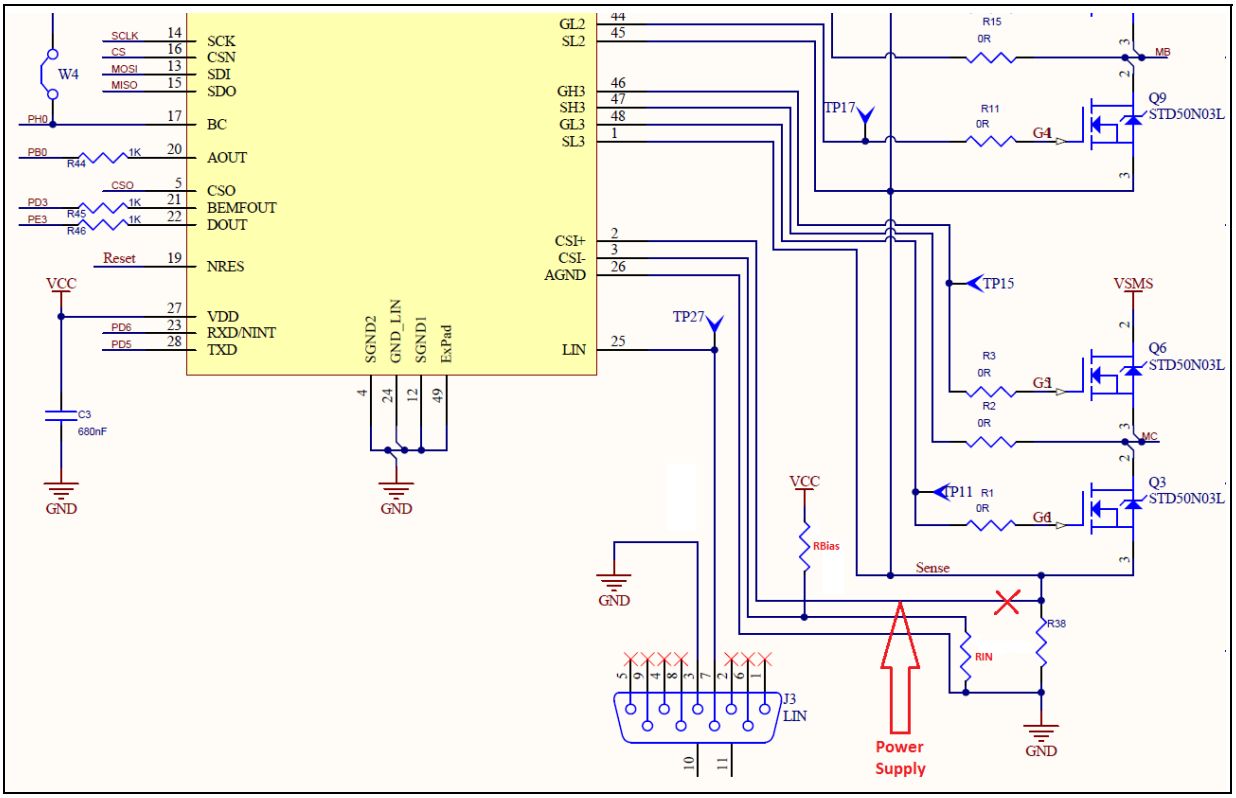
		CSO DC offset		
Gain	**Resistor**	**Min**	**Typ**	**Max**
20	215	0.202 V	0.304 V	0.416 V
30	143	0.188 V	0.292 V	0.407 V
70	60.4	0.196 V	0.304 V	0.424 V
100	42.2	0.193 V	0.304 V	0.426 V

These voltages are worst case given the external and internal resistor tolerances. There is a small overlap that drops below the worst case 0.2 V CSO minimum voltage. The worst case difference is at the gain of 30 with a 0.012 V error. This translates to a very small sense current. If this is an issue the next 1% resistor value lower will improve this to above the 0.2 V threshold.

3.1 Bench evaluation

To verify that the additional resistors did not somehow adversely affect the transfer function of the CSO circuit a bench evaluation was performed. The two resistors were inserted into a test board as shown in *Figure 9* below and the CSI+ pin was driven with a finely adjustable power supply.

Figure 9. Inserted bias resistors for testing



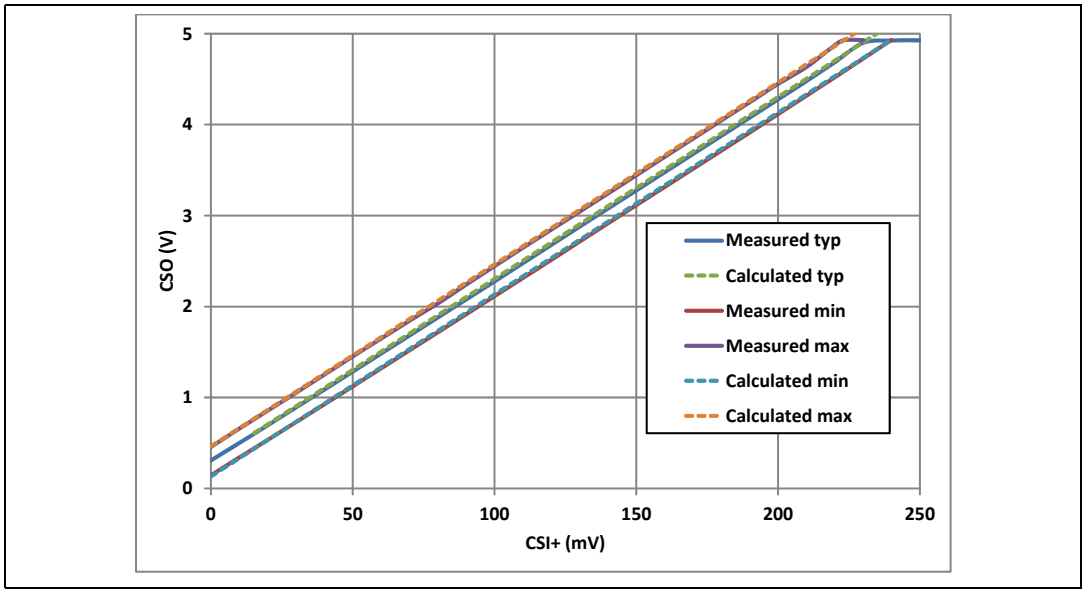
The L99ASC03G was programmed to not drive the inverter and the CSO gain was set to 20. The resistors used were 2 x 20 turn potentiometers adjusted to precisely 10.00 k Ohms and 215 Ohms. VCC was measured as 4.982 V. VX was not measurable and the overall gain, calculated from the collected data, varied from 19.5 to 19.8. The circuit was tested from VIN = 0 V to 250 mV in ~10 mV increments. This data was compared to the calculated values generated by *Equation 13*

where:

- VCC = 5 V
- VX=2.5 V
- RIN=215 Ohms
- RBias = 10 kOhms
- Av = 20

Figure 10 below compares the calculated versus measured transfer curves at a gain set at 20.

Figure 10. CSO vs. VIN at Av=20, calculated vs actual



As can be seen, the additional resistors did not affect the gain of the system. It only changed the zero current starting point.

3.2 Conclusion

Adding external resistors to set the CSO output offset to 0.2 V at 0 A is not difficult and does not adversely affect the gain. Low external resistor values have a small effect on the DC offset.

The DC offset issues can be easily calibrated out prior to and even during motor operation. This can be done by reading the CSO pin when the motor is not driving current or when the driven phase is in recirculation mode.

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
19-Mar-2014	1	Initial release.
16-May-2018	2	Changed Rpn L99ASC03 in L99ASC03G.