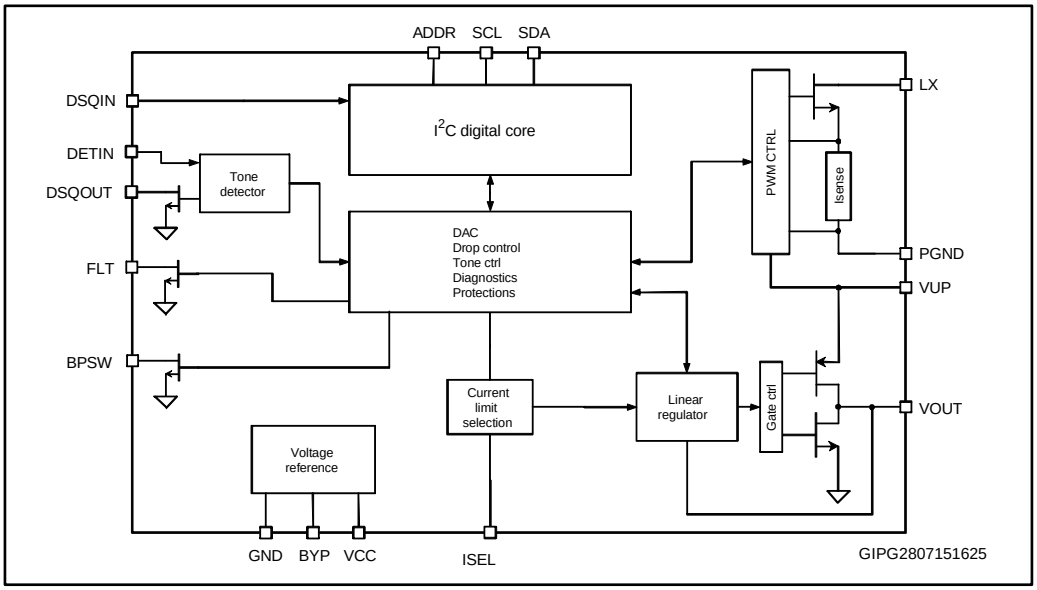
AN4175
Application note

LNBH25 supply and control IC with step-up and I²C interface

Introduction

This application note provides additional information and suggestions about the correct use of the LNBH25 device. All waveforms shown are based on the evaluation boards STEVAL-CBL009V1 and STEVAL-CBL010V1 described in *Section 5: "Component selection guide"* . The LNBH25 is a low-cost integrated solution for supplying/interfacing satellite LNB modules. Its performance is very good with the minimum quantity of external components. It includes all functions needed for the LNB supply and interface, in accordance with international standards. Moreover, it includes an I^2C bus interface and, thanks to a fully integrated step-up DC-DC converter, it works with a single input voltage supply range from 8 V to 16 V.

Figure 1: Internal block diagram



Contents

List of tables

List of figures

1 Block diagram description

The LNBH25 internal blocks are described in the following sections.

1.1 Step-up controller

The LNBH25 features a built-in step-up DC-DC converter that, from a single supply source ranging from 8 V to 16 V, generates the voltages that allow the linear post-regulator to work with minimum power dissipation. The external components of the DC-DC converter are connected to the LX and VUP pins (see *Figure 12: "STEVAL-CBL009V1 evaluation board schematic for DiSEqC1.x communication"* and *Figure 13: "STEVAL-CBL010V1 evaluation board schematic for DiSEqC 2.0 communication"*). No external power MOSFET is needed.

1.2 Voltage reference block

This block includes the undervoltage lockout circuit, which disables the whole circuit when the supplied VCC pin drops below a fixed threshold (4.7 V typ.) and a power-on reset sets all the I^2C registers to zero when the VCC turns on and rises from zero above the threshold (4.8 V typ.). If the input voltage is lower than LPD (low power diagnostic) minimum thresholds (6.7 V typ.), the PNG I²C bit is set to “1” by the voltage reference block and the FLT pin is set low.

1.3 I^2C interface digital core and diagnostic

The device main functions are controlled by I^2C bus, the data communication protocol from the main microprocessor to the LNBH25 and vice versa, which takes place through SDA and SCL pins. By writing to 4 control registers, all the LNBH25 functions can be managed. Moreover, 2 status registers can be read back and 8 diagnostic functions are received by the IC. The LNBH25 I^2C interface address can be selected between two different addresses by setting the voltage level of the dedicated ADDR pin.

Eight bits report the diagnostic status of eight internal monitoring functions:

OLF: overload fault. If the output current required exceeds the current limit threshold or a short-circuit occurs, OLF I^2C bit is set to "1".

OTF: overtemperature fault. If an overheating occurs, (junction temperature exceeds 150 °C typ.) the OTF I^2C bit is set to "1".

PNG: power not good. If the input voltage (VCC pin) is lower than LPD minimum threshold (6.7 V typ.) the PNG I^2C bit is set to "1".

VMON: voltage monitoring. If the output voltage (VOUT pin) is lower than VMON specification thresholds, the VOM I^2C bit is set to "1".

PDO: pull-down overcurrent. If the device output rises to a voltage level higher than the output nominal voltage selected, PDO I^2C bit is set to "1". This may happen due to an external voltage source present on the LNB output (VOUT pin).

TDET: tone detection. 22 kHz tone presence is detected on the DETIN pin.

TMON: tone monitoring. If the 22 kHz tone amplitude and/or the tone frequency is out of the guaranteed limits (refer to the datasheet.), the TMON I²C bit is set to "1".

IMON: minimum output current diagnostic to detect if no LNB is connected on the bus or cable is not connected to the IRD, the LNBH25 is provided with a minimum output current flag by the IMON I²C bit, which is set to "1" if the output current is lower than 12 mA (typ.).

1.4 Tone detector

This block provides a complete circuit to decode the 22 kHz burst code present on the DETIN pin in a digital signal by the DSQOUT pin where an open drain MOSFET is connected. The tone is also monitored and a dedicated bit (TMON) provides the diagnostic function described in *Section 1.1: "Step-up controller"*.

1.5 Linear post-regulator and current limit

The output voltage selection and the current selection commands join this block, which manages all the LNB output functions. This block gives feedback to the I^2C interface overcurrent protection and output settings. The linear post-regulator current limit threshold can be set by an external resistor connected to the ISEL pin.

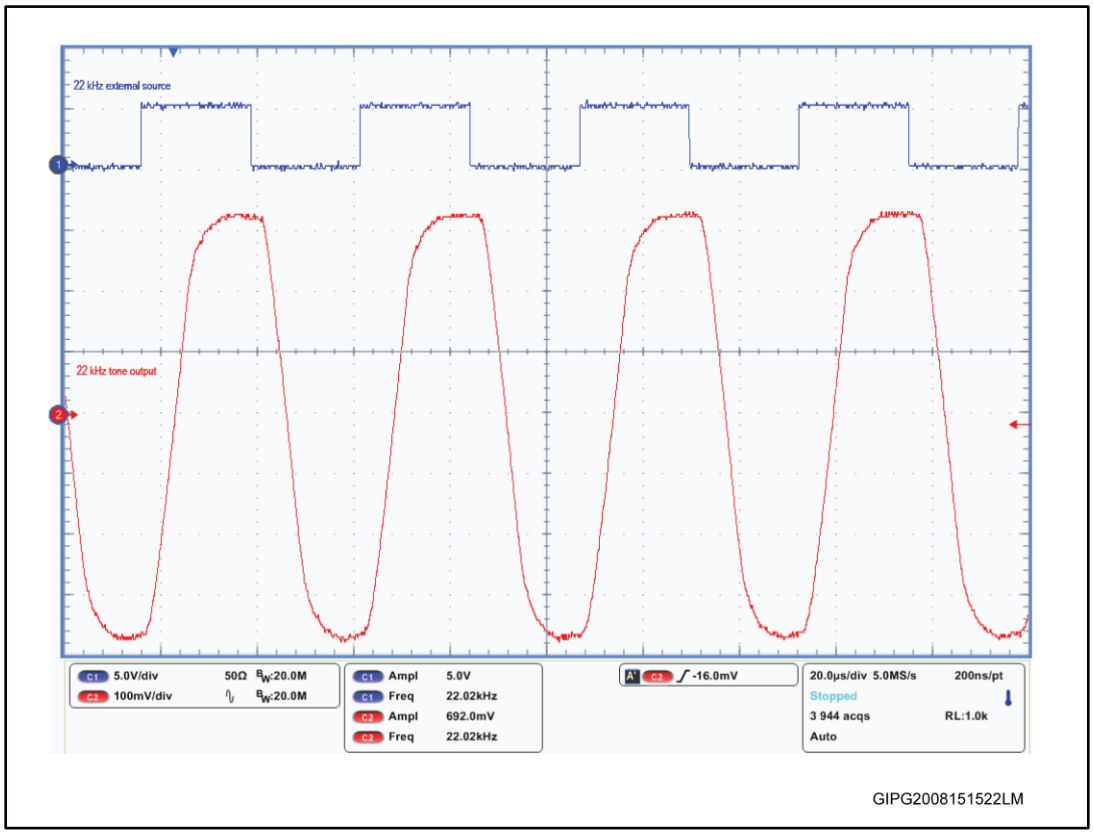
2 DiSEqC data encoding

The internal 22 kHz tone generator is factory-trimmed in accordance with current DiSEqC™ standards and its waveform is internally controlled by the LNBH25 tone generator in terms of rise/fall time and amplitude. The 22 kHz tone can be controlled in different ways through DISQIN logic pin and two I²C bits (EXTM and TEN).

2.1 22 kHz external source (EXTM=TEN=1)

If an external 22 kHz source DiSEqC data is available, it can be connected to the DSQIN logic pin (TTL compatible). The EXTM and TEN I²C bits must be set to "1". In this case the frequency and the duty cycle of the output tone are defined by the external 22 kHz signal on the DSQIN pin.

Figure 2: 22 kHz external source



Before sending the TTL signal to the DSQIN pin, the EXTM and TEN bits must be previously set to "1". When the DSQIN internal circuit detects the 22 kHz TTL external signal code, the LNBH25 activates the 22 kHz tone on the VOUT pin with about 1 µs delay from TTL signal activation, and it stops with about 60 µs delay after the 22 kHz TTL signal on DSQIN has expired, refer to *Figure 3: "22 kHz external source activation delay"* and *Figure 4: "22 kHz external source deactivation delay"*.

Figure 3: 22 kHz external source activation delay

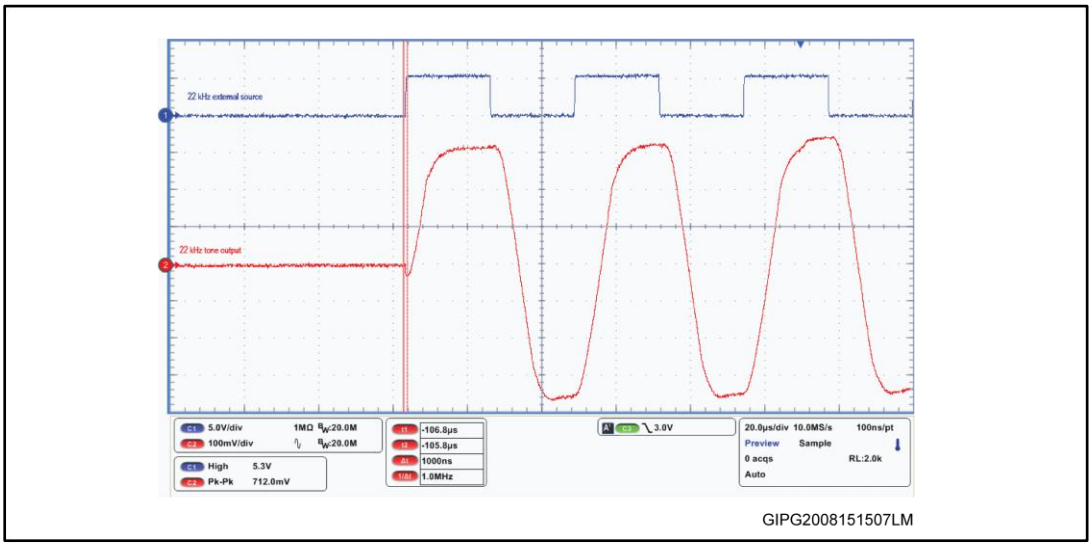
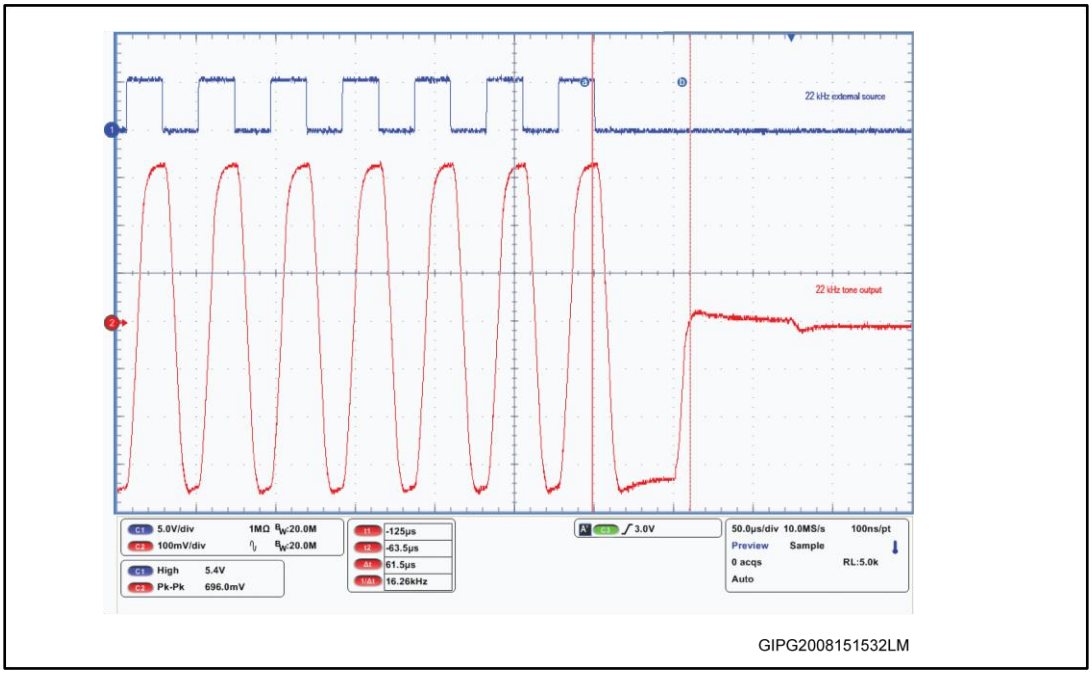


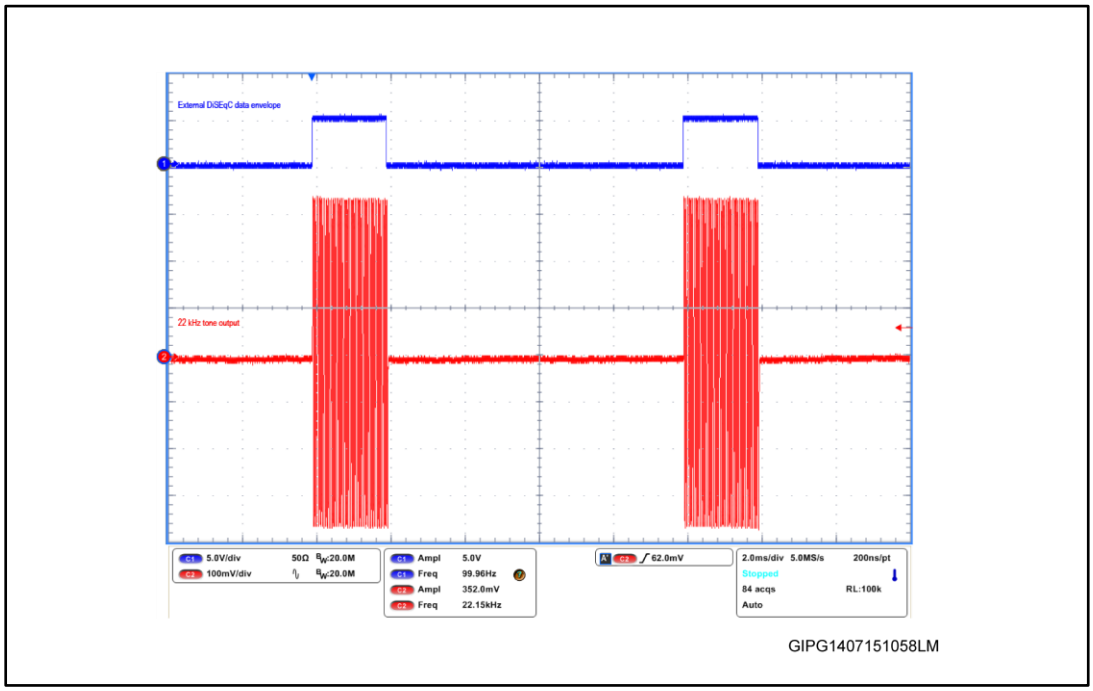
Figure 4: 22 kHz external source deactivation delay



2.2 DiSEqC data envelope source (EXTM=0; TEN=1)

Using an external DiSEqC data envelope source connected to the DSQIN logic pin, the I²C tone control bits must be set: EXTM = 0 and TEN = 1. In this manner, the internal 22 kHz signal is superimposed to the VOUT DC voltage to generate the LNB output 22 kHz tone. During the period in which the DSQIN is kept high, the internal control circuit activates the 22 kHz tone output.

Figure 5: DiSEqC data envelope source



22 kHz tone on the VOUT pin is active with about 6 µs delay from the DSQIN TTL signal rising edge, and it stops with a delay time in the range from 15 µs to 60 µs after the 22 kHz TTL signal on DSQIN has expired (refer to *Figure 6: "DiSEqC data envelope source activation delay"* and *Figure 7: "DiSEqC data envelope source deactivation delay"*).

Figure 6: DiSEqC data envelope source activation delay

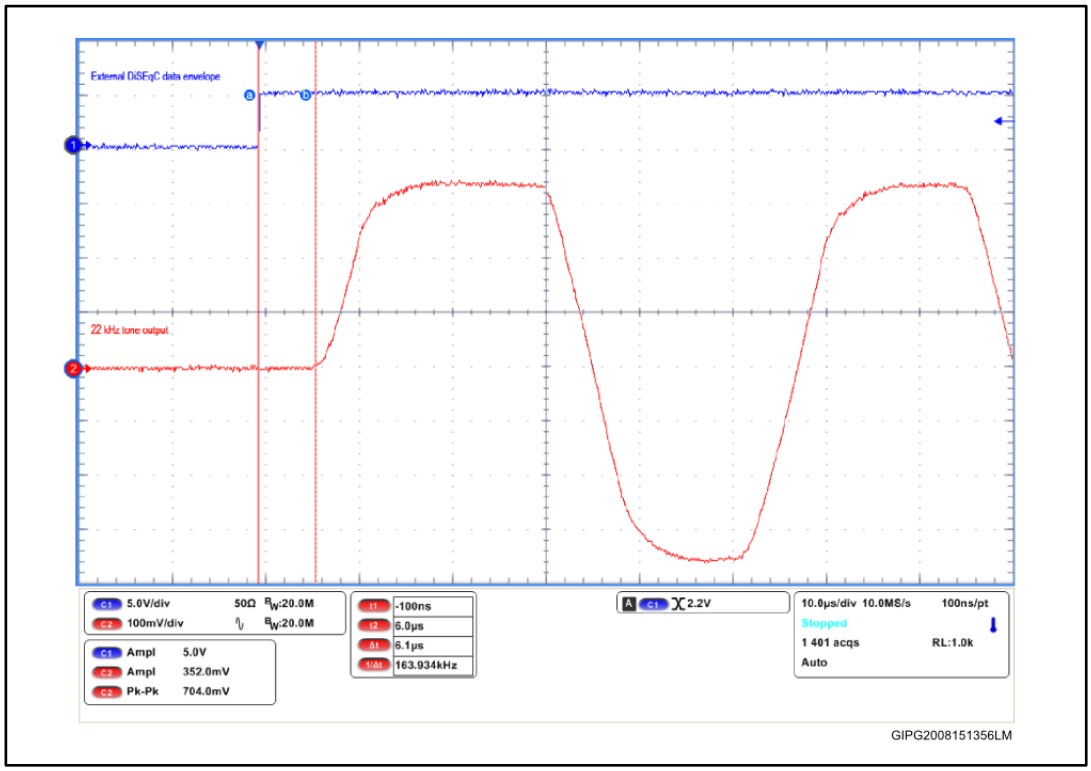
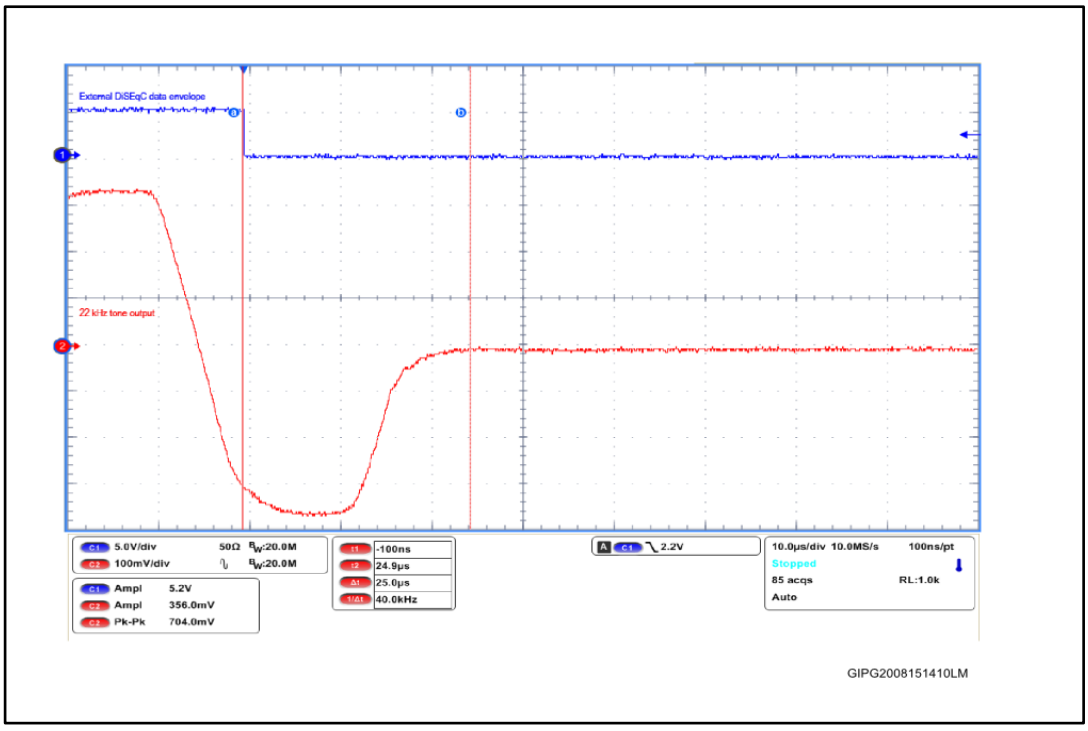


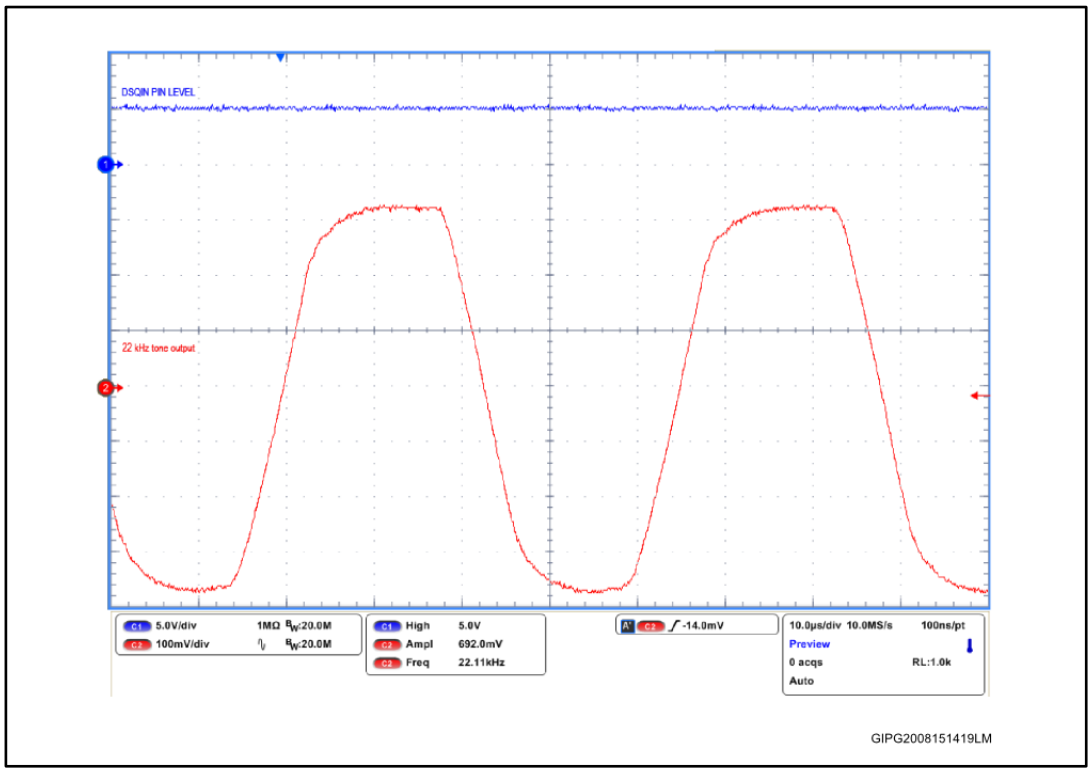
Figure 7: DiSEqC data envelope source deactivation delay



2.3 22 kHz tone in continuous mode (EXTM=0; TEN=1; DSQIN pin=H)

If a 22 kHz presence is requested in continuous mode, the integrated tone generator can be activated through the TEN I²C bit. In this case the DSQIN TTL pin must be pulled high and the EXTM bit set to "0".

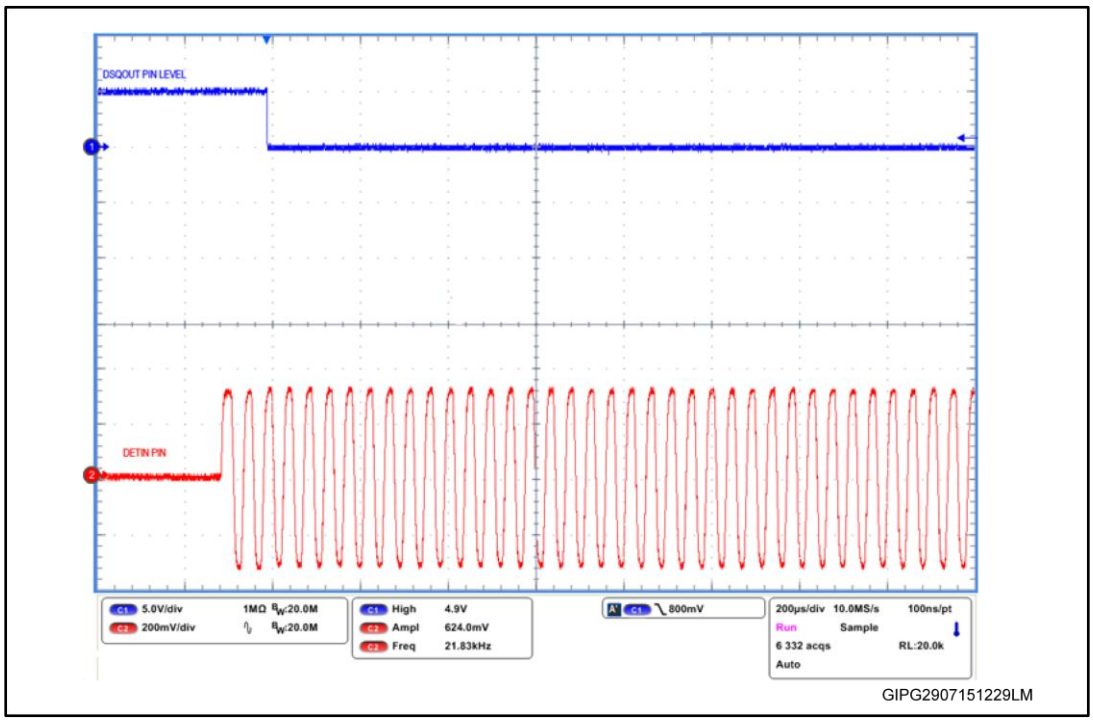
Figure 8: 22 kHz tone in continuous mode



3 DiSEqC 2.0 implementation

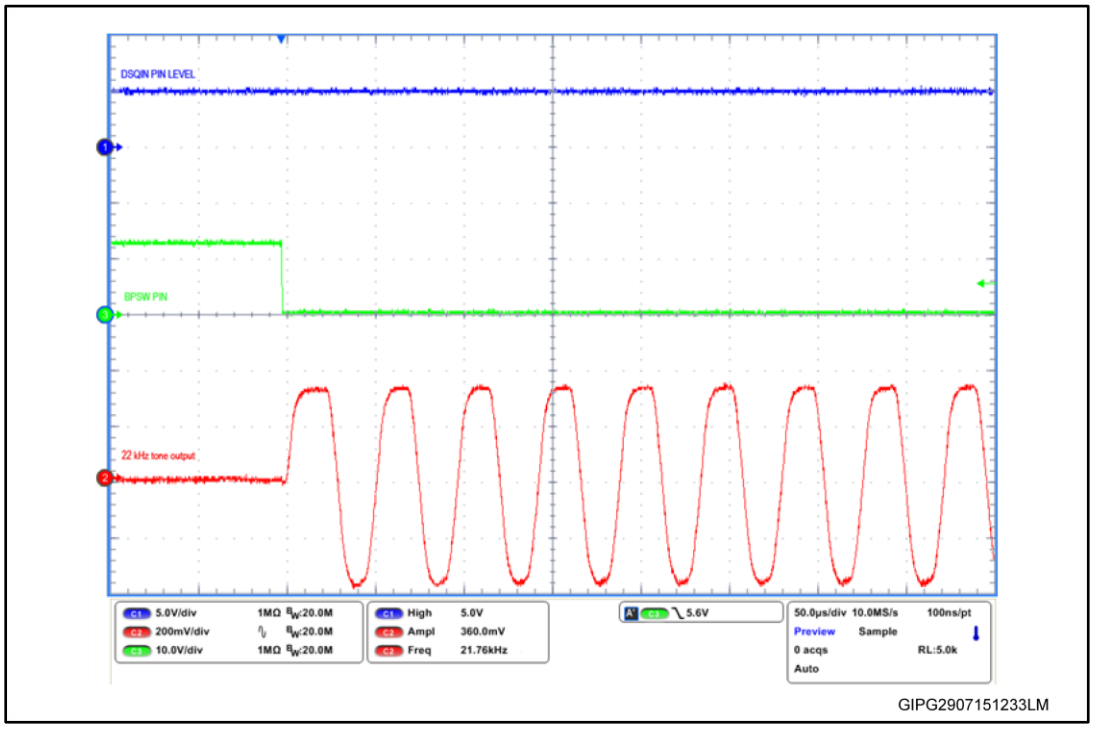
The built-in 22 kHz tone detector completes the fully bi-directional DiSEqC 2.0 interfacing. The input pin (DETIN) must be AC coupled to the DiSEqC bus, and extracted PWK data is available on the DSQOUT pin, please refer to the below figure.

Figure 9: DSQOUT output pin



To comply with the bi-directional DiSEqC 2.0 bus hardware requirements, an output RL filter is needed. In order to avoid 22 kHz waveform distortion during tone transmission, the LNBH25 is provided with the BPSW pin to be connected to an external transistor, which allows the output RL filter in DiSEqC 2.x applications to be bypassed while in transmission mode (refer to the below figure). Before starting tone transmission by the DSQIN pin, make sure that the TEN bit is set to "1" and after ending tone transmission, make sure that the TEN bit is set to 0.

Figure 10: BPSW pin behavior during tone transmission



4 Pin description

The LNBH25 is available in QFN24L with exposed pad package for surface mount assembly. The below figure shows the device pinout while *Table 1* briefly summarizes the pin functions.

Figure 11: Pin configuration (marking view)

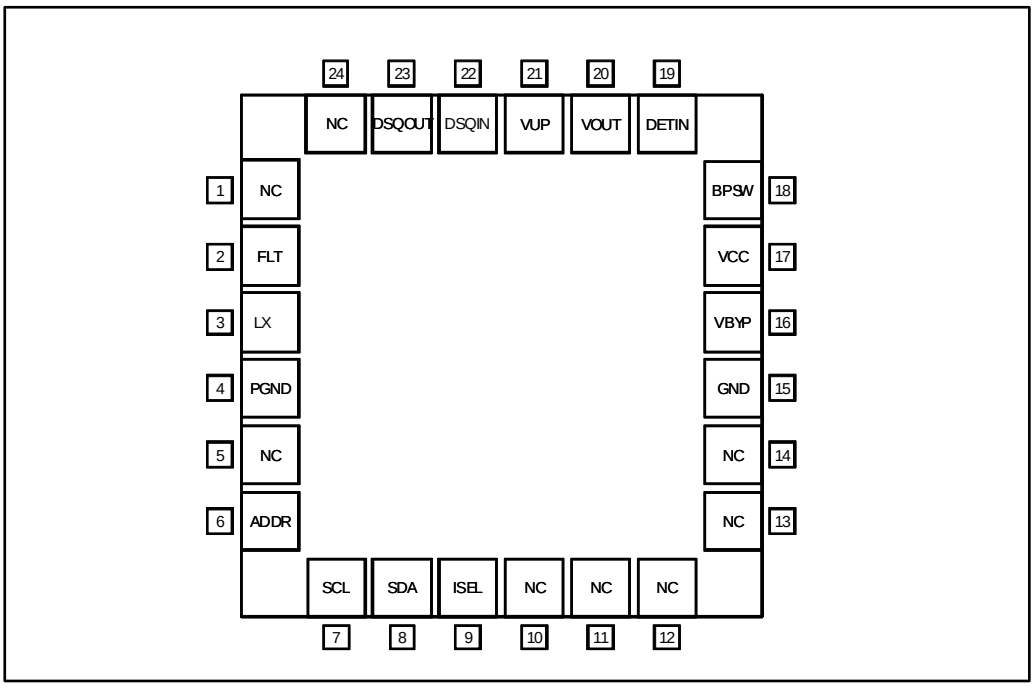


Table 1: Pin description

Pin	Symbol	Name	Function
2	FLT	FLT	Open drain output for IC fault conditions. It is set low in case of overload (OLF bit) or overheating status (OTF bit) is detected. To be connected to pull-up resistor (5 V max.)
3	LX	NMOS drain	Integrated N-channel power MOSFET drain
4	PGND	Power ground	DC-DC converter power ground to be connected directly to the exposed pad
6	ADDR	Address setting	Two I^2C bus addresses available by setting the address pin level voltage
7	SCL	Serial clock	Clock from/to I^2C bus
8	SDA	Serial data	Bi-directional data from/to I^2C bus
9	ISEL	Current selection	The resistor RSEL connected between ISEL and GND defines the linear regulator current limit threshold. Refer to output current limit selection
15	GND	Analog ground	Analog circuit ground. To be connected directly to the exposed pad

Pin	Symbol	Name	Function
16	BYP	Bypass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended to connect an external ceramic capacitor only. Any connection of this pin to external current or voltage sources may cause permanent damage to the device
17	VCC	Supply input	8 to 16 V IC DC-DC power supply
18	BPSW	Switch control	To be connected to an external transistor to be used to bypass the output RL filter needed in DiSEqC 2.x applications during the DiSEqC transmitting mode (see typical application circuits). Set to ground if it is not used
19	DETIN	Tone detector input	22 kHz tone decoder input, must be AC coupled to the DiSEqC 2.0 bus. Set to ground if it is not used
20	VOUT	LNB output port	Output of the integrated very low drop linear regulator. See truth table for voltage selections and description
21	VUP	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor
22	DSQIN	DSQIN for DiSEqC envelope input Or external 22 kHz TTL input	It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on the EXTM I²C bit setting as follows: EXTM=0, TEN=1: it accepts the DiSEqC envelope code from the main µcontroller. The LNBH25 uses this code to modulate the internally generated 22 kHz carrier. If EXTM=TEN=1: it accepts the external 22 kHz logic signals, which activate the 22 kHz tone output (refer to data encoding application information). Pull up high if the tone output is activated by TEN I²C bit only
23	DSQOUT	DiSEqC output	Open drain output of the tone detector to the main microcontroller for DiSEqC 2.0 data decoding. It is low when tone is detected to the DETIN input pin. Set to ground if it is not used
Epad	Epad	Exposed pad	To be connected with power ground and to the ground layer through vias to dissipate heat
1, 5, 10, 11, 12, 13, 14, 24	NC	Not internally connected	Not internally connected pins. These pins can be connected to GND to improve thermal performance

5 Component selection guide

The LNBH25 application schematics in *Figure 12: "STEVAL-CBL009V1 evaluation board schematic for DiSEqC1.x communication"* and *Figure 13: "STEVAL-CBL010V1 evaluation board schematic for DiSEqC 2.0 communication"* , show the typical configurations for a single LNB power supply for DiSEqC 1.x and DiSEqC 2.0 communication respectively.

Figure 12: STEVAL-CBL009V1 evaluation board schematic for DiSEqC1.x communication

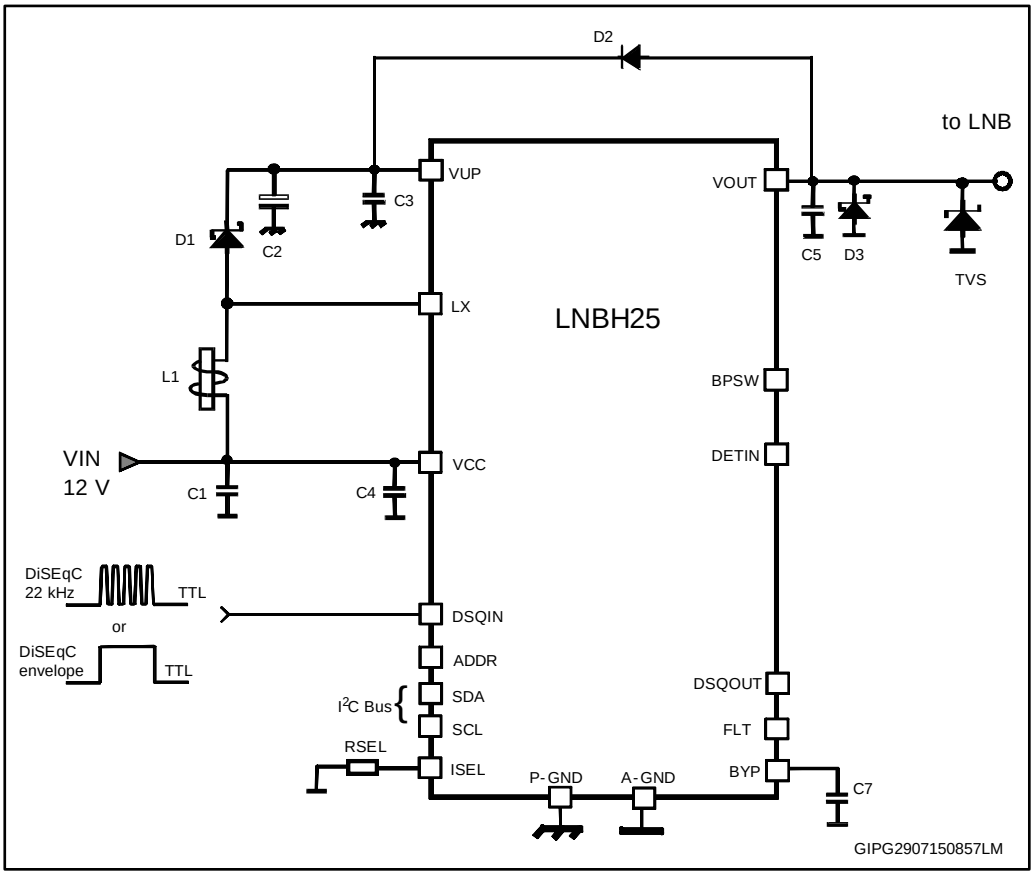
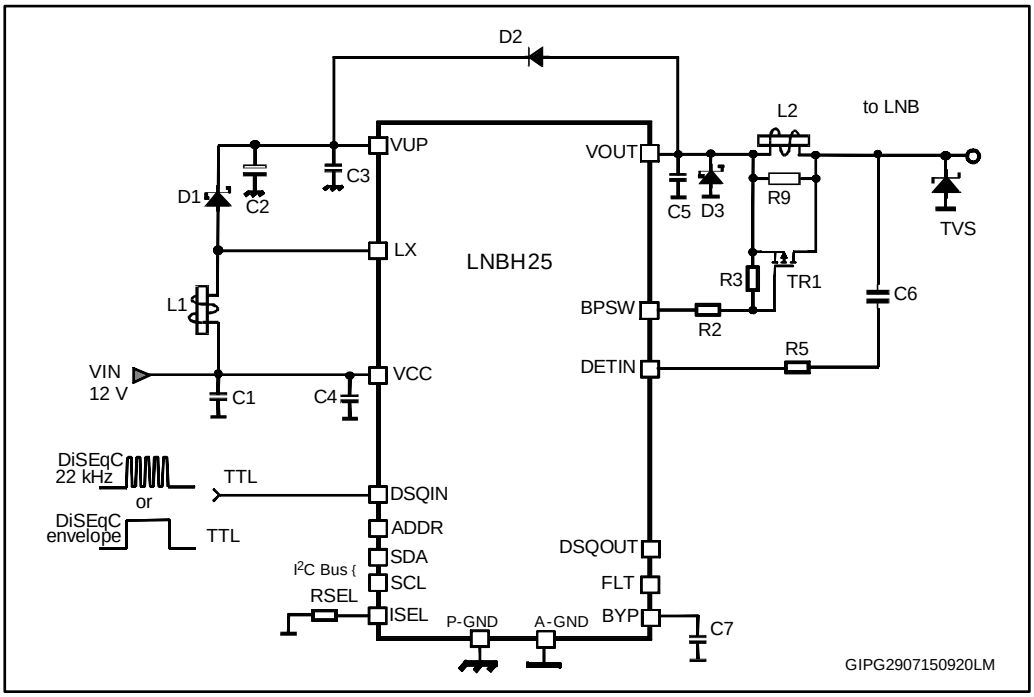


Figure 13: STEVAL-CBL010V1 evaluation board schematic for DiSEqC 2.0 communication



For both pictures, TVS diode has to be used if surge protection is required.

Table 2: LNBH25 evaluation board BOM list

Component	Notes
IC1	LNBH25 (QFN24L) exposed pad
C1	10 µF, 25 V ceramic capacitor
C2	100 µF, 50 V electrolytic capacitor
C3	1 µF, 50 V ceramic capacitor
C6	0.01 µF, 35 V ceramic capacitors
C4, C5, C6	0.22 µF, 50 V ceramic capacitor
D1	STPS130A or any similar Schottky diode
D2	S1A general purpose diode
D3	BAT43 (or any Schottky diode with $I_{F(AV)}$ > 0.2 A, V_{RRM} > 25 V) or BAT30, BAT54, TMM BAT43, 1N5818
TVS	LNBTVS22-XX TVS protection diode is suggested. Any other solution can be used depending on the requested surge protection level
L1	10 µH inductor with I_{SAT}>I_{PEAK}
L2	220 µH inductor with current rating higher than the rated output current
TR1	SI2003BDS 30 V PMOS
RSEL	16.2 kΩ 1/16 W resistor

Component	Notes
R2 , R3	4.7 kΩ resistor
R5	10 kΩ resistor
R9	15 hm 1/4W resistor

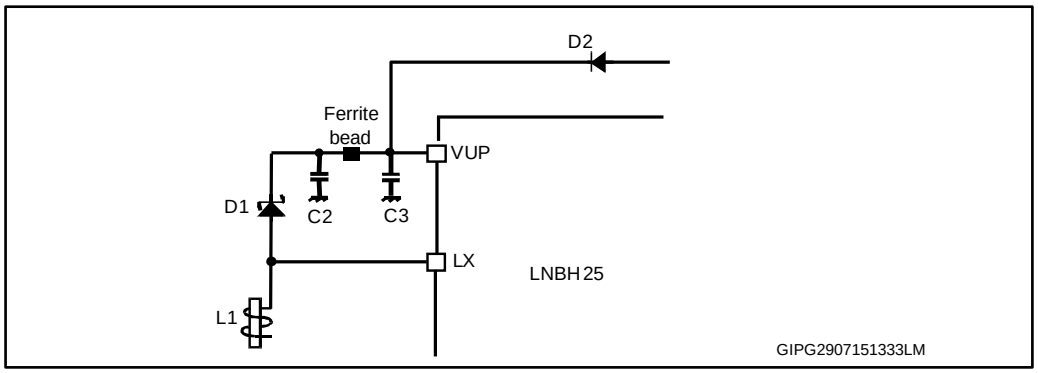
5.1 Input capacitors

A ceramic bypass capacitor (C1 in *Figure 12: "STEVAL-CBL009V1 evaluation board schematic for DiSEqC1.x communication"* and *Figure 13: "STEVAL-CBL010V1 evaluation board schematic for DiSEqC 2.0 communication"*) between 10 µF and 47 µF placed near the LNBH25 is needed for a stable operation. In any case, a ceramic capacitor in the range from 100 nF to 470 nF is recommended to reduce the switching noise on the input voltage pin (C4 in *Figure 12: "STEVAL-CBL009V1 evaluation board schematic for DiSEqC1.x communication"* and *Figure 13: "STEVAL-CBL010V1 evaluation board schematic for DiSEqC 2.0 communication"*).

5.2 DC-DC converter output capacitors

Low-cost electrolytic capacitors are needed on the DC-DC converter output stage (C2 in Figure 12 and Figure 13). Moreover, a ceramic capacitor between 1 µF and 4.7 µF is recommended to reduce high frequency switching noise (C3 in Figure 12 and Figure 13). The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To further reduce switching noise, a ferrite bead is recommended between the capacitors (refer to Figure 14).

Figure 14: DC-DC converter output stage with ferrite bead



The capacitor voltage rating must be at least 25 V, but if the highest voltage selection condition is used (V_{SEL1}= V_{SEL2}= V_{SEL3}= V_{SEL4} = 1), 35 V or higher voltage capacitors are suggested.

5.3 DC-DC converter Schotty diode

In typical application conditions, 1 A Schottky diode is suitable for the LNBH25 DC-DC converter. Taking into consideration that the DC-DC converter Schottky diode must be selected depending on the application conditions,(V_{RRM} > 25 V) one N-channel Schottky diode, such as the STPS130A is recommended. The average current flowing through the Schottky diode is lower than I_{peak} and can be calculated using the equation 1. In worst-case conditions, such as low input voltage and higher output current, a Schottky diode capable of supporting the I_{peak} should be selected. I_{peak} can be calculated using equation 2.

Equation 1: Id = IOUT x VOUT/VIN

Table 3: Recommended Schottky diode

Vendor	Order code	I_F(AV)	V_F(max.)
STMicrolectronics	1N5818	1 A	0.50 V
	1N5819	1 A	0.55 V
	STPS130A	1 A	0.46 V
	STPS1L30A	1 A	0.30 V
	STPS2L30A	2 A	0.45 V
	1N5822	3 A	0.52 V
	STPS340	3 A	0.63 V
	STPS3L40A	3 A	0.5 V

5.4 DC-DC converter inductor

The LNBH25 operates with a 10 µH inductor for the entire range of supply voltage and load current. The inductor saturation current rating (where inductance is approximately 70% of zero current inductance) must be greater than the switch peak current (I_{peak}) calculated at:

- maximum load (IOUTmax.)
- minimum input voltage (VINmin.)
- maximum DC-DC output voltage (VUPmax. = VOUTmax. + 1 V)

In this condition the switch peak current is calculated using the formula in equation 2:

Equation 2:

$$Ipeak = \frac{VUPmax. \cdot IOUTmax.}{Eff \cdot VINmin.} + \frac{VINmin.}{2LF}\left(1 - \frac{VIN\,min.}{VUPmax.}\right)$$

where:

Eff: is the efficiency of the DC-DC converter (93% typ. at the highest load)

L: is the inductance (10 µH typ.)

F: is the PWM frequency (440 kHz typ.)

Here below an example by using 10 µH coil.

The application condition as follows:

VOUTmax. = 19.150 V (supposing V_{SEL1} = V_{SEL2} = V_{SEL4} = 1, V_{SEL2} = 0)

VINmin. = 11 V

VUPmax. = VOUTmax. +V_{DROP} = 19.150 V+1 V = 20.150 V IOUTmax. = 500 mA

Eff = 90%

By using equation 1, I_{peak} is:

Equation 3:

$$Ipeak = \frac{20.150 \cdot 0.5}{0.9 \cdot 11} + \frac{11}{2 \cdot 10 \cdot 10^{-6} \cdot 440 \cdot 10^{3}} \left(1 - \frac{11}{20.150}\right) = 1.23\,A$$

Table 4: Recommended inductors

Supplier	Order code	I_{SAT}(A)	DRC(mΩ)	Mounting type
Coilcraft	LPS6235-103MLB	2.3	100	SMT
TDK	SLF6045-100M1R6	1.6	39	
EPCOS	B82472G6103M	1.9	53	

Several inductors suitable for the LNBH25 are listed in the above table, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information since many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the I_{peak} current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize power losses and, consequently, to maximize total efficiency.

5.5 Output current limit selection

The linear regulator current limit threshold can be set through an external resistor connected to ISEL pin. The resistor value defines the output current limit using the below equation:

Equation 4 :

$$I_{max.}\ typ.\ (A) = \frac{13915}{RSEL^{1.111}}$$

with ISET = 0

$$I_{max.}\ typ.\ (A) = \frac{6808}{RSEL^{1.068}}$$

with ISET=1

where RSEL is the resistor connected between the ISEL pin and GND. The highest selectable current limit threshold is 1.0 A (typ.) with RSEL = 11.5 kΩ.

5.6 Undervoltage diode protection

During a short-circuit removal on the LNB output, negative voltage spikes may occur on the VOUT pin. To prevent reliability problems, a low-cost Schottky diode is used between this pin and GND.

5.7 DiSEqC 2.0 implementation and inductor selection

To comply with DiSEqC 2.x requirements, an output R-L filter is needed. The internal 22 kHz signal is superimposed to the VOUT DC voltage to generate the LNB output 22 kHz tone and the LNBH25 is provided with the BPSW connected to an external transistor (refer to Figure 13), which allows bypassing the output RL filter during the 22 kHz tone transmission. This solution allows the 22 kHz tone to pass without any losses due to the R-L filter impedance. By the way, respect to the minimum DC voltage requirement, it is recommended to use an inductor with a current rating higher than the rated output current and a low DRC to minimize the voltage drop.

For example:

IOUT = 500 mA

DRC=33 m (Coilcraft inductor DO3340P-224)

Equation 6:

VDROP (V) = DCR (Ω) x IOUT (A) = 0.440 x 0.5 = 0.22 V

Several inductors suitable for the LNBH25 are listed in the below table:

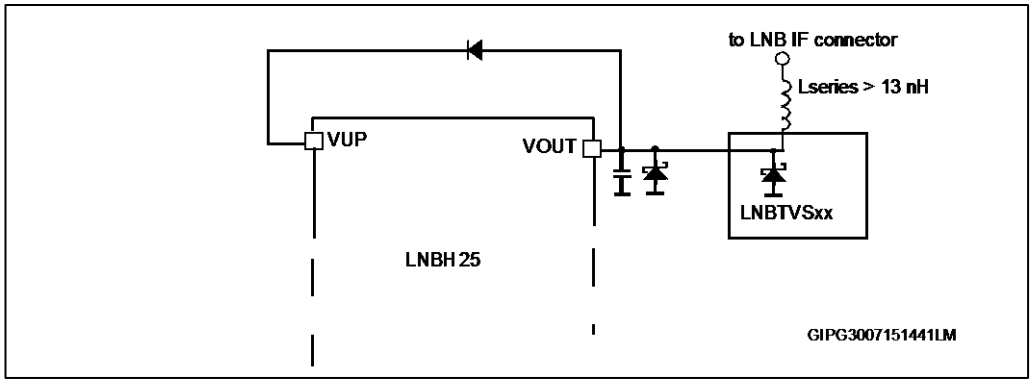
Table 5: Recommended inductors for output R-L filter

Supplier	Order code	I_{SAT} (A)	DRC(m)	Mounting type
Sumida	CD104-221MC	1.6	67	S.M.D
	RHC110-221M	2.4	88	T.H.
Toko	822LY-221K	1.3	70	T.H.
	824LY-221K	1.72	76	T.H.
	A671HN-221L	2.44	21	T.H.
	A814LY-221M	2.0	75	S.M.D
Panasonic	ELC08D221E	1.8	51	T.H.
	ELC11D221E	3.2	40	T.H.
Coilcraft	DO5010H-224	2.4	380	SMT
	MSS1278-224	2.3	360	SMT
	DO3340P-224	1.6	440	SMT

5.8 TVS diode

The LNBH25 device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. The LNBH25 device doesn't withstand such high energy discharges, so transient voltage suppressor (TVS) devices are used to protect the LNBH25 and other devices electrically connected to the antenna cable.

Figure 15: Recommended TVS diode connection



The LNBTVS, developed by STMicroelectronics, is a dedicated lightning and electrical overstress surge protection for LNB voltage regulators. This protection complies with the stringent IEC61000-4-5 standard with surges up to 500 A with a whole range of products for a cost/performance optimization.

The correct choice of the TVS diode must be taken into account according to the maximum peak power dissipation that the diode supports.

Table 6: Recommended ST LNBTVS

Order code	$VBR_{typ.}$ (V)	Ppp (W) 10/100 µs
LNBTVS4-220	23.1	1800
LNBTVS4-221	23.1	2000
LNBTVS4-222S	23.1	2000
LNBTVS6-221S	21.3	3000

Select the TVS diode, which is able to support the Ppp(W) whose value is indicated in *Table 5: "Recommended inductors for output R-L filter "*.

6 Layout guidelines

Due to high current levels and fast switching waveforms, which radiate noise, a proper PC board layout and a star ground configuration to protect sensitive analog ground are very important. Besides, lead lengths should be minimized to reduce stray capacitances, trace resistance, and radiated noise. Ground noise could be minimized by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Input bypass capacitors (C1 and C4) should be placed as close as possible to VCC and GND and the DC-DC output capacitors (C2 and C3) as close as possible to VUP. Excessive noise on the VCC input may falsely trigger the undervoltage circuitry, resetting the I^2C internal registers. If this occurs, the registers are set to zero and the LNBH25 is in shutdown mode.

6.1 PCB layout

Any switch mode power supply requires a good design of the PCB (printed circuit board) layout in order to achieve the top of performance in terms of system functionality. Component placing, GND trace routing and their widths are usually the major issues. Basic rules, commonly used for DC-DC converters for a good PCB layout, should be followed. All traces, carrying current, should be drawn on the PCB as short and thick as possible. This should minimize resistive and inductive parasitic effects, gaining system efficiency.

Figure 16: STEVAL-CBL009V1 top layer

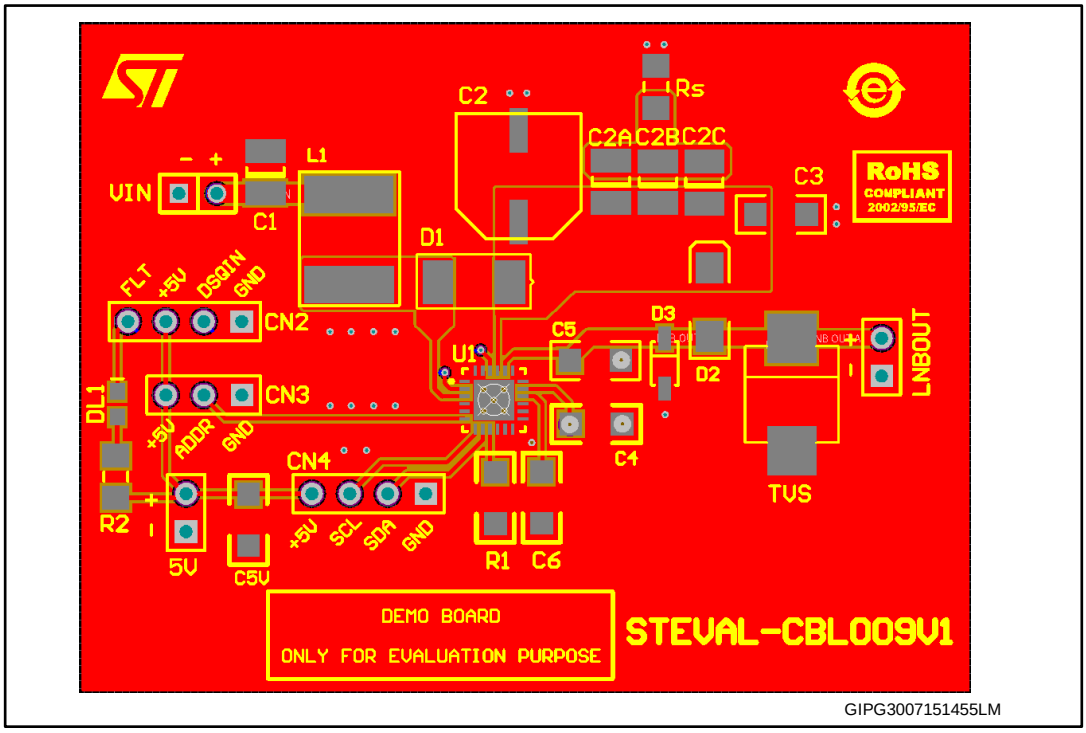


Figure 17: STEVAL-CBL009V1 bottom layer

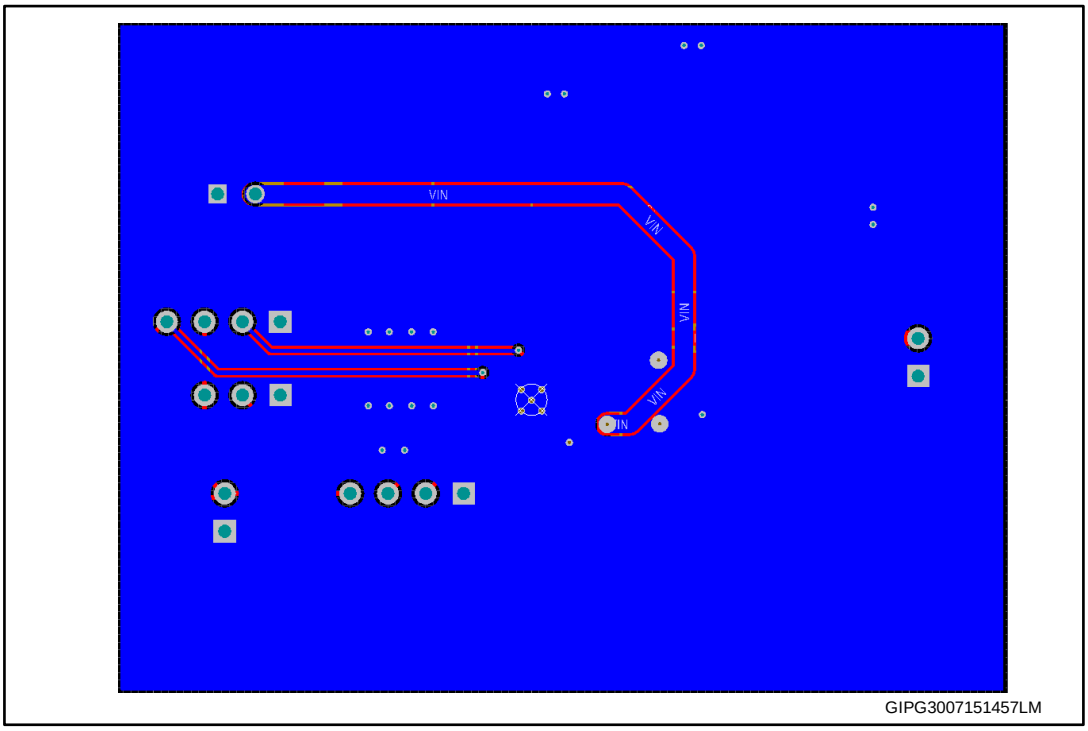


Figure 18: STEVAL-CBL009V1 component layout

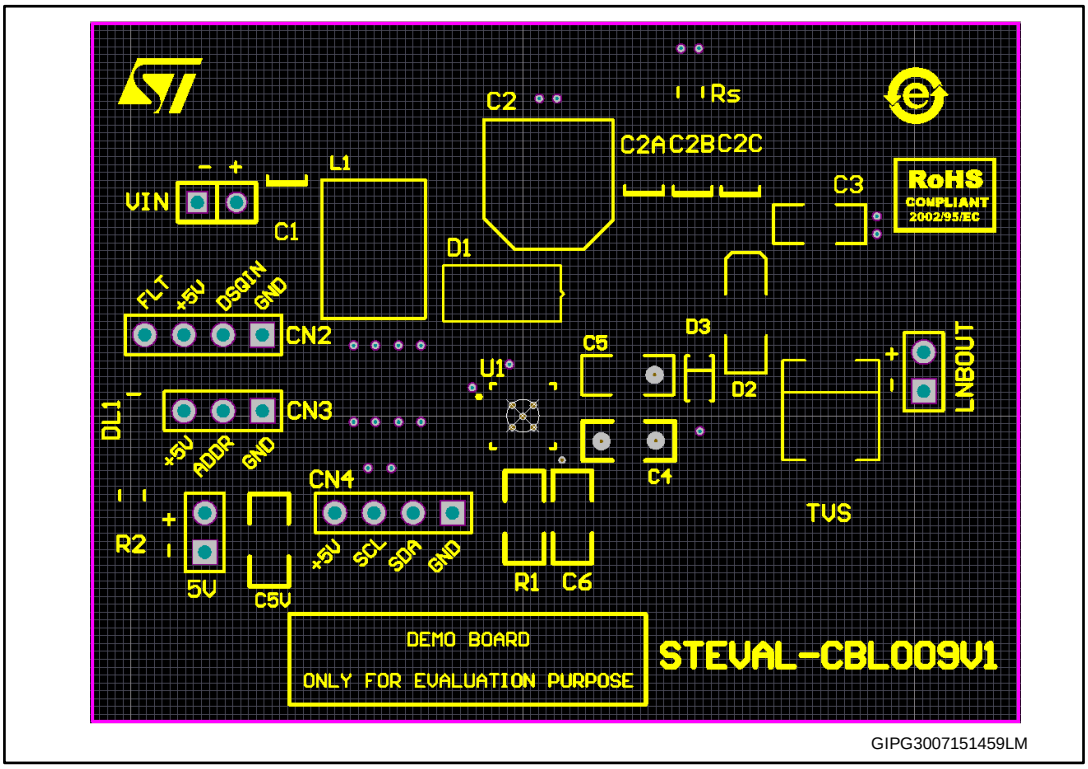
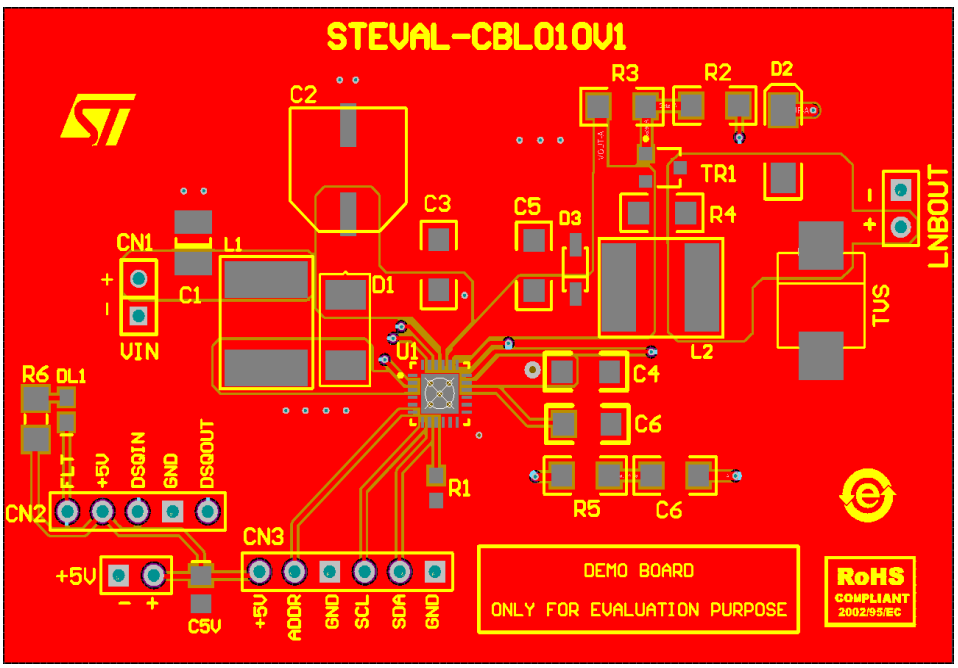
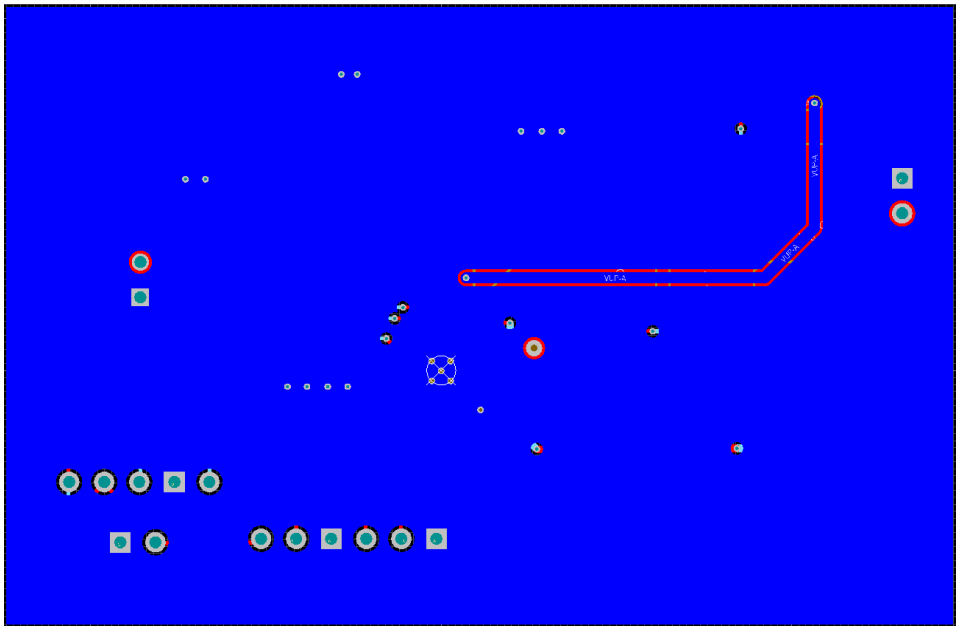


Figure 19: STEVAL-CBL010V1 top layer



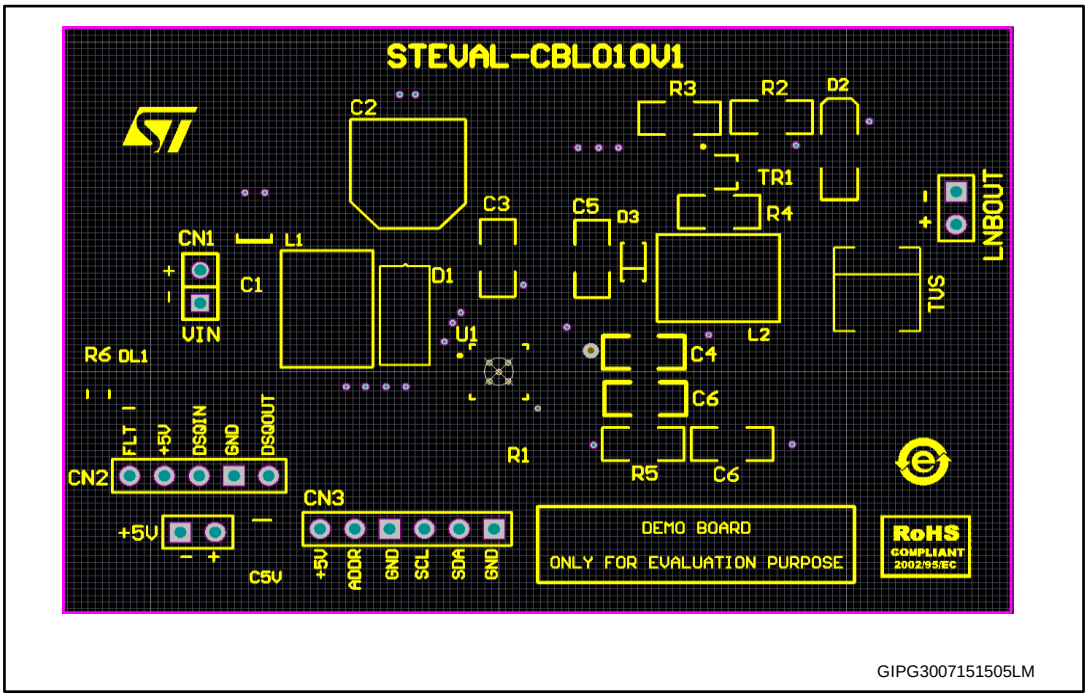
GIPG3007151500LM

Figure 20: STEVAL-CBL010V1 bottom layer



GIPG3007151503LM

Figure 21: STEVAL-CBL010V1 component layout



6.2 Start-up procedure

To test the board, you need:

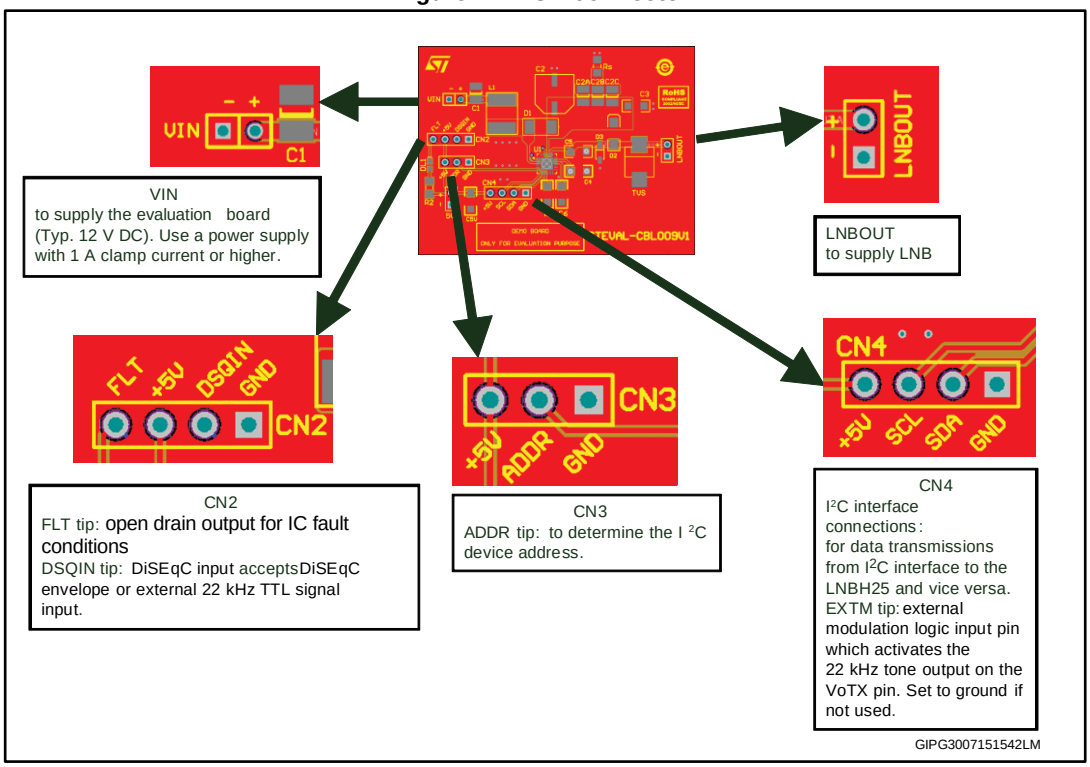
- I^2C BUS interface
- LNBH25/26 testing software
- Dual output power supply
- Electronic load

Step 1: the LNBH25/26 testing software

Step 2: plug the I^2C connector in CN4

Step 3: supply the evaluation board with CN1

Figure 22: PCB connector



7 Revision history

Table 7: Document revision history

Date	Revision	Changes
21-Aug-2015	1	First release.
04-Sep-2015	2	Updated pin configuration figure, the LNBH25 evaluation board BOM list table and DC-DC converter inductor section.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.