AN4069
Application note

5 V and 12 V power line protection based on STEF05 and STEF12 electronic fuses

Introduction

This demonstration board is based on the STEF05 and STEF12 electronic fuses (E-fuses). It is designed to help developers to evaluate the benefit of the complete protection offered by the E-fuse family and to customize their own application. The E-fuse family of hot-swap converters is designed to replace the mechanical fuses on low voltage power lines.

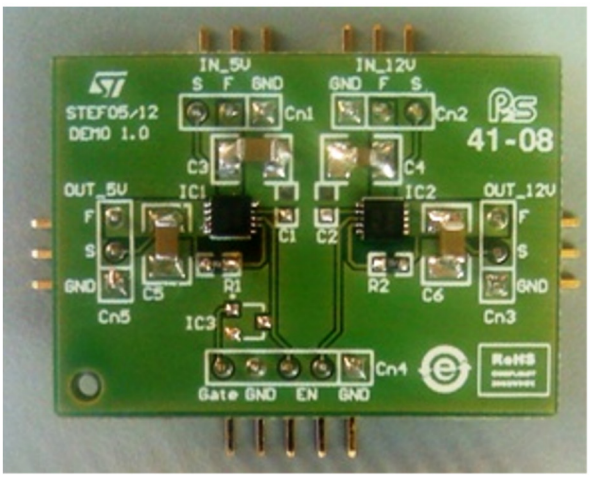
The STEF05 and STEF12 are integrated electronic fuses optimized for monitoring the output current and input voltage. Connected in series to the 5 V/12 V rails, they are capable of protecting the electronic circuitry on their output from overcurrent and overvoltage.

The turn-on time is programmable by means of an external capacitor, allowing the control of the inrush current at startup and during hot-swaps.

When an overload condition occurs, the E-fuse limits the output current to a predefined safe value. If the anomalous overload condition persists, it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, when power is re-applied the E-fuse initially limits the output current to a safe value, and then again goes into an open state. Both devices are equipped with a thermal protection circuit. The intervention of thermal protection is signaled to the board monitoring circuits through a signal on the ENABLE/FAULT pin that can be connected to other parts belonging to the same family to cause a simultaneous shutdown during failure events.

Unlike mechanical fuses, which must be physically replaced after a single event, E-fuses do not degrade in their performance after short-circuit/thermal protection interventions and can be reset either by re-cycling the supply voltage or by using the ENABLE pin.

Figure 1. Board image



AM11044v1

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1 Features

- Input voltages: 5 V and 12 V
- Continuous current: 3.6 A typ. each
- Adjustable slew rate for output voltage
- Overvoltage clamp
- Undervoltage lockout
- Programmable short-circuit current limit
- Overload current limit
- Controlled output voltage ramp
- Thermal latch protection
- Fault condition flag
- ENABLE pin.

2 Board characteristics

The demonstration board is provided with a STEF05PUR for the 5 V rail, a STEF12PUR for the 12 V rail, and a MOSFET switch connected to the ENABLE/FAULT pins to reset the E-fuses in case of thermal fault.

The board provides for separate or linked ENABLE pins, in order to allow either the observation of each single E-fuse or the complete 5 V/12 V protection application.

The short-circuit current limit is programmed to the standard values (2.9 A for the STEF05, 4.4 A for the STEF12), by means of a 22 Ω resistor placed on each channel. This resistor can be replaced by the user in order to set the desired current level.

The dV/dt control capacitor, used to set up the turn-on time and slew rate, is optional.

Figure 2. Demonstration board layout - top layer

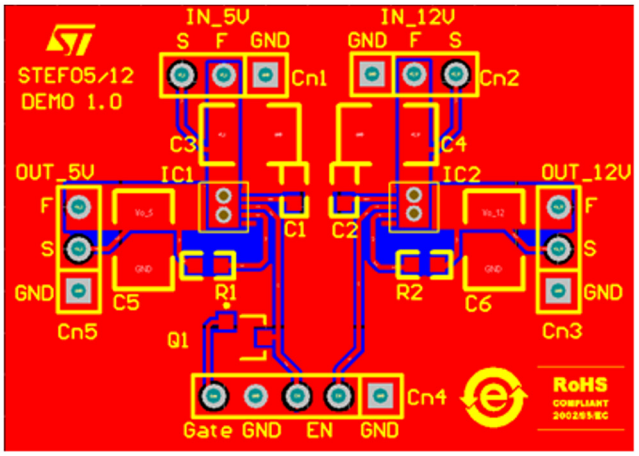
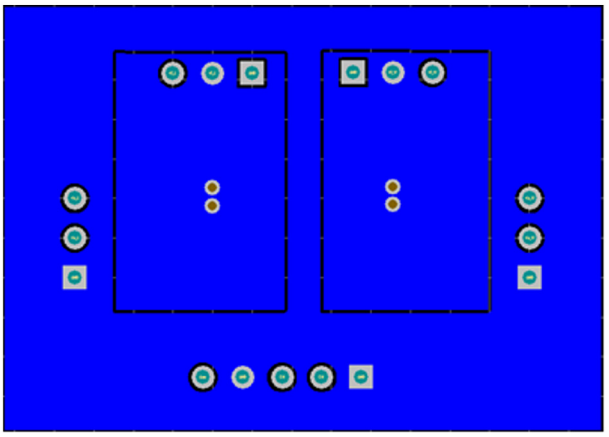


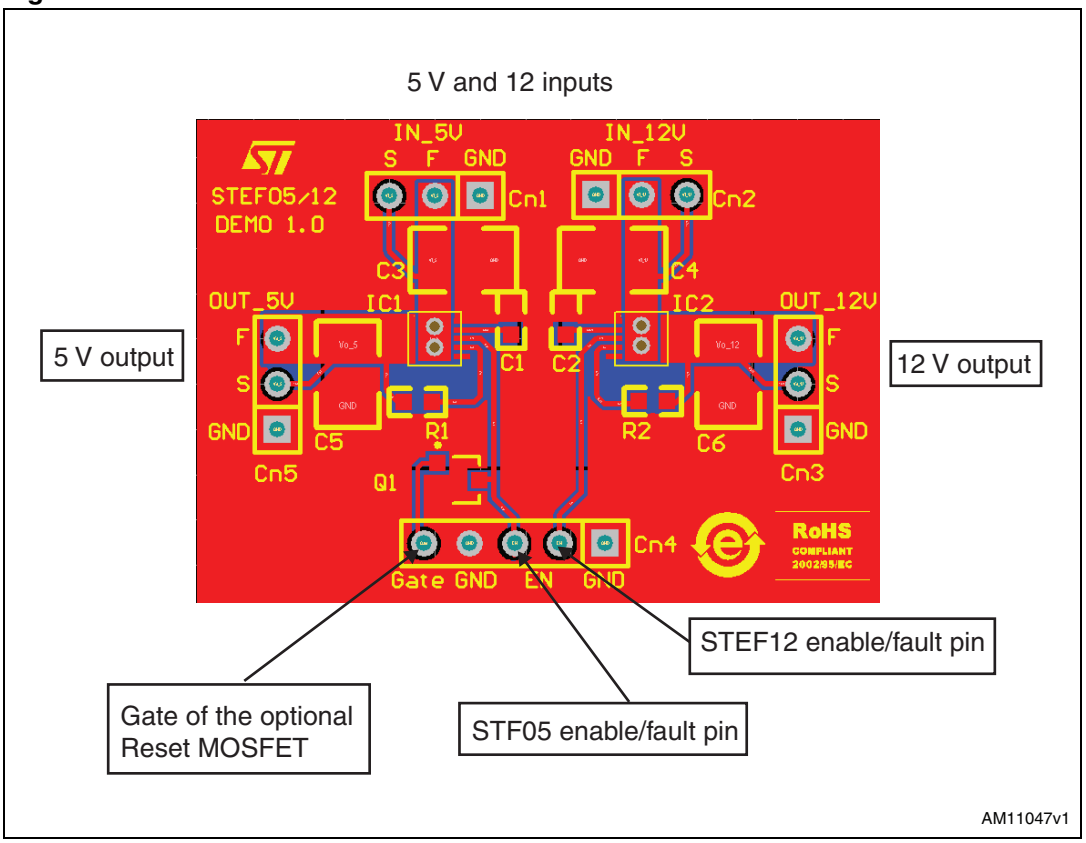
Figure 3. Demonstration board layout - bottom layer



3 Board testing

Once 5 V and 12 V are supplied to the Cn1 and Cn2 inputs, the board buffers the circuitry on its output (Cn3, Cn5) with the same voltage shown at its input, with a small voltage fall due to the internal N-channel MOSFET $R_{DS(on)}$.

Figure 4. Demonstration board connections



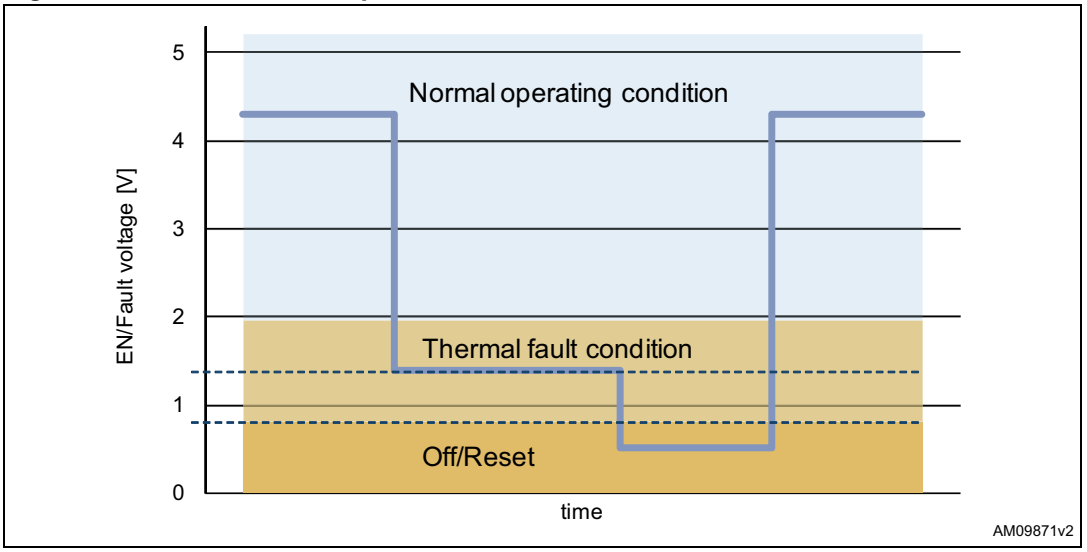
4 ENABLE/FAULT pin, thermal latch

The board provides for separate or linked ENABLE pins, in order to allow either the observation of each single E-fuse or the complete 5 V/12 V protection application. The Q1 MOSFET mounted on the board is connected to the 5 V device ENABLE pin only. This open drain circuit can be used to remotely control the device reset, by biasing the GATE pin with a positive voltage (5-10 V).

If this feature is not used, the MOSFET gate should be kept at GND (jumper on Cn4 pins 4-5). In this way the MOSFET does not influence the ENABLE/FAULT pin. To obtain a simultaneous shutdown and reset of both the devices, in the case of a thermal fault event on one of them, pins 2-3 of CN4 can be shorted together.

The devices can be reset from a thermal latch status also by re-cycling the power supply. The following diagram shows the ENABLE/FAULT pin signal levels in all the operating modes.

Figure 5. ENABLE/FAULT pin status



A thermal fault event can occur in the case of overload, short-circuit on the output or, under certain dissipation conditions, in the case of overvoltage on the input, causing a voltage clamp. In such cases the device output is disconnected, the ENABLE/FAULT pin is driven into an intermediate voltage level (~1.4 V) and the system is latched in this status. A reset can be achieved by pulling the ENABLE/FAULT pin down to the off/reset region (V_{EN} <0.8 V), and then releasing it again.

The same effect can be obtained by re-cycling the power supply to the board.

5 Output dV/dt circuit

The demo board comes with no $C_{dV/dt}$ mounted. In this condition, after an initial delay time of typically 500 µs for the STEF05 and 350 µs for the STEF12, the output voltage is supplied with a slope defined by the internal dv/dt circuitry.

The total time from the enable signal going high and the output voltage reaching the nominal value is typically 1 ms. The output voltage slew rate can be customized by mounting the dV/dt capacitors (C1, C2). The suggested values range is 10 pF to 1 nF.

Given the desired time interval Δt during which the output voltage goes from zero to its maximum value, the capacitance to be added on the $C_{dv/dt}$ pin can be calculated using the following theoretical formulas:

- STEF05 dV/dt setting $C_{dvdt} = 50 \times 10\text{-}9\Delta t - 30 \times 10\text{-}12$
- STEF12 dV/dt setting $C_{dvdt} = 24 \times 10\text{-}9\Delta t - 30 \times 10\text{-}12$

Figure 6. STEF05 delay time and VOUT ramp-up time

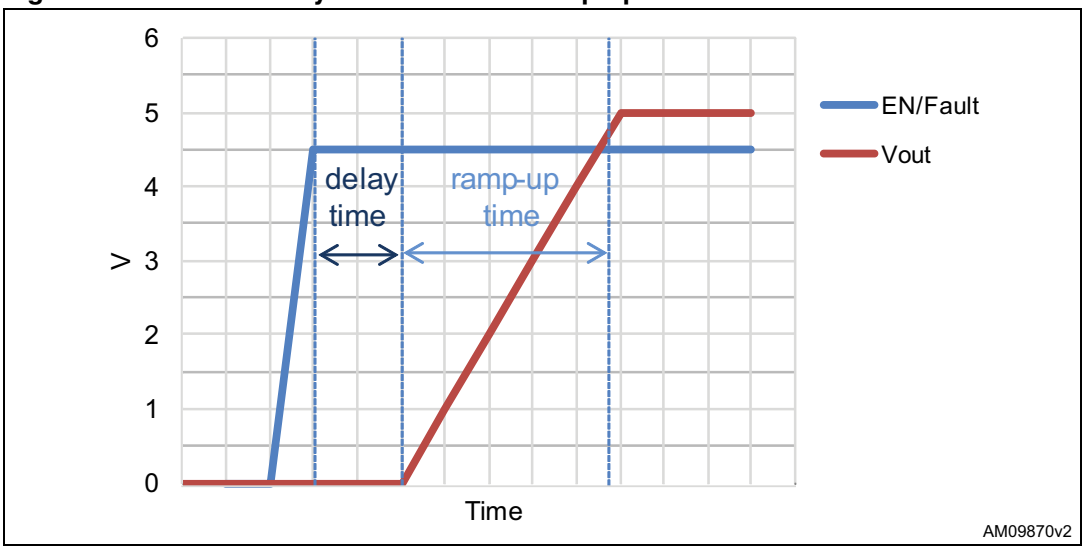
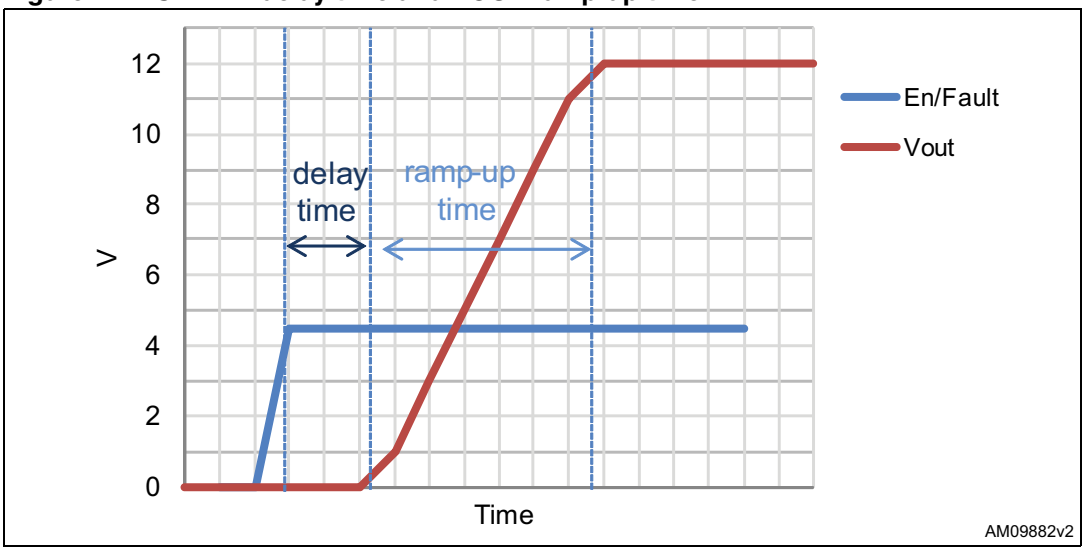


Figure 7. STEF12 delay time and VOUT ramp-up time



6 Current limit circuit

The short-circuit current limit on the board is pre-programmed to the standard values (2.9 A for the STEF05, 4.4 A for the STEF12), by means of a 22 Ω resistor placed on each channel. The current limit values can be customized by changing the R1, R2 resistors according to the desired peak current setting, as shown in the following charts.

Figure 8. STEF05: current limit vs. R-limit

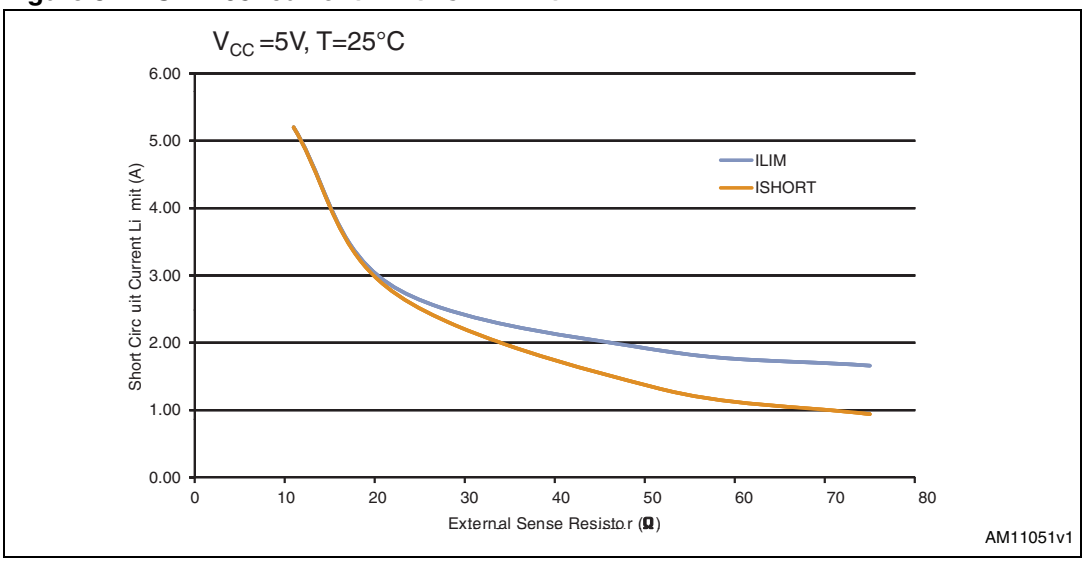
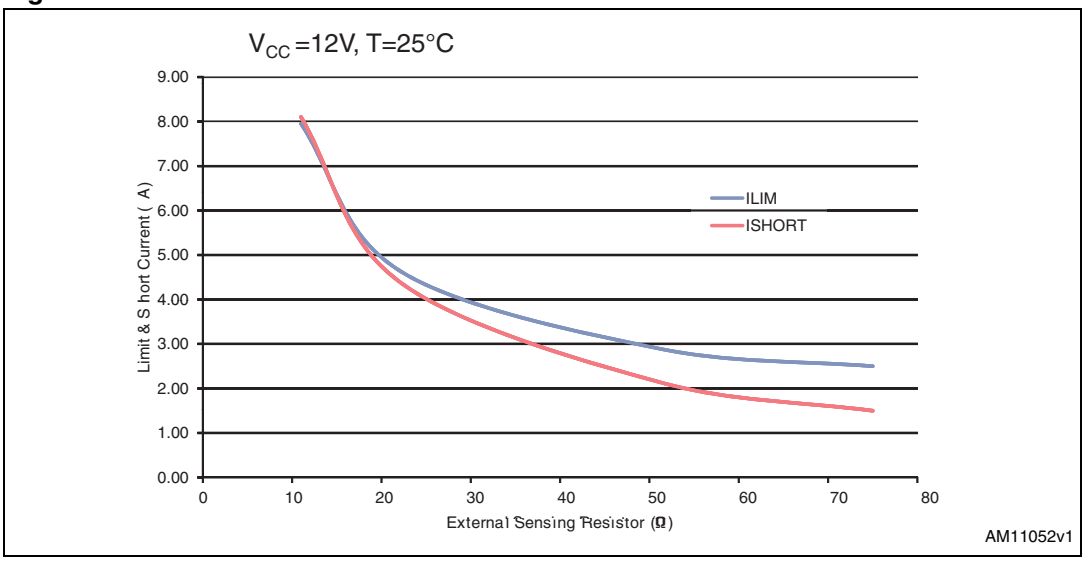


Figure 9. STEF12: current limit vs. R-limit



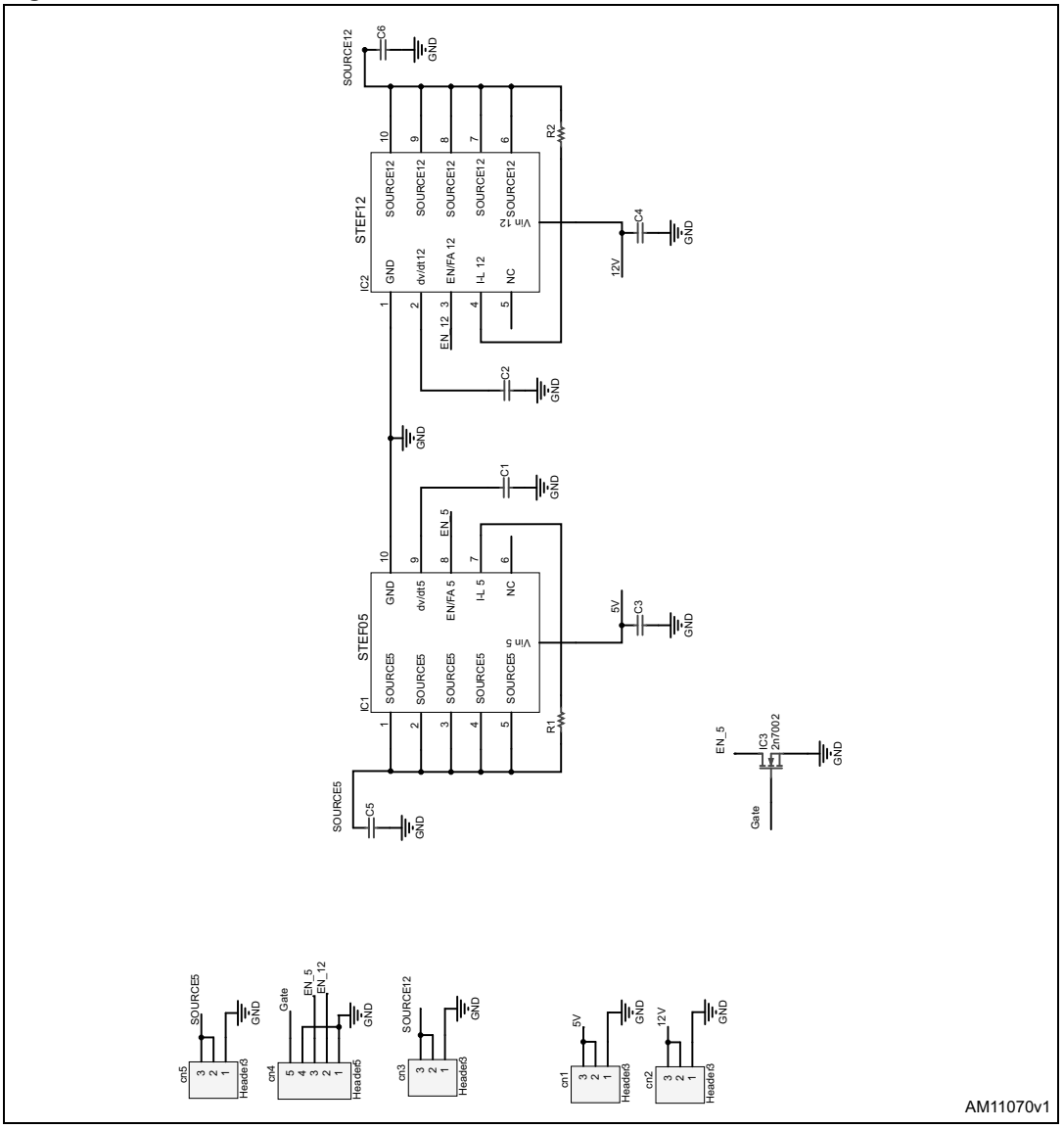
7 Overvoltage clamping circuit

This internal protection circuit clamps the output voltage to a maximum safe value, typically 6.65 V on the STEF05 and 15 V on the STEF12, if the input voltage exceeds these thresholds.

The output voltage remains at those levels until the overvoltage condition is removed or a thermal fault occurs.

8 Demonstration board schematic and BOM list

Figure 10. Schematic



8.1 Bill of material

Table 1. BOM

Reference	Part/value	Manufacturer	Manufacturer code
IC1	STEF05	STMicroelectronics	STEF05PUR
IC2	STEF12	STMicroelectronics	STEF12PUR

Table 1. BOM (continued)

Reference	Part/value	Manufacturer	Manufacturer code
C3,C4	10 µF/25 V, ceramic X7R, 1210	muRata	GRM32DR71E106KA12L
		KEMET	C1210C106K3RAC7800
C5,C6	47 µF/25 V, ceramic X7R, 1210		
C1,C2	Not mounted, 0603		
R1, R2	22 Ω, 0603		
Q1	MOSFET, SOT23-5L	STMicroelectronics	2N7002
Cnx	Connectors, strip line 90°		

Note: The Q1 transistor is connected only to the ENABLE pin of the STEF05 device. Simultaneous control of both the devices can be achieved by putting a jumper on pins 2-3 of CN4.

9 Device order codes

Table 2. Device order codes

Order codes	Package	Packaging
STEF05PUR	DFN10 (3 x 3 mm) tape and reel	DFN10 (3 x 3 mm) tape and reel
STEF12PUR	DFN10 (3 x 3 mm) tape and reel	DFN10 (3 x 3 mm) tape and reel

10 Revision history

Table 3. Document revision history

Date	Revision	Changes
12-Mar-2012	1	Initial release.