AN3978
Application note

Designing a digital output module with the L6370Q intelligent power switch STEVAL-IFP020V1

Introduction

The L6370Q is a single channel high-side driver chip intended for driving resistive, inductive or capacitive loads in industrial environments. It provides an embedded fast demagnetization feature for inductive load switch-off. The chip evaluates load disconnection (in channel ON state), output short connection to V_{CC} or GND, overtemperature, supply voltage undervoltage and provides feedback to a control unit. An integrated extensive set of electrical protections makes the application safe and reliable for use in harsh conditions.

This application note documents an example of an application design with the L6370Q component. It guides the user on how to choose application external components, provides appropriate schematic diagrams and PCB design, and an overview of immunity test results.

Application main features

- Galvanic isolated digital output module
- Single channel topology
- 2.5 A output current
- 100 mΩ output MOSFET R_{DSON}
- 9.5 V to 35 V supply voltage range
- Output current limiting
- Thermal shutdown
- Open ground protection
- Internal negative voltage clamping to V_S - 50 V for fast demagnetization
- Undervoltage lockout with hysteresis
- Open load detection
- Two diagnostic outputs
- Output status LED indication
- Non-dissipative short-circuit protection
- Protection against surge pulses (IEC61000-4-5)
- Immunity against burst transient (IEC61000-4-4)
- ESD protection (IEC61000-4-2)
- Compact design thanks to small component packages (L6370Q in QFN 7 x 7 mm)

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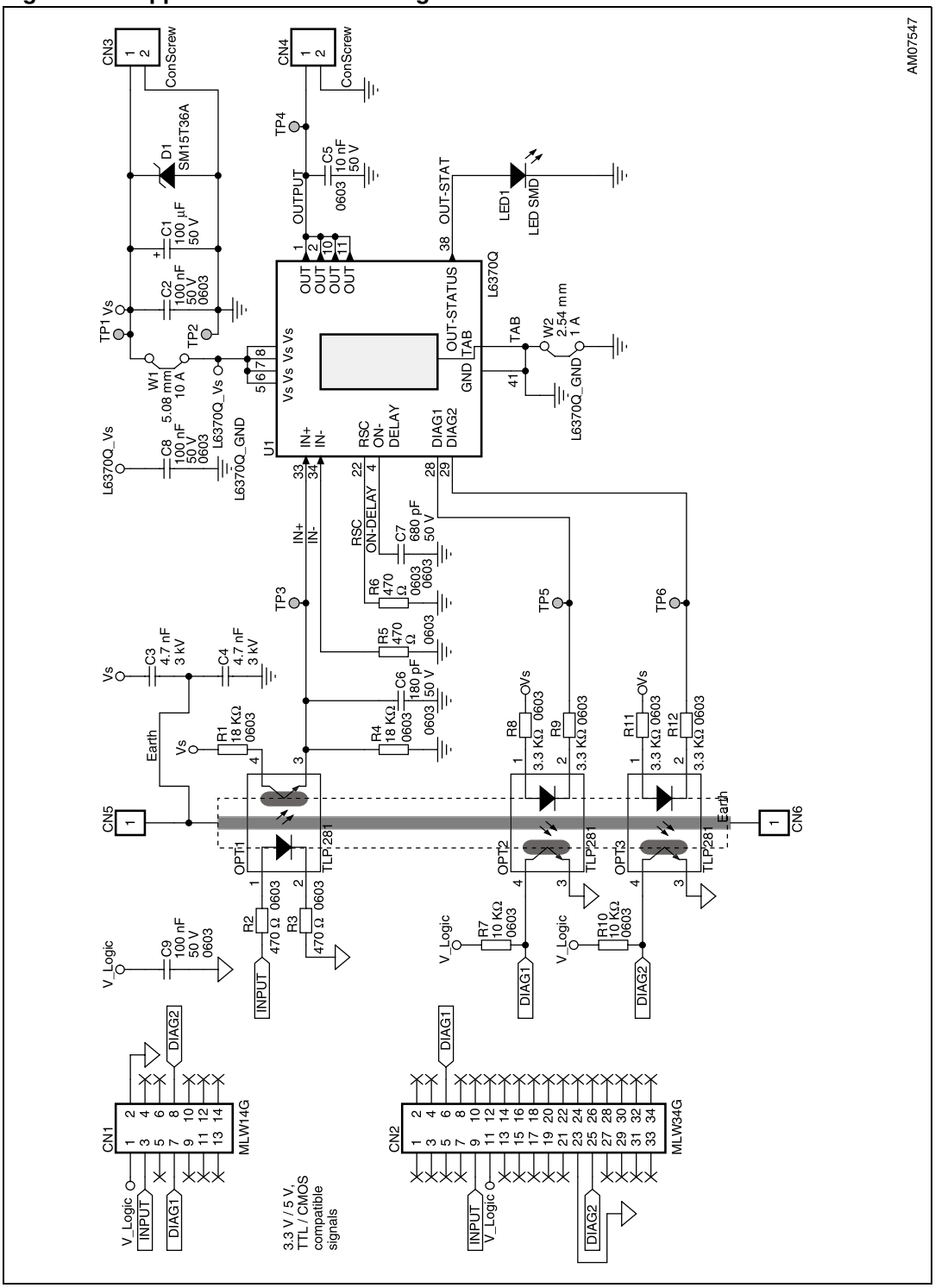
1 Schematic design

A complete application schematic diagram is visible in *Figure 1*.

Figure 1. Application schematic diagram



Section 1.1 to *Section 1.5* show how the L6370Q chip features are configured, which external components are used, and how they are dimensioned.

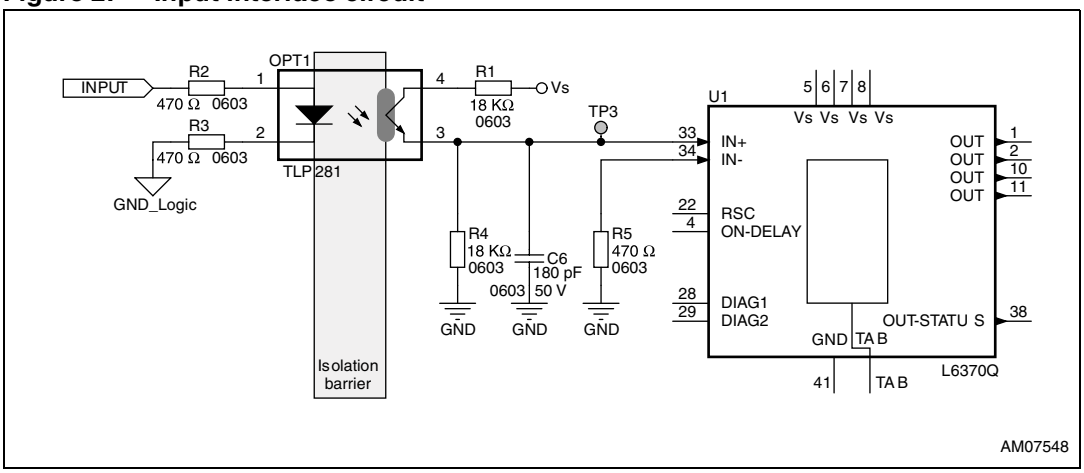
1.1 Input interface

The aim of the design is to provide a galvanic isolated output module. It requires the use of isolators on the control / feedback signals. In the case of STEVAL-IFP0020V1, cost effective, compact size optocouplers (TLP281) have been selected.

Important parameters for the application design are:

- Collector-emitter voltage higher than 80 V - which exceeds the L6370Q absolute maximum ratings and therefore doesn't limit supply voltage range
- Isolation voltage higher than 2500 Vrms - usually sufficient for this kind of application
- Current transfer ratio (depends on LED current) - LED and output phototransistor currents must be adjusted accordingly.

Figure 2. Input interface circuit

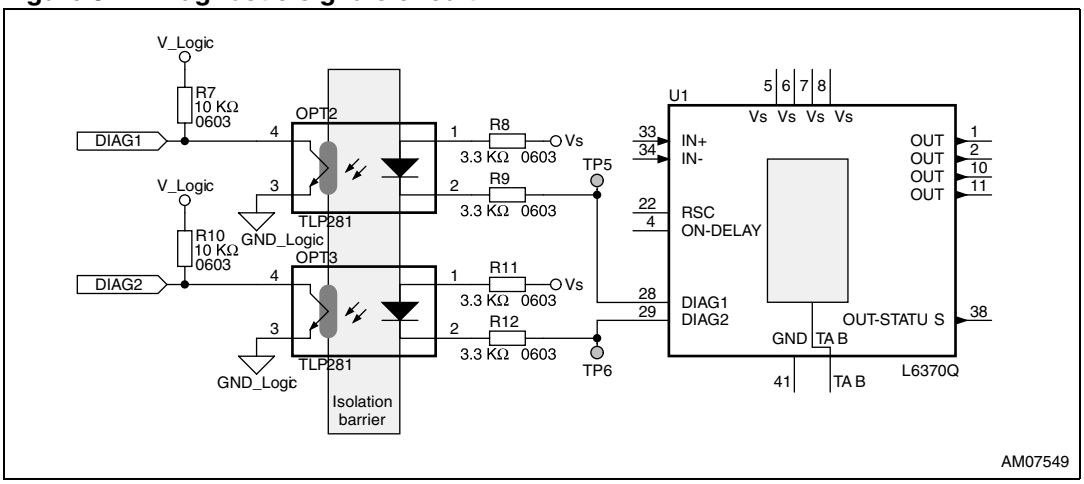


The input interface connection can be seen in *Figure 2*. LED current ranges between approximately 2.4 mA, considering a 3.3 V signal level, and 4.3 mA for 5 V logic level. Symmetrical LED resistor connection should positively influence EMC immunity. To achieve the maximum tolerance of IN+ threshold (2 V according to the datasheet, considering that IN- = 0 V), the required minimum phototransistor current is approximately 0.11 mA (2 V / 18 kΩ). This means that CTR of the optocoupler must be at least ~5% (0.11 mA / 2.4 mA). This is in accordance with the TLP281 datasheet which shows a much higher CTR.

1.2 Diagnostic signal interface

The diagnostic signal interface is implemented in a similar way to the input interface. The appropriate part of the schematic diagram can be seen in *Figure 3*.

Figure 3. Diagnostic signals circuit



In this case, the optocoupler LED current appears in the range from 1.3 mA to 5.2 mA depending on supply voltage Vs. Symmetrical LED resistors are chosen in order to optimize EMC immunity and split power dissipation. In order to comply with the logic levels on the control side, an appropriate external pull-up resistor is necessary. The value selected for the L6370Q application is 10 kΩ.

If the L6370Q open drain diagnostic driver is OFF, no current flows through the optocoupler LED and the optotransistor is therefore OFF. Logic high level is provided by the 10 kΩ pull-up resistor.

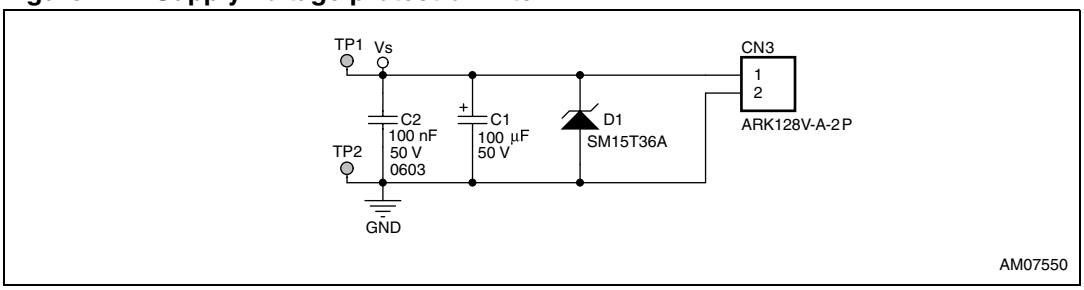
If the diagnostic is active (ON), the optocoupler LED is powered and the optotransistor conducts a current depending on a load. Minimum current to ensure TTL low level compatibility (0.7 V max.) is:

$(V_{logic} - V_{Imax}) / PullUp = (5\ V - 0.7\ V) / 10000 = 0.43\ mA$. This condition is also in accordance with TLP281 characteristics.

1.3 Supply voltage line protection

L6370Q supply voltage lines are protected against surges, reverse polarity and other disturbances with the external filter, as shown in *Figure 4*.

Figure 4. Supply voltage protection filter



A Transil™ diode is used to clamp high energy surge pulses followed by a capacitive filter to suppress noise disturbance and limit application EMI. Capacitor C1 (100 µF) has a low ESR parameter in order to effectively suppress supply voltage fluctuations.

1.4 Short-circuit current limit settings

Configuration of the current limit is done by the external resistor connection between the RSC pin and GND. A 470 Ω resistor is used in the STEVAL-IFP020V1 application to adjust the maximum current limit, which is 3.2 A (typ.), due to the fact that 0 < RSC < 5 kΩ, according to the L6370Q datasheet.

1.5 ON-DELAY configuration

ON-DELAY pin functionality is well described in the L6370Q datasheet. Basically, it is used to disable the power stage if an overcurrent condition lasts longer than the adjusted t_{ON}. This feature also suppresses diagnostic activation in case of short-time overload or short-circuit.

A capacitor value of 680 pF connected between the ON-DELAY and GND adjusts the ON- DELAY time to:

$$t_{ON} = 1.28 * C_{ON} = 1.28\ \mu s/pF * 680\ pF = 870.4\ \mu s$$

2 PCB layout

The demonstration board PCB layout has been developed by applying standard rules, avoiding signal loops and minimizing track length.

Figure 5. Demonstration board PCB layout - top side

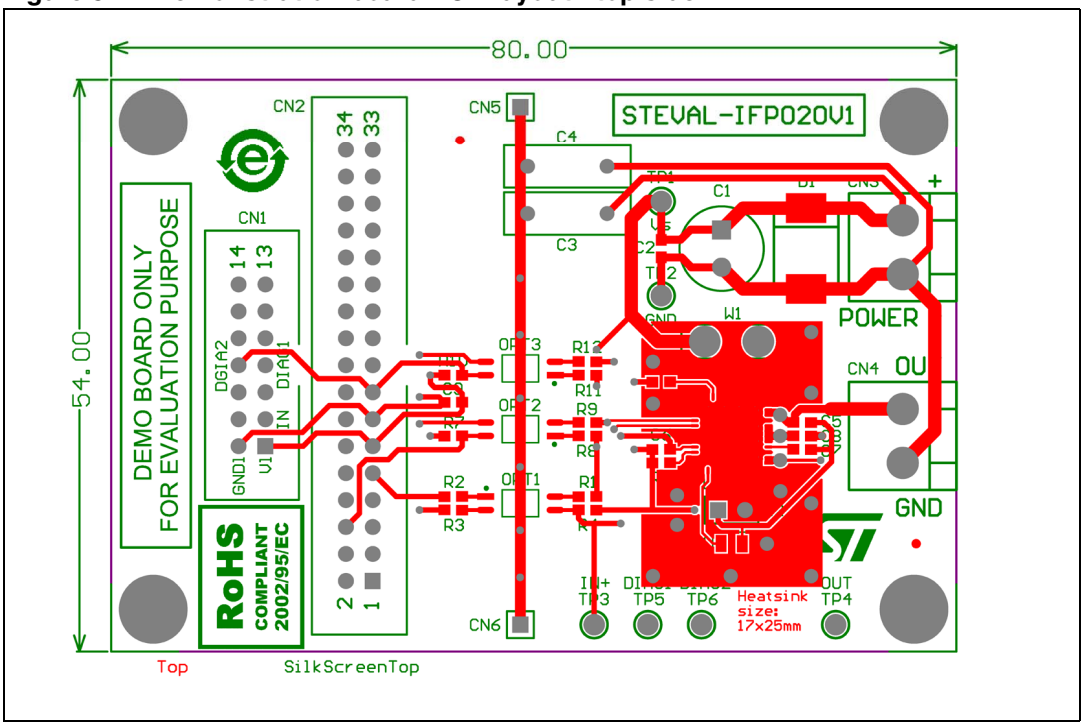
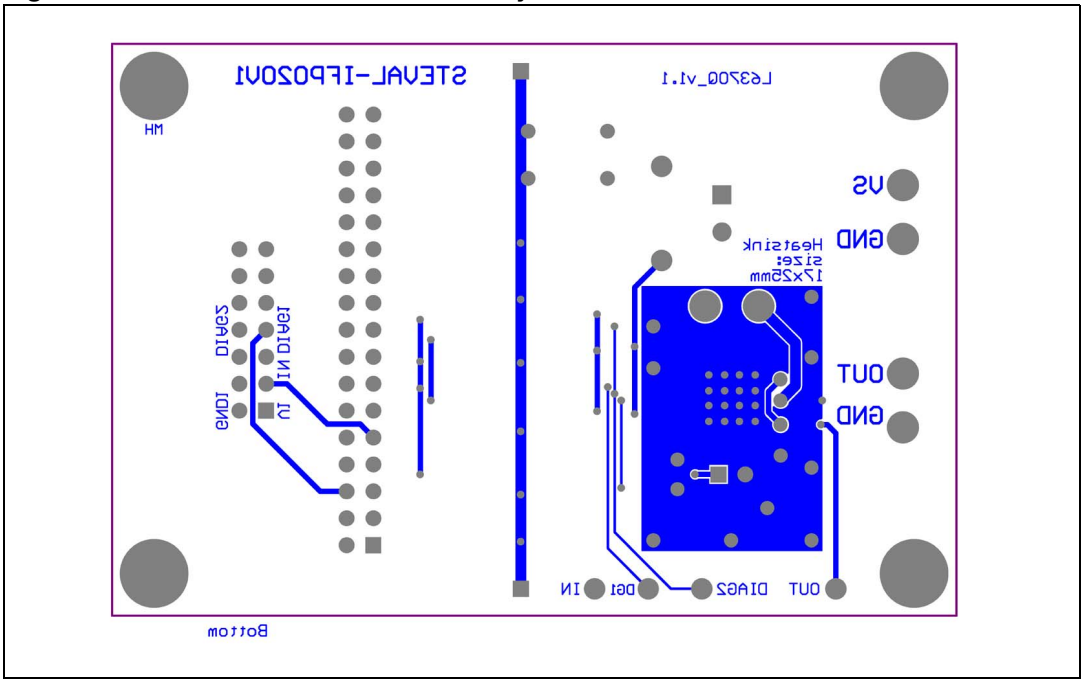


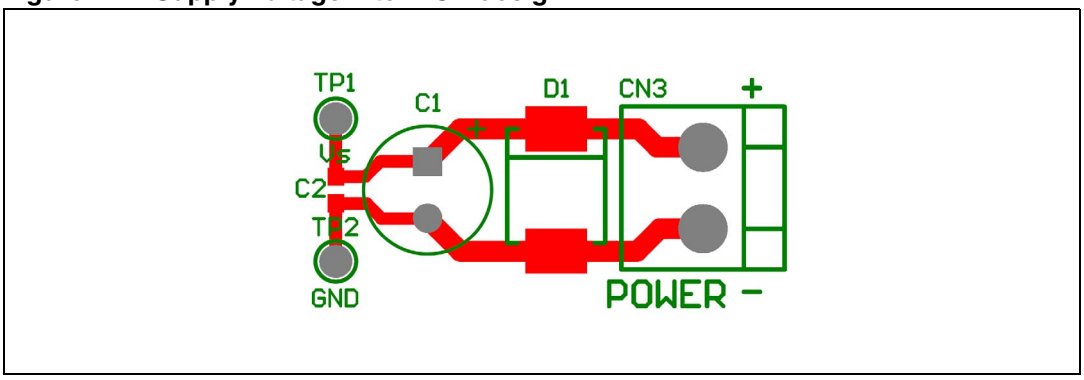
Figure 6. Demonstration board PCB layout - bottom side



2.1 Supply voltage filter layout

It is important to place the supply voltage filter components in the right order and make the routes accordingly. A correct reference is visible in *Figure 7*.

Figure 7. Supply voltage filter PCB design



The power supply is connected to CN3. The first component on the track should always be a Transil diode (D1) in order to ensure a low-impedance path to the supply connector and to minimize loop which may create electromagnetic disturbances. The next component is a large bulk capacitor (C1). Its function is to cover energetic peaks during output current transients and optimize EMI performance. The last stage of the filter is a ~100 nF ceramic capacitor (C2). Points TP1 and TP2 are central reference points for power (Vs and GND) distribution for the application.

2.2 Earth coupling

The board is equipped with a connection to earth protection line. Two high voltage coupling capacitors - C3 and C4 (4.7 nF / 3 kV) are assembled on the board. It is recommended to lead their connection tracks directly to power supply connector CN3 to suppress charge/discharge current intervention of application reference supply points (TP1, TP2). The charge/discharge currents are generated, for instance, by burst or surge noise in the environment or during EMC tests.

3 EMC requirements

3.1 Description of the procedure to evaluate the robustness of the L6370Q

The reference to evaluate the robustness of the L6370Q product is the IEC61131-2 international standard. This international standard gives all the requirements and conditions of tests that must be performed on the programmable logic controllers (PLC) and their associated peripherals.

The IEC61131-2 standard specifies the Electromagnetic Compatibility (EMC) requirements and the nature of the tests to perform in order to determine if the system meets these requirements (paragraph 7: “Electromagnetic Compatibility EMC Requirements” and paragraph 8: “Electromagnetic Compatibility (EMC) Type Tests and Verifications” of the Ed2 of the standard). The levels of each test depend on the zone where the system is installed. The most typical industrial environmental levels correspond to zone B: local power distribution zone and dedicated power distribution zone (see table 28: “EMC immunity zones” of the IEC61131-2-Ed2 standard). The following paragraphs recall the test levels for this zone.

3.2 Burst tests (according to the IEC61000-4-4)

The fast transient burst tests must be applied on all the input pins of the system.
A capacitive clamp-coupling device (50-200 pF) must be used as described in the IEC61000-4-4 standard. The required burst voltage levels are: analog or digital I/O: +/-1 kV, dc power line: +/-2 kV. The PLC system continues to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (B criterion according to the IEC61131-2 standard).

3.3 Surge test (according to the IEC61000-4-5)

Since the voltage surge consists of a single but energetic pulse, the L6370Q device embeds the appropriate protections. Moreover, additional external protection (filter) is necessary, see *Section 2.1* for an example. The absorbed energy complies at least with the requirements of the IEC61131-2 standard. The high energy surge test must be applied on all output / supply voltage terminals of the system. For all digital outputs and I/O power, the coupling method is a 42 Ω serial resistance and a 0.5 µF capacitor. The required voltage surge levels are 0.5 kV (line-to-line and line-to-earth coupling modes). The PLC system continues to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (B criterion according to the IEC61131-2 standard).

4 EMC testing

The EMC requirements according to IEC61131-2 have been verified. Application tests showed much better results than the requirements given by the industrial standard. The test results are listed in the tables below. No additional protection devices have been used in the application.

Table 1. Application EFT (burst) robustness, applied to supply voltage lines

Configuration	EFT test signal amplitude, test results at polarity (+ / -)				
	1 kV	2 kV	3 kV	4 kV	5 kV
Standard demonstration board configuration	A / A	A / A	A / A	B / B	B / B
Primary and secondary GNDs shorted	A / A	A / A	A / A	A / A	A / A

Table 2. Application EFT (burst) robustness, applied to output lines

Configuration	EFT test signal amplitude, test results at polarity (+ / -)				
	1 kV	2 kV	3 kV	4 kV	5 kV
Standard demonstration board configuration	A / A	A / A	A / A	B / B	B / B
Primary and secondary GNDs shorted	A / A	A / A	A / A	A / A	A / A

According to *Table 1* and *Table 2*, it is clear that the chosen optical isolators functionality is influenced by the burst noise. Therefore, performance criteria A is achieved with up to 3 kV burst amplitude, the system then behaves according to criteria B.

A trial has been carried out and primary and secondary GNDs have been shorted in order to limit common mode transients across the optical isolation. In this configuration the performance criteria A is fulfilled also for higher burst amplitudes.

Therefore, the application designer should choose different isolators if a higher level of immunity must be achieved. Selection should target isolators with a high CMR (“Common Mode Rejection”) parameter.

Table 3. Application surge test results, surge applied to supply lines

Configuration	Mode	Surge test signal amplitude, test results at polarity (+ / -)			
		1 kV	2 kV	3 kV	4 kV
Standard demonstration board configuration	Common (CM)	A / A	A / A	A / A	A / A
	Differential (DM)	B / B	B / B	B / B	B / B

Table 4. Application surge test results, surge applied to output lines

Configuration	Mode	Surge test signal amplitude, test results at polarity (+ / -)				
		1 kV	1.5 kV	2 kV	2.5 kV	3 kV
Standard demonstration board configuration	Common (CM)	B / B	B / B	B / B	B / B	B / B
	Differential (DM)	B / B	B / B	B / B	B / B	B / B

Table 3 and *Table 4* indicate application surge immunity. Supply voltage and output ports have been tested in common mode (CM) as well as in differential mode (DM). When surge has been applied to supply lines in common mode, the application worked without any influence, see *Table 3*. Differential mode influences the L6370Q operation due to the fact that high energy surge pulses cause short-time power interruptions on the chip supply.

Immunity of the output in differential mode depends on the supply voltage capacitive filter. Selection of the supply capacitor (C1) dramatically influences the achieved test result. Practical tests showed that applications with a low ESR (0.074 Ω) 100 µF capacitor passed 3 kV successfully and failed at -3.5 kV. The same result has been achieved with a standard 220 µF SMD capacitor (ESR = 0.18 Ω). Applications with a standard 100 µF SMD (ESR = 0.34 Ω) capacitor usually failed at -2.5 kV, and with a 47 µF SMD capacitor (ESR = 0.68 Ω), at -2 kV.

5 Ordering information

The application board is orderable in the same way as all STMicroelectronics products. The appropriate ordering code is STEVAL-IFP020V1. It contains the application board assembled according to the descriptions above, board documentation, PCB fabrication data such as Gerber files, assembly files (Pick and Place), and component documentation.

6 Conclusion

This application note may be used as a guide when designing the L6370Q application.

The document shows that the L6370Q application works in harsh environments without any problems and that the industrial standard requirements are fulfilled. Moreover, the test levels are higher than requested for the majority of final products. The L6370Q application requires a minimum amount of external components, which has a positive influence on the application costs.

Appendix A Demonstration board photo

Figure 8. Demonstration board - top view

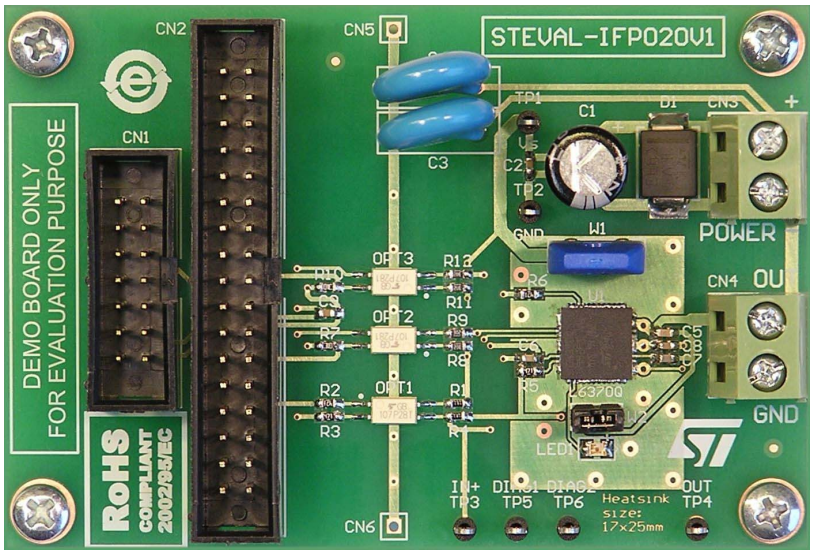
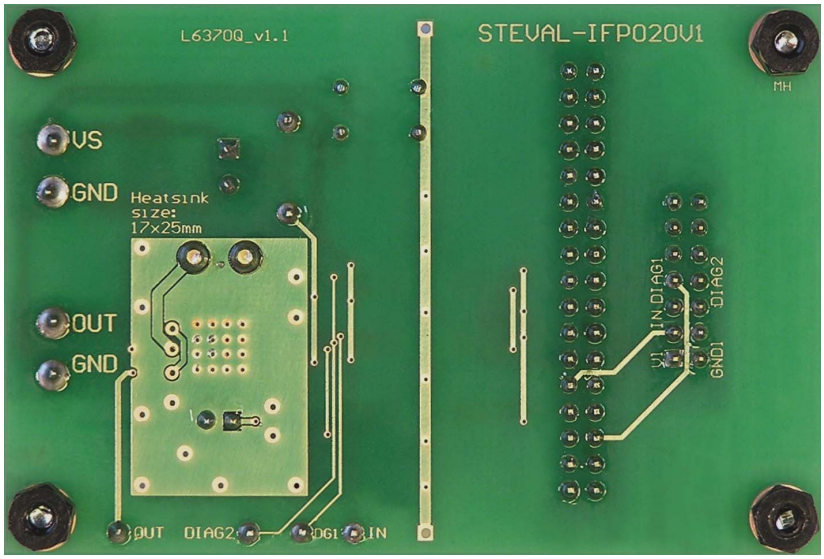


Figure 9. Demonstration board - bottom view



Appendix B Bill of material

Application components are listed in *Table 5*.

Table 5. Bill of material

Desig-nator	Quan-tity	Comment	Description	Footprint	Manufacturer / ordering code	
C1	1	100 µF / 50 V	Electrolitic capacitor	CAP D8x11.5	Rubycon	50ZL100MEFC8X11.5
C2, C8, C9	3	100 nF	Capacitor	1608[0603]	Any	
C3, C4	2	4.7 nF /3 kV	Capacitor	Cap_HV_RM7.5	Any	
C5	1	10 nF / 50 V	Capacitor	1608[0603]	Any	
C6	1	180 pF / 50 V	Capacitor	1608[0603]	Any	
C7	1	680 pF / 50 V	Capacitor	1608[0603]	Any	
CN1	1	MLW14G	Header, 14-pin, dual row, with key	MLW14G	Any	
CN2	1	MLW34G	Header, 34-pin, dual row, with key	MLW34G	Any	
CN3, CN4	2	ARK128V-A-2P	Terminal block 2-pin	MKDS1.5_2pin	Any	
CN5, CN6	2	Header 1 x 1	Header, 1-pin	HDR1X1	Any	
D1	1	SM15T36A	Transil	DIODE SMC	STMicroelectronics	SM15T36A
LED1	1	Green	LED 0805 green	2012[0805]_ TO_DIODE_reflow	Any	
OPT1, OPT2, OPT3	3	TLP281	Optocoupler	HPMF4	Any	
R1, R4	2	18 KΩ	Resistor	1608[0603]	Any	
R2, R3, R5, R6	4	470 Ω	Resistor	1608[0603]	Any	
R7, R10	2	10 KΩ	Resistor	1608[0603]	Any	
R8, R9, R11, R12	4	3.3 KΩ	Resistor	1608[0603]	Any	

Table 5. Bill of material (continued)

Desig-nator	Quan-tity	Comment	Description	Footprint	Manufacturer / ordering code	
TP1, TP2, TP3, TP4, TP5, TP6	6		Test point	Test_Point_Small	Any	
U1	1	L6370Q	Intelligent power switch	VFQFPN48_PADS	STMicroelectronics	L6370QTR
W1	1	5.08 mm	Shorting link	Shorting link 5.08 mm 10 A	Any	
W2	1	2.54 mm	Jumper	Jumper 2P 2.54 mm	Any	

References

1. L6370Q device datasheet
2. IEC61131-2: Programmable Controllers - Equipment Requirements and Tests
3. IEC61000-4-4: Electrical fast transient/burst immunity test
4. IEC61000-4-5: Surge immunity test.

Revision history

Table 6. Document revision history

Date	Revision	Changes
05-Dec-2011	1	Initial release.