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Application note

AVS kit guidelines

Introduction

The AC line voltage around the world varies widely. Power supply designers cover this problem by using a doubler/bridge switch to double the 120 V nominal AC line voltage, if the application is plugged on 120 V AC mains. In the case of operation on the 230 V AC line voltage, the doubler switch is nonactive. Thus, the input voltage of the application power supply after the rectifier bridge is always closed to the peak line voltage of the 230 V AC line whatever is the real line voltage.

The AVS kit is used to regulate the input voltage of power supplies, which are mainly switched-mode power supplies (SMPS). AVS kit still allows EMC standard compliance (inrush current limitation, conducted noise, noise immunity) as soon as a proper circuit is designed.

AVS8, AVS10, and AVS12 are automatic AC line voltage selectors used in full range switch mode power supply (SMPS). These automatic line voltage selectors are made of two devices, an integrated circuit (IC) and a customized triac. The triac automatically modifies the structure of the input diode bridge to keep the same DC voltage range thanks to the IC control.

The purpose of this document is to describe the AVS kit features and explain how to adapt the power supply to various nominal line voltages. This document also provides technical recommendations in terms of how to implement the AVS kit in the application.

1 Doubler / bridge circuit principle

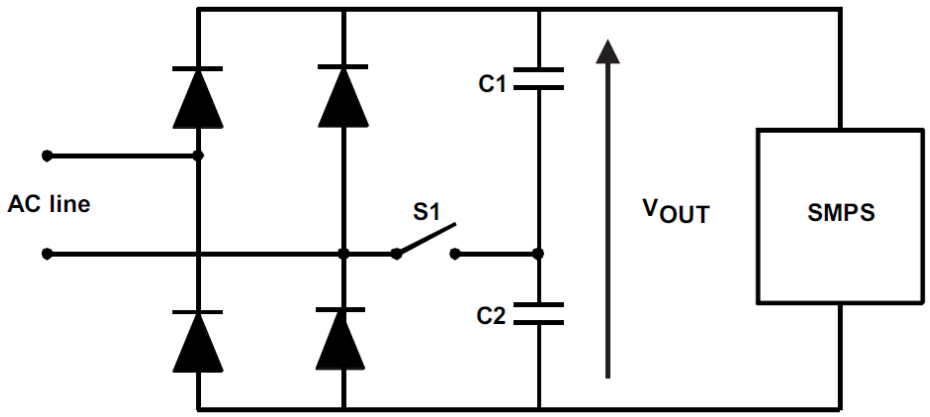
AC line voltages over the world can be divided mainly into two categories:

- 100 to 120 V nominal rms voltage, 50 Hz and/or 60 Hz systems (for example for Japan or USA). Electronic equipment is usually designed to run in the 88 to 132 V range.
- 220 to 240 V nominal rms voltage, 50 Hz and/or 60 Hz systems (for example for Europe or South Korea). Equipment has to be designed to run in the 184 to 276 V range.

The doubler/bridge circuit principle is shown in Figure 1. There are two modes according to the AC line voltage:

- **Doubler mode**: When the AC input voltage is in the 100 to 120 V range, the switch S1 is closed. During the positive half-cycle of the AC line voltage, the C1 capacitor is charged to the peak line voltage. During the negative half-cycle of the AC line voltage, the C2 capacitor is also charged to the peak line voltage. The voltage across the series association of C1 and C2 (VOUT) is then equal to approximately twice the peak line voltage.
- **Bridge mode**: When the line voltage is in the 220 to 240 V range, the switch S1 is open. C1 and C2 capacitors are simultaneously charged during each AC line half-cycle. VOUT is then around the peak line voltage thanks to the diode bridge.

Figure 1. Doubler/Bridge circuit principle



2 AVS description

2.1 Kit description

The AVS kit circuit replaces the traditional manual switch found in some appliance power supplies. This circuit eliminates SMPS failures incurred by inadvertently positioning the mechanical switch in the wrong position. This solution improves the power supply reliability with a reduced size and a low cost solution.

The AVS kit is composed of two devices:

- A triac specially designed for this application. This triac is called AVS08CB or AVS10CB orAVS12CB in a TO-220 package.
- A controller (AVS1ACP08 or AVS1BCP08) which senses the AC line voltage. This IC is optimized for low consumption and high security triggering of the triac. The IC controller is available in an eight pin DIPS package.

There are three AVS kits each dedicated to a particular power range:

- AVS08: Used for SMPS < 200 W. AVS08 is composed of an AVS1BCP08 controller and an AVS08CB triac.
- AVS10: Used for SMPS up to 300 W. AVS10 is composed of an AVS1ACP08 controller and an AVS10CB triac.
- AVS12: Used for SMPS up to 500 W. AVS12 is composed of an AVS1ACP08 controller and an AVS12CB triac.

2.2 AVS implementation

A typical application diagram for the AVS is shown in Figure 2 and Figure 3. The Figure 2 defines the application schematic with a DC resistive power supply (D1, R5, R6, C2) and the Figure 3 defines the application schematic with a capacitive power supply (D1, D2, R5, C2, C3). To reduce the standby power supply the capacitive power supply is preferred.

Component values used with the AVS kit are defined in Section Appendix A. Section Appendix B defines the printed AVS board.

The AC switch automatically modifies the structure of the input diode bridge to keep the same DC voltage range. The AVS is compatible with 50 and 60 Hz mains frequencies and operates on two mains voltage ranges:

On range I (100 to 120 V rms): The AC line rms voltage can vary from 88 to 132 V and the triac remains on. The bridge operates as a voltage doubling circuit.

On range II (220 to 240 V rms): The AC line voltage varies from 184 to 276 V and the triac is off. The circuit operates as a full wave bridge.

Figure 2. **AVS kit implementation with a DC resistive power supply**

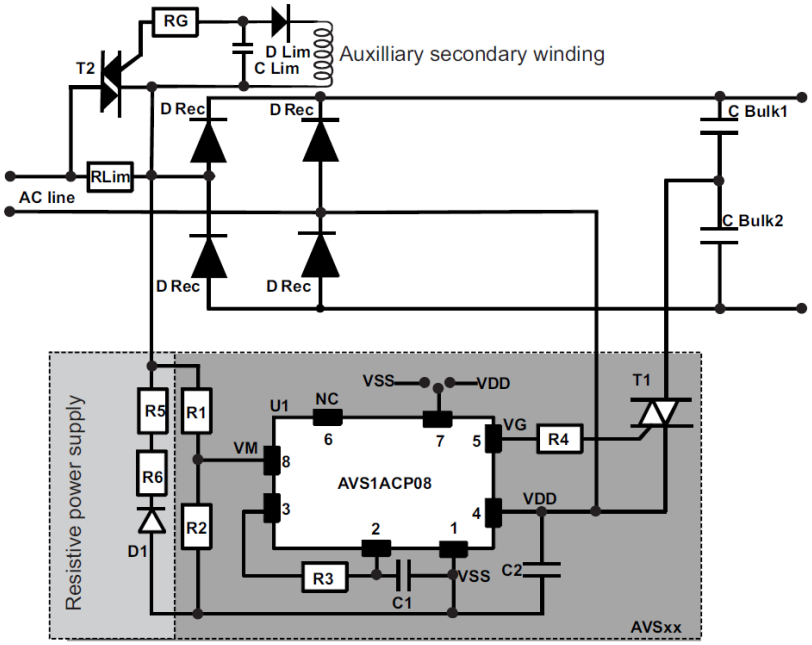
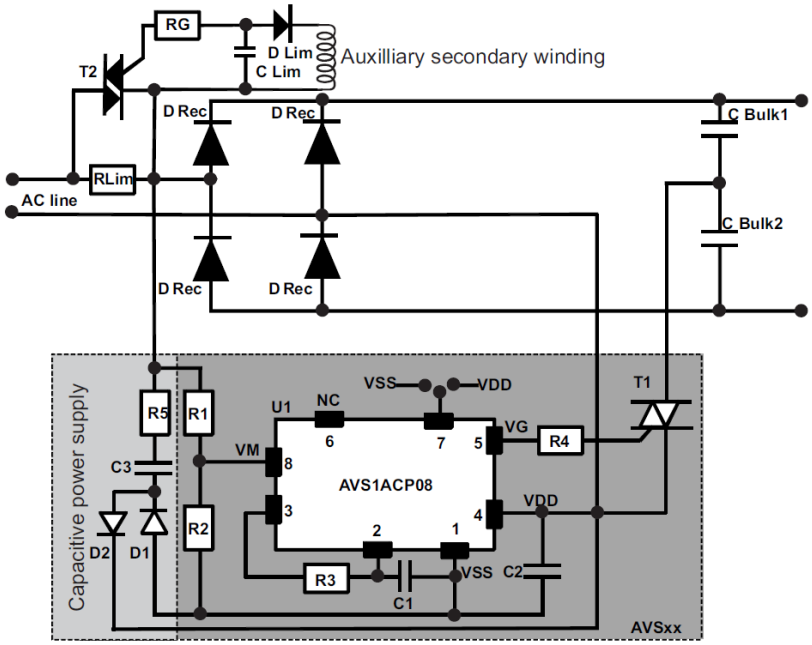


Figure 3. **AVS kit implementation with a DC capacitive power supply**



Note: *Note T2, R_G, R_{Lim}, C_{Lim}, and D_{Lim} are components, which define the inrush current limiter circuit. A non-sensitive T2 triac must be used to ensure a good dV/dt characteristic. The R_{Lim} resistor is short-circuited by the triac just after the power supply is started. This to limit the power losses of the power supply compare to the classical solution with the NTC thermistor.*

2.3 IC power supply

The DC power supply of the AVS can be implemented with a DC resistive or a capacitive power supply. The series circuit D1, R5, R6, and C2 define the DC resistive power supply (see Figure 2). The series circuit D1, D2, R5, C3, and C2 define the DC capacitive power supply (see Figure 3). To reduce the standby power supply, a DC capacitive power supply is preferred.

Pin 1 of the AVS IC, V_{SS}, is a shunt regulator that provides a -9 V (typ.) Output. The structure of the supply regulator is a shunt regulator and its current must be lower than 30 mA. To have good behavior of the circuit against mains voltage spikes, pin 4 (V_{DD}) of the integrated circuit has to be connected directly with A1 of the triac.

Eq. (1) and Eq. (2) define respectively R5 and R6 resistors value for the DC resistive power supply and C3 capacitor value for the capacitive power supply.

I_{CI} is the average current supplied to the IC in doubler mode. As the triac gate current is pulsed, the I_{CI} is equal to 3 mA.

$$\left(R_5 + R_6\right) = \frac{V_{RMS_Min} \cdot \sqrt{2}}{I_{CI} \cdot \pi} \quad (1)$$

$$C_3 = \frac{1}{2\pi \cdot F_{Min} \cdot \sqrt{\left(\frac{V_{RMS_Min} \cdot \sqrt{2}}{I_{CI} \cdot \pi}\right)^2 - (R_5)^2_{Max}}} \quad (2)$$

Eq. (3) and Eq. (4) define the power dissipated respectively by the DC resistive and capacitive power supply without considering the losses through the diode and the AVS IC voltage regulator.

$$P_{R_Max} = \frac{\left(V_{RMS_Max}\right)^2}{2 \cdot (R_5 + R_6)Min} \quad (3)$$

$$P_{C_Max} = (R_5)_{Max} \cdot \frac{\left(V_{RMS_Max}\right)^2}{(R_5)^2_{Min} + \frac{1}{\left(2 \cdot \pi \cdot F_{Max} \cdot C_{3_Max}\right)^2}} \quad (4)$$

Where:

- F is the AC line frequency
- R5 and R6 are the supply resistors for the DC resistive power supply
- R5 the inrush limiter for the DC capacitive power supply
- V_{RMS_Min} the minimum rms AC line voltage
- C2 the bulk capacitor
- C3 the supply capacitor for the DC capacitive power supply

Table 1 gives the components value of the DC resistive and capacitive power supplies whatever the AC line voltage value.

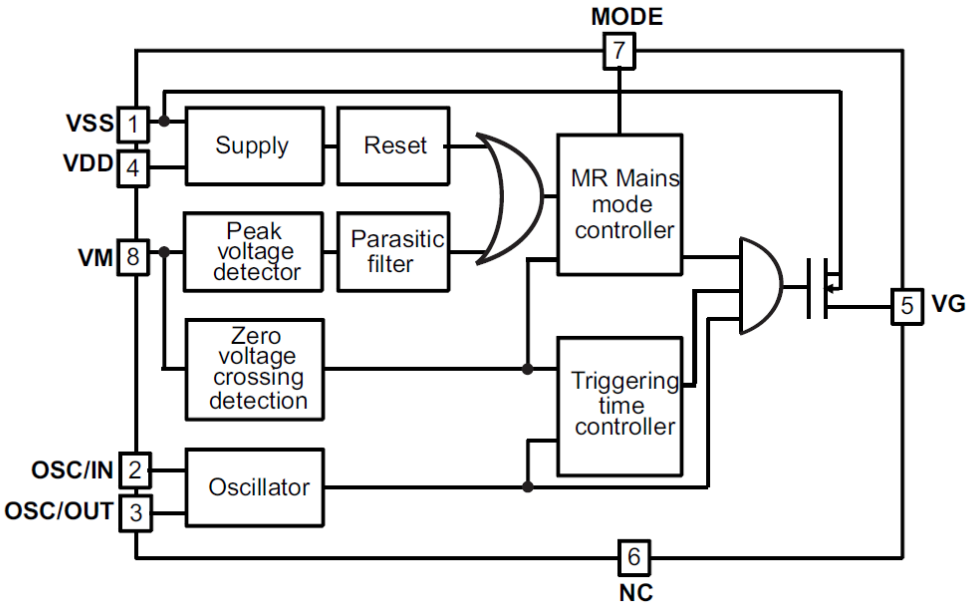
Table 1. DC resistive and capacitor power supply components value

DC power supply	R5	R6	C2	C3
Resistive	9.1 kΩ at 5% 1 Watt	9.1 kΩ at 5% 1 Watt	33 µF at 16 V 10%	Not applicable
Capacitive	100 Ω at 5% 2 Watt	Not applicable	33 µF at 16 V 10%	220 nF at 400 V AC X2

2.4 AVS block description

The Figure 4 shows the block diagram of the AVS IC. Advantages of this AVS integrated circuit are ease of circuit design, lower power dissipation, a smaller component count, and additional safety features.

Figure 4. AVS block diagram



2.4.1 Parasitic filter

The Triac of the AVS kit is a sensitive gate Triac specified to remain off when subjected to dV/dt of 50 V/µs. Circuit layout is critical in preventing false dV/dt turn on of the Triac. The IC of the AVS kit circuit has a built in digital filter that suppresses the effect of all spikes of less than 200 µs duration.

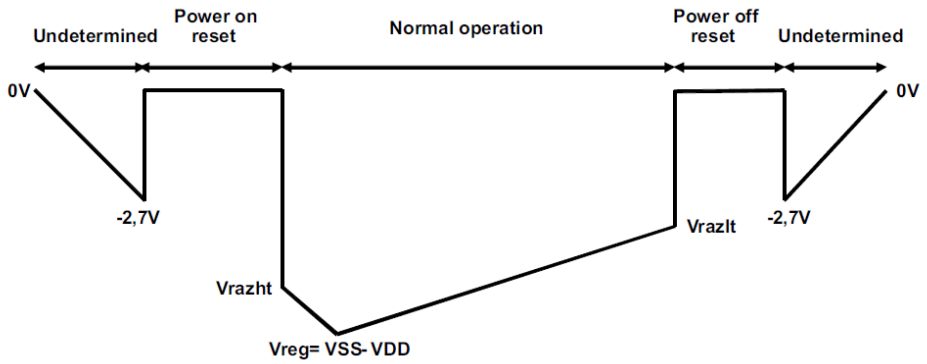
2.4.2 Gate current pulses

Pin 5 drives the gate of the Triac through a 390 Ohm resistor. The gate current is made up of a pulse train with a 230 µs period and a 23 µs pulse width. The duty cycle of the pulses is typically 10%. The period and pulse width of the gate current is controlled by the oscillator and set by R3 / C1.

2.4.3 AVS start-up

The triac triggering is valid (on range I) after the validation of power-on reset (charge of supply capacitor C) and a delay of eight mains periods (see Figure 5) to permit the charge of the bulk SMPS input capacitors (C1 and C2) and to ensure that the AC line voltage is stable on range II.

Figure 5. Power on reset description



Eq. (5) and Eq. (6) define the delay time between the power on and the triac triggering respectively with a resistive (Figure 2) and capacitive power supply (Figure 3).

This time takes into account the time to DC power supply output reaches the power on reset activation voltage (V_{razht} = 0.89 • V_{reg}) of the IC control and the delay of eight mains periods.

$$td_{\mathrm{Resistive}} = \left(\frac{0.89 \cdot V_{reg} \cdot \left(R_5 + R_6\right) \cdot C_{2_\mathrm{Max}}}{\left(V_{RMS_\mathrm{Min}} \cdot \frac{\sqrt{2}}{\pi}\right) - \left(\left(R_5 + R_6\right) \cdot I_{ss_qc}\right)} \right) + \left(\frac{8}{F_{\mathrm{Min}}} \right) \quad (5)$$

$$td_{Capacitive} = \left(\frac{0.89 \cdot V_{reg} \cdot \cdot C_{2_\mathrm{Max}}}{\left(\frac{V_{RMS_Min}}{\sqrt{R_{5_\mathrm{max.}}^2 + \frac{1}{\left(2 \cdot \pi \cdot C_{3_\mathrm{Min}}\right)^2}}} \cdot \frac{\sqrt{2}}{\pi} \right) - I_{ss_qc}} \right) + \left(\frac{8}{F_{\mathrm{Min}}} \right) \quad (6)$$

With:

- F the AC line frequency
- R5 and R6 the supply resistors for the DC resistive power supply
- R5 the inrush limiter for the DC capacitive power supply
- V_{RMS_Min} the minimum rms AC line voltage
- C2 the bulk capacitor
- V_{reg} the voltage regulated
- I_{SS_qc} the quiescent supply current of the AVS circuit = 0.7 mA

With the component values define in Section Appendix A or in Table 1, the delay time is around 250 ms for a DC resistive and a capacitive power supply in the worst case.

2.4.4 AC line voltage detection

The triac control is implemented through a comparison of the AC line voltage (V_M on pin 8) with an internal threshold voltage (V_{TH}). When the AC mains voltage increases from range I to range II the triac gate current is removed. The doubler circuit is turned off within one mains period (the triac can only turn off when its current reach zero). That means the delay between line voltage increase and doubler circuit turn-off can reach up to 16.7 ms or 20 ms respectively for 60 and 50 Hz operations.

Eq. (7) defines the condition on the voltage across the pin 8 of the IC control to remove the triac gate pulses (bridge mode). Eq. (8) defines the condition on the voltage across the pin 8 of the IC control to apply the triac gate pulses (doubler mode).

$$V_M > V_{TH}\,(V_{thres1}) \tag{7}$$

$$V_M < V_{TH} - V_H\,(V_{thres2}) \tag{8}$$

With V_{TH} typ. = 4.25 V and V_H typ. = 0.4 V

When the mains voltage drops from range II to range I, there are two options according to to the pin 7 level. Typical timing diagrams for the two modes are given in Figure 6 and Figure 7.

1. V_{Mode} (pin 7) = V_{DD}: The triac triggering pulse is activated eight AC line periods after the power on reset of the IC and if a low line voltage is sensed. If the AC line voltage changes from typically 110 V to 230 V, then the AVS circuit turns the triac off. If the AC line voltage changes back from 230 V to 110 V, the AVS IC controller waits eight mains cycles before to turn the triac on (see Figure 6). This is done to check if the AC line voltage is a stable 110 V value and that the voltage reduction is not a short voltage dip.
2. V_{Mode} (pin 7) = V_{SS}: The triac control remains locked to range II until the circuit is reset. This means that if the device is turned into a bridge mode, it remains in the bridge mode, even if the AC line voltage suddenly dips into the 110 V range (see Figure 7).

Figure 6. Timing diagram with V_{mode} (pin 7) = V_{DD}

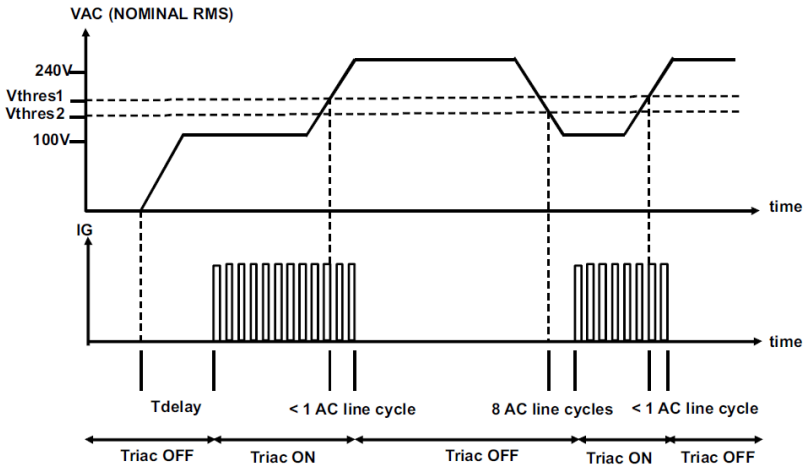
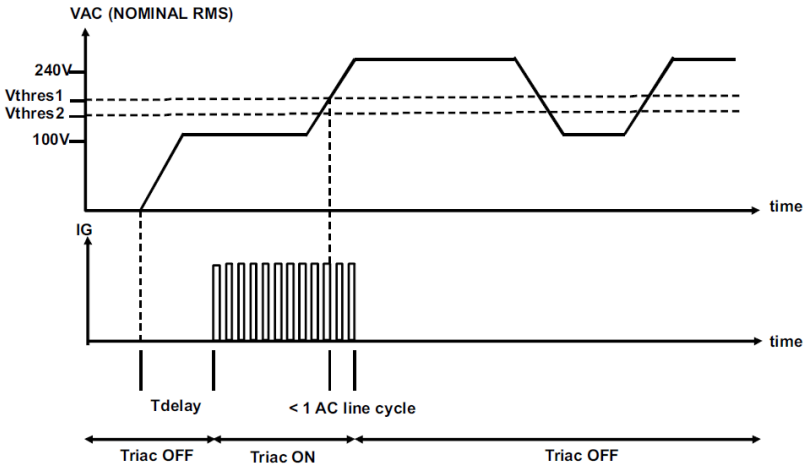


Figure 7. **Timing diagram with V_{mode} (pin 7) = V_{SS}**



The AC line voltage measurement is implemented through the detection of the AC line peak voltage. R1 and R2 resistor values are defined according to Eq. (9), Eq. (10) and Eq. (11).

Eq. (9) defines the condition for R1 and R2 resistors to limit the power dissipation and to improve the AC line voltage measurement.

$$800\ k\Omega < R_1 + R_2 < 2\ M\Omega \tag{9}$$

Eq. (10) defines R1 and R2 resistors to switch from doubler operation to bridge operation (from range I to range II).

$$\frac{R_1}{R_2} = \left(\left(Max\ \text{rms voltage on range I} - \frac{V_{REG}}{\sqrt{2}}\right) \cdot \frac{\sqrt{2}}{V_{TH}}\right) - 1 \tag{10}$$

Where:

- V_{REG} typ = -9 V
- V_{TH} typ = 4.25 V

Eq. (11) defines R1 and R2 resistors to switch from bridge operation to doubler operation (from range II to range I).

$$\frac{R_1}{R_2} = \left(\left(Max\ \text{rms voltage on range II} - \frac{V_{REG}}{\sqrt{2}}\right) \cdot \frac{\sqrt{2}}{V_{TH} - V_H}\right) - 1 \tag{11}$$

Where:

- V_{REG} typ = -9 V
- V_{TH} typ = 4.25 V
- V_H typ = 0.4 V

For rms voltage on range, I (110 V) and II (230 V) R2 and R1 resistor values are respectively 18 kΩ and 1 MΩ at 1%.

3 Thermal rating of triac

The knowledge of the maximum triac current ITM and the current pulse width tp in the worst Case conditions allow the definition of the triac power dissipation (see Eq. (12) and Eq. (13)).

Where:

- I_{TRMS} is the rms triac current
- V_{t0} the threshold voltage of the triac
- R_t the on-state of the triac
- F the AC line frequency.

$$P_T = 4 \cdot t_P \cdot F \cdot IT_M \cdot \frac{V_{to}}{\pi} + \left(R_t \cdot t_P \cdot F \cdot (TT_{TM})^2\right) \quad (12)$$

With

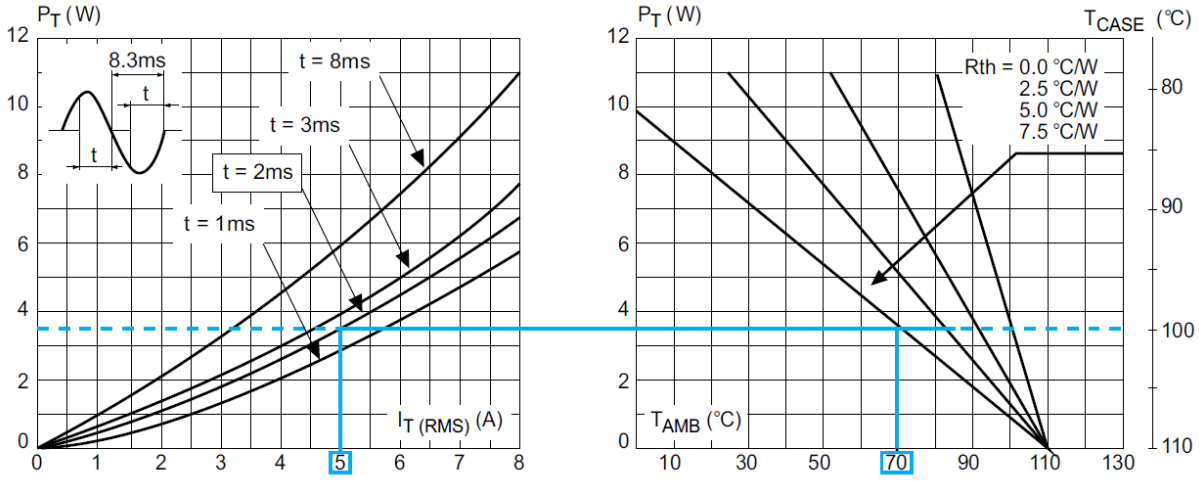
$$IT_{RMS} = IT_M \cdot \sqrt{t_P} \cdot \sqrt{F} \quad (13)$$

Eq. (14) and Eq. (15) define the junction temperature of the triac according to the ambient to junction thermal resistance and case to junction thermal resistance.

$$T_J - T_C = R_{TH(j-c)AC} \cdot P_T \quad (14)$$

$$T_C - T_{amb} = R_{TH(c-a)} \cdot P_T \quad (15)$$

Figure 8. AVS thermal management



For example, the Figure 8 (left) gives losses P_T versus IT_{RMS} for this application dedicated for the AVS10CB triac. Figure 8 (right) allows the evaluation of the external heat sink R_{TH} versus P_T and T_{amb} when T_j = 110 °C for the same triac. These curves come from Eq. (10), Eq. (11), Eq. (12), and Eq. (13).

For example, with an AVS10CB triac, if t_p = 2 ms and I_{TRMS} = 5 A then the triac dissipated power P_T = 3.8 W. If the maximum junction temperature is T_j = 110 °C and the maximum case temperature T_c = 100 °C with a heatsink thermal resistance $R_{TH(c-a)}$ = 7.5 °C/W, then the maximum operating ambient temperature (T_a) could be 70 °C.

4 Conclusion

This paper describes an efficient way of implementing an automatic doubler/bridge circuit.
The primary use of this circuit is in 75 W to 500 W SMPS. Other innovative uses are possible.
The main advantages of the AVS solution are:

- High efficiency: Losses are just 2 W vs. 5 to 10 W for discrete schemes
- Safety: Uses digital spike suppression, hysteresis, validation of range, a failsafe mode, and good control
- Space optimization: Small supply resistor and good reliability
- Ease of use: Eliminates errors when the line range has to be selected manually by the end user
- Available solutions for various power ranges:
  - AVS08 < 200 W
  - AVS10 up to 300 W
  - AVS12 up to 500 W

Appendix A AVS bill of material

Table 2. **AVS bill of material**

Components		Qty.	Reference	Observations	Supplier
Resistor		1	R1	1 MΩ at 1%	ND
Resistor		1	R2	18 kΩ at 1%	
Resistor		1	R3	91 kΩ at 1%	
Resistor		1	R4	390 Ω at 5%	
Resistor	DC resistance power supply	1	R5	9.1 kΩ at 5%, 1 W	
	Capacitive power supply	1		100 Ω□at 5%, □□W	
Resistor	DC resistance power supply	1	R6	9.1 kΩ at 5%, 1 W	
	Capacitive power supply	1		Not applicable	
Capacitor		1	C1		
Capacitor		1	C2		
Capacitor	Resistance power supply	0	C3	100 pF at 5%, 16 V	
	Capacitive power supply	1		33 µF at 10%, 16 V	
Diode		1	D1	Not applicable	
Diode	Resistance power supply	0	D2	220 nF at 400V AC X2	
	Capacitive power supply	1		1N4007	
Triac		1	IC2	AVS10CB / AVS12CB	STMicroelectronics
Integrated circuit		1	IC1	AVS1ACP08	

Appendix B Printed AVS circuit with a resistive power supply

Figure 9. **Product pinouts**

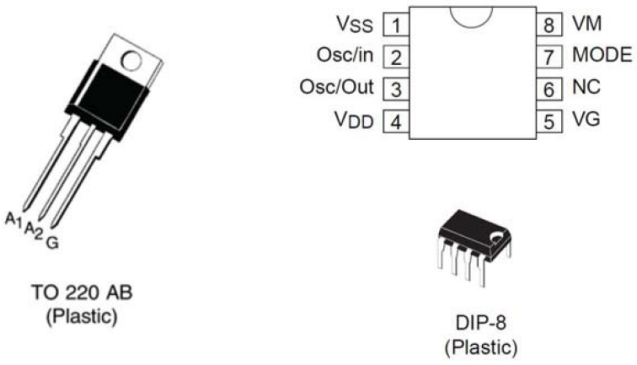


Figure 10. **Component layout**

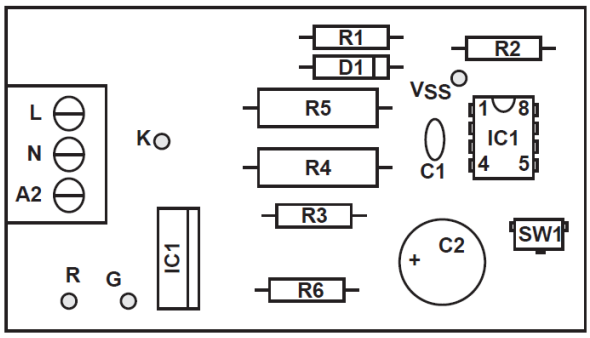
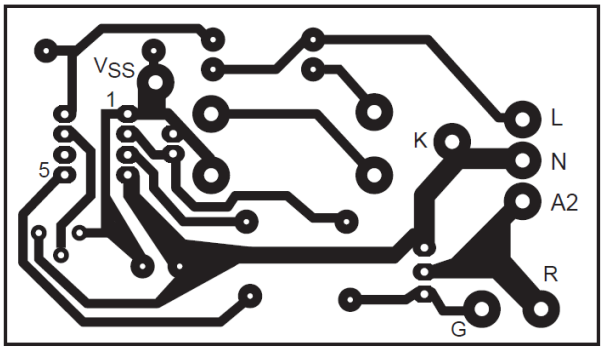


Figure 11. **Printed circuit layout (copper side) 1:1 scale**



Revision history

Table 3. **Document revision history**

Date	Revision	Changes
October-1990	1	First issue.
10-May-2004	2	Style sheet update. No content change.
09-Jun-2009	3	Updated *Figure 1*, F*igure 10*, *Figure 11,* and T*able 1*. Reformatted to current standards.
09-Jan-2015	4	Added information on doubler/bridge circuit principle, IC power supply design, design and operation of the AVS IC, and the thermal rating of the Triac.Added AVS08.
18-Dec-2015	5	Updated *Chapter 2.4.2*.
25-Jan-2017	6	Updated *Equation 4*, *Equation 10*, *Equation 11* and *Table 2*.
15-Dec-2023	7	Document reworked to improve readability. No content changes.

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