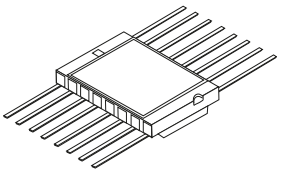
# Minimizing the SET-related effects on the output of a voltage linear regulator

## Introduction

This application note deals with the effects of SET (single event transient) on the RHFL4913A low-drop linear regulator. After a short description of the phenomenon, some solutions for coping with these effects are introduced and discussed.

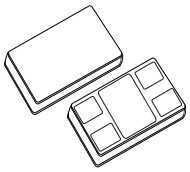
The RHFL4913A voltage regulator is an adjustable high-performance positive voltage regulator with exceptional radiation performance. It is tested in accordance with the Mil Std 883E method 1019.6, in ELDRS conditions. The device is available in the FLAT-16 and the new SMD5C hermetic ceramic package, as shown in the images below, and the QML-V die is specifically designed for space and harsh radiation environments.

**Figure 1. FLAT-16**



FLAT-16

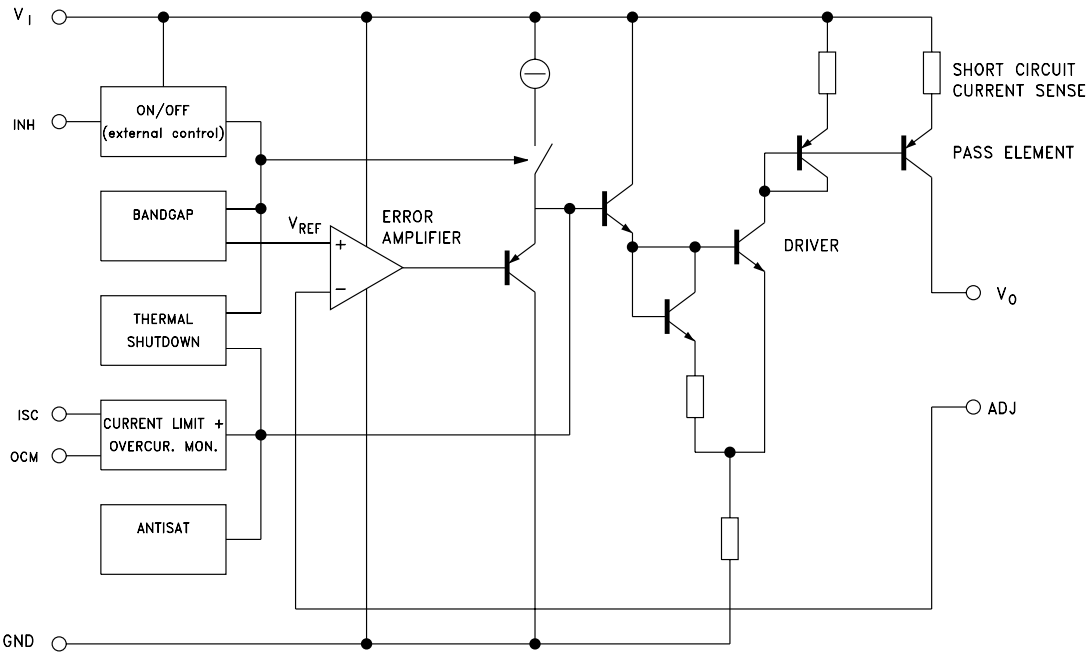
**Figure 2. SMD5C**



SMD5C
5-connection SMD

# 1 Block diagram

Figure 3. **Internal block diagram**




The RHFL4913A operates with an input supply of up to 12 V. To adjust the output voltage, the R2 resistor must be connected between the $V_O$ and ADJ pins. The R1 resistor must be connected between the ADJ and ground. Resistor values can be derived from the following equation:

$$V_O = V_{ADJ}\,(R1 + R2)/R1 \quad (1)$$

The $V_{ADJ}$ is 1.23 V, controlled by the internal temperature-compensated band-gap block.

The minimum output voltage is therefore 1.22 V and the minimum input voltage is 3 V. The adjustable RHFL4913A is functional as soon as the ($V_I$ - $V_O$) voltage difference is slightly above the power element saturation voltage. The ADJ pin to ground resistor value must not be greater than 10 kΩ, in order to keep the output feedback error below 0.2 %. A minimum of 0.5 mA $I_O$ must be set to ensure perfect no-load regulation. It is advisable to dissipate this current into the divider bridge resistor. All available $V_I$ pins, as well as all available $V_O$ pins, should always be externally interconnected, otherwise the stability and reliability of the device cannot be guaranteed. The inhibit function switches off the output current electronically, and therefore very quickly.

According to Lenz's Law, external circuitry reacts with Ldi/dt terms, which can be of high amplitude where a serial coil inductance exists. Large transient voltage would develop on both device terminals. It is advisable to protect the device with Schottky diodes to prevent negative voltage excursions. In the worst case, a 14 V Zener diode can protect the device input. The device has been designed for high stability and low dropout operation. Therefore, tantalum input and output capacitors with a minimum 1 µF are mandatory.

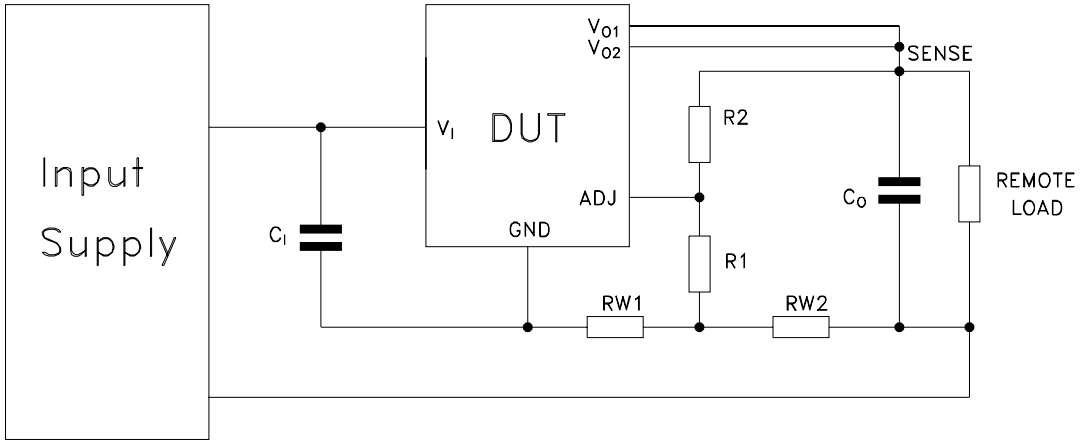
The ESR capacitor range is from 0.01 Ω to over 20 Ω . This range is useful when ESR increases at a low temperature. When large transient currents are expected, larger value capacitors are necessary. In the case of high current operation with short circuit events expected, caution must be exercised with regard to capacitors. They must be connected as close as possible to the device terminals. As some tantalum capacitors may permanently fail when subjected to high charge-up surge currents, it is recommended to decouple them with 470 nF polyester capacitors.

As the RHFL4913A adjustable voltage regulator is manufactured with very high speed bipolar technology (6 GHz fT transistors), the PCB layout must be designed with exceptional care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation. The benefit is an SVR performance extended to far higher frequencies.

In order to replace a standard 3-terminal industry device, fixed voltage versions areavailable.

A separate Kelvin voltage sensing line provides the ADJ pin with exact load “high potential” information. But variable remote load current consumption induces variable Iq current (Iq is roughly the $I_{OUT}$ current divided by the $h_{FE}$ of the internal PNP series power element) routed through the parasitic series line RW2 resistor. To compensate for this parasitic voltage, an RW1 resistor can be introduced to provide the necessary compensating voltage signal to the ADJ pin, as shown in figure below.

**Figure 4. Application schematic for remote load operation**




In the case of an FPGA power supply, as these devices are very sensitive to VDD transients beyond a small percentage of their nominal supply voltage (usually 1.5 V), special attention must be taken to mitigate possible heavy-ion disturbances. The worst case heavy-ion effect can be summarized as the following: the RHFL4913A internal control loop being cut (opened) or short-circuited for a sub-microsecond duration. During such an event, the RHFL4913A die power element can either provide excessive current or current supply stoppage to the output ($V_{OUT}$) for a duration of about one microsecond, after which time the voltage regulator smoothly recovers to nominal operation. To mitigate these “transients”, it is recommended to firstly implement the PCB layout using the following notes:

- Minimizing series/parallel parasitic inductances of the PC path;
- Using a low ESR 47 µF tantalum $V_{OUT}$ filtering capacitor with a 470 nF ceramic capacitor in parallel with the former (to reduce dynamic ESR);

With this implementation, the ELDO simulated worst transient case shows no more than a 90 mV deviation from the nominal line voltage value.

# 2 Mitigation technique for SET

As we know, the characteristics of the voltage transient on the output of a voltage regulator, consequent to the transfer of energy related to an ion strike with the silicon, is a critical issue in space applications. Large undershoot can cause erratic operations in memories and microprocessors, while overshoot of an excessive amplitude can lead to the degradation - or even the destruction - of CMOS devices. For example, for most FPGA the recommended operating voltage is 1.5 V with 1.6 V the maximum limit (in some applications it is restricted to 1.575 V to maintain a further safety margin). The latter applies to both static and dynamic operating conditions.

The recommendations in this application note are based on the outcomes of an experimental analysis conducted at Texas A&M University (Cyclotron Single Event Effects Test facility on device behavior in a heavy ion environment). For more information please refer to “SEE test report V3.0 - Heavy Ion SEE test of RHFL4913A from STMicroelectronics with SET mitigation circuitry”, issued by NASA on November 18th, 2006.

During these experiments, the configurations, illustrated in Figure 5 and Figure 6, were found capable of reducing the SET transient's characteristics on the voltage regulator output at a level acceptable for most critical applications, e.g. FPGA supply.

**Figure 5. Baseline bias configuration with remote feedback**

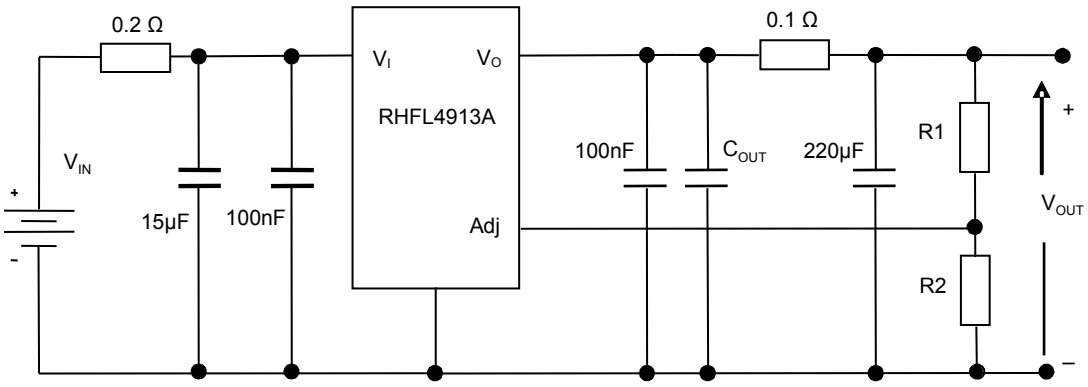
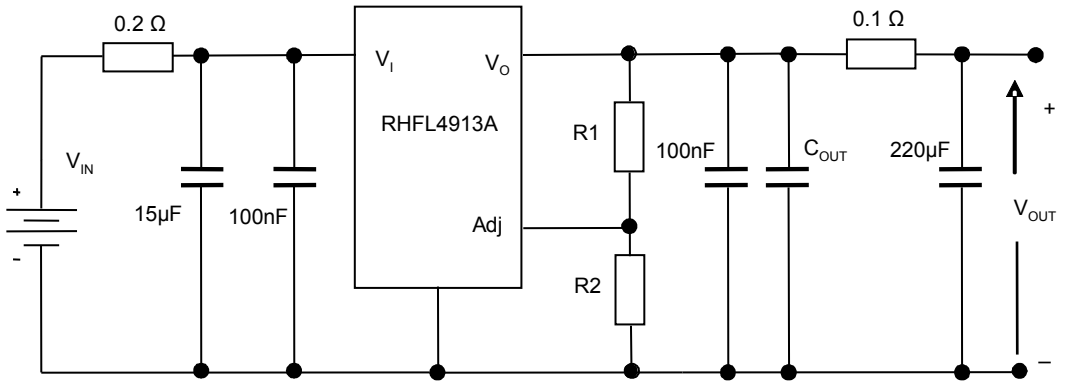



**Figure 6. Local feedback configuration**



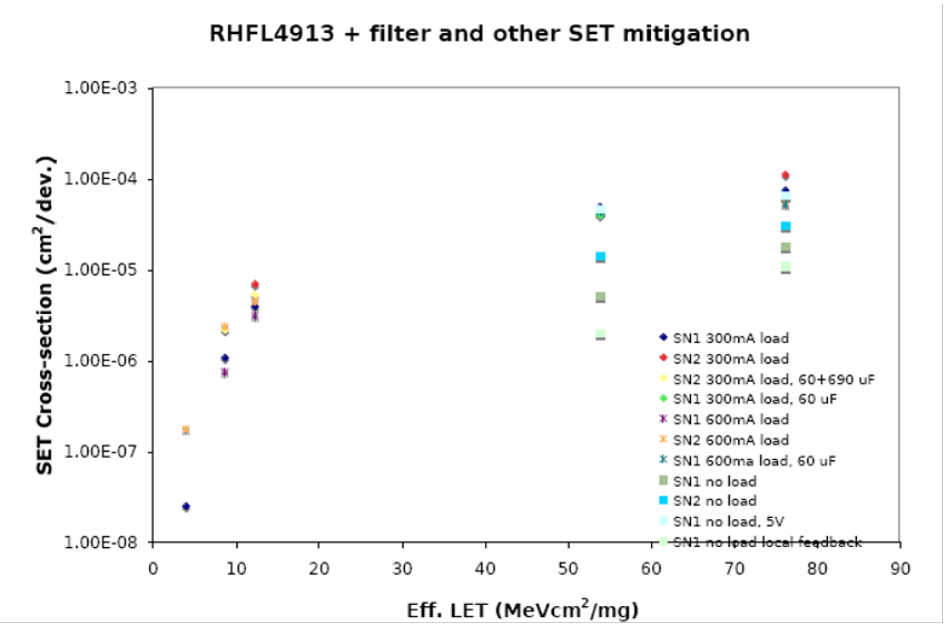

Each of the two options has its own advantages and drawbacks. In the scheme shown in Figure 5, as the R resistor is located between the voltage regulation output and the output voltage setting resistors, the regulation - especially with the load - is expected to be much better and thus the output voltage more precise compared to the second option; the latter option should have superior SET immunity.

For both configurations, the characteristics of the transients can be summarized as follows:

1. In many of the SETs observed, both short (< 100 nsec) and long-duration (max 2 µsec) pulses are present;
2. SET cross-section increases with the LET, as expected;
3. SETs associated to the highest LET are those with the longest transients (provided the other conditions are the same);
4. Irrespective of the LET, at a fixed $V_{IN}$ = 3.3 V the max $V_{OUT}$ deviation measured is < 140 mV, using high-quality, low-ESR, low-ESL capacitors, (i.e., ceramic or tantalum); higher ($V_{IN}$-$V_{OUT}$) dropout increases the max $V_{OUT}$ excursion;
5. The short-duration pulses are mostly dependent on the ESL of the capacitors used, and also dependent on the stray inductances. Therefore, they cannot be suppressed by simply increasing the cap value. The only way to minimize them is with an action at board level.
6. In the scheme of Figure 5, all long-durat es can be suppressed by adding a capacitor of at least 60 µF before the filter.

Even the SET cross-section is limited, at least for LET up to 53 Mev*cm²/mg, as shown in figure below.

**Figure 7. SET cross-section vs. LET diagram**




As can be seen, the best solution recommended in critical applications is the one given in Figure 5, with an additional capacitor of at least 60 µF connected before the RC filter.

Finally, some additional recommendations in order to minimize the output voltage glitches:

- Use low ESR (< 30 mΩ), low ESL (10 - 20 nH) ceramic capacitors or others rated for high speed applications.
- ESL can be reduced using an array of parallel capacitors.
- GND: implement star bus topology or a plane.
- $C_{IN}$ as close to $V_{IN}$ - GND pads as possible.
- A 10 nF cap between OUT and ADJ runs as an effective noise filter and improves stability; it is essential in remote sensing configuration.

In conclusion, most SETs can be mitigated by means of external components: input and output resistors, output series Schottky diodes, and RC filters, resulting in greatly reduced SET sensitivity and remaining SETs with small amplitude (below 200 mV) and short duration (< 20 ns).

## Revision history

Table 1. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 23-Jun-2010 | 1 | Initial release. |
| 13-Apr-2021 | 2 | Updated Section 2 Mitigation technique for SET. |

# Contents

# List of figures