AN2798
Application note

Complete DDR2/3 memory power supply controller based on the PM6670AS

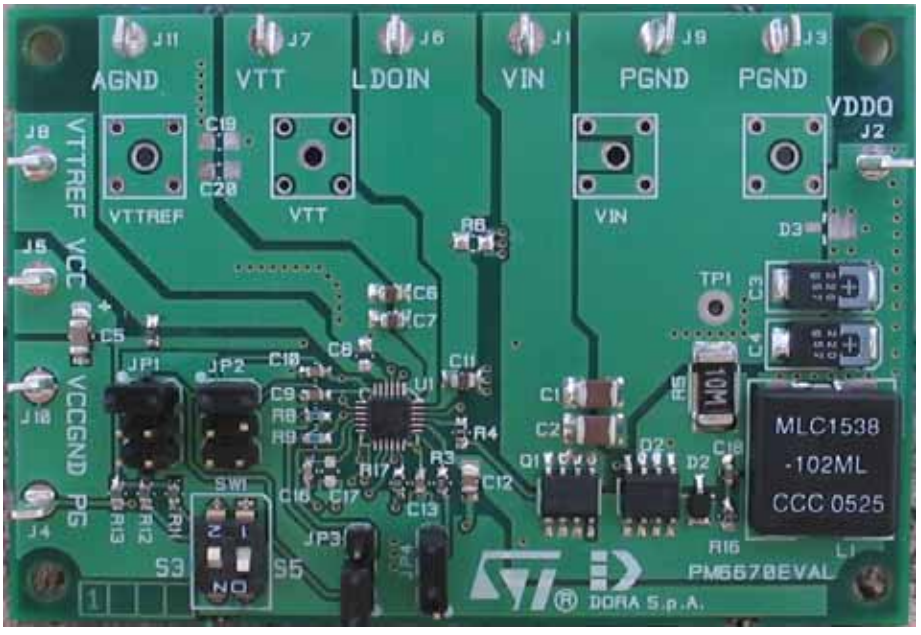
Introduction

The PM6670AS device is a complete DDR2/3 power supply regulator for portable applications designed to meet JEDEC specifications. It integrates a constant on-time (COT) buck controller, a 2 A peak sink/source low dropout regulator and a 15 mA low-noise buffered reference.

The COT architecture assures fast transient response supporting both polymeric and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple. The 2 A peak sink/source linear regulator provides the memory termination voltage with fast load transient response.

The device is fully compliant with system sleep states S3 and S4/S5, setting the LDO output to high impedance in suspend-to-RAM state and performing the tracking discharge of all outputs in suspend-to-disk state.

Figure 1. PM6670AS demonstration board



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1 Main features

1.1 Switching section (VDDQ)

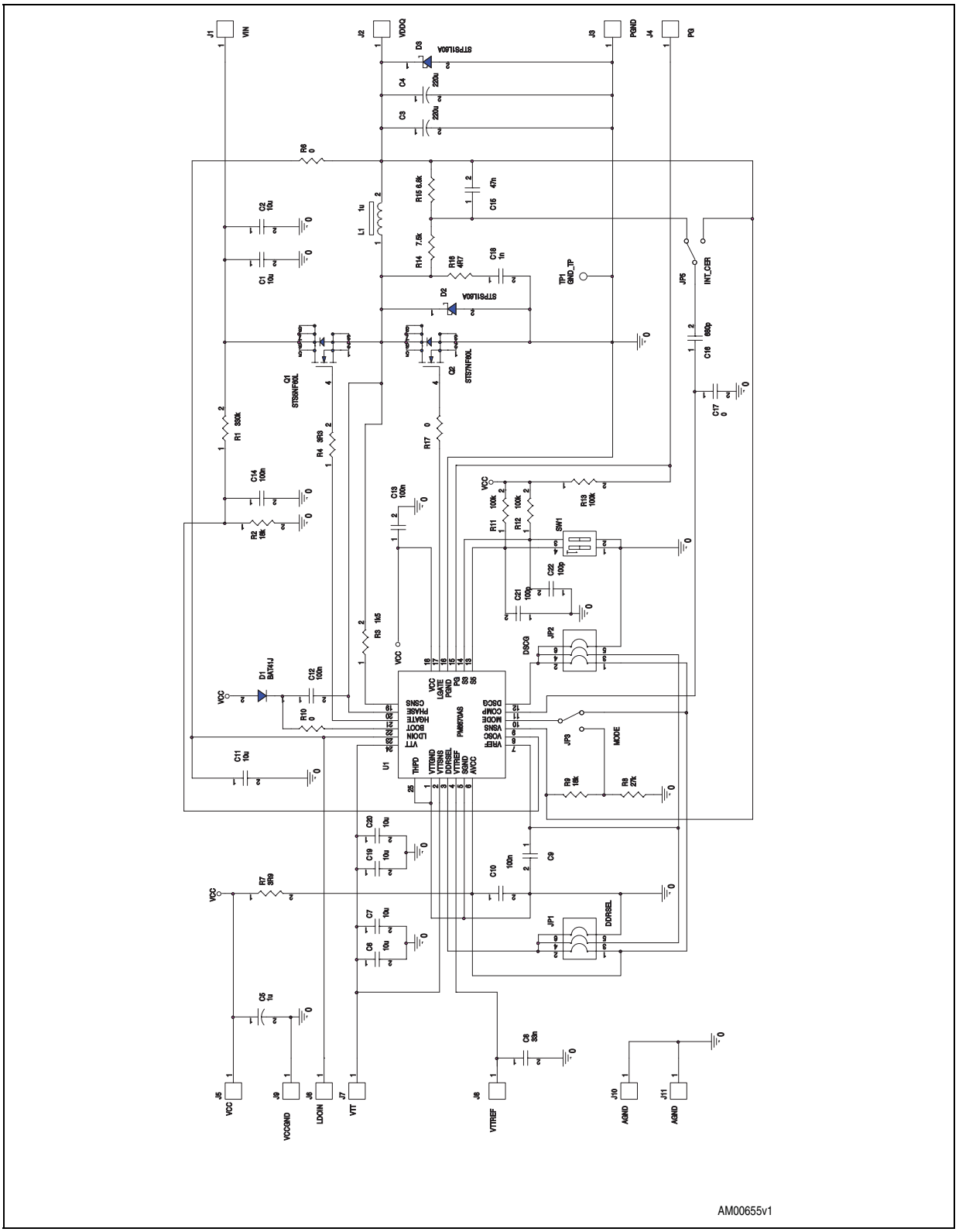
- 4.5 V to 36 V input voltage range
- 0.9 V, ± 1 % voltage reference
- 1.8 V (DDR2) or 1.5 V (DDR3) fixed output voltages
- 0.9 V to 2.6 V adjustable output voltage
- 1.237 V ± 1 % reference voltage available
- Very fast load transient response constant on-time loop control
- No-RSENSE current sensing using low-side MOSFETs' RDSON
- Negative current limit
- Latched OVP, UVP and thermal shutdown
- Fixed 3 ms soft-start
- Selectable pulse-skipping at light load
- Selectable non-audible (33 kHz) pulse-skip mode
- All ceramic output capacitor applications supported
- Output voltage ripple compensation

1.2 Reference and termination voltages (VTTREF and VTT)

- 2 A peak LDO with foldback for VTT
- Remote VTT output sensing
- High-Z VTT output in S3
- All ceramic output capacitor applications supported
- ±15 mA low-noise buffered reference for VTTREF

2 Demonstration kit schematic

Figure 2. PM6670AS demonstration board schematic



2.1 Component list

Table 1. PM6670AS demonstration board bill of materials

Qty	Component	Description	Package	Part number	MFR	Value
2	C1, C2	Ceramic, 50 V, X5R, 20%	SMD 1210	UMK325BJ106KM-T	Taiyo Yuden	10 µ
2	C3, C4	POSCAP, 4 V, 15 m, 20%	SMD 7343 (D)	4TPE220MF	Sanyo	220 µ
1	C5	Ceramic, 6.3 V, X5R, 10%	SMD 3216-12		Standard	1 µ
3	C6, C7, C11	Ceramic, 6.3 V, X5R, 10%	SMD 0805	JMK212BJ106KG-T	Taiyo Yuden	10 µ
1	C8	Ceramic, 50 V,X7R, 20%	SMD 0603		Standard	33 n
4	C9, C10, C13, C14	Ceramic, 50 V, X7R, 20%	SMD 0603		Standard	100 n
1	C12	Ceramic, 50 V, X7R, 10%	SMD 0805		Standard	100 n
1	C15	Ceramic, 50 V, X7R, 10%	SMD 0603		Standard	6n8
1	C16	Ceramic, 50 V, X7R, 10%	SMD 0603		Standard	680 p
1	C17	Ceramic, 20%	SMD 0603		Standard	N.M.
1	C18	Ceramic, 50 V, X7R, 10%	SMD 0805		Standard	1 n
2	C19, C20	Ceramic, 6.3 V, X5R, 10%	SMD 0805	JMK212BJ106KG-T	Taiyo Yuden	N.M.
1	R1	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	330 k
1	R2	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	18 k
1	R3	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	1.5 k
1	R4	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	3R3
1	R6	Chip Resistor, 0.1 W, 1%	SMD 0805		Standard	0
1	R7	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	3R9
1	R8	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	39 k
1	R9	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	39 k
1	R10	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	0
3	R11, R12, R13	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	100 k
1	R14	Chip Resistor, 0.1 W, 1%	SMD 0805		Standard	7k5
1	R15	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	6k8
1	R16	Chip Resistor, 0.1 W, 1%	SMD 0805		Standard	4R7
1	R17	Chip Resistor, 0.1 W, 1%	SMD 0603		Standard	0
1	L1	SMT, 10.6 Arms, 4.36 mΩ	13.8 x 13.2 mm	MLC1538-152ML	Coilcraft	1.5 µ
1	Q1	N-Channel, 60 V	SO-8	STS7NF60L	ST	
1	Q2	N-Channel, 60 V	SO-8	STS7NF60L	ST	
1	D1	Schottky, 100 V, 0.2 A	SOD-323	BAT41J	ST	
1	D2	Schottky, 60 V, 1 A	DO214-AC	STPS1L60A	ST	
1	D3					N.M.
1	U1	Controller	VFQFPN-24	PM6670AS	ST	

Table 1. PM6670AS demonstration board bill of materials (continued)

Qty	Component	Description	Package	Part number	MFR	Value
11	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10,J11	Header, single pin				
3	JP1, JP2, JP3	Jumper, 2 x 3, 100 mils				
1	JP5	PCB pads selector				
1	TP6	Test point				
1	SW1	Dip switch 2	DIP-2		Standard	

3 Component assembly and layout

Figure 3. Topside component placement

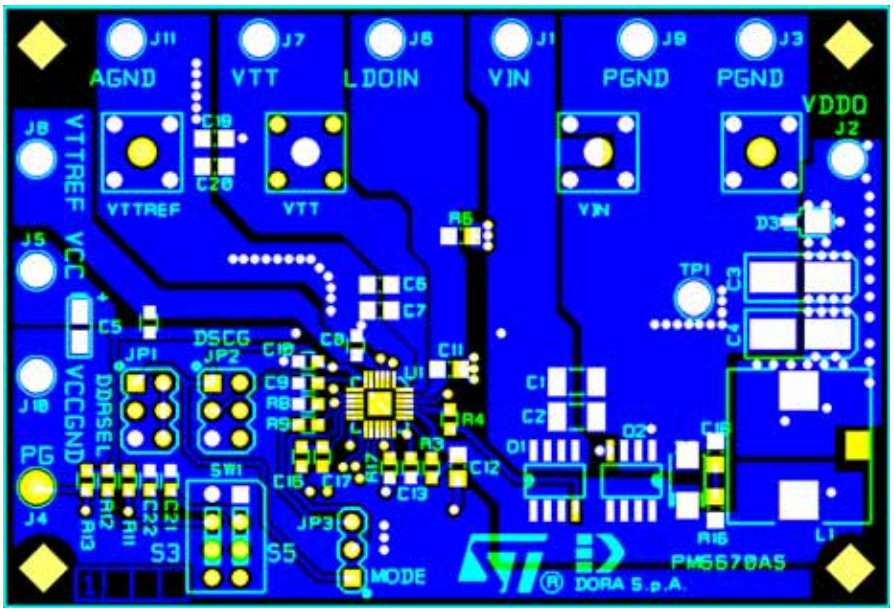


Figure 4. Topside view

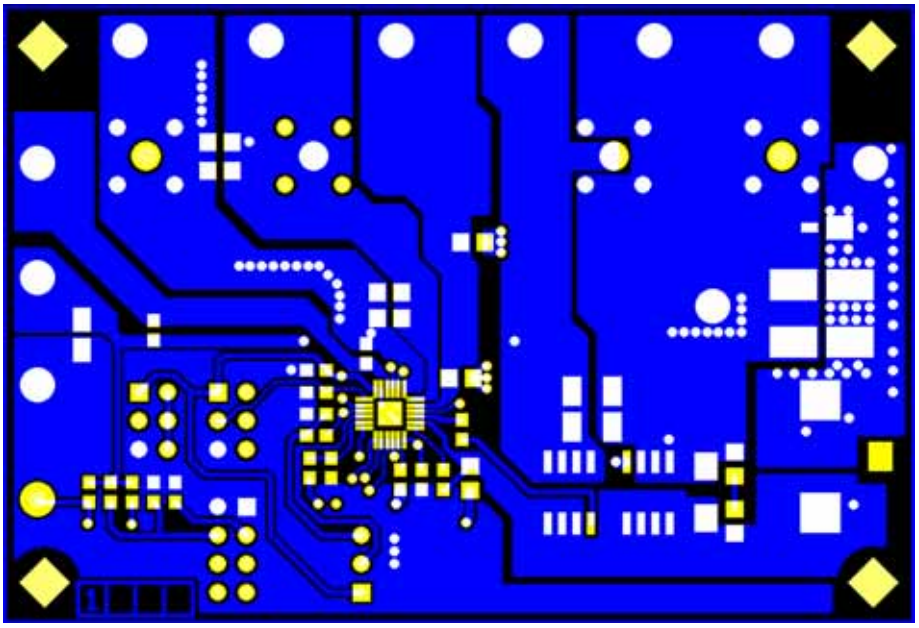


Figure 5. Layer 2 view

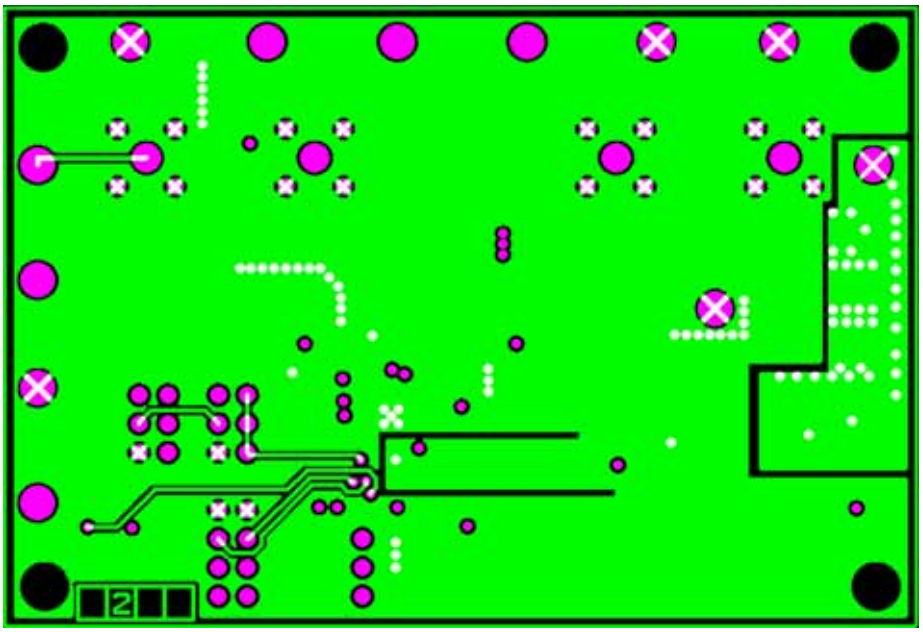


Figure 6. Layer 3 view

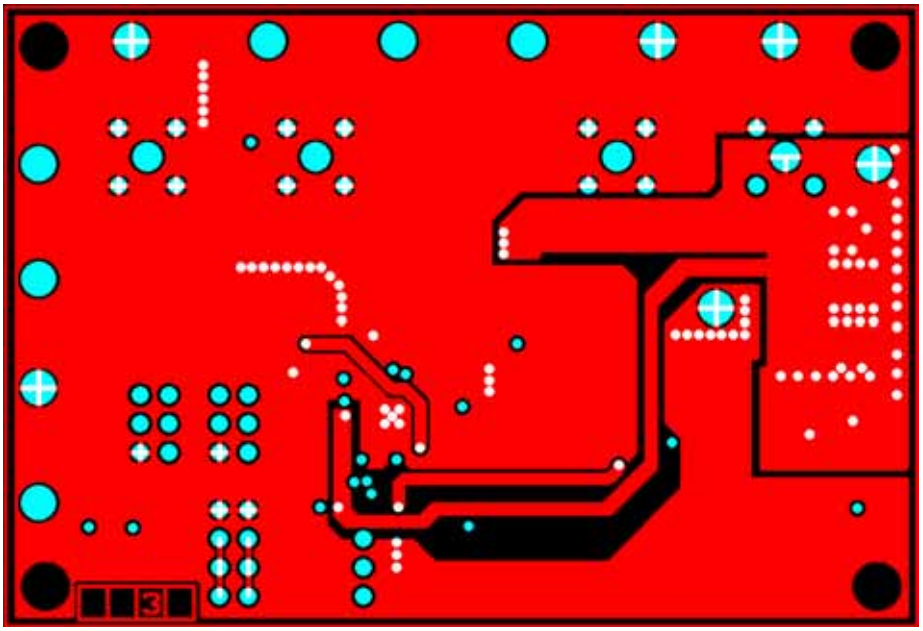


Figure 7. Bottomside view

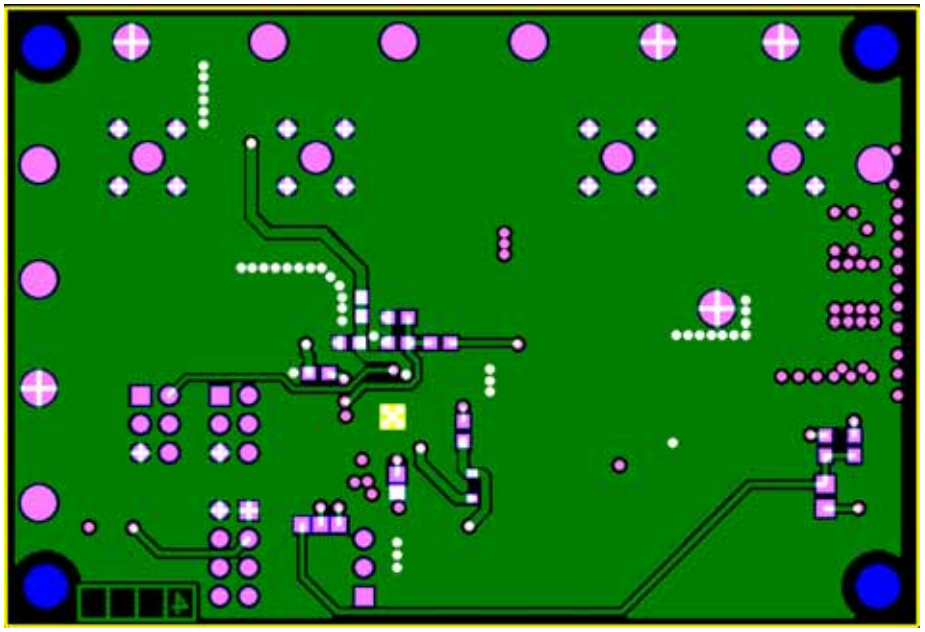
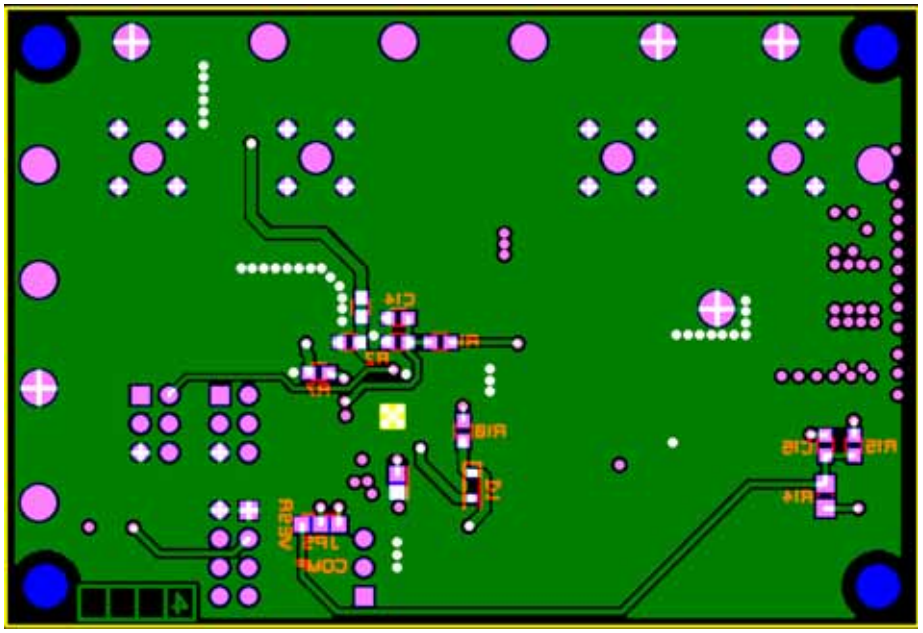


Figure 8. Bottomside component placement



4 I/O interface

The PM6670AS demonstration board has the following test points as given in *Table 2*.

Table 2. PM6670AS demonstration board input and output interface

Test point	Description
VIN	Battery input voltage positive terminal
PGND	Battery input and VDDQ output common return
VDDQ	VDDQ output
LDOIN	LDO linear regulator input
VTT	VTT output (LDO)
AGND	VTT and VTTREF outputs common return
VTTREF	VTTREF output
VCC	+ 5 V supply, positive terminal
VCCGND	Signal ground and VCC supply return
PG	VDDQ output Power Good signal
TP1	Connection point between power and signal grounds

4.1 Recommended equipment

4 V to 36 V, 30 W power supply

Active loads

Digital multimeters

200 MHz four-trace oscilloscope

5 Configuration

The PM6670AS board allows the user to choose the desired mode of operation using four jumpers (JP1, JP2, JP3 and JP5) and two resistors. Refer to the following configuration description.

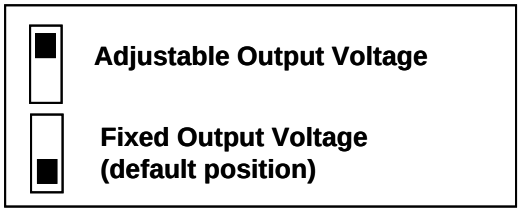
5.1 JP3 fixed or adjustable output voltage (MODE pin)

The JP3 jumper is used to choose between fixed output voltage (1.5 V or 1.8 V) and a user-defined output voltage in the range 0.9 V to 2.6 V. When connected in the lower position, the fixed output voltage is selected and the voltage depends on the setting of the DDRSEL pin (see *Section 5.2*).

If JP3 is in the upper position, the output voltage is given by:

$$VDDQ_{ADJ} = 0.9 \times \frac{R8 + R9}{R8}$$

Figure 9. JP3 (MODE) setting



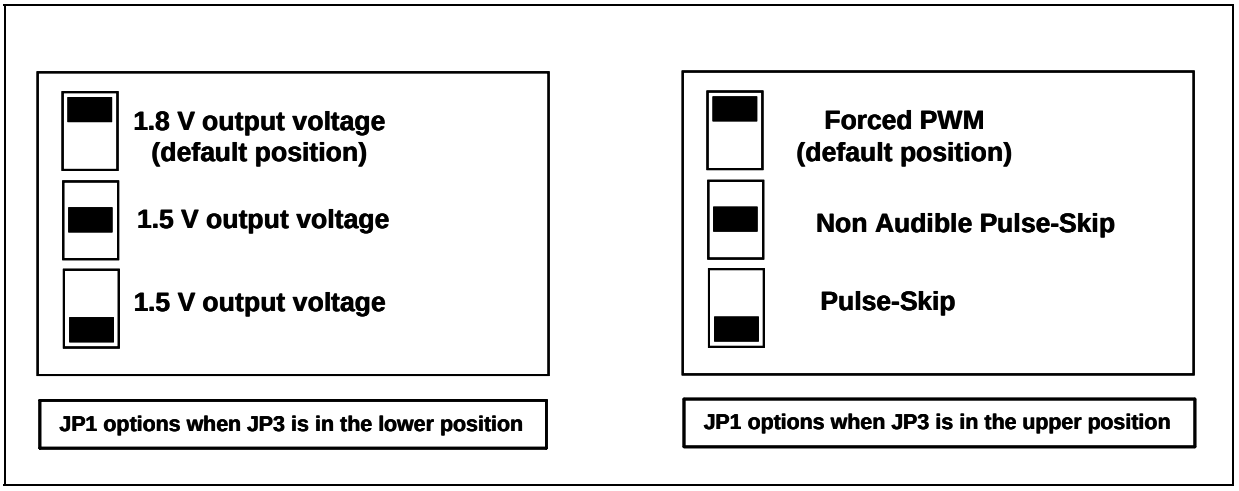
Both the R8 and R9 resistors are set to 39 kΩ (1.8 V by default) and can be changed by the user.

5.2 JP1 DDR2/DDR3 or power-saving mode (DDRSEL pin)

The JP1 jumper allows different options depending on the JP3 configuration. If the fixed output voltage is selected (JP3 in the lower position), the user can choose between 1.8 V (DDR2) or 1.5 V (DDR3), connecting JP1 as shown in *Figure 10*, and the pulse-skip mode is set by default.

When the adjustable output voltage is selected (JP3 in the upper position), the same jumper allows choosing between forced PWM, pulse-skip and non-audible pulse-skip modes as shown in *Figure 10 on page 14*.

Figure 10. JP1 (DDRSEL) setting

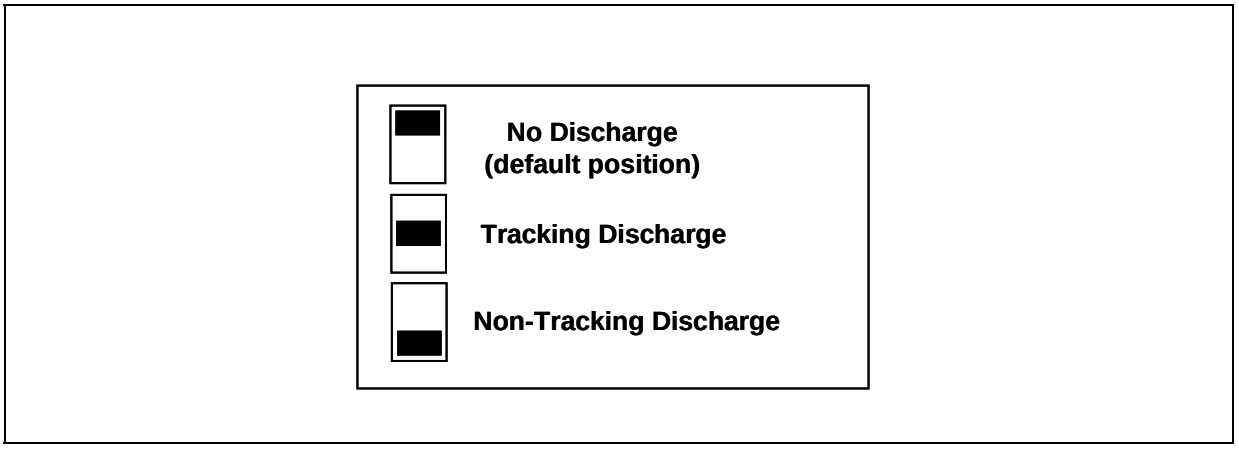


5.3 JP2 output discharge (DSCG pin)

The JP2 jumper is used to select the desired output discharge when both S3 and S5 signals are tied low. In the upper position the outputs are not discharged at all, while in the lower position the outputs are independently discharged using the internal MOSFETs (22 Ω for VDDQ and VTT, 1.5 kΩ for VTTREF).

The tracking discharge is programmed by putting JP2 in the central position. This discharge mode relies on the connection of the LDOIN pin to the VDDQ output, see *Section 6: Test setup on page 16* for details. If an external rail is used to supply the LDO, the tracking discharge cannot be used because the device can be damaged while attempting to sink 1 A from the LDO input.

Figure 11. JP2 (DSCG) setting

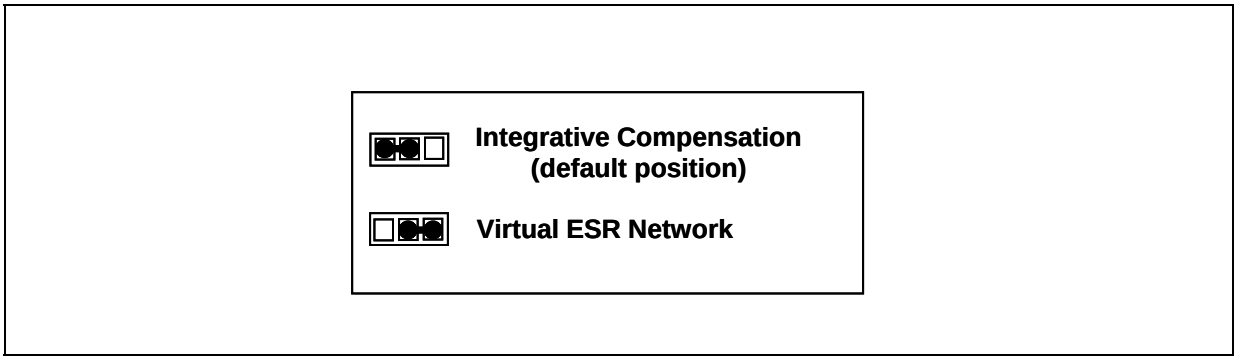


5.4 JP5 compensation network (COMP pin)

The JP5 jumper is located on the bottom side of the PM6670AS board and allows connecting the integrator input (COMP pin) to the output through a simple capacitor (integrative compensation) or using the "virtual ESR" network for very low ESR output capacitor applications (e.g. all ceramic output capacitor applications). The integrative compensation is set by default.

Refer to the PM6670AS datasheet for details about ceramic output capacitor applications and the virtual ESR design.

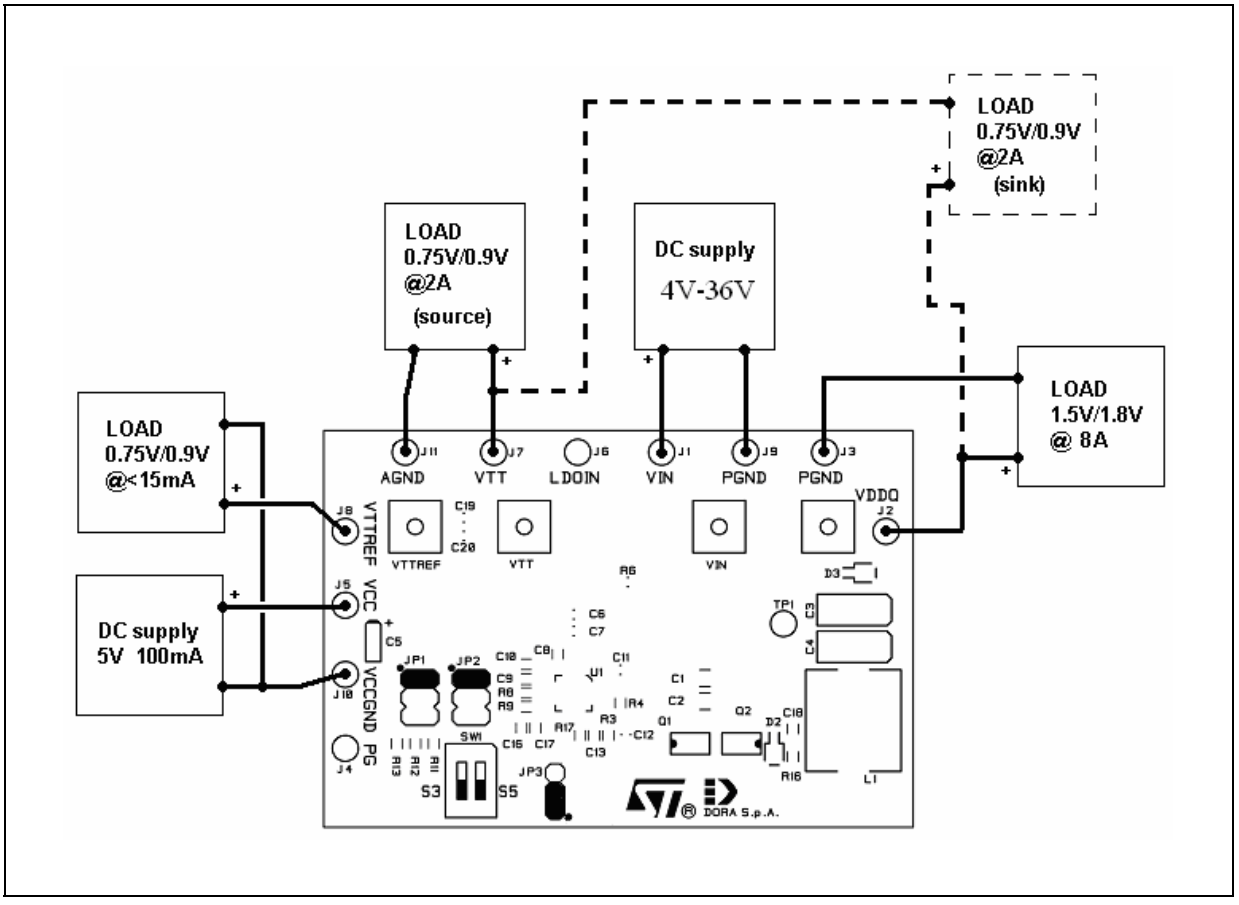
Figure 12. JP5 (COMP) setting



6 Test setup

Figure 13 shows the suggested setup connections between the PM6670AS demonstration board, the loads and the external supply. The LDO input (LDOIN) is connected to VDDQ by default (R6 = 0 Ω).

Figure 13. PM6670AS test setup



7 Getting started

The following step-by-step power-up and power-down sequences are provided in order to correctly evaluate the PM6670AS board performance.

7.1 Power-up sequence

Working in an ESD-protected environment is highly recommended. Check all wrist straps and mat-earth connections before handling the PM6670AS board.

1. Connect power supplies as shown in the PM6670AS test setup (*Figure 13*) and insert the meters in order to perform the desired performance evaluation. Connect the scope-probes as desired.
2. Set the JP1 through JP5 jumpers in order to properly configure the PM6670AS board. Set the S3-S5 switches to the on position (upper position). Do not change any of the jumper settings when the board is powered.
3. Set the VCC supply to 5 V ± 5 % and the current limit to 100 mA.
4. Set the VIN supply to a voltage in the range 4.5 V to 36 V. An initial test at 24 V and 3 A current limit is suggested.
5. Set all loads to 0 A.
6. Turn on the VIN supply.
7. Turn on the VCC supply.
8. Vary the VDDQ load from 0 A to 8 A.
9. Vary the VTT load from 0 A to 2 A to test source capability. To test sink capability use the dashed VTT load shown in *Figure 13*.
10. Vary the VTTREF load to test source capability.
11. Vary the VIN supply from 4.5 V to 36 V.

7.2 Power-down sequence

1. Decrease the VTTREF and VTT loads to 0 A.
2. Reduce the VDDQ load to 0.
3. Decrease the VCC supply from 5 V to 3.8 V in order to test the UVLO.
4. Increase the VCC supply from 3.8 V to 5 V to restart the device.
5. Use the S3-S5 switches to enter/exit the S0-S3-S5 states.
6. Turn off the VDDQ load.
7. Turn off the VCC supply.
8. Turn off the VIN supply.

8 PM6670AS evaluation tests

8.1 VDDQ, VTT and VTTREF turn-on (soft-start)

The VDDQ soft-start is divided in 4 steps. In each step the current limit is increased by ¼ of the nominal value. This behavior is well understood by loading the rail, as performed in the test. VTT and VTTREF soft-starts are performed at their maximum available current.

Figure 14. VDDQ soft-start at 180 mΩ load, pulse-skip mode

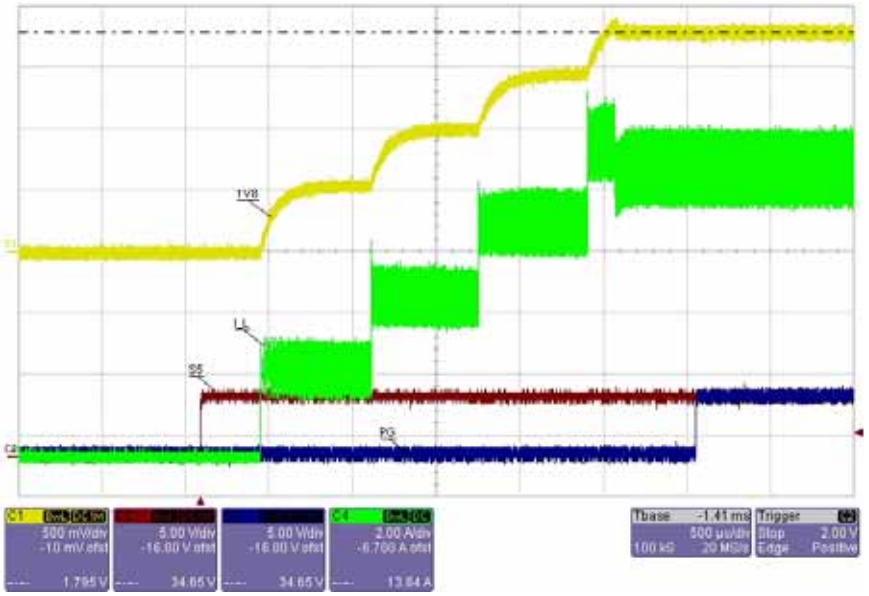
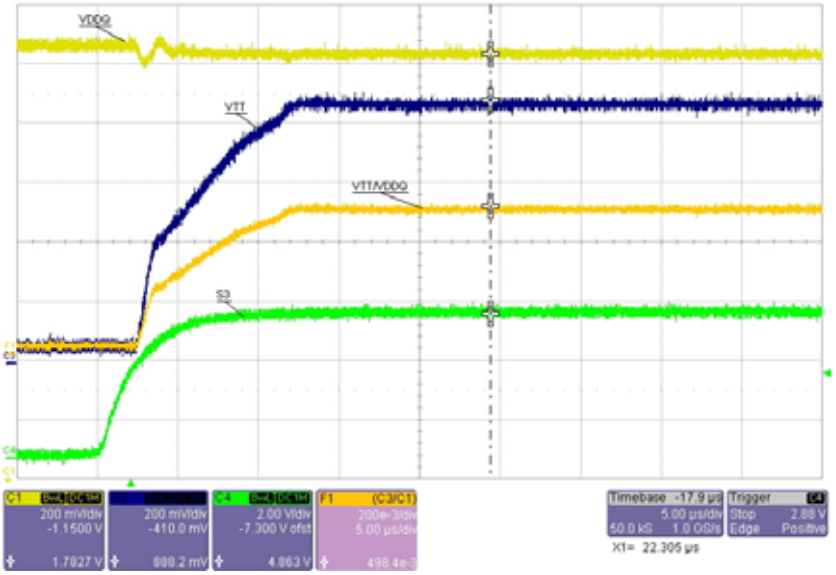


Figure 15. VTT turn-on (S0), pulse-skip mode

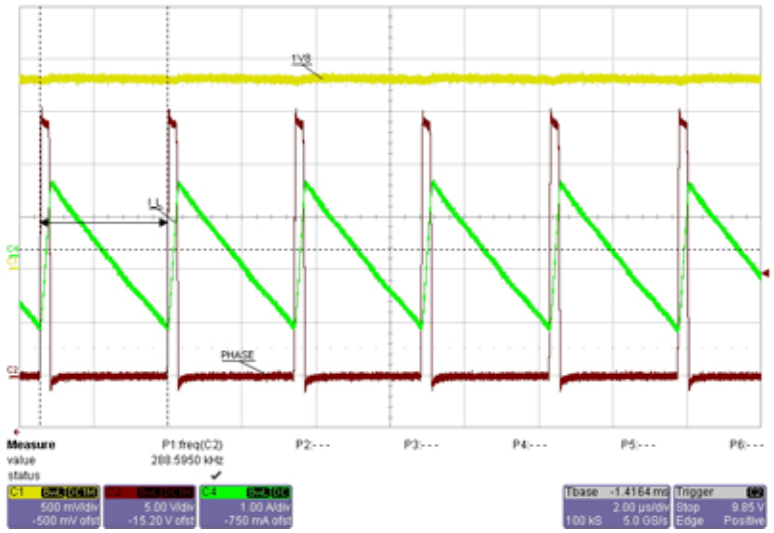


8.2 VDDQ working modes

8.2.1 VDDQ forced PWM mode

When the forced PWM working mode is selected (JP3 and JP1 in the upper position), the inductor current is allowed to become negative and the following waveform can be captured.

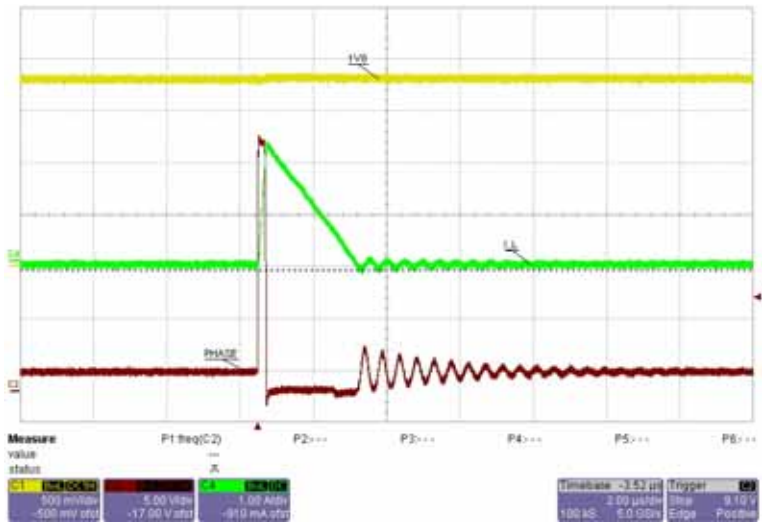
Figure 16. VDDQ = 1.8 V, VIN = 24 V, IVDDQ = 0 A, forced PWM mode



8.2.2 VDDQ pulse-skip mode

The default working mode is the pulse-skip algorithm, in which the low-side MOSFET is turned off when the inductor current becomes equal to zero. This behavior allows reaching maximum efficiency.

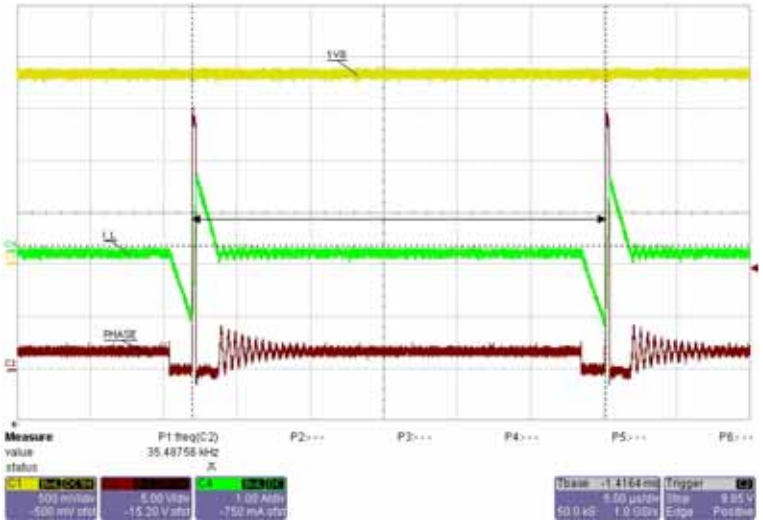
Figure 17. VDDQ = 1.8 V, VIN = 24 V, IVDDQ = 0 A, pulse-skip mode



8.2.3 VDDQ non-audible pulse-skip mode

In order to avoid an insufficient switching frequency, the non-audible pulse-skip mode can be selected (JP3 in the upper position and JP1 in the middle). So doing, the minimum switching frequency allowed is 33 kHz as depicted in the following picture.

Figure 18. VDDQ = 1.8 V, VIN = 24 V, no load, non-audible pulse-skip mode (33 kHz)



8.3 VDDQ, VTT and VTTREF load regulation

Figure 19 through *21* refer to VDDQ, VTT and VTTREF output voltage versus load current. The switching section works in pulse-skip mode and directly supplies VTT LDO.

Figure 19. VDDQ load regulation - VIN = 24 V

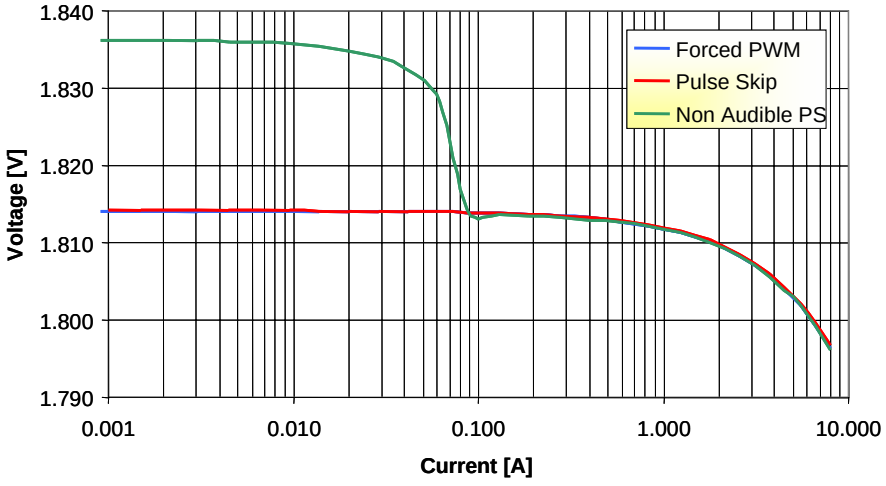


Figure 20. VTT load regulation - LDOIN = VDDQ (VDDQ in forced PWM mode)

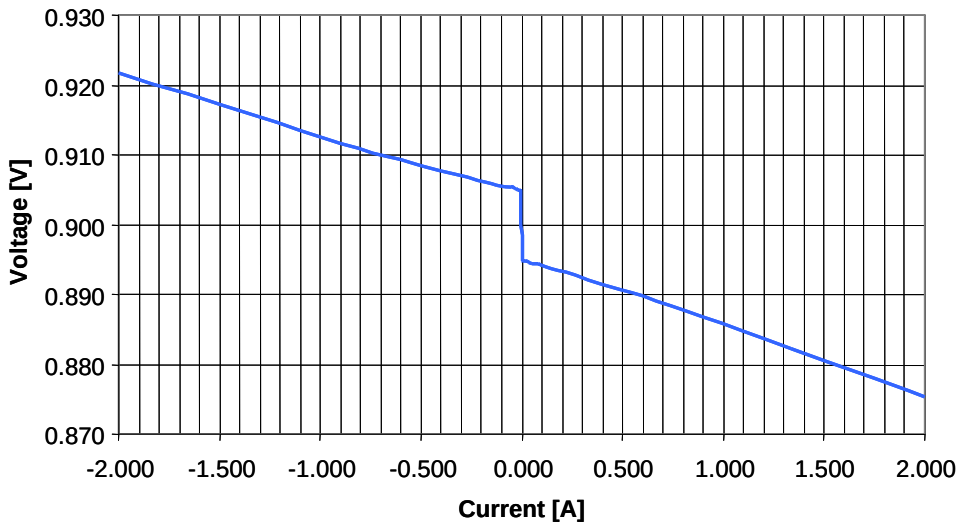
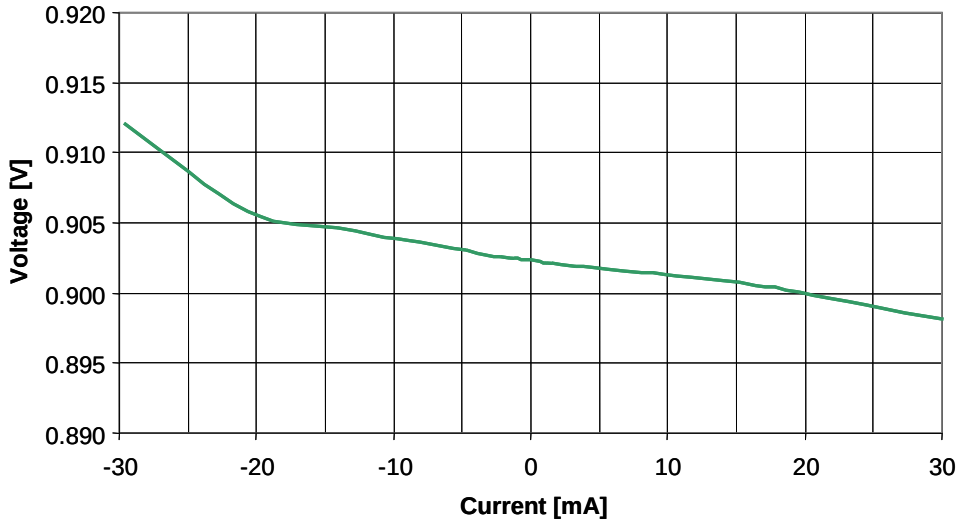


Figure 21. VTTREF load regulation (VDDQ in forced PWM mode)



8.4 VDDQ and VTT load transient responses

Load transient responses are evaluated by loading VDDQ and VTT output rails with a current slew rate of 2.5 A/µs.

Figure 22. VDDQ load transient (VIN = 24 V, LOAD = 0 A to 8 A at 2.5 A/µs) (pulse-skip mode)

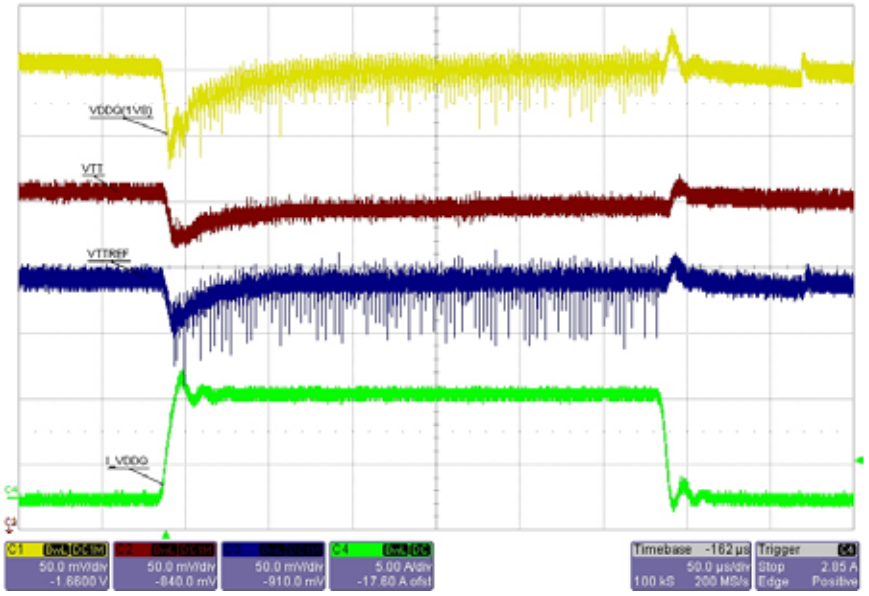
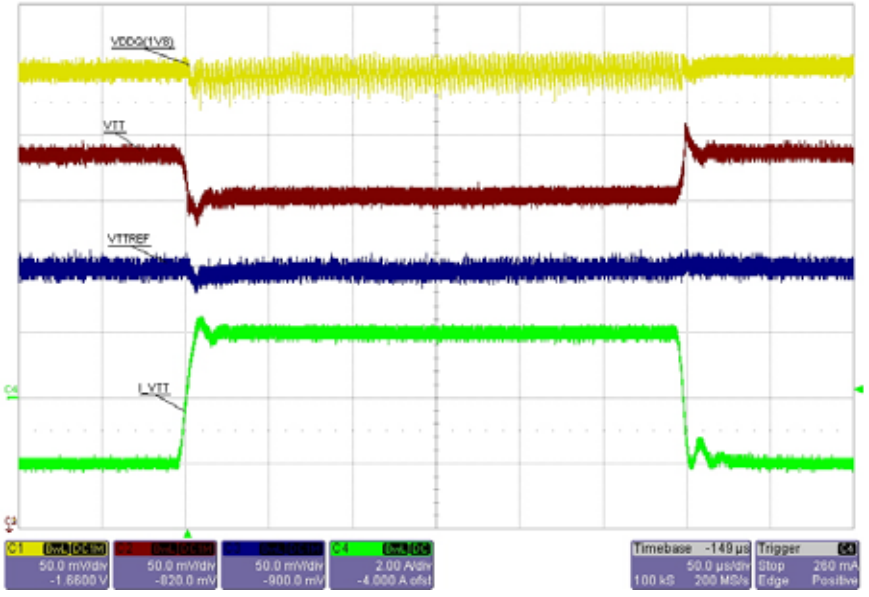


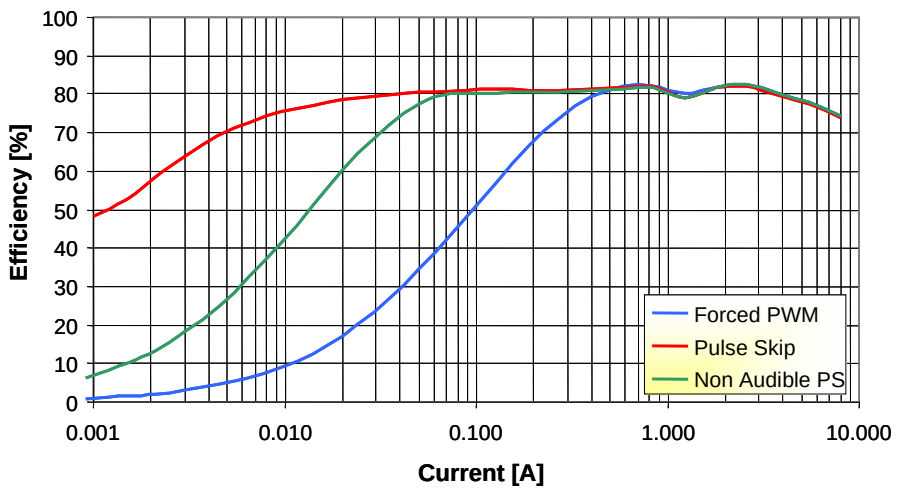
Figure 23. VTT load transient (VIN = 24 V, LOAD = – 2 A to 2 A at 2.5 A/µs) (pulse-skip mode)



8.5 VDDQ efficiency

The three working modes lead to different power efficiency. The test setup is VIN = 24 V, FSW = 330 kHz, VDDQ = 1.8 V. The following graph summarizes the results.

Figure 24. Forced PWM (blue), non-audible pulse-skip (green), pulse-skip (red) VDDQ efficiency vs. output current



8.6 VDDQ gate drivers

The PM6670 internal MOS driver turns on and off the high-side and low-side external MOSFET, avoiding cross-conduction. In *Figure 24* and *25* the gates signals are depicted without load and with load.

Figure 25. External MOS gate signals (VIN = 24 V, LOAD = 0 A) (pulse-skip mode)

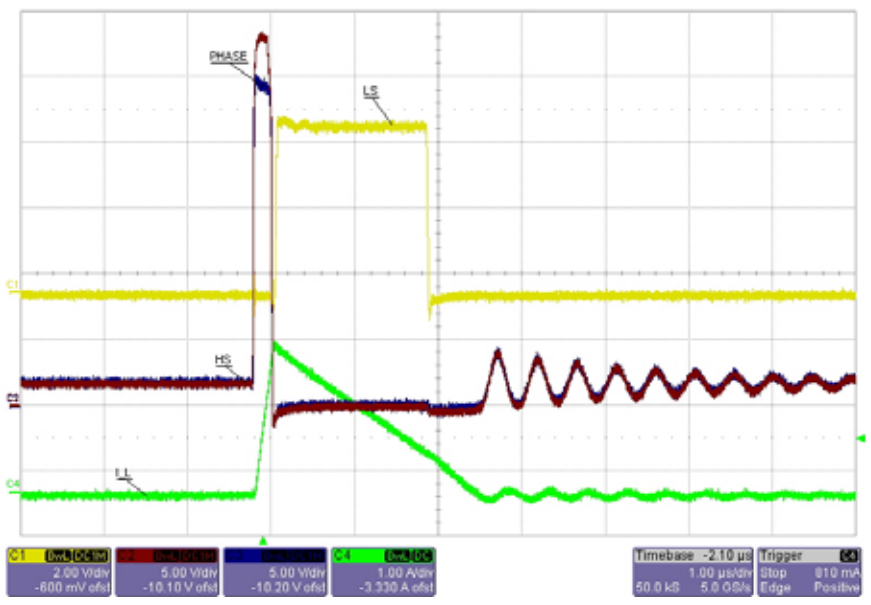
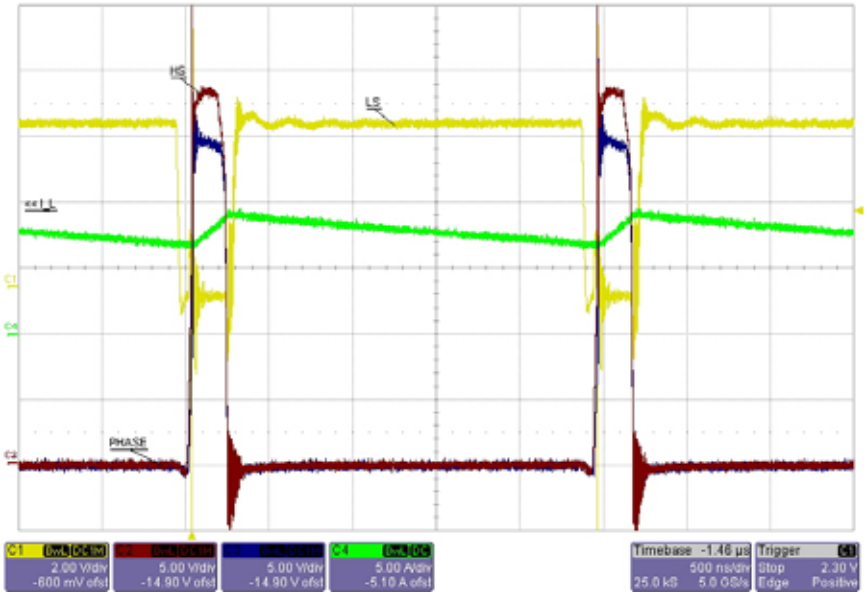


Figure 26. External MOS gate signals (VIN = 24 V, LOAD = 8 A) (pulse-skip mode)



8.7 VDDQ, VTT and VTTREF turnoff (soft-end)

Tracking discharge

The jumper JP2, if placed in the middle, allows the output tracking discharge. When S3 and S5 are pulled down, VTT discharges VDDQ by sinking 1 A and, at the same time, tracks the VDDQ remaining half. When VDDQ reaches about 400 mV, the output discharge MOSFETs are all closed and each rail is finally discharged.

Figure 27. VDDQ, VTTREF, VTT output voltages and LDO input current, tracking discharge, no load on any rail

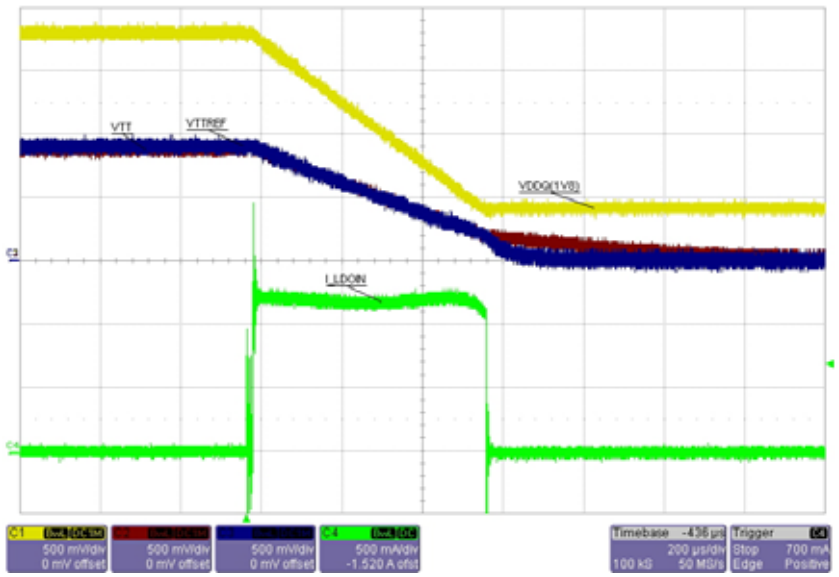


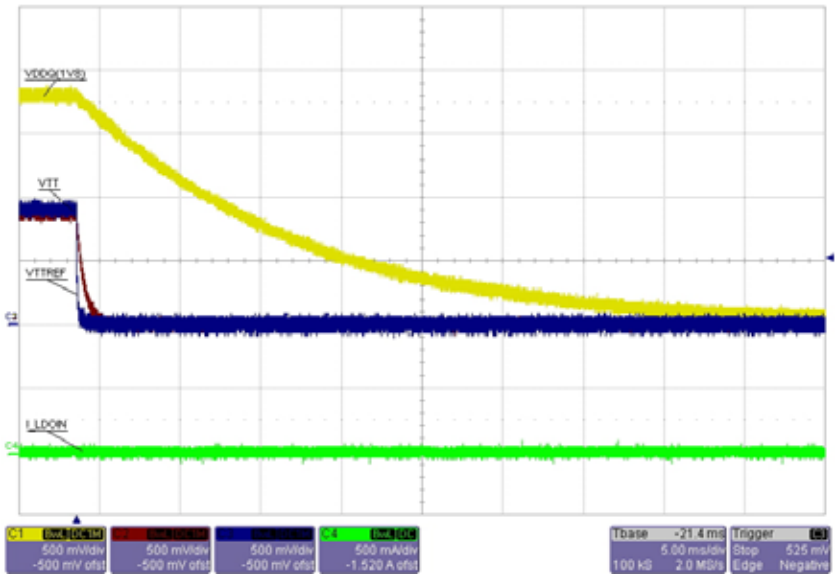
Table 3. Measured discharge resistance in soft-discharge mode

	VDDQ output	VTTREF output	VTT output
Measured N.T.D. discharge MOSFET's RDSon	25 Ω	1.5 kΩ	23 Ω

Non-tracking discharge

When the non-tracking discharge is programmed (JP2 in the lower position) and S3-S5 are both tied to GND, each output rail is discharged through its discharge MOSFET, as depicted in the following picture.

Figure 28. VDDQ, VTTREF and VTT, non-tracking discharge, no load on any output

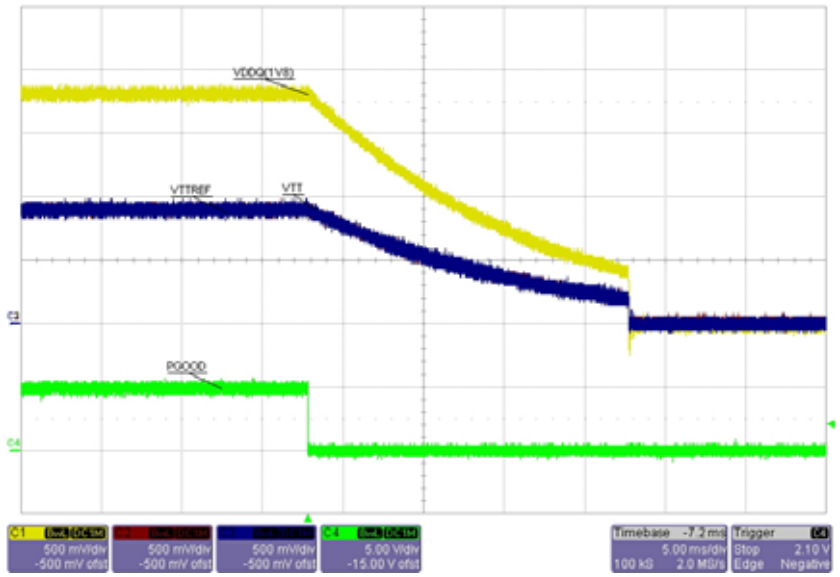


8.8 UV, OV and thermal protections

Latched UV protection

If the output voltage is lower than the 70 % nominal value, the undervoltage state is entered and the discharge MOSFETs are turned on (as in the non-tracking soft-end).

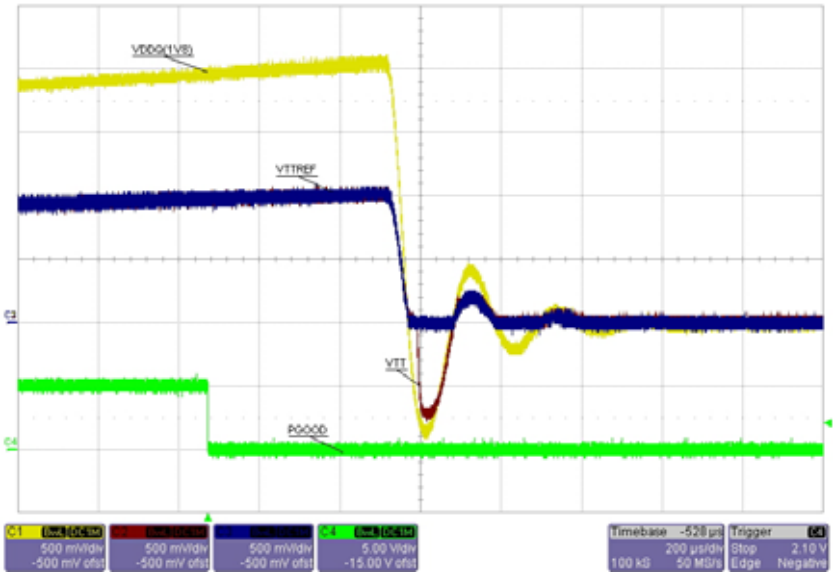
Figure 29. UV protection, pulse-skip mode



Latched OV protection

If the output voltage is higher than the 115 % nominal value, the overvoltage state is entered and the low-side MOSFET is turned on. VTT and VTTREF are discharged through their discharge MOSFETs.

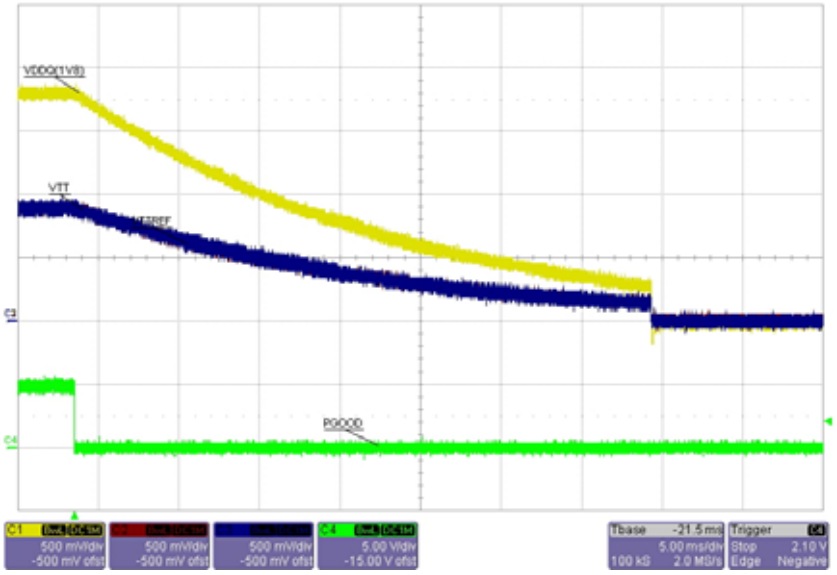
Figure 30. OV protection, pulse-skip mode



Latched thermal shutdown

If the junction temperature rises up to 150 deg, the thermal protection circuit turns off the device and discharges the output rails by performing the non-tracking discharge soft-end.

Figure 31. VDDQ, VTT, VTTREF and inductor current, thermal shutdown, pulse-skip mode



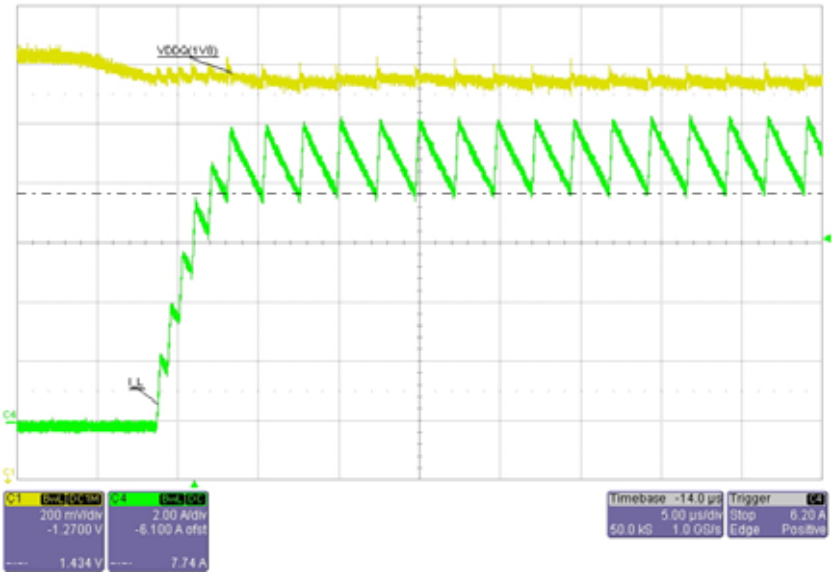
8.9 VDDQ current limit

The valley current limit avoids any high side turning on if the inductor current is higher than the programmed value. This current limit can be designed with the following equation:

$$I_{CL} = \frac{100\mu A \times R_{ILIM}}{R_{LS,DSon}}$$

The current sensing is performed by comparing the voltage drop in the low-side MOSFET, during the TOFF period, with the voltage drop given by an injected current and the current limit resistor.

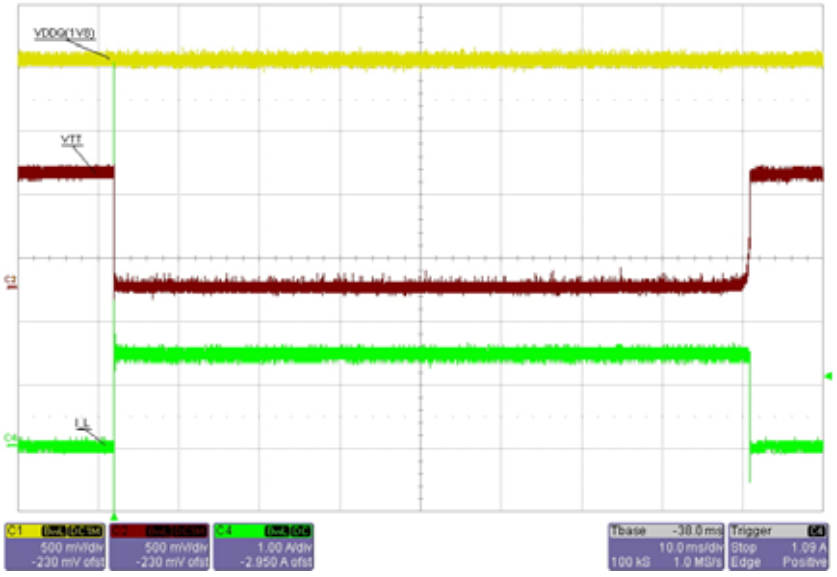
Figure 32. VDDQ current limit protection during a load transient (0 A to 10 A at 2.5 A/µs)



8.10 VTT current limit (foldback)

VTT LDO has a foldback protection feature which reduces the current limit to 1 A when the VTT output voltage is outside the ± 10 % Power Good window. The current limit is restored to 2 A when the output voltage re-enters the Power Good window.

Figure 33. VTT current limit during an output short

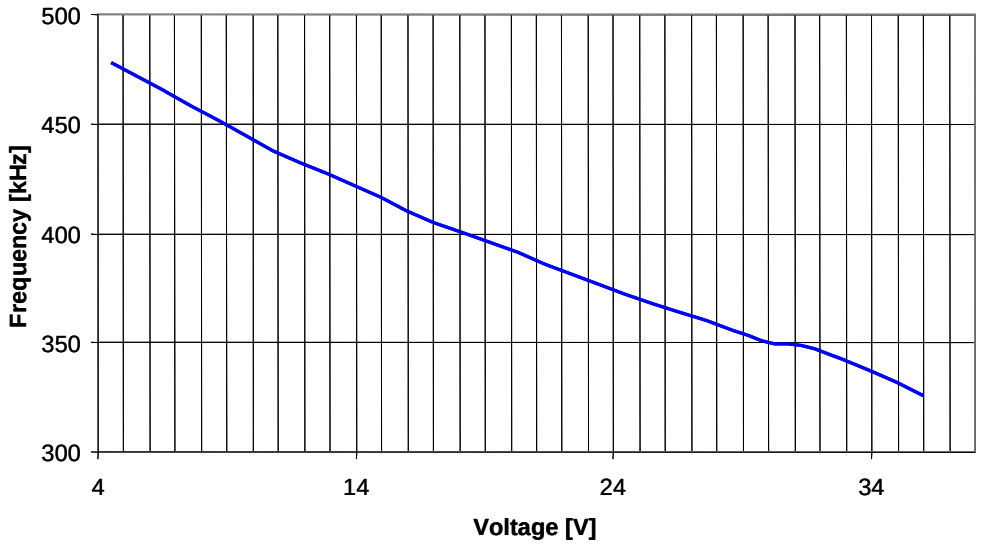


8.11 Switching frequency

Switching frequency vs. input voltage

The constant on-time controller leads to a quasi-constant switching frequency, slightly following the input voltage.

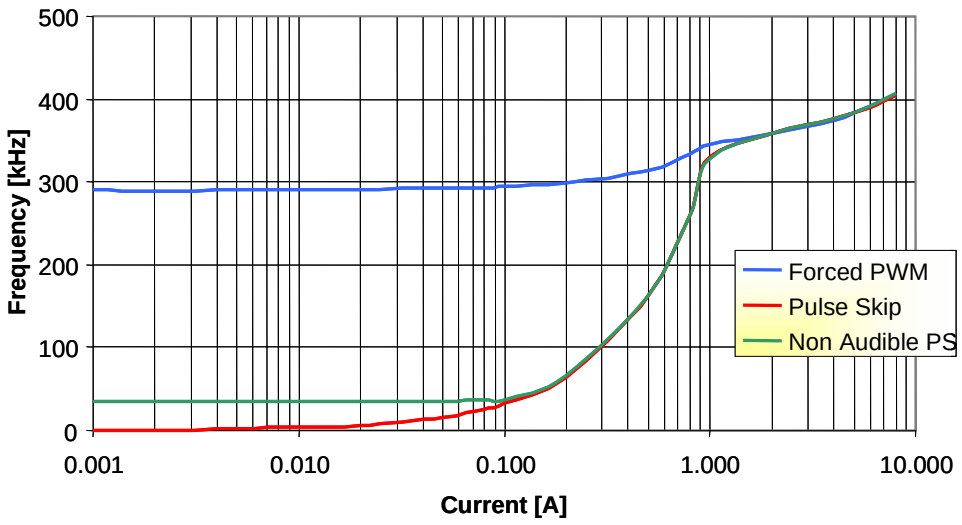
Figure 34. Switching frequency vs. input voltage, VDDQ = 1.8 V, IVDDQ = 4 A, forced PWM mode



Switching frequency vs. output current

The switching frequency can decrease to very low values in pulse-skip mode instead in non-audible pulse-skip there is a lower limit (about 33 kHz). With increasing load, however, the switching frequency increases a bit, as a consequence of conduction and switching losses.

Figure 35. Forced PWM (blue), non-audible pulse-skip (green) and pulse-skip (red), switching frequency vs. output current, VDDQ = 1.8 V, VIN = 24 V



8.12 Thermal behavior

The IC internal maximum and average temperature can be monitored by an IR camera. For the measurements in *Figure 36* through *39* the test setup is:

- V_{IN} = 24 V
- F_{SW} = 360 kHz
- Pulse-skip mode
- I_{VDDQ} = 4 A
- VTT rail powered by VDDQ
- T_{AMB} = 25 °C

By increasing the VTT current, the IC temperature changes as depicted in the following pictures.

Figure 36. I_{VTT} = 0 A, average IC temperature = 37.5 °C, max internal IC temperature = 40.1 °C

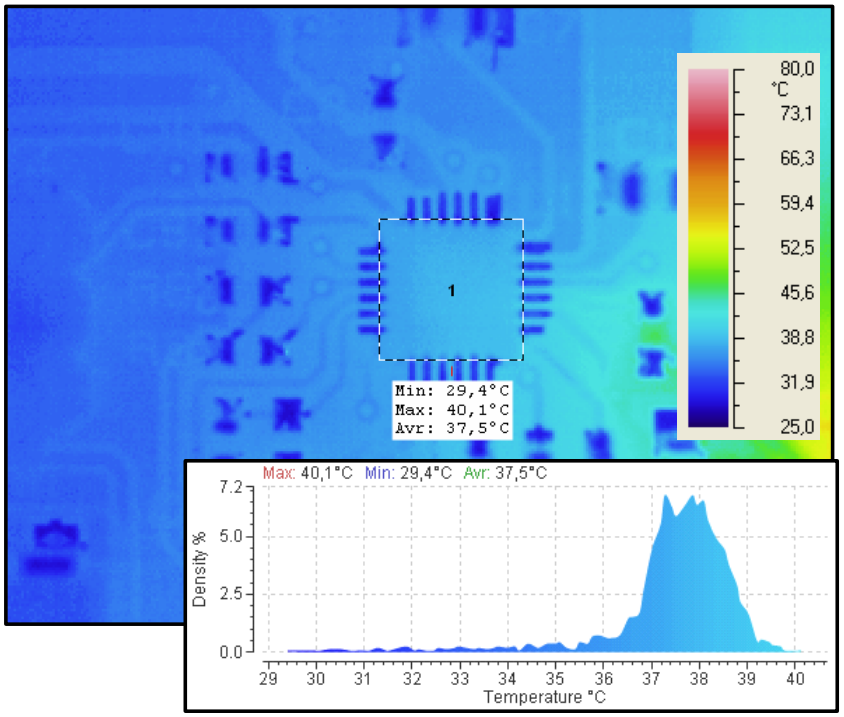


Figure 37. I_{VTT} = 0.5 A, average IC temperature = 48.8 °C, max internal IC temperature = 54.3 °C

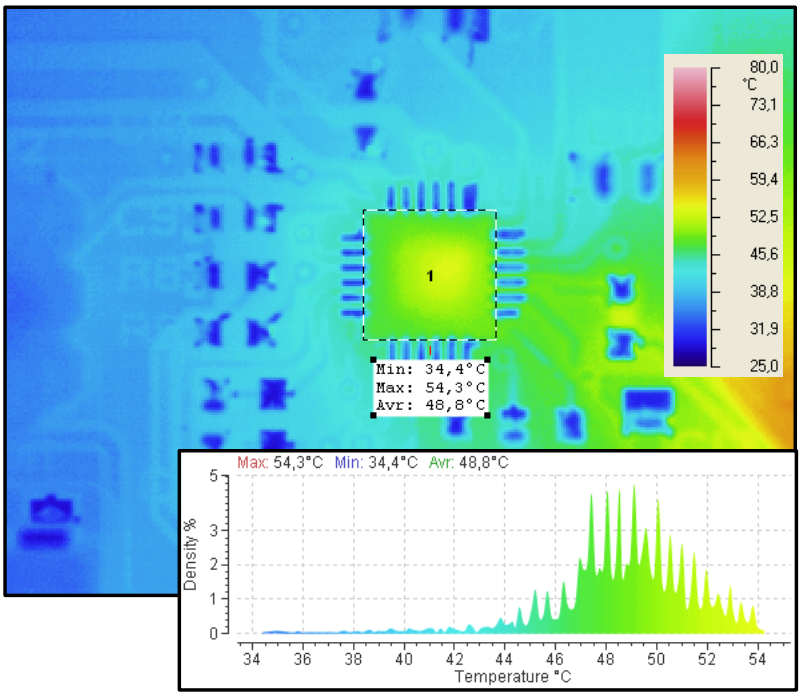


Figure 38. I_{VTT} = 1 A, average IC temperature = 60.5 °C, max internal IC temperature = 72.7 °C

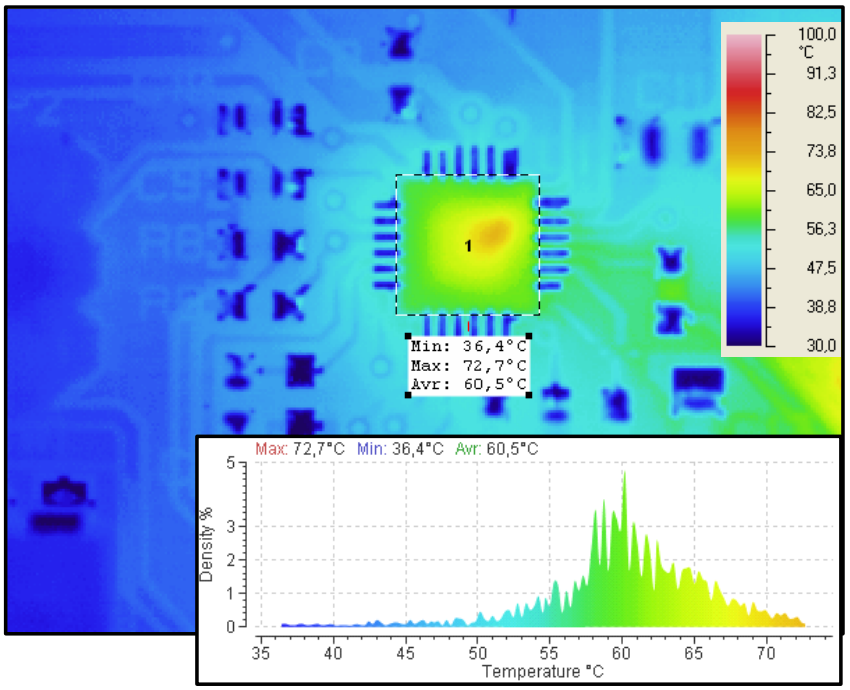
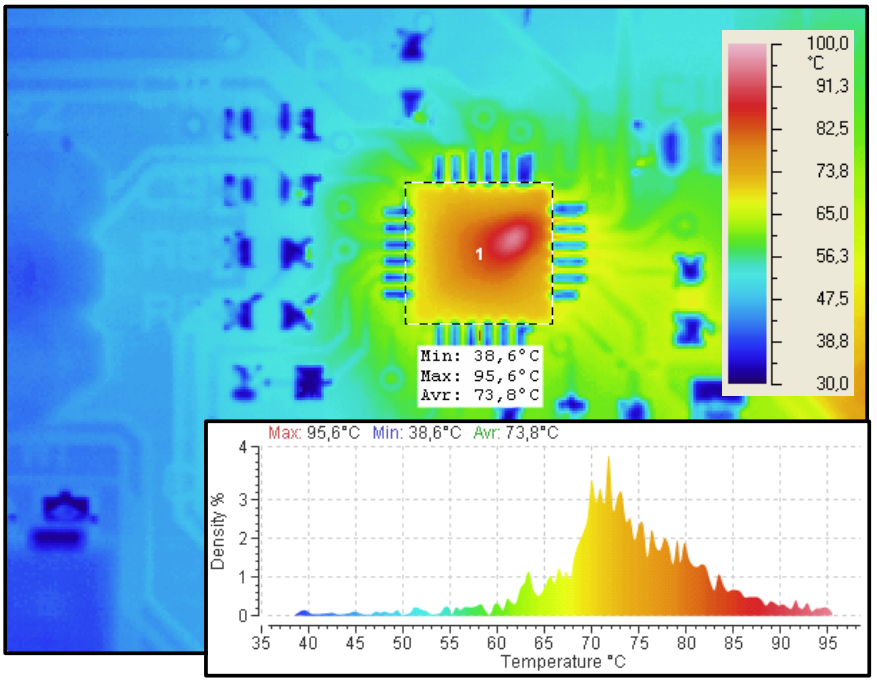


Figure 39. I_{VTT} = 1.5 A, average IC temperature = 73.8 °C, max internal IC temperature = 95.6 °C



9 Revision history

Table 4. Document revision history

Date	Revision	Changes
04-Nov-2008	1	Initial release.

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