AN2592
Application note

Achieving 32-bit timer resolution with software expansion for STM32Cube and Standard Peripheral Library

Introduction

In many applications, 32-bit resolution is required to measure external signals with long periods (up to several hundreds of seconds), or to generate delays or periodic signals with similar periods.

The STSW-STM32009 and X-CUBE-TIM-32RES firmwares offer, on STM32F10x, STM32L0xx (X-CUBE-TIM-32RES only) and STM32L15x microcontrollers, the possibility of chaining two 16-bit timers to obtain 32-bit resolution.

This result is achieved thanks to a specific configuration of the timers, and to the use of the timer link system.

This application note gives general guidelines to emulate a 32-bit timer, focusing on the two basic operating modes (Input capture and Output compare).

Each mode is treated independently and, each time, examples of applications are provided.

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1 Timer synchronization

1.1 Timer link system presentation

In the STM32F10x, STM32L0xx and STM32L15x microcontrollers, the embedded timers can be linked together for timer synchronization or chaining purposes.

Using the timer link system, a timer configured in Master mode can:

- reset the counter of the slave timer
- start and/or stop the slave timer counter
- clock the slave timer counter.

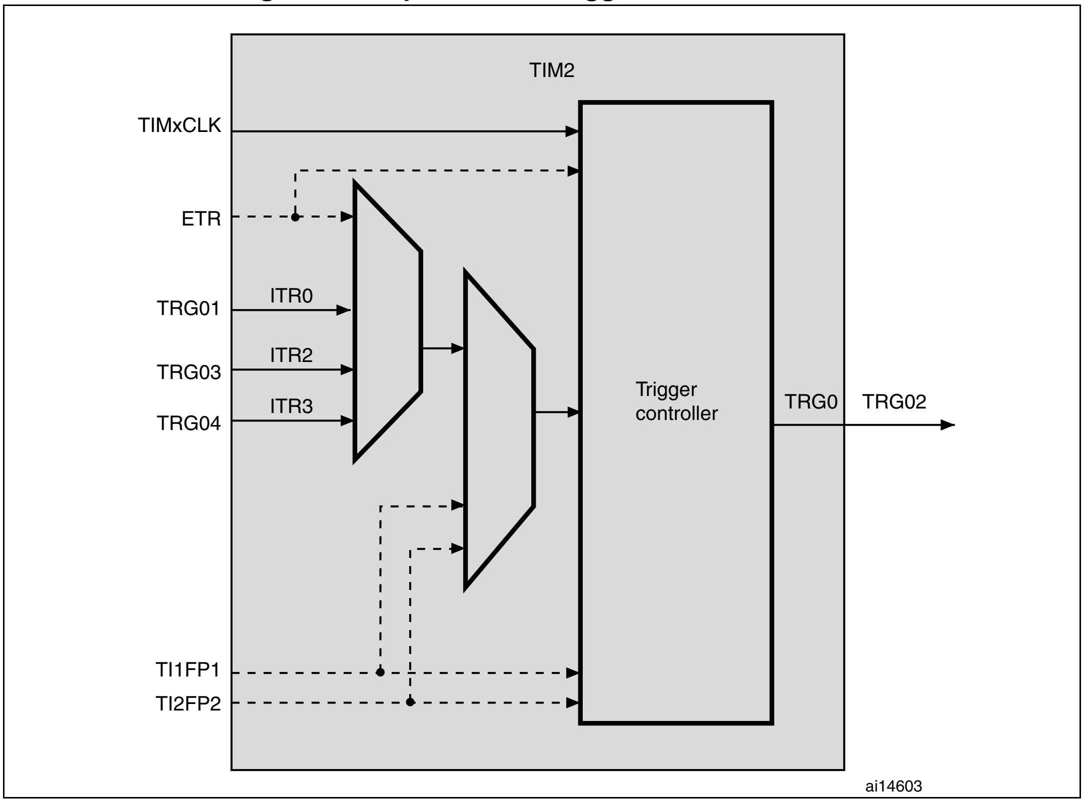
1.2 How to synchronize two timers using the link system

Note: Details of implementation described in this section apply to STM32F10x only, for STM32L0xx and STM32L15x refer to the dedicated reference manuals and firmwares.

In addition to the TIMx_CHx pins, timers have several internal triggers that are indispensable for linking and chaining operation.

Figure 1 shows a simplified representation of the timer block, that highlights the internal triggers. TIM2 is used as an example.

Figure 1. Simplified TIM2 trigger controller block



The internal triggers (ITR0, ITR2 and ITR3) are used when TIM2 is configured in the Slave mode. They then determine which master controls TIM2.

For example, if TIM2 uses ITR2 as an internal trigger, this means that TIM2 is synchronized with TIM3.

These triggers can be easily redirected to the master by setting the right combination of TS bits in the SMCR register.

The trigger output, TRGO, is used when TIM2 is configured in the Master mode. It then determines which events or signals are sent to the slave timers for synchronization.

Different events or signals can be transmitted to the slave, as listed below. They are selected using the MMS bits in the CR2 register.

- reset event
- enable event
- update event
- compare pulse
- OCxREF, where x is 1, 2, 3 or 4.

Once the master trigger output, TRGO, and the slave's internal triggers, ITRx, are configured, the two timers are chained.

Four different slave modes can be selected using the SMS bits in the SMCR register:

- Reset mode: the rising edge of the trigger signal reinitializes the counter and generates an update of the registers.
- Gated mode: the slave counter start and stop are both controlled by the high level on the trigger input.
- Trigger mode: the start of the slave counter is controlled by the rising edge of the trigger input signal.
- External clock mode1: the slave counter is clocked by the rising edges of the selected trigger input signal.

2 32-bit input capture timer resolution

Note: Details of implementation described in this section apply to STM32F10x only, for STM32L0xx and STM32L15x refer to the dedicated reference manuals and firmwares.

2.1 Principle

To measure the period of an external signal, the timer can be used in input capture mode. The frequency range that can be measured with the 16-bit timer depends on the TIMxCLK signal.

For example, if the timer of an STM32F10x is clocked by 72 MHz (TIMxCLK = 72 MHz), the minimum frequency F that can be measured is:

$$F = \frac{TIMxCLK}{ARR} = \frac{72 \times 10^6}{0xFFFF} = 1098\ Hz$$

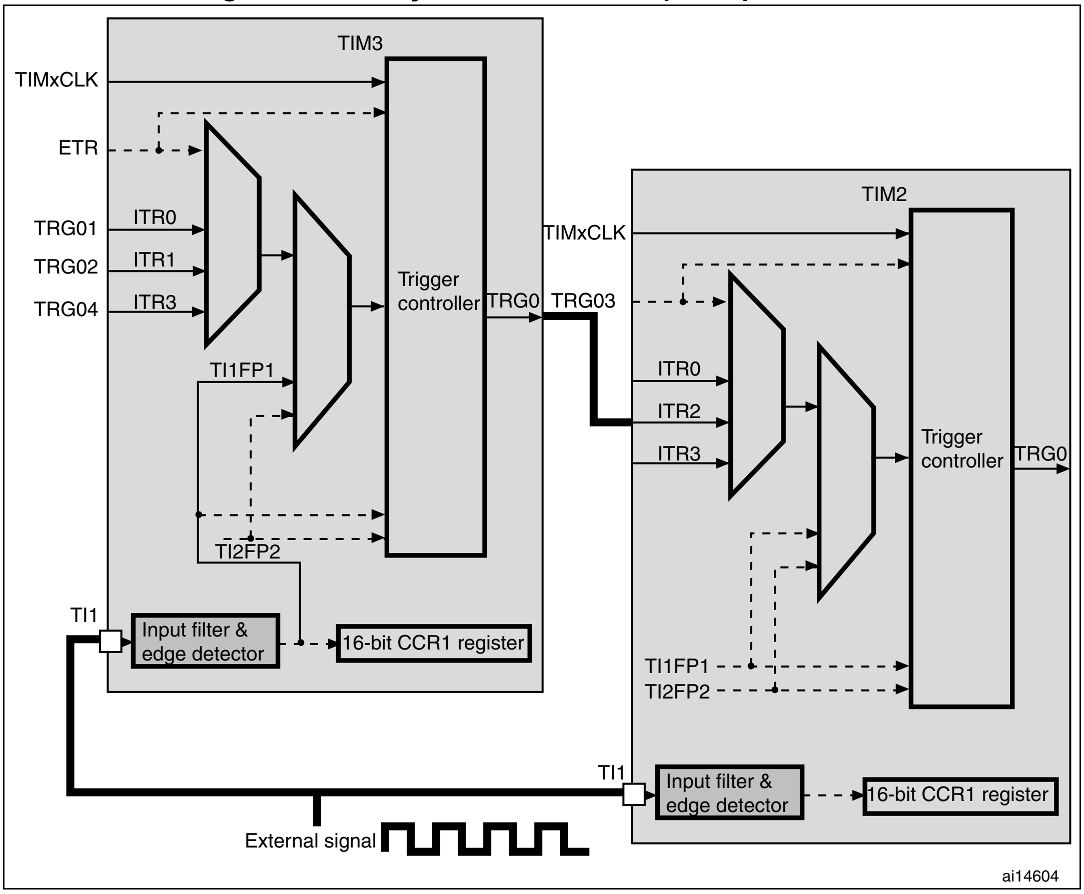
In some applications, the user needs to measure large periods. The idea is to increase the timer resolution from 16-bit to 32-bit using a specific configuration based on the timer link system.

2.2 Timer configuration

The measure is performed by two timers synchronized in a specific mode. The master measures the LSB part of the external signal period/frequency and the slave measures the MSB part. The two timers are used in input capture mode.

Figure 2 further explains the typical internal connection of the master and slave timers. TIM3 is used as the master for the TIM2 timer.

Figure 2. Timer synchronization in input capture mode



2.2.1 TIM3 master configuration

The master timer is used to measure the LSB part of the external period or frequency. To do so, it is configured as follows:

- no prescaler is used
- the external signal is connected to channel 1 and the rising edge is configured as the active edge.

The input capture module is used to latch the value of the counter after a transition detected by the corresponding input channel. To get the external signal period, two consecutive captures are needed and the period is calculated by subtracting these two values.

To avoid this method and facilitate the input capture measurement, the master counter is reset after each rising edge detected on the timer input channel by:

- selecting TI1FP1 as the input trigger by setting the TS bits in the SMCR register
- selecting the reset mode as the slave mode by configuring the SMS bits in the SMCR register.

Using this configuration, when an edge is detected, the counter is reset and the period of the external signal is automatically given by the value on the CCR1 register.

2.2.2 TIM2 slave configuration

The slave timer is used to measure the MSB part of the external frequency. To do so, it is configured as follows:

- prescaler is fixed to 0xFFFF
- the external signal is connected to channel 1 and the rising edge is configured as the active edge.

2.2.3 Master and slave synchronization

Master configuration

- Use the master update event as the master trigger output (TRGO).
- Enable the Master/Slave mode.

Slave configuration

- Select the slave input trigger: the master trigger output (TRGO) used as the input trigger for the slave.
- Enable the Master/Slave mode.
- Use the external clock mode 1 as the Slave mode: the slave is clocked by the update event of the master timer. That is, when the master counter is overflow, the slave counter is incremented.

Using this configuration, each time the period to be measured exceeds the 16-bit master timer Auto-reload register, an update event is generated to clock the slave timer.

When the active edge is detected on the master and slave timer inputs, the two counter values are copied into the master CCR1 register and the slave CCR1 register, respectively.

Since the slave is clocked by the master update event, the number of master overflow is recorded by the slave as the MSB part of the 32-bit input capture register; the LSB is read on the Master CCR1.

The external signal frequency is calculated on each master input capture interrupt as follows:

$$\text{ExtSignalFreq} = \frac{72 \times 10^6}{\text{MSB} \times 65535 + \text{LSB}}$$

LSB is the master capture compare register value (TIM3 CCR1 register value).

To get the MSB value, two consecutive captures are needed and the MSB variable is calculated by subtracting these two values, as shown below:

- If MSB1 > MSB2 then MSB = 0xFFFF – ((MSB1 – MSB2)) – 1
- If MSB1 < MSB2 then MSB = (MSB2 – MSB1) – 1

MSB1 and MSB2 are given by the slave capture compare value (TIM2 CCR2 register value).

Since the master timer is used in Reset mode, when the active edge is detected on the master timer, the counter is reinitialized and an update is generated. To avoid this additional update event, 1 is subtracted from the MSB value.

Using this method, the lowest frequency that can be measured on STM32F10x (with TIMxCLK equal to 72 MHz) is 17 mHz, instead of 1098 Hz when a 16-bit timer is used.

For STM32L1xx, the lowest measurable frequency is equal to 7.56 mHz instead of 488 Hz with a 16-bit timer only.

3 32-bit input capture resolution using one timer

Note: Details of implementation (e.g. used Timers) applies to STM32L0 only. For other products refer to the dedicated reference manuals and firmwares.

3.1 Principle

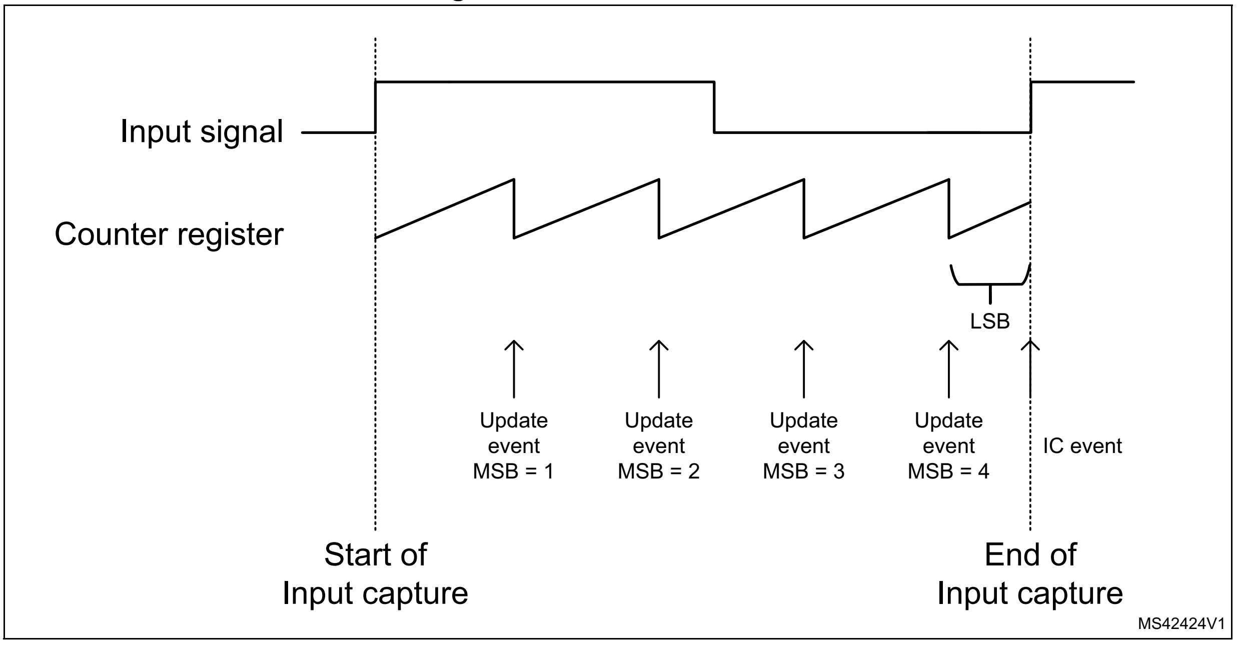
To measure the period of an external signal, the timer can be used in input capture and upcounting mode. Both modes are activated with rising edge of input signal. When counter reaches ARR value (set to maximum 0xFFFF) the MSB is increased. When another rising edge is detected, the LSB is captured.

The external signal frequency is calculated on each master input capture interrupt as

$$\text{ExtSignalFreq} = \frac{\text{SystemCoreClock}}{\text{MSB} \times 65535 + \text{LSB}}$$

The sequence of events is shown in *Figure 3*.

Figure 3. Generation of events



The timer is configured as follows:

- No prescaler is used
- The external signal is connected to channel 2 and the rising edge is configured as the active edge.
- TI1FP1 is selected as the input trigger by setting the TS bits in the SMCR register
- The reset mode is selected as the slave mode, by configuring the SMS bits in the SMCR register so that the counter value is reset every raising edge
- Enable Input Capture and Update interrupts

3.2 Interrupt processing

It might happen that Input Capture and Update interrupts are called simultaneously. In such case is necessary to ensure that the Update interrupt is processed first (and the MSB updated). Only then the Input capture interrupt can be processed, and the frequency of the external input signal computed.

4 32-bit output compare timer resolution

Note: Details of implementation described in this section apply to STM32F10x microcontrollers only, for STM32L0xx and STM32L15x products refer to the dedicated reference manuals and firmwares.

4.1 Principle and timer configuration

The idea is to use two timers to generate a 32-bit resolution output compare signal; one timer that gives the MSB, and the other that provides the LSB of the 32-bit output compare signal.

Compare pulse is one of the master modes offered by the STM32 timers. With the Compare pulse mode selected, each time the CC1IF flag is to be set, that is, as soon as there is a compare match, the master trigger output (TRGO) sends a positive pulse.

In addition, if the timer master is being used in output compare mode, the LSB or MSB part of the 32-bit output compare signal is loaded into the master CCRx register. When the counter of the master reaches the loaded value, it triggers the other timer, causing it to generate the missing MSB or LSB.

To generate the MSB or the LSB part of the output compare signal, the slave timer must wait for the master trigger output signal and then start counting in order to introduce the missing 16-bit (LSB or MSB) part. For this, the slave timer has to be configured in the one-pulse mode (OPM).

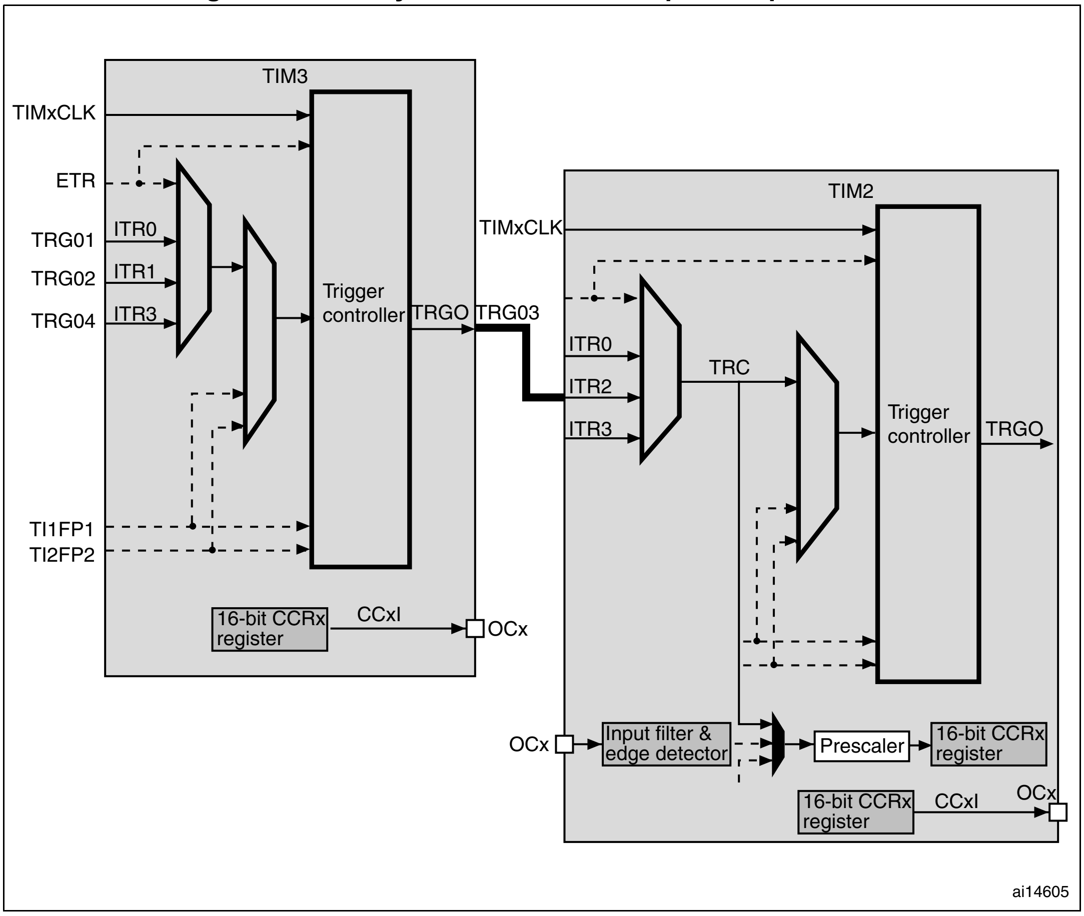
The one-pulse mode is a particular case of the input capture and output compare modes. It allows the counter to be started in response to a stimulus, and to generate a pulse with a programmable length after a programmable delay.

The counter start can be controlled through the slave mode controller and the waveform can be generated in output compare mode. If the one-pulse mode (OPM) is selected by setting the OPM bit in the CR1 register, the counter stops automatically at the next update event.

The STM32 timers offer the possibility of redirecting the internal trigger (ITR) and of using it as the input signal for the capture/compare array. In this case, the internal trigger can be used as a stimulus for a slave timer initially configured in one-pulse mode (OPM). This is done by configuring the CCxS bits in the CCMRx register to be mapped on TRC.

This configuration enables the user to cascade the two timers to obtain a 32-bit time base resolution. *Figure 4* explains how the two timers are cascaded.

Figure 4. Timer synchronization in output compare mode



TIM3 is the master timer used in output compare mode; the trigger output (TRGO3) sends a positive pulse when the CC1IF flag is to be set as soon as a compare match occurs.

To connect the TRGO3 output of TIM3 to TIM2, TIM2 must be configured in slave mode using ITR2 as the internal trigger.

Then the slave mode controller is configured in trigger mode. This causes the TIM2 counter to be started at a rising edge of the TIM3 trigger signal (that corresponds to the TIM3 compare match).

The two timers are configured as described below.

TIM3 master configuration

- configure TIM3 in output compare mode, the CCRx register must be loaded with the LSB or the MSB part of the signal
- use the timer master compare pulse event as the trigger output (TRGO)
- set the prescaler value
- enable the master/slave mode.

TIM2 slave configuration

- TIM2 is used in one-pulse mode, so there are three steps of configuration:
  – the input capture module
  – the output compare module and the trigger controller
  – and the synchronization part.
- to configure the TIM2 timer, the user has to:
  – map TRC onto TIx by writing CCxS = '11' into the TIMx_CCMRx register
  – configure ITR2 as the trigger for the slave mode controller (TRGI) by writing TS = '010' in the TIMx_SMCR register
  – use the trigger mode as the slave mode by writing SMS to '110' in the TIMx_SMCR register: the counter start is controlled by the master
  – configure the output compare mode by setting the right combination of the OCxM bits in the TIMx_CCMRx register (OCxM can be set to '000', '001', '010' or '011'). The CCRx register must be loaded with the MSB or the LSB part
  – set the prescaler value
  – select the output pin by configuring the CCxS bits in the TIMx_CCMRx register
  – enable the one-pulse mode by setting the OPM bit in the TIMx_CR1 register. This causes the counter to stop at the next update event. So the counter start is controlled by the master but the stop is controlled by the counter itself.

4.2 Output compare mode configuration

4.2.1 Output compare active mode example

The following example is calculated for STM32F10x. Therefore, the maximum clock frequency is considered as 72 MHz. For STM32L1xx, 32 MHz has to be used instead.

Master configuration

TIM3 is used as the master timer in output compare active mode. For STM32F10x, TIM3CLK is equal to 72 MHz, no prescaler is used, so the TIM3 counter clock is equal to:

TIM3 counter clock = TIM3CLK/(prescaler + 1) = 72 MHz

TIM3 generates the LSB part of the 32-bit output compare delay, and this delay value is loaded into the CCR1 register.

Slave configuration

TIM2 is used as the slave timer in one-pulse mode as described below:

- channel 1, channel 2 and channel 3 are used in output compare active mode. The corresponding CCRx registers are loaded with the MSB part
- the prescaler is set to 0xFFFF
- the trigger mode is used as the slave mode

TIM2 is a slave for TIM3 so ITR2 is used as the internal trigger (TS = ‘010’ in TIM2_SMCR register).

In one-pulse mode, the edge detection on TIM2 IC4 (TRC) sets the TIM2 counter enable (CEN) bit, which enables the counter.

When a match is found between the capture/compare register and the counter, the output compare function assigns the corresponding output pin with a programmable value determined by the output compare mode and the output polarity. In this example, after the programmed delays, the TIM2 pins are set to their active mode.

In this example, the three capture compare register values are TIM2_CCR1 = MSB1 = 0xC000, TIM2_CCR2 = MSB2 = 0xA000 and TIM2_CCR3 = MSB3 = 0x8000, respectively. TIM3_CCR1 = LSB = 0x8534.

The equations of the TIM2 output compare delays are given below.

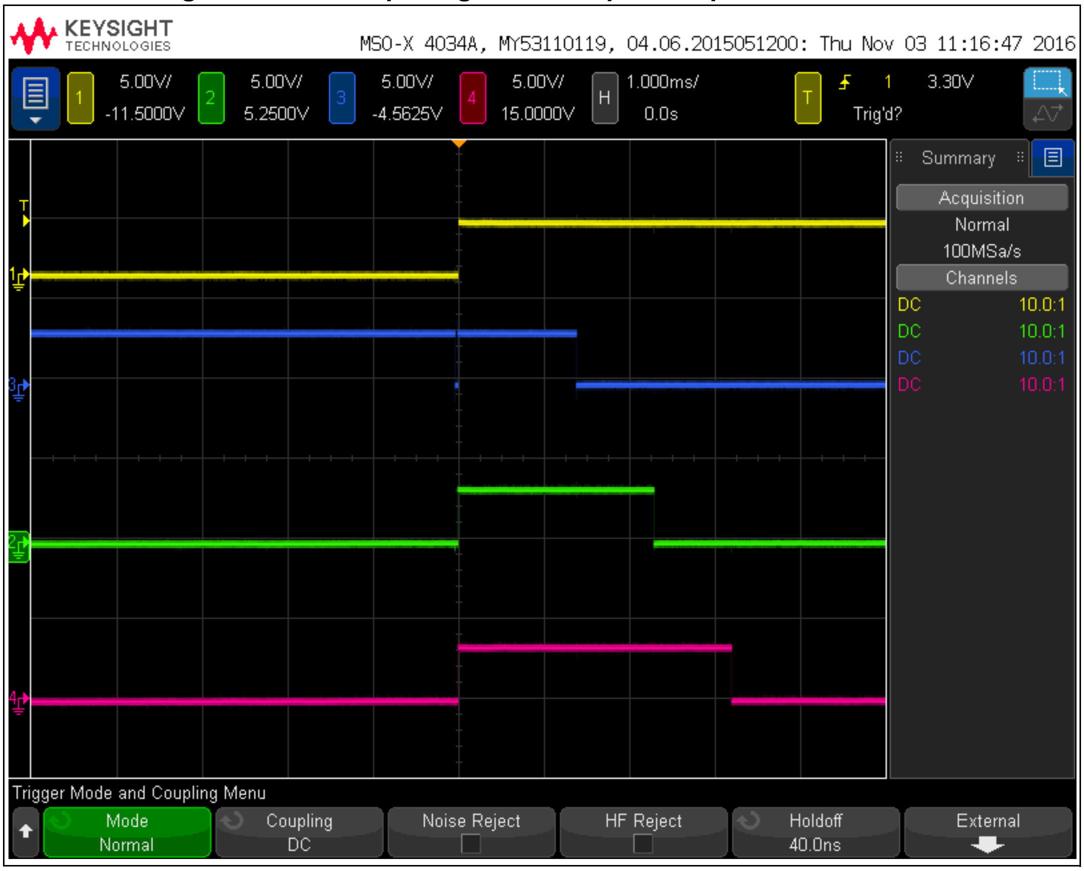
$$\text{CC1 delay} = \frac{\text{MSB1} \times 65536 + \text{LSB}}{72 \times 10^6}, \text{ which gives CC1 delay} = 44.74 \text{ s}.$$

$$\text{CC2 delay} = \frac{\text{MSB2} \times 65536 + \text{LSB}}{72 \times 10^6}, \text{ which gives CC2 delay} = 37.28 \text{ s}.$$

$$\text{CC3 delay} = \frac{\text{MSB3} \times 65536 + \text{LSB}}{72 \times 10^6}, \text{ which gives CC3 delay} = 29.82 \text{ s}$$

Figure 5 shows the three signals.

Figure 5. TIM2 output signals in output compare active mode



4.2.2 Output compare toggle mode example

The following example is calculated for STM32F10x. Therefore, the maximum clock frequency is considered to be 72 MHz, while 32 MHz must be used for STM32L1xx and STM32L0xx.

Master configuration

TIM3 is used as the master timer in output compare toggle mode. TIM3CLK is equal to 72 MHz. The prescaler is set to 0xFFFF.

TIM3 generates the MSB part of the 32-bit output compare delay, and this delay value is loaded into the CCR1 register.

Slave configuration

TIM2 is used as the slave timer in one-pulse mode as described below:

- channel 1, channel 2 and channel 3 are used in output compare toggle mode. The corresponding CCRx registers are loaded with the LSB part
- the prescaler is set to 0x0
- the trigger mode is used as the slave mode.

TIM2 is a slave for TIM3 so ITR2 is used as the internal trigger (TS = ‘010’ in TIM2_SMCR register).

In one-pulse mode, the edge detection on TIM2 IC4 (TRC) sets the TIM2 counter enable (CEN) bit, which enables the counter.

When a match is found between the capture/compare register and the counter, the output compare function assigns the corresponding output pin with a programmable value determined by the output compare mode and the output polarity. In this example, when the match is found between the counter and the TIM2_CCRx registers, the TIM2 pins toggle and capture compare interrupts are generated. In the corresponding routine, the TIM2_CCRx registers are updated in order to have three periodic signals with three different frequencies.

In this example, the three capture compare register values are TIM2_CCR1 = LSB1 = 0x5FFF, TIM2_CCR2 = LSB2 = 0x9FFF and TIM2_CCR3 = LSB3 = 0xEFFF, respectively. TIM3_CCR1 = MSB = 0x1.

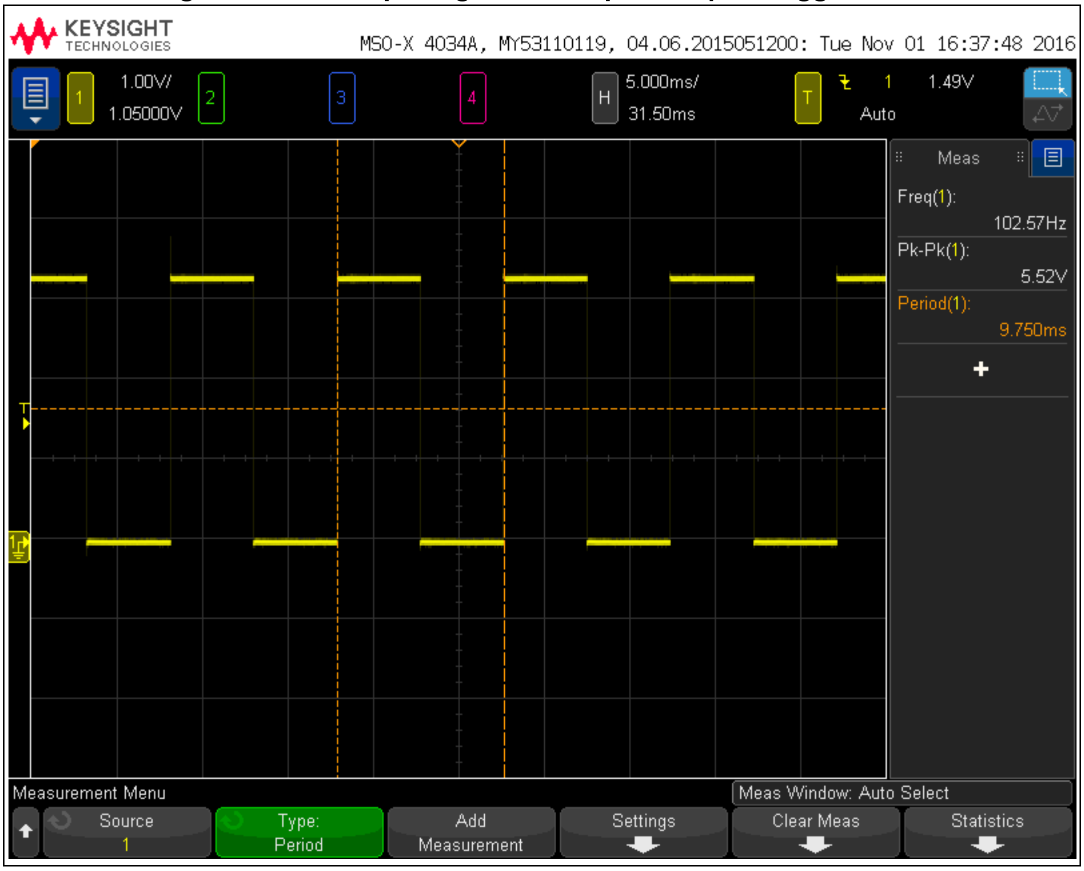
$$\text{CC1 delay} = \frac{\text{MSB} \times 65536 + \text{LSB1}}{72 \times 10^6}\text{, which gives: CC1 delay} = 1.25\ \text{ms}.$$

$$\text{CC2 delay} = \frac{\text{MSB} \times 65536 + \text{LSB2}}{72 \times 10^6}\text{, which gives: CC2 delay} = 1.48\ \text{ms}.$$

$$\text{CC3 delay} = \frac{\text{MSB} \times 65536 + \text{LSB3}}{72 \times 10^6}\text{, which gives: CC3 delay} = 1.76\ \text{ms}.$$

Figure 6 shows the three signals.

Figure 6. TIM2 output signals in output compare toggle mode



5 Conclusion

The described methods and algorithms indicate how to overcome some product limitations, allowing the user to implement features available only in more performing product lines.

The described examples demonstrate the difference in code size and overall performance.

The LowLayer version (STSW-STM32009) requires approximately only one quarter of overall system resources, while the one based on Cube (X-CUBE-TIM-32RES) is much more robust.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
31-Aug-2007	1	Initial release.
11-Jan-2011	2	Changed part number references to STM32F10x.
25-Jun-2013	3	Added STM32L15x part number. Changed “The maximum frequency” to “The frequency range” in *Section 2.1: Principle* and added a note. Changed “the maximum frequency” to “the lowest frequency” in *Section 2.2.3: Master and slave synchronization* and added a note. Added an introduction to *Section 4.2.1: Output compare active mode example* and to *Section 4.2.2: Output compare toggle mode example*. Updated *Figure 5* and *Figure 6* titles. Updated the disclaimer.
16-Nov-2016	4	Extended document scope to STM32L0xx with introduction of X-CUBE-TIM-32RES firmware, hence updated document title, *Introduction* and *Section 5: Conclusion*. Removed former *Table 1: Applicable products* and former *Figure 6: TIM2 Channel 1 output signal in output compare toggle mode*. Added *Section 3: 32-bit input capture resolution using one timer* and *Note:* in *Section 4: 32-bit output compare timer resolution*. Updated *Section 1.1: Timer link system presentation*, *Section 1.2: How to synchronize two timers using the link system*, *Section 2: 32-bit input capture timer resolution*, *Section 2.1: Principle*, *Section 2.2.3: Master and slave synchronization*, *Section 4.2.1: Output compare active mode example* and *Section 4.2.2: Output compare toggle mode example* Updated *Figure 5: TIM2 output signals in output compare active mode* and *Figure 6: TIM2 output signals in output compare toggle mode*.

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