AN2439
Application note

27 W Output power ultra wide range input flyback converter

Introduction

As the telecommunications market grows, the need for suitable PSUs (Power Supply Unit) for equipment grows as well. For products used in telecommunications, the available voltage is either the mains voltage (from 88 V_{AC} to 265 V_{AC}) or 48 V_{DC} (from 36 V_{DC} to 72 V_{DC}). Power supplies that are able to manage input AC voltage in the full range of 88Vrms to 265Vrms are quite common while ultra wide range (from 36 V_{DC} to 264 V_{AC}) power supplies are not as common. The main advantage in using a UWR PSU is the savings in design and qualification. Instead of designing and qualifying two PSUs, the work is done once. Cost advantages come from bigger volume production as there is just one product that meets a larger range of electrical specifications.

Disadvantages are the difficulties in having a high performance system in working condition. This application note describes a UWR flayback converter that can be used to supply a DSLM (DSL Multiplexer).

The advantage in using a flyback converter in this application is the moderate variation of the duty cycle with the input voltage. The main drawback is the high value of the rms current in the secondary winding, in the output diode and in the output capacitor.

Contents

1 Board description

The electrical specifications for this converter are listed in the table below:

Table 1. Electrical specifications

Item	Value
Isolated	Yes
Input	AC and DC voltage
Minimum DC input voltage	36 V
Maximum DC input voltage	72 V
Minimum AC input voltage	88 V
Maximum AC input voltage	265 V
Number of outputs	2
Output voltage 1	5 V
Output voltage 2	3.3 V
Maximum output current 1	2 A
Maximum output current 1	5 A
Maximum precision error on output 1	3%
Maximum precision error on output 2	3%
Total output power	27 W

As already specified, the selected topology is a flyback converter. In continuous mode the relation between output and input voltage of the converter is:

Equation 1

$$\frac{V_{OUT}}{V_{IN}} = n \bullet \frac{D}{1-D} \Rightarrow D = \frac{n \bullet V_{OUT}}{V_{IN} + n \bullet V_{OUT}} = \frac{V_R}{V_{IN} + V_R}$$

Where n is the turn ratio and V_R the reflected voltage. It is easy to verify that for an input voltage that changes between 36 V and 375 V $(375V = 2 \bullet 265)V$ and 70 V as reflected voltage, the duty cycle changes from about 70% (at minimum input voltage) to about 16%.

Buck type topologies are not suitable because the duty cycle varies widely (from 9%- to 90% for a forward converter in the same condition for example), worsening the efficiency and making the design very complex.

A second design choice was to use a switching post regulator that has, as input voltage, the output voltage of the flyback and the output as 3.3 V. The purpose of this is to meet the requested precision in both outputs and to avoid using another secondary winding where the root mean square current would be very high. Assuming a 90% of efficiency for this step down converter, the total current sunk from the output of the flyback is 5.7 A. The buck converter for the post regulation is described in *Section 1.4 on page 7*.

In order to limit the high root mean square current at the secondary side, another design choice was to have a flyback converter that works, most of the time, in continuous conduction mode. The controller used in this application is the L5991 [*1.*] which is a current

mode controller. In continuous conduction mode for the lower input voltages, the duty cycle is greater than 50% which requires a slope compensation to ensure stable operation of the current loop. The slope compensation is implemented through a circuit described in *Section 1.2 on page 5*.

The switching frequency was selected to be equal to 70 kHz and the reflected voltage to be equal to 70 V.

In order to have the same wake-up time for the different input voltages, an active start-up was implemented instead of the most commonly used passive circuits. The active start-up circuit is described in *Section 1.1*.

In order to improve efficiency, the converter has two different inputs, one for the AC voltage (88 V_{ACrms} to 265 V_{ACrms}) and one for the DC voltage (36 V_{DC} to 72 V_{DC}). The input stage of the converter is described in *Section 1.3 on page 7*.

1.1 Active start-up with external high voltage current source [2.]

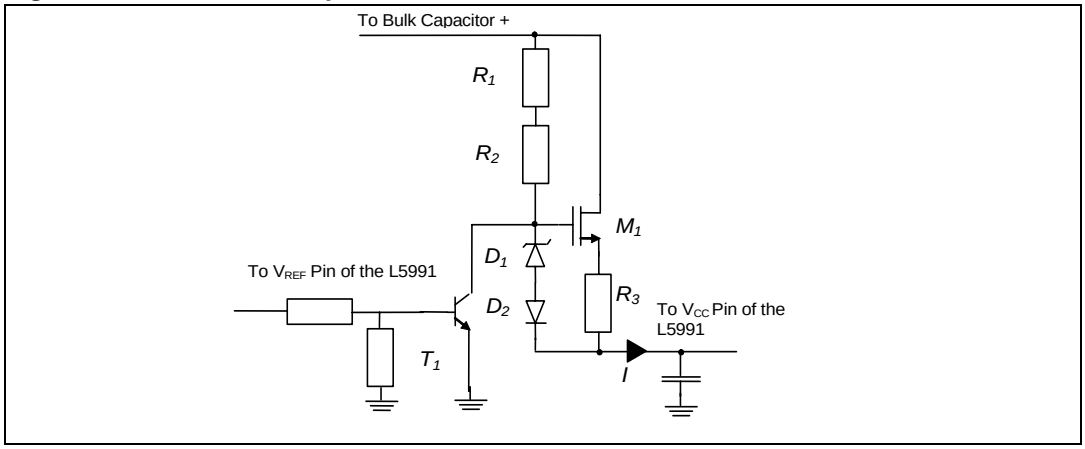
The circuit of the active start-up is shown in *Figure 1*. Through R_1 and R_2 the 600 V MOSFET M_1 (STQ1NK60ZR) is switched on. The back-to-back diodes (D_1 is a 15 V zener diode and D_2 is a standard diode 1N4148) are used to set the voltage between the gate and the resistor R_3 pin not connected with the source of M1. The resistor R_3 is used to limit the current provided to the capacitor connected to V_{CC} of the L5991. The circuit behaves as a constant current generator and its current can be calculated according to the following equation:

Equation 2

$$I = \frac{V_Z - V_d - V_{TH}}{R_3}$$

Where V_Z is the D_1 zener break-down voltage, V_d the diode D_2 voltage drop when forward biased and V_{TH} is the gate to source on threshold voltage of the MOSFET M_1.

Figure 1. Active start up circuit



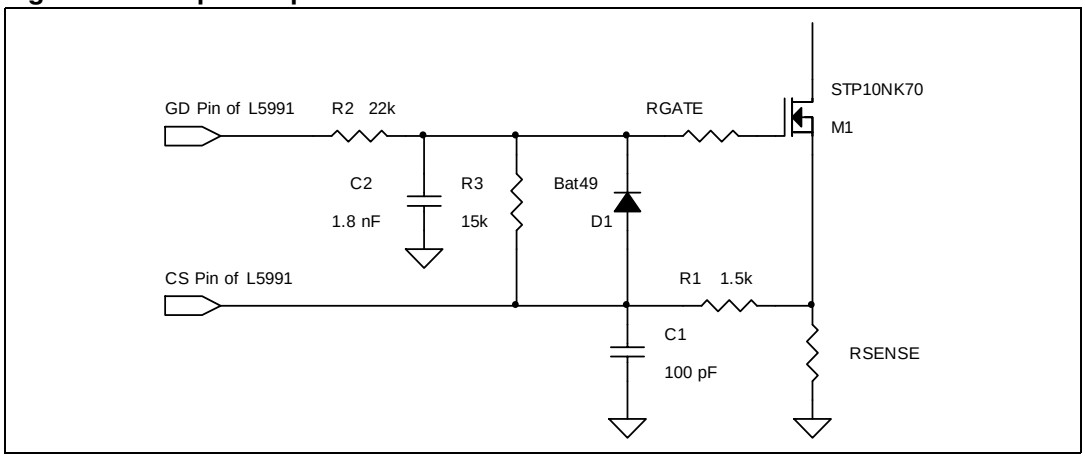
When we connect the converter to the mains, the controller (L5991) is initially off, and the small signal bipolar transistor T_1 is also off. The gate of the MOSFET M_1 is biased through R_1 and R_2 and the current generator starts to work charging the V_{CC} capacitor. As the V_{CC} voltage exceeds its On Threshold, the L5991 starts to operate and sets the V_{REF} pin (pin 4) to 5 V. This voltage turns on the small bipolar transistor T_1 that pulls down the gate of M_1

switching it off. As a result, as the controller is on, the current generator stops working, and the controller is supplied by the auxiliary winding of the flyback converter.

1.2 Slope compensation

The circuit for slope compensation is shown in *Figure 2*. When the main MOSFET (STP10NK70Z) is switched on, the GD pin (Gate Driver) of the L5991 goes high up to a voltage of about 14 V. Capacitor C_2 is charged through resistor R_2. If the time constant RC is large enough, compared to the switching period, we can assume that the voltage across capacitor C_2 is a linear ramp. This voltage is added to the CS pin (Current Sense) through the partition divider R_3, R_1+R_{SENSE} and provides the needed slope compensation. When the MOSFET M_1 is switched off, the gate driver pin of the L5991 pulls down the anode of diode D_1. Capacitor C_2 is then fast discharged and ready for the next cycle.

Figure 2. Slope compensation circuit



Equation 3 gives the waveform expression of the voltage across the capacitor C_2. In this formula V_D is the forward voltage drop on diode D_1 and V_{GD} is the voltage on gate driver pin of the L5991 (Pin 10), when it is high. As a rule of thumb, in order to have approximately a linear ramp across C_2, the time constant C_2R_T is selected in the range of ten times the switching period.

Equation 3

$$V_C(t) = V_{GD} \bullet \frac{R_1 + R_3 + R_{SENSE}}{R_1 + R_2 + R_3 + R_{SENSE}} \bullet \left(1 - e^{\frac{-t}{C_2 \bullet R_T}}\right) + V_D \bullet e^{\frac{-t}{C_2 \bullet R_T}}$$

Neglecting R_{SENSE} it can be simplified as:

Equation 4

$$V_C(t) \cong V_{GD} \bullet \frac{R_1 + R_3}{R_1 + R_2 + R_3} \bullet \left(1 - e^{\frac{-t}{C_2 \bullet R_T}}\right) + V_D \bullet e^{\frac{-t}{C_2 \bullet R_T}}$$

R_T is the equivalent resistance across capacitor C_2:

Equation 5

$$R_\tau = \frac{R_2 \bullet (R_1 - R_3 - R_{SENSE})}{R_1 + R_2 + R_3 + R_{SENSE}} \cong \frac{R_2 \bullet (R_1 - R_3)}{R_1 + R_2 + R_3}$$

The slope compensation voltage added on CS Pin of the L5991 is:

Equation 6

$$V_s(t) = \frac{R_1 - R_{SENSE}}{R_2 + R_3 + R_{SENSE}} \bullet V_C(t) \cong \frac{R_1}{R_2 + R_3} \bullet V_C(t)$$

We know that if we add a ramp whose slope is one half of the primary side equivalent demagnetizing current slope (m_a), the current loop is stable for any duty cycle lower than one. As consequence the requested amount of slope compensation needed to guarantee stable operation is:

Equation 7

$$m_S = \frac{1}{2} \bullet \frac{V_R}{L_m} \bullet R_{SENSE}$$

In the last equation V_R is the reflected voltage and Lm the magnetizing inductance at primary side. The value of R_{SENSE} has to be calculated taking into account the slope compensation we add and of course the maximum peak current at the primary side (I_{PKP}).

Equation 8

$$R_{SENSE} = \frac{1V}{I_{PKP} + \frac{1}{2} \bullet \frac{V_R}{L_m} \bullet \frac{D_{MAX}}{f_{sw}}}$$

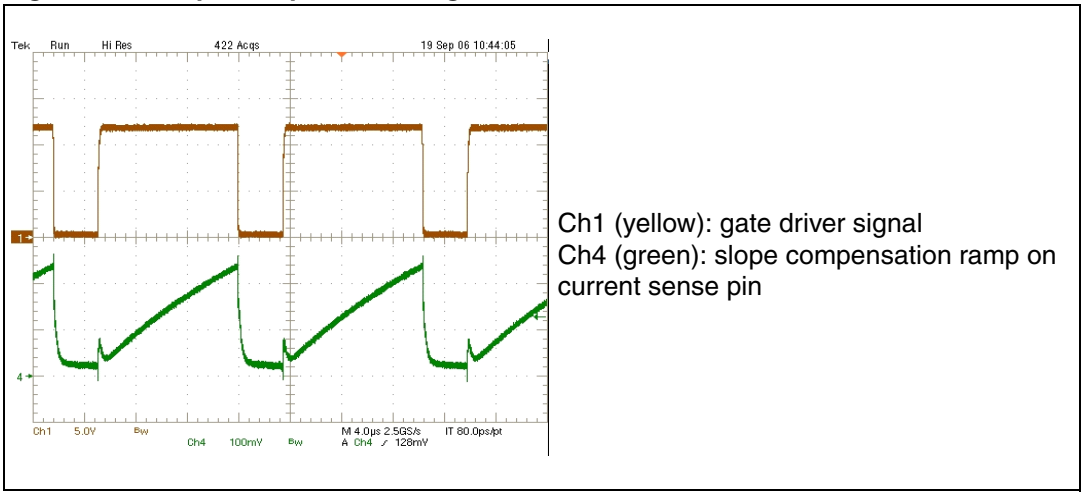
The maximum value of the voltage we add at the current sense pin is:

Equation 9

$$V_{SMAX} = m_s \bullet \frac{D_{MAX}}{f_{sw}} = \frac{R_1}{R_2 + R_3} \bullet V_C\left(\frac{D_{MAX}}{f_{sw}}\right)$$

Figure 3 shows the gate driver signal and the slope compensation signal measured at the CS pin.

Figure 3. Slope compensation signal



Ch1 (yellow): gate driver signal
Ch4 (green): slope compensation ramp on current sense pin

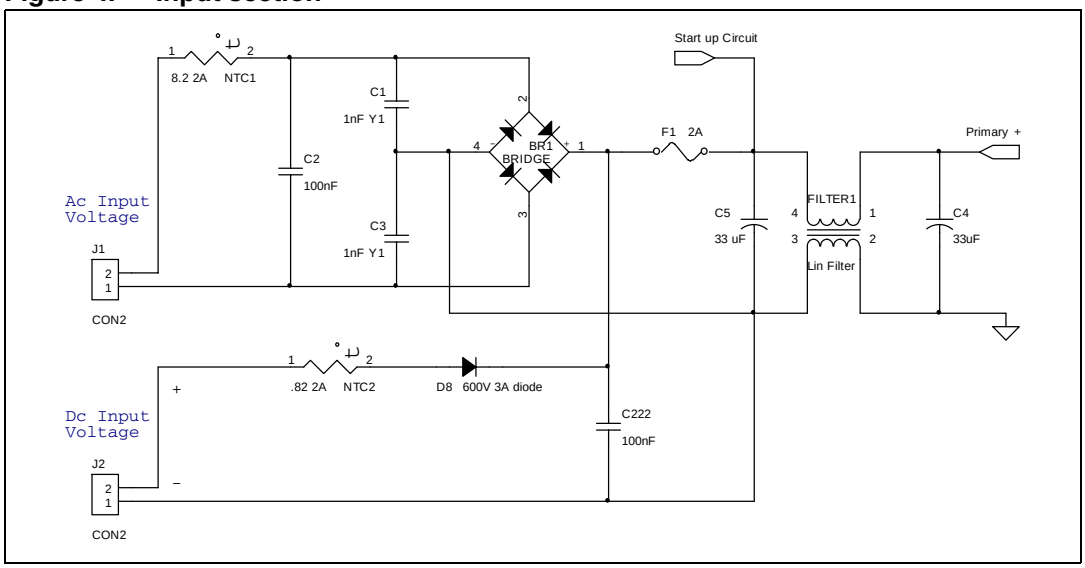
1.3 Input section

The schematic of the input section is given in *Figure 4*. We used two separated connectors for the AC input voltage (88 V_{AC} to 265 V_{AC}) and for the DC input voltage (36 V_{DC} to 72V_{DC}). The system works correctly if we feed the converter with the Dc voltage in the AC input voltage connector. We used a separated connector in order to gain efficiency.

Using the additional connector for the Dc input voltage we use two different NTCs to limit the inrush current in the two cases. NTC1 has to limit the inrush current, considering as worst case the maximum AC Peak input voltage. NTC2 has to limit the inrush current, considering as worst case the maximum DC voltage (72 V) which means that NTC2 can be lower than NTC1 and dissipates less energy.

The DC voltage is connected to the bulk capacitors through one diode (used for protection in case we connect the Dc input with the wrong polarity) so we cut one half of power dissipation compared to the power we would dissipate in the bridge.

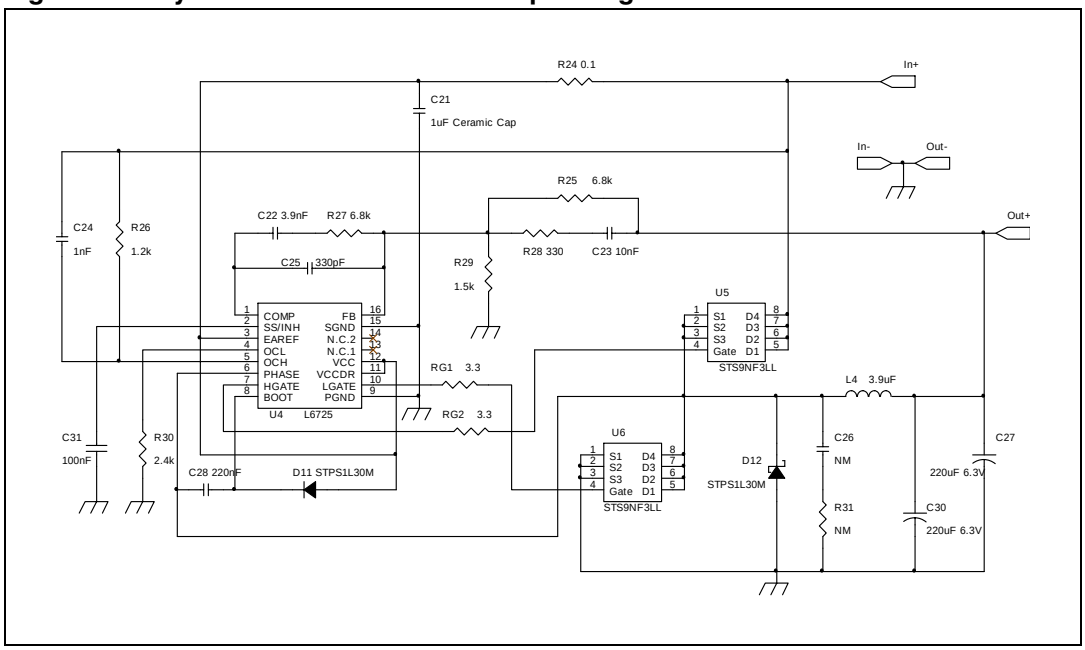
Figure 4. Input section



1.4 Buck DC-DC converter post regulator [3.]

The second output of 3.3 V, able to provide up to 5 A to its load, is obtained using a switching post regulation. The post regulator is a synchronous buck converter based on the L6725 controller and the schematic is given in *Figure 5*.

Figure 5. Synchronous buck converter post regulator



The two MOSFET STS12NF3LL (U5 and U6 in the schematic) are driven with 180 degrees of phase shift. The gate driver signal value is 5 V when high, as the L6725 is supplied with the 5 V that is, the output of the flyback main converter.

This situation is not optimum for the two MOSFETs, as their R_{DSON} is higher when the gate signal is 5 V compared to when the gate signal is 10 V [4.]. It could seem that the two MOSFETs are oversized, but taking into account the low driving signal, they are not.

1.5 Flyback converter

The primary side of the flyback converter schematic is given in *Figure 6* and the secondary side is given in *Figure 7*.

The bill of material of the entire circuit is given in *Table 2*, *3*, *4*, and *5*.

Figure 6. Flyback converter primary side schematic

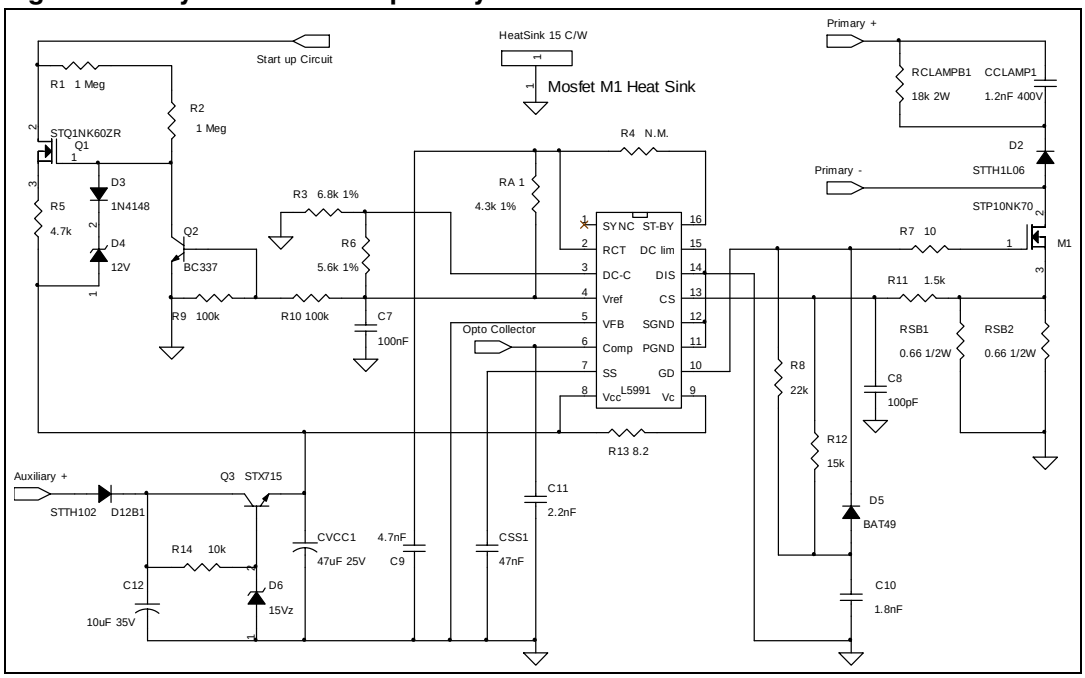


Figure 7. Flyback converter secondary side schematic

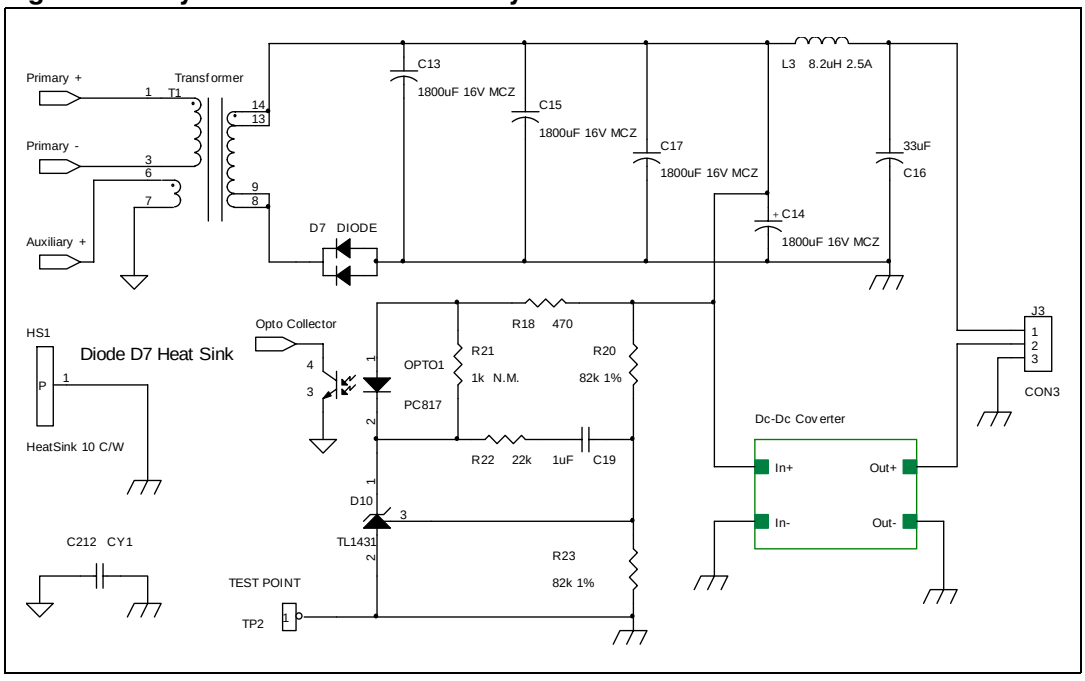


Table 2. Input section (schematic *Figure 4*)

Quantity	Part reference	Part name	Description
1	BR1	Bridge	600 V 3 A Bridge diodes
2	C3,C1	1 nF Y1	
1	C2, C222	100 nF	
1	NTC2	.82 2[a]	
1	D8	600 V 3 A	600 V 3 A diode
1	F1	2 A	
2	C4, C5	33 µF	400 V Electrolytic capacitor
1	Filter1	4.7 mH 3A	Line filter
1	NTC1	8.2 2[a]	

Table 3. Primary side flyback converter (schematic *Figure 6*)

Quantity	Part reference	Part name	Description
2	R2,R1	1 Meg	
1	R5	4.7 k	
2	R10,R9	100 k	
1	R3	6.8 k 1%	
1	R6	5.6 k 1%	
1	R14	10 k	
1	RA1	4.3 k 1%	
1	R4	N.M.	
1	R13	8.2	
1	R12	15 k	
1	R8	22 k	
1	R7	10	
1	R11	1.5 k	
2	RSB2,RSB1	0.66 1/2 W	
1	RCLAMPB1	18 k 2 W	
1	U2	L5991	STMicroelectronics primary controller with standby
1	D2	STTH1L06	STMicroelectronics turbo 2 ultra fast high voltage rectifier
1	D3	1N4148	
1	D4	12Vz	12 V Break down Zener diodeo
1	D5	BAT42	STMicroelectronics small signal Schottky diode

Table 3. Primary side flyback converter (schematic *Figure 6*) (continued)

Quantity	Part reference	Part name	Description
1	D6	15Vz	
1	Q1	STQ1NK60ZR	STMicroelectronics N-CHANNEL 600 V SuperMESH™ MOSFET
1	Q2	BC337	
1	Q3	STX715	STMicroelectronics NPN transistor
1	U1	HeatSink 15 C/W	
1	M1	STP10NK70Z	STMicroelectronics N-Channel 700 V Zener-protected SuperMESH™ MOSFET
1	D12B1	STTH102	STMicroelectronics high efficiency ultra fast diode
1	C12	10 µF 35 V	
1	CVCC1	47 µF 25 V	
1	CCLAMP1	1.2 nF 400 V	
1	CSS1	47 nF	
1	C8	100 pF	
1	C9	4.7 nF	
1	C10	1.8 nF	
1	C11	2.2 nF	
4	C2	100 nF	

Table 4. Secondary side flyback (schematic *Figure 7*)

Quantity	Part reference	Part name or value	Description
1	C212	CY1	
1	C16	33 µF	
4	C13, C14, C15, C17	1800 µF 16 V MCZ	Rubycon high current low ESR electrolytic capacitor
1	C19	1µF	
1	D7	STPS16H100	STMicroelectronics high voltage power Schottky rectifier
1	T1	Transformer	
1	D10	TL1431	STMicroelectronics programmable voltage reference
1	C24	1nF	
1	R18	470	
2	R20,R23	82 k 1%	

Table 4. Secondary side flyback (schematic *Figure 7*) (continued)

Quantity	Part reference	Part name or value	Description
1	R21	1k N.M.	
1	L3	8.2uH 2.5°	
2	R22,R8	22k	
1	OPTO1	PC817	Optocoupler

Table 5. DC-DC converter (schematic *Figure 4*)

Quantity	Part reference	Part name or value	Description
1	C25	330 pF	
1	R24	0.1 Ω	
2	R25,R27	6.8 kΩ	
1	R26	1.2 kΩ	
1	R28	330 Ω	
1	R29	1.5 kΩ	
1	R30	2.4 kΩ	
1	R31	N.M.	
2	RG2,RG1	3.3 Ω	
1	C21	1 µF	Ceramic capacitor
1	C22	3.9 nF	
1	C23	10 nF	
1	C24	1 nF	
1	C25	330 pF	
1	C26	N.M.	Not mounted
1	C27, C30	220 µF 6.3 V ZA	Rubycon ZA electrolytic capacitor
1	C28	220 nF	
4	C31	100 nF	
2	D12,D11	STPS1L30M	STMicroelectronics low drop power Schottky rectifier
1	L4	3.9 µF	6A Rated current inductor
1	U4	L6725	STMicroelectronics low cost adjustable step-down controller
2	U5,U6	STS12NF3LL	STMicroelectronics N-Channel 30 V low gate charge STripFET™ II Power MOSFET

1.6 Transformer

The details of the transformer used are listed below.

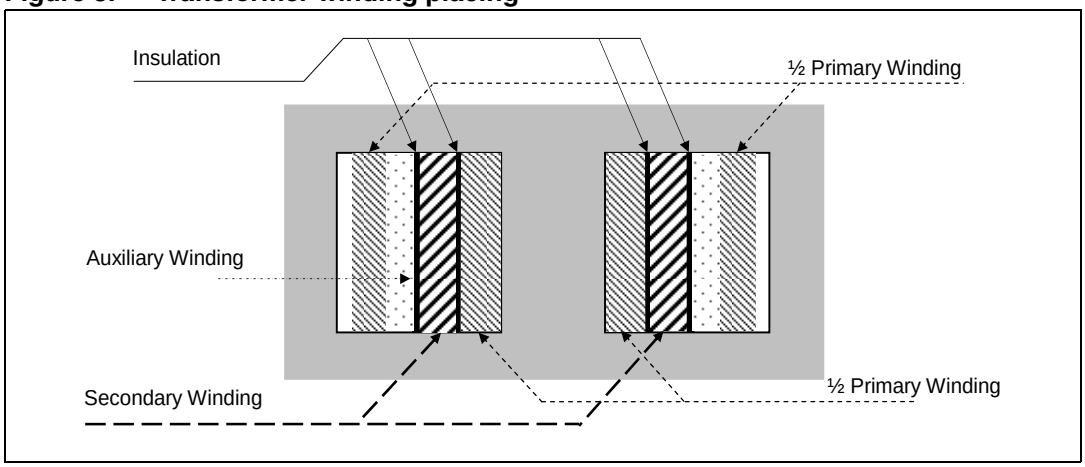
- Electrical characteristics
  - Primary inductance value: 450 µH
  - Primary leakage inductance: 12 µH
- Magnetic core
  - Material: N67
  - Type: ETD29
  - Air gap: ≈ 0.2 mm

Table 6. Winding size

Winding	Number of turns	Wire size
Primary winding	46	AWG26
Secondary winding	4	AWG26X4
Auxiliary winding	10	AWG40

Figure 8 describes the used and suggested placing of the windings.

Figure 8. Transformer winding placing



1.7 Board tests

The tests performed aim to evaluate the converter behavior in terms of efficiency, safe operating area of the devices, and line and load regulation.

1.8 Start-up tests

In a flyback converter the most critical conditions for the mains switch (when no abnormal event occurs), in terms of maximum drain current and of maximum drain voltage, are during the start-up phase. The max values for drain voltage and current were measured in both full

load and no load condition that are the two extreme points in terms of load and for minimum, maximum, and nominal input voltages. The results are shown in *Table 7*.

Table 7. Start-up measures

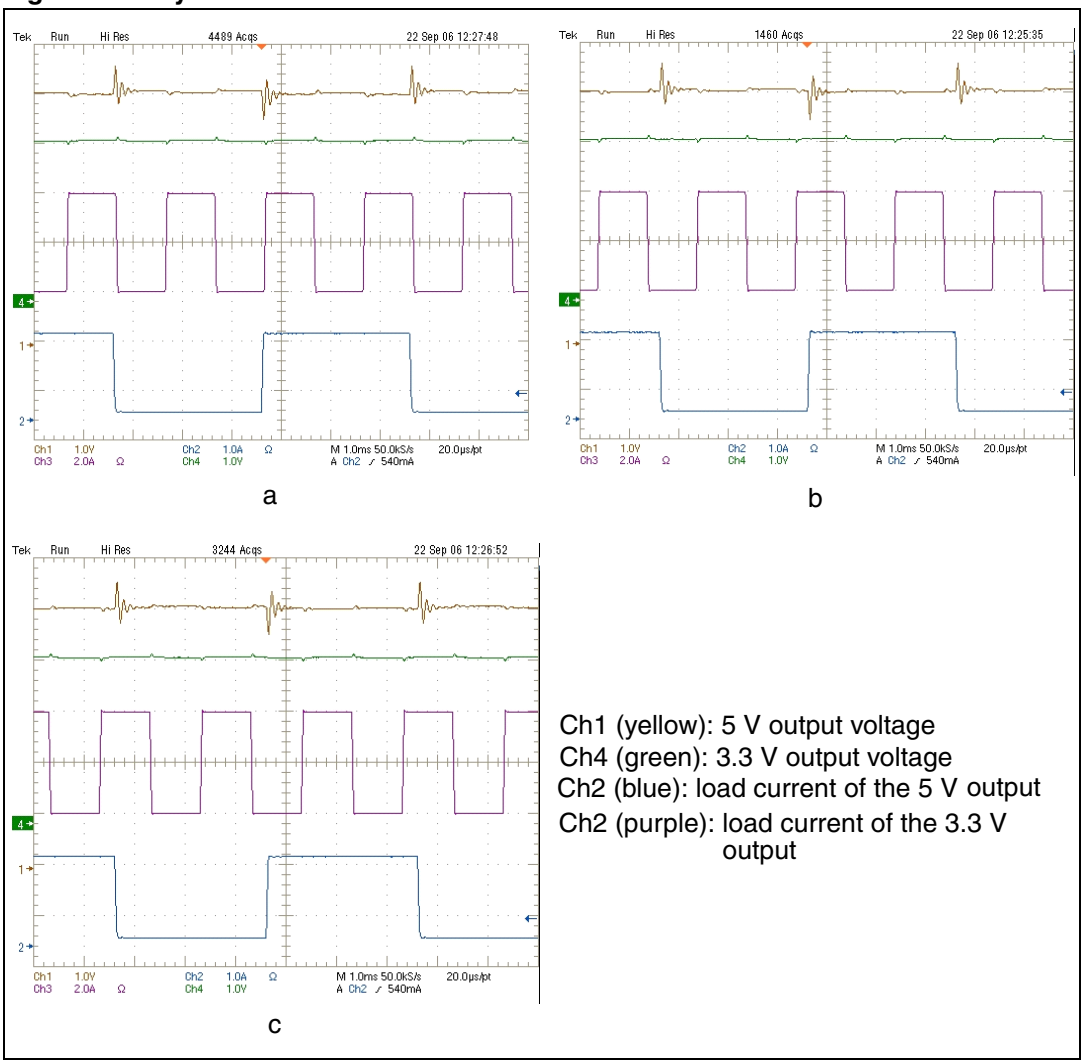
V_{in}	$V_{drainMax}$(V)		$I_{drainMax}$(A)	
	No load	Full load	No load	Full load
36 V_{DC}	235	288	2.03	2.55
48 V_{DC}	256	313	2.09	2.66
72 V_{DC}	277	320	2.07	2.50
88 V_{AC-rms}	320	318	2.06	2.26
115 V_{AC-rms}	362	391	2.18	2.45
230 V_{AC-rms}	526	543	2.37	2.54
265 V_{AC-rms}	562	581	2.13	2.5

The drain voltage is well below the break down voltage of the MOSFET. In the worst case there is at least 100 V of safety margin. The maximum peak value of the drain current, during the start-up phase, is higher then the steady state value (around 2 A). The difference is not too high, thanks also to the soft start, and it means that there is no risk for the transformer to saturate during start-up.

1.9 Dynamic load regulation tests

The behavior of the system was verified also in dynamic load condition. Both loads are square wave shaped. Both have step change between 10% and 90% of their respective maximum nominal load and vice versa. The results are shown in *Figure 9*.

Figure 9. Dynamic load waveforms



1.10 Steady state tests

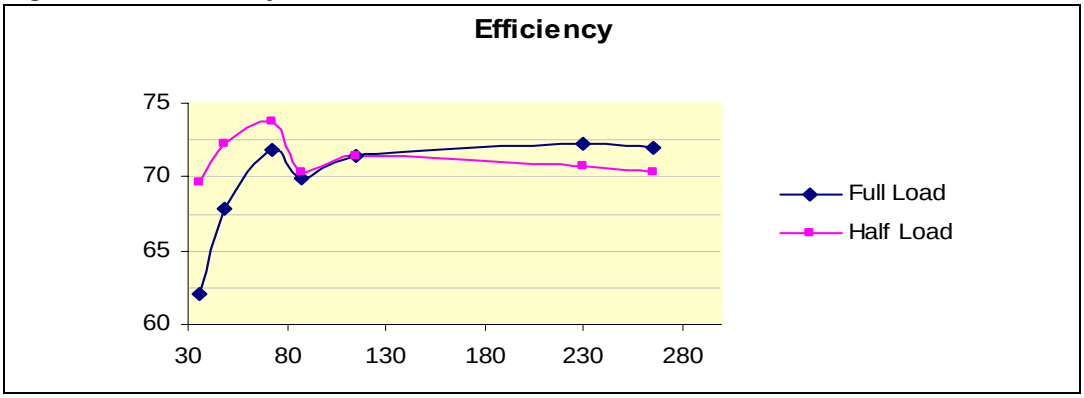
The aim of these tests is to evaluate the performance of the converter in steady state condition, measuring the converter efficiency for minimum, maximum and nominal input voltages.

Table 8. Steady state full load and half load condition efficiency measures

V_{in} (V)	Full load			Half load		
	P_{IN} (W)	P_{OUT} (W)	η(%)	P_{IN} (W)	P_{OUT} (W)	η(%)
36 V_{DC}	43.5	27	62	19.4	13.5	70
48V_{DC}	39.8	27	68	18.7	13.5	72
72V_{DC}	37.6	27	72	18.3	13.5	74
88V_{AC}	38.6	27	70	19.2	13.5	70
115 V_{AC}	37.8	27	71	18.9	13.5	71
230V_{AC}	37.4	27	72	19.1	13.5	71
265V_{AC}	37.5	27	72	19.2	13.5	70

The efficiency as it is possible to see from *Table 8* is not high, ranging between 64% and 72% in full load condition and between 70% and 74% in half load condition. The main reason of this poor efficiency is the high power dissipation on the output diode of the flyback (more than 5 W at low input voltage) that returns to the rest of the flyback converter. The transformer has to deliver more power than necessary, increasing the losses on the transformer itself. Because of this, the power MOSFET has to conduct more current than necessary. The Input section is also affected because the diode or the bridge diodes and the NTC have to conduct higher current.

Figure 10. Efficiency chart



1.11 Static load and line regulation

These tests aim to evaluate the precision of the output voltage and how it is affected by line voltage and load in steady state condition. *Table 9* and *Table 10* show the output voltages in different load conditions for different input voltages. For the 5 V output the minimum and maximum values are 5.099 V and 5.145 V inside the tolerance specified in *Table 1*. The

minimum and maximum values for the 3.3 V output are 3.348 and 3.357 which are both inside the tolerance.

Table 9. Static line and load regulation

V_{in} (V)	Both output in full load		Both output in no load	
	V_{OUT1} (V)	V_{OUT2} (V)	V_{OUT1} (V)	V_{OUT2} (V)
36 V_{DC}	5.099	3.357	5.145	3.351
48 V_{DC}	5.099	3.355	5.145	3.351
72 V_{DC}	5.100	3.354	5.144	3.351
88 V_{AC}	5.100	3.355	5.145	3.350
115 V_{AC}	5.100	3.355	5.145	3.350
230 V_{AC}	5.100	3.352	5.145	3.350
265 V_{AC}	5.100	3.352	5.145	3.351

Table 10. Static line regulation and crossed load regulation

V_{in} (V)	V_{OUT1} Full load V_{OUT2} no load		Vout1 No load Vout2 full load	
	V_{OUT1} (V)	V_{OUT2} (V)	V_{OUT1} (V)	V_{OUT2} (V)
36 V_{DC}	5.116	3.348	5.129	3.357
48 V_{DC}	5.116	3.348	5.129	3.357
72 V_{DC}	5.116	3.348	5.129	3.357
88 V_{AC}	5.117	3.349	5.129	3.356
115 V_{AC}	5.117	3.349	5.129	3.356
230 V_{AC}	5.117	3.349	5.129	3.356
265 V_{AC}	5.117	3.349	5.129	3.356

Figure 11 and *Figure 12* show the drain voltage (Ch3, purple waveform) and current (Ch2 blue waveform) of the flyback MOSFET. *Figure 11* shows the waveforms when the circuit is fed with the input voltage of 36 V_{DC}, which is the minimum input voltage, and *Figure 12* shows when the input is 265 V_{AC} which is the maximum input voltage.

The load is the maximum for both the output. *Figure 11* and *Figure 12* allow comparing the difference between the two extreme points of the input voltage range. When the input is at its minimum, the flyback is working in continuous mode with a peak current close to 2 A and a maximum duty cycle near to 75%. When the input voltage is at its maximum, the system works in discontinuous mode with a duty cycle close to 15% and a peak current of about 1.8 A. *Figure 13* shows the same waveforms when circuit is fed with the nominal values of the input voltage (48 V_{DC}, 115 V_{AC} and 230 V_{AC}) and in full load condition.

Figure 11. Steady state waveforms with minimum and maximum input voltage - full load at 36 V_{DC}

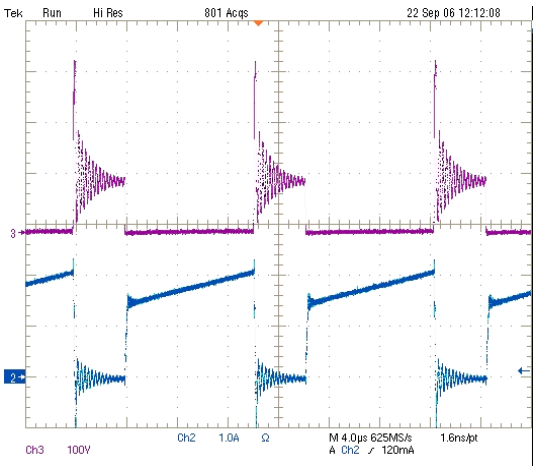


Figure 12. Steady state waveforms with minimum and maximum input voltage - full load at 264 V_{AC}

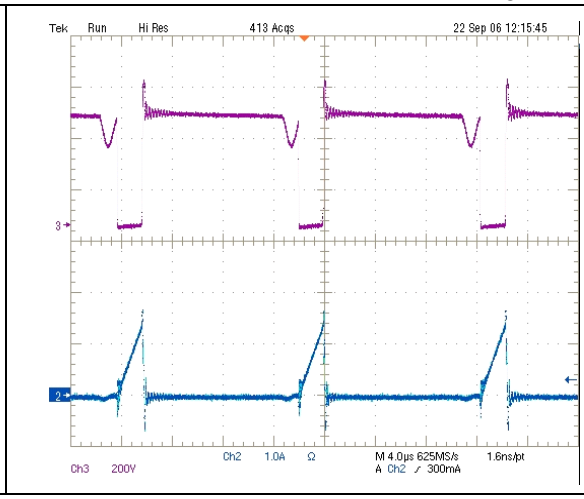
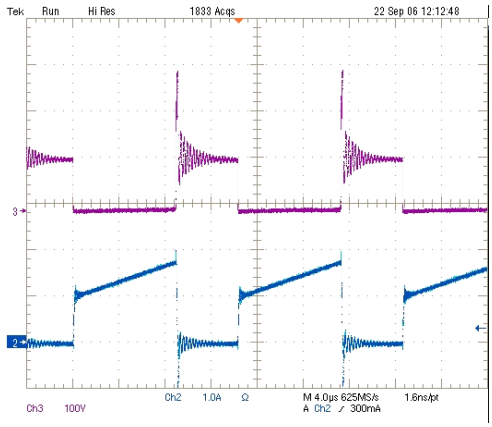
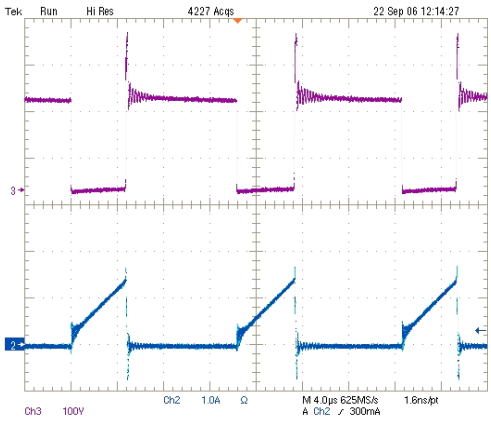


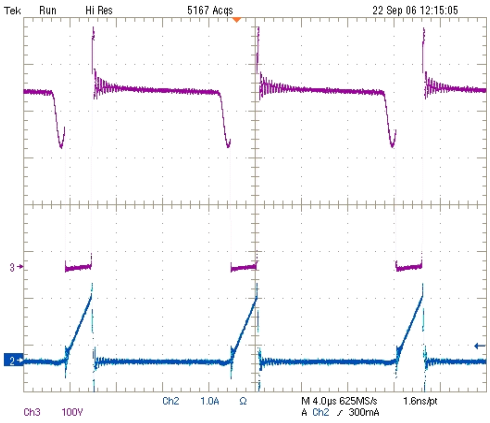
Figure 13. Steady state waveforms with nominal input voltage



a



b



c

Ch2 (blue): drain current
Ch3 (purple): drain voltage

(a) Full load waveforms at 48 V_{DC}
(b) Full load waveforms at 115 V_{AC}
(c) Full load waveforms at 230 V_{AC}

2 Conclusions

In this application note an ultra-wide range input voltage converter was presented. The topology used for the main converter is the well known flyback topology. The additional circuits used as active start-up circuit and slope compensation were described in detail. The tests results of the board were also presented. The most obvious result is the moderate efficiency of the converter. This result is only slightly related to the ultra wide range input. It is mainly due to the low output voltage and high current load of the flyback converter. In the secondary side flyback diode, the power dissipation is close to 5 W. This high power dissipation in the secondary side affects the performances, in terms of power dissipation, of the transformer, the primary side part of the flyback and of the input section.

In order to increase efficiency we can use a flyback with higher output voltage, 12 V for example, for the same power rate and obtain the output voltages requested in the electrical specifications with two switching post regulators. In this case, of course, the cost increases.

3 References

1. L5991 datasheet
2. AN1729 "L6565 - Based low cost SMPS for TV with Less then 1 W stand by consumption"
3. L6725 datasheet
4. STS12NF3LL datasheets

4 Revision history

Table 11. Revision history

Date	Revision	Changes
25-Jun-2006	1	First issue