## Introduction

Unused CMOS inputs which are left floating experience a gradual charging of the gate input capacitance. A floating input may see an increase in static current, as both the NMOS and PMOS outputs turn on and conduct current simultaneously. Alternatively, if the gate voltage reaches the threshold level with voltages between 0.8 V and 2.0 V applied to the inputs, the outputs tend to oscillate. Large numbers of gates left floating, in a 16-bit bus driver for example, cause large amounts of current to be drawn by the IC. The floating gate charges up at a rate determined by its leakage current. Intermittent or random circuit errors may be seen with floating inputs, as outputs switch to a different state for no apparent reason.

A common solution for this issue is to connect the floating inputs to VCC or to ground through a pull-up or pull-down resistor. The disadvantage of this is that an extra component and extra board space are needed and the resistor dissipates extra power. Hence, this pull-up resistor method is recommended for AC-powered systems and not for battery-operated equipment where power consumption is critical. Instead, a special feature called bus hold circuit is used.

Bus hold is an improved version of the internal pull-up resistor. It is a weak latch that recalls the last valid state of a pin when it is three-state. Bus hold provides a small positive feedback current on device inputs. When an input changes logic state, the bus hold circuit returns a small current to the device input, effectively adding to the transition of the input. This positive feedback then holds the final logic level until an active driver toggles the input voltage to the opposite logic state, where bus hold again holds the logic state. A number of logic families use an integrated bus hold circuit which eliminates the need for external resistors and saves board space. The circuit is shown in *Figure 1: "Generic bus hold circuitry"*.

Figure 1: Generic bus hold circuitry
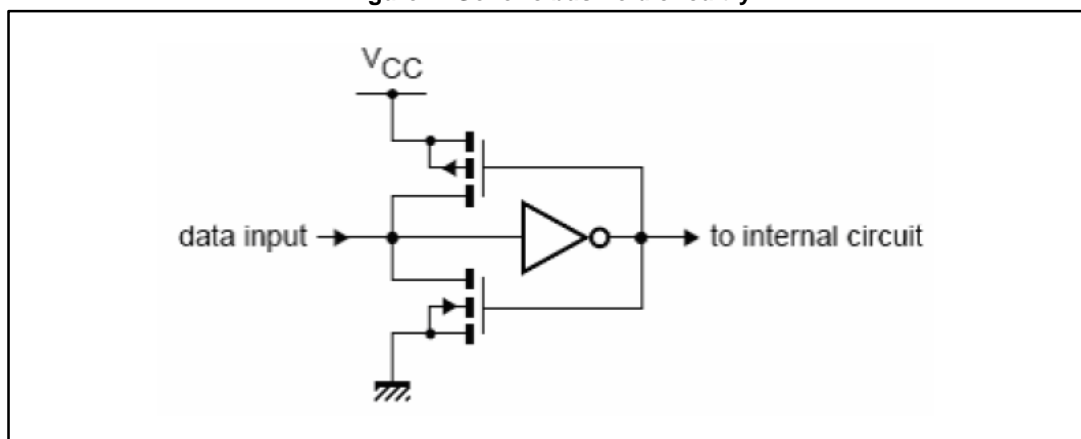
Contents

1 Bus hold advantages

- Reduces part count by eliminating the pull-up resistors
- Saves board space
- Prevents floating buses and thereby avoids device oscillations
- Reduces bus loading
- Does not toggle the bus when the bus is released
- Reduces power dissipation

Bus hold circuitry holds the input of a device at the last known state. This feature eliminates the need to use pull-up resistors to prevent the device inputs from floating and causing potential system errors. Eliminating pull-up resistors significantly reduces part count and assembly costs. Thus, the bus hold option is particularly important in applications where space and cost are at a premium and the elimination of pull-up resistors is a possibility.

In floating inputs, there is a possibility that the external bias appearing on the input buffer makes the buffer operate around its threshold point. In such cases, the floating inputs might start oscillating. Since a floating input has very high impedance, noise injected from other components on the board can cause the input to move around the threshold point of the input buffer. Each time the input voltage crosses the threshold point, the input buffer changes state, adding noise to the system which can potentially cause the device to oscillate. These oscillations can also increase the power consumption of the device. The heat dissipation thereof might also damage the device.

Adding a pull-up resistor adds bus loading every time the bus toggles low. With bus hold, the devices are optimally sized to reduce loading on the bus. Once the transition has been made through the toggle point, the bus hold input assists the driver rather than fighting it and causing a current drain. In this way, it consumes much less current compared to a circuit with a pull-up resistor when the device switches low. In other words, it is easier to overdrive a bus hold input than to drive a pull-up resistor of equivalent value LOW.

When using pull-up resistors, the bus is pulled high when released, causing unnecessary transitions where the logic was initially LOW. Bus hold components always retain the last known state, thus avoiding transitions. Thus, there is no toggling when the bus is released.

In all power sensitive applications, the current leakage of the pull-up resistor (when the bus is low) can be avoided with a bus hold input. Also, since the input avoids unnecessary transitions through the input threshold, the device power dissipation is reduced (ΔIcc).

2 Circuit operation

The integrated bus hold circuits act like dynamic pull-up/pull-down resistors as follows (see also *Figure 2: "Bus hold schematic representation"*):

- When the input is "low", the output of the inverter is "high" so the lower NMOS is ON and acts like a pull-down resistor.
- When the input is "high", the output of the inverter is "low" so the upper PMOS is activated and acts like a pull-up resistor.

Figure 2: Bus hold schematic representation
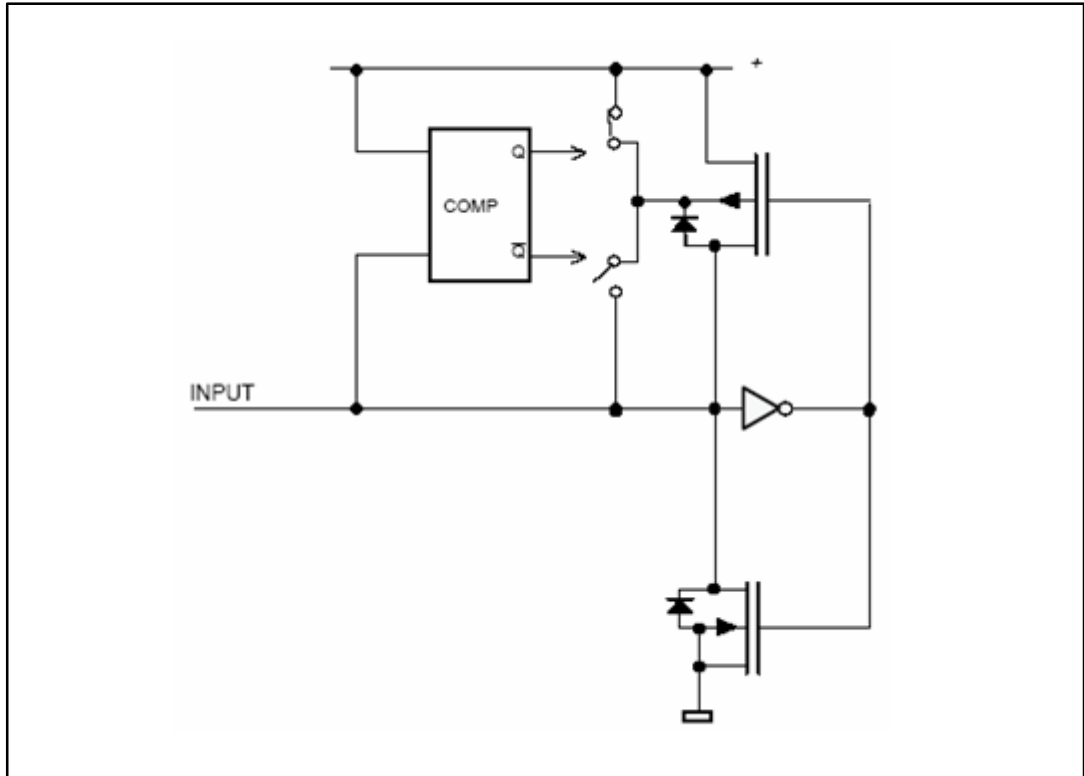
When the input voltage rises, the input current flowing into the circuit slowly increases, since the NMOS is conducting. Around the threshold of the CMOS, the PMOS starts conducting and NMOS stops conducting. At that point, the input current reverses direction and starts flowing out of the circuit. As the input voltage continues to increase, the current slowly decreases till the input voltage reaches VCC.

While the input remains below VCC, the bulk terminal of the PMOS remains connected to VCC. When the input exceeds VCC by 0.7 V, the bulk terminal is switched to the input. This mechanism prevents the input over-voltage from affecting the VCC.

3 Electrical specifications

Bus hold specifications identify the current required to sustain the logic at the threshold levels (Vih and Vih) and the overdrive current required to toggle the logic state of the device when there is a genuine signal from an external driver. The input current levels of a bus hold circuit should approach zero when the input voltage approaches zero or VCC. As shown in *Figure 3: "Bus hold characteristics for VCXH family at VCC = 3.0 V"*, current levels are at their highest near the input toggle point as the bus hold circuit attempts to pull the device away from the threshold region.

The bus hold current is specified as $I_{I(HOLD)}$ for sustaining both LOW and HIGH states. For the VCXH family, the sustaining current is normally ±75 µA minimum.

$I_{I(HOLD)}$ = -75 µA implies the minimum current the bus hold circuit is guaranteed to sink to if a logic LOW input is raised to 0.8 V.

$I_{I(HOLD)}$ = 75 µA implies the minimum current the bus hold circuit is guaranteed to source to if a logic HIGH input is lowered to 2.0 V.

$I_{I(HOLD)}$ = ±500 µA implies the maximum current that the external driver has to sink/source to switch a bus hold input from logic HIGH to LOW or vice versa.

Figure 3: Bus hold characteristics for VCXH family at VCC = 3.0 V
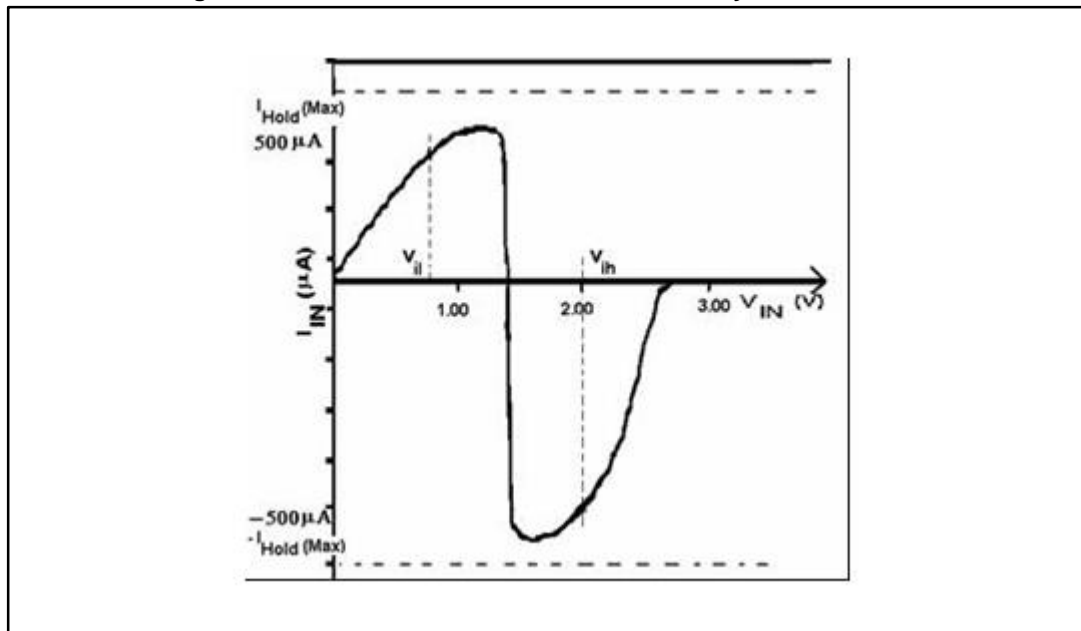
If "n" bus hold enabled inputs are tied to a data bus, the bus driver should be capable of driving (n x 500 µA), as the overdrive currents are additive for every bus hold circuit on a data-bus.

4   External resistors with bus hold circuitry

Pull-up resistors should not be used with an IC that has bus hold circuitry on its input pins. Adding a pull-up resistor to a pin with bus hold causes higher than necessary current demand on the bus hold driver. If the pull-up resistor is weak, it cannot switch the logic state from initial low to high in the time required.

If the initial state of the bus hold circuitry is "high" and the driver pulls the line LOW, the pull-up resistors contend with the driver. Then the output driver has to sink enough current to overcome the pull-up resistor in addition to the hold current of the bus hold circuit.

In some applications, the bus should become HIGH when all the outputs driving the bus are in tri-state. This is normally accomplished using a pull-up resistor. As the pull-up resistor value increases, the over drive current required to toggle the logic state also increases. The driver has to sink/source more current to power up the bus hold device that is held LOW initially.

The bus with pull-up can be modeled as an RC circuit with the bus and interconnect capacitance given by C (see *Figure 4: "RC circuit at input of bus hold circuitry"*). The worst case value of a pull-up resistor is calculated using the maximum over-drive current guaranteed by the device. R_T can be computed as:

$R_T \leq (V_{cc} - V_{th})/I_{IHOLDMAX}$

For example, in the case of the 54VCXH163245, for V_{CC} = 3.6 V, threshold voltage V_{th} = 1.8 V, and $I_{IHOLDMAX}$ = 500 µA, the pull-up resistor of the RC circuit should not be more than 3.6 kΩ.

Figure 4: RC circuit at input of bus hold circuitry
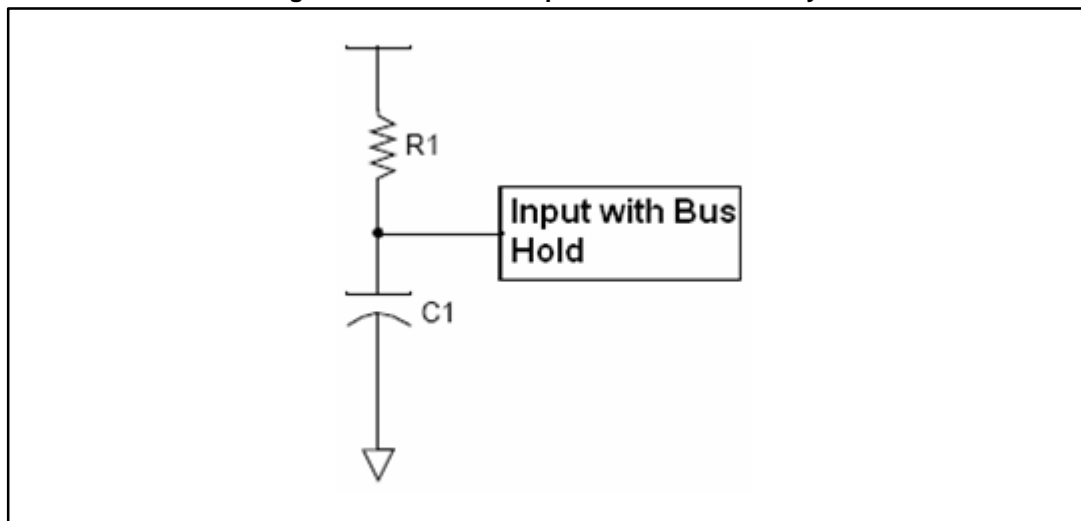
If the resistor size is increased beyond R_T, the bus hold latch prevents the capacitor from being charged to a voltage that is high enough to override the bus hold.

Therefore, the circuit never transitions out of the initial LOW state into the required HIGH state. Having a high value pull-up resistor also increases the switching time of the device as the RC time constant increases and the overdrive current sunk/sourced by the bus hold driver is increased. This calculation holds true when a resistor pulls a switch or other device up from ground.

This effect is demonstrated graphically in *Figure 5: "Typical bus hold characteristics of 54VCXH163245 and the effect of various pull-up resistor values"* which shows the typical bus hold characteristics and the effect of various pull-up resistors on the circuit. The maximum current here is at the most 250 µA. As per the calculations above, the pull-up resistor should not exceed 7 or 8 kΩ.

For pull-up resistors less than 8 Ω there is no intersection of the load line with the bus hold

characteristics. So there is no problem in pulling up an initial low state bus hold to logic high as required.

For larger resistance values, the load line intersects the bus hold characteristics and the intersection point becomes the maximum voltage level up to which the bus hold is pulled up from LOW. The input is never pulled HIGH beyond this point.

There is a consequent increase in the bus hold sustaining current to hold the device in the last valid logic state against the influence of the pull-up resistor, thereby increasing the current consumption.

Figure 5: Typical bus hold characteristics of 54VCXH163245 and the effect of various pull-up resistor values
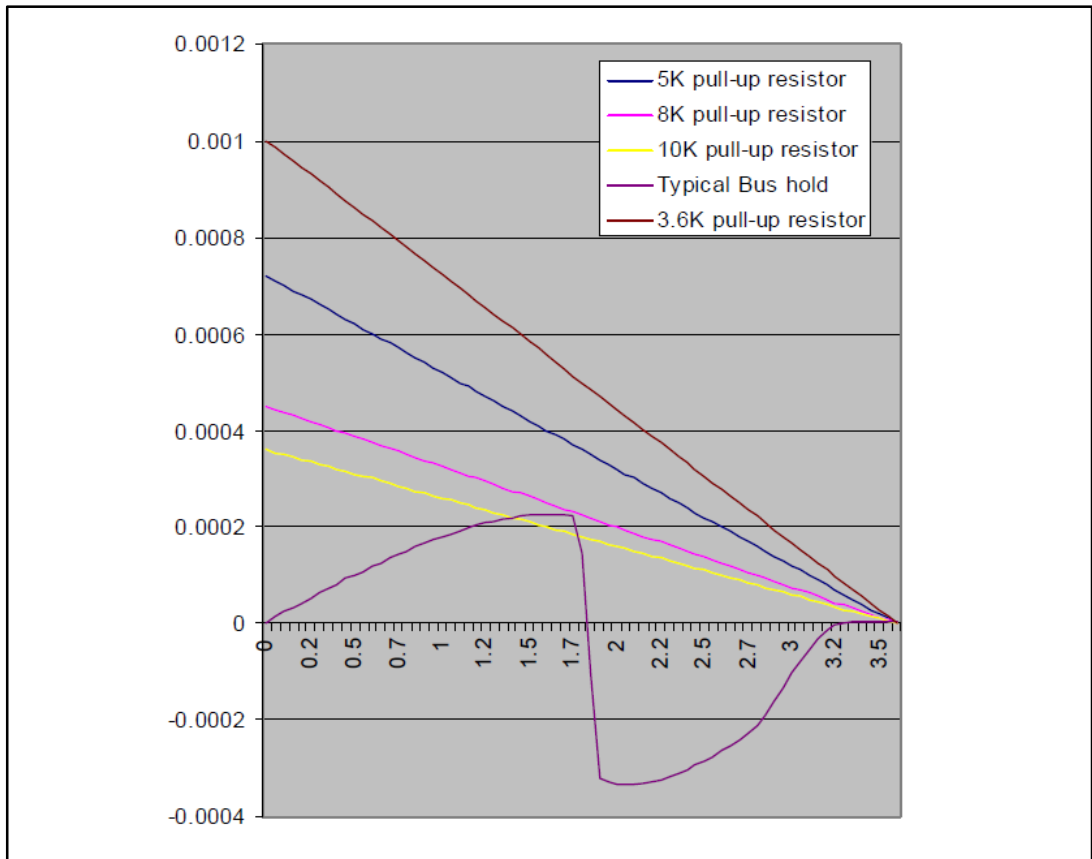
5 Conclusion

To summarize, an optimum pull-up resistor should be high enough to keep the power dissipation low, but at the same time low enough to switch logic states within the time required. More importantly, it should guarantee that the voltage level on the bus is a valid logic state. Due to such complex influencing factors, it is strongly recommended to avoid using pull-up resistors on bus hold inputs unless absolutely necessary.

Components with bus hold offer several advantages over the use of external pull-up or pull-down resistors. The bus hold circuit holds the last known valid state of the input when the bus starts to float. It acts as a weak clamp at the output and maintains the last known state. Since it is weak, it requires only a relatively small current to keep the input in the required state. The bus hold also does not need much current to overcome the clamp once an active driver toggles the input. In this way, bus hold circuitry effectively replaces pull-up resistors, reducing power dissipation and increasing the savings on space and component costs

6 Revision history

Table 1: Document revision history

Date	Revision	Changes
16-May-2005	1	Initial release
26-Jul-2016	2	*Section 4: "External resistors with bus hold circuitry"*: replaced 74VCXH1632245 with 54VCXH163245.

IMPORTANT NOTICE – PLEASE READ CAREFULLY