AN2131
APPLICATION NOTE

HIGH POWER 3-PHASE AUXILIARY POWER SUPPLY DESIGN BASED ON L5991 AND ESBT STC08DE150

1. INTRODUCTION

This application note deals with the design of a 3-Phase auxiliary power supply for 150W dual output SMPS, using the L5991 PWM driver and the STC08DE150 ESBT as main switch. The combination of these ST's parts aims at obtaining a high efficiency solution for high DC input voltage, typical requirement of any three phase application. The L5991 driver is an upgraded version of the UC384X current mode PWM driver. It boasts some very interesting additional features.

The necessity to handle both high output power and wide input voltage leads to design a flyback stage working in mixed operation mode: discontinuous and continuous. The continuous current mode introduces a right half plan zero in the loop-transfer function which makes the feedback stabilization difficult; the study on the frequency response, reported in the present document, has been carried out using MATLAB.

Furthermore, the slope compensation is implemented and deeply explained. It is necessary to remove sub-harmonic oscillations when the duty cycle is higher than 50%.

Finally the experimental results are analyzed to better understand the benefits given by the use of the ESBT in this application.

2. DESIGN SPECIFICATIONS AND PRELIMINARY REMARKS.

The table 1 lists the converter specification data and the main parameters fixed for the demo board.

If we look at the specs, particularly at the power and at the input voltage range, and after a brief description of the differences between continuous and discontinuous mode, it will soon be clear that it is very difficult and not convenient to design a flyback converter working in discontinuous mode.

Figure 1 shows a simplified schematic diagram of a flyback converter.

The discontinuous mode, shown in figure 2, has no front-end step in its primary current, i_T, and at turn-off, the secondary current i_D, is a decaying triangle which drops to zero before the next turn-on.

In the continuous mode, shown in figure 3, the primary current i_T has a front-end step and the characteristic appearance of a rising ramp on a step. During the transistor off time (figure 3), the secondary current has the shape of a decaying triangle sitting on a step with the current still remaining in the secondary at the instant of the next turn-on. There is, therefore, still some energy left in the secondary at the instant of next turn-on.

The two modes show significantly different operating properties and usages. The discontinuous mode responds more rapidly and with a lower transient output voltage spike to sudden changes in load current and input voltage. On the other hand, discontinuous mode provides a secondary peak current in the range of two or three times the continuous mode. This can be easily understood by comparing figure 2 and figure 3.

The secondary current average value is equal to the DC load current, as reported in both the above mentioned figures. Assuming also closely equal off time, it is obvious that the triangle in the discontinuous mode must show a much larger peak than the trapezoid of the continuous mode to get the same average value. Therefore, in the discontinuous mode, the larger secondary peak current, at the beginning of turn-off, will cause a greater RFI problem.

Secondary rms current in the discontinuous mode can be up to twice that in the continuous mode. This requires larger secondary wire size and output filter capacitors with larger ripple current ratings for the discontinuous mode. Rectifier diodes will also have a higher temperature rise in the discontinuous mode because of the larger secondary rms current.

Primary peak currents for the discontinuous mode are about twice those in the continuous mode. As a result, the discontinuous mode requires a higher current rating and possibly a more expensive power transistor. Also, the higher primary current in the discontinuous mode results in a greater RFI problem.

Despite all these relative disadvantages, the discontinuous mode is much more used for low

power applications. This is due to two reasons. Firstly, as mentioned above, the discontinuous mode, with an inherently lower transformer magnetizing inductance, responds more quickly and with a lower transient output voltage spike to rapid changes in output load current or input voltage. Secondly, because the transfer function of the continuous mode has a right half plane zero, the error amplifier bandwidth must be drastically reduced to stabilize the feedback loop. As a consequence, the transient response is much slower.

Finally, referring to the power spec of our demo, it is clear that the discontinuous mode cannot be used because it would determine a very high primary and secondary peak current with a higher cost of all the main components involved: power transistor, secondary diode and output capacitor.

Table 1. Converter Specification data and Fixed Parameters

Symbol	Description	Values
V_{inmin}	Rectified minimum Input voltage	250
V_{inmax}	Rectified maximum Input voltage	850
V_{out1}	Output voltage 1	24V/6.25A
V_{out2}	Output voltage 2	5V/0.075A
V_{aux}	Auxiliary Output voltage	15V/0.01A
P_{out}	Maximum Output Power	150W
η	Converter Efficiency	>75%
F	Switching frequency	90 kHz
Fsb	Stand-by switching frequency	35 kHz
V_{spike}	Max over voltage limited by clamping circuit	200V

Figure 1. Simplified Schematic Diagram of a Flyback Converter

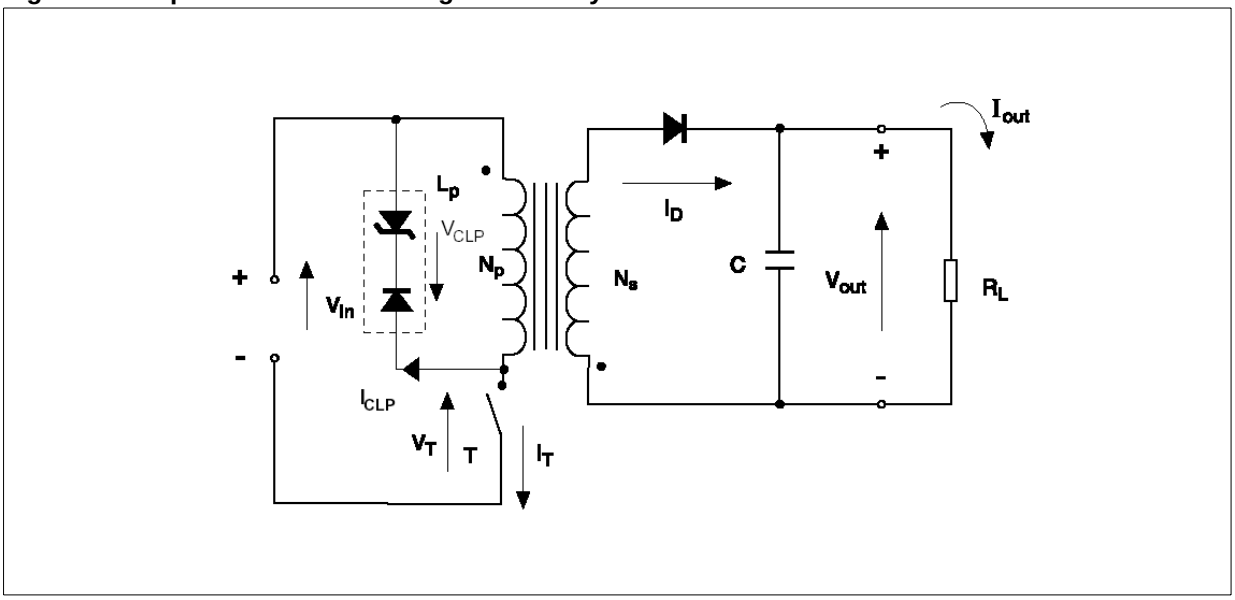


Figure 2. Discontinuous Mode Flyback Waveforms

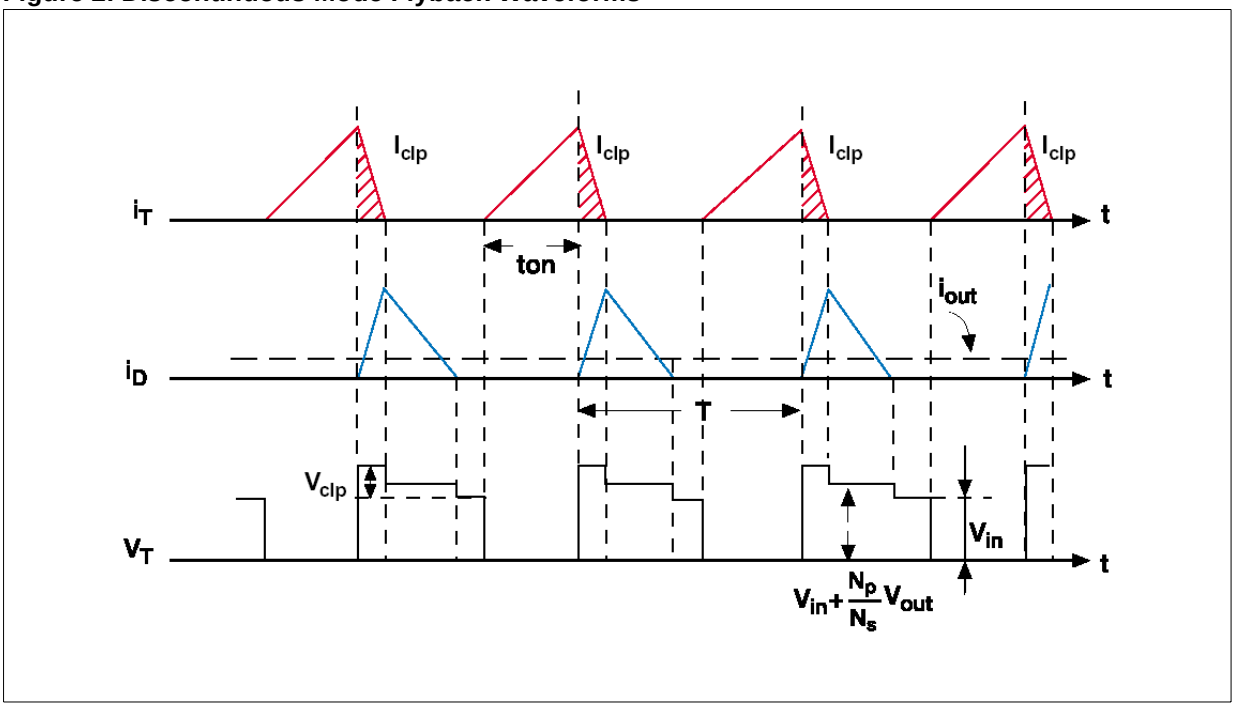
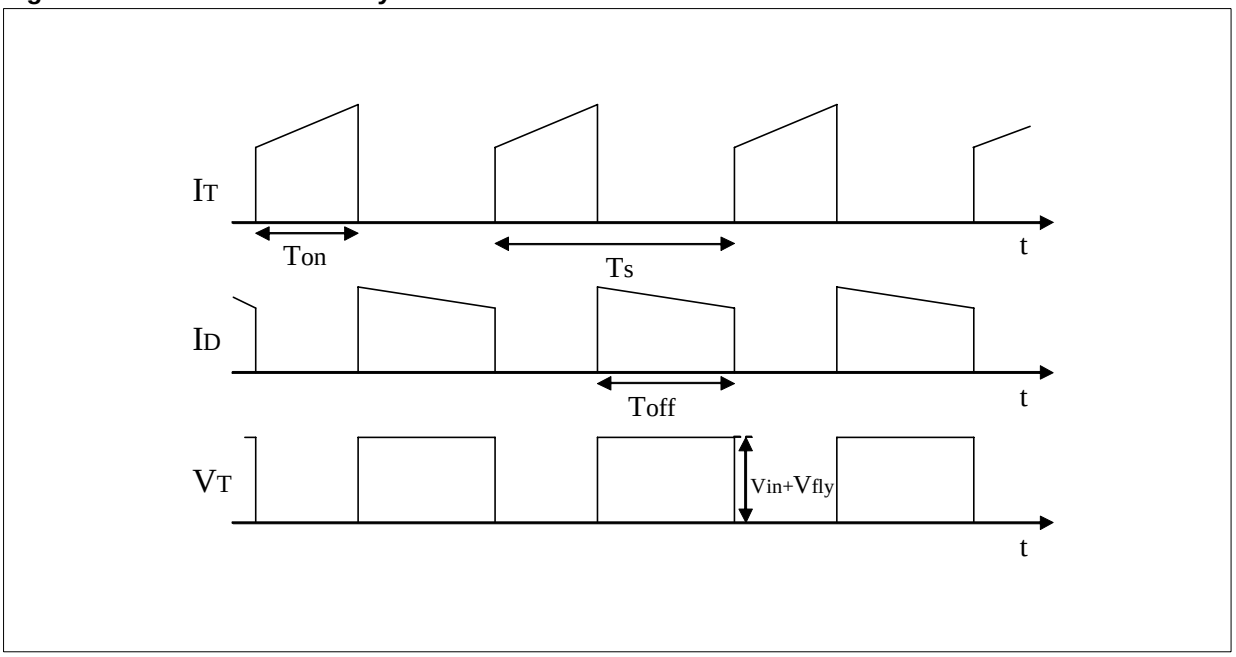


Figure 3. Continuous Mode Flyback Waveforms



3. FLYBACK CONTINUOS MODE WITH L5991

The minimization of the power drawn from the mains under light load conditions (Stand-by, Suspend or some other idle modes) is an issue that has recently become of great interest, mainly because new and more severe standards are coming into force.

The key point of this strategy is a low switching frequency. It is well-known that many of the power loss sources in a lightly loaded flyback waste energy proportionally to the switching frequency, hence this should be reduced as much as possible. On the other hand, it is equally well-

known that a low switching frequency leads to bigger and heavier magnetics and makes filtering more troublesome. It is then advisable to make the system operate at high frequency under nominal load condition and to reduce the frequency when the system works in a low-consumption mode. This requires a special functionality of the controller. It should be able to automatically recognize the condition of light or heavy load and then adequate its operating frequency accordingly.

The L5991 PWM controller, with its "Stand-by function", meets exactly this requirement. This application note will deal with the design of a flyback using L5991 PWM driver, while deeper details about the driver itself can be found in the dedicated application note AN1049.

The specifications table reports the two values of the switching frequency, 90kHz for normal mode and 35kHz for stand-by mode.

4. FLYBACK STAGE DESIGN

The continuous mode operation, as any switching topology, is identified by observing the steady state behavior of the energy storage component. In the flyback topology, the storage element is represented by the magnetization transformer inductance, which is charged by the primary winding during the on time, and discharged by the secondary winding during the off time. The flyback topology will hence be working in continuous mode if the secondary winding current does not reach zero at the end of the off time.

As previously said, the mixed mode implies a discontinuous mode operation for low load and/or higher input voltage. The boundary depends on the output power for a given input voltage. The higher is the input voltage the higher is the output power when the continuous mode starts. Theoretically, there isn't any restriction to fix the boundary between continuous and discontinuous mode. It will be given by imposing design equation for others relevant circuit parameters.

The maximum duty cycle, that in a discontinuous mode flyback is imposed to prevent the continuous mode operation, in this case must be fixed establishing a good trade-off between primary and secondary side performance. There are two opposite effects: by increasing the duty cycle the rms current at primary side can be reduced, while the rms current at secondary side will be increased. This means that a higher duty cycle imposes a less stressful condition to any parts in the primary path, and a more stressful condition to the secondary path. In the same way, to decrease the duty cycle causes an optimization of secondary side and a deterioration of primary side performances.

The higher duty cycle is a further help to easily design the flyback stage for a wide range voltage input. On the other hand, the higher duty cycle implies a higher reflected voltage to promptly demagnetize the flyback transformer.

For such a high power flyback stage, an important parameter to monitor is the current ripple at secondary side; it is needed either to lower rms current or to reduce RFI. Further consideration concerns the reflected flyback voltage which is imposed in order not to overcome the maximum breakdown of the power switch.

The above consideration plus some cost issues generate a clear figure of how to impose design equations. Moreover, since design specifications imply a high power output only, the following calculation will consider the influence of both low power and auxiliary outputs negligible.

In continuous operation mode the relationship between input and output voltage is only dependent on the duty cycle and not on the frequency. The relationship is given by the following formula:

$$\frac{V_{Out1}}{V_{in}} = \frac{N_{S1}}{N_P} \cdot \frac{D}{1-D} \qquad \text{Eq. 1}$$

Eq. 1 is ideal and does not take into consideration real effects such as the voltage drops on the power switch and on the output diode. Including these two voltage drops it is possible to get the first design equation and calculate the turn ratio between input and the higher power output (Vout1).

$$\frac{N_P}{N_{S1}} = \left(\frac{Vin - Vcs_{on}}{Vout1 + Vd1_{fw}} \right) \cdot \frac{D}{1-D} \qquad \text{Eq. 2}$$

Where, V_{CSon} and V_{d1fw} are respectively the voltage drop on the power switch and on the secondary side diode. Eq. 2 is valid for any input voltage. The second design equation comes from the maximum power switch breakdown, defining first V_{fly}, the flyback reflected voltage, and then calculating the maximum switch breakdown voltage.

$$V_{fly} = \frac{N_P}{N_{S1}} \cdot \left(Vout1 + Vd1_{fw} \right) \qquad \text{Eq. 3}$$

$$BV = V_{fly} + V_{spike} + V_{in\max} + m\arg in \qquad \text{Eq. 4}$$

Eq. 4 also includes the safe design margin and the allowed voltage spike fixed by clamping network design. By combination of Eq. 3 and Eq. 4, the maximum primary/secondary turn ratio is finally obtained.

$$V_{fly} \le BV - V_{spike} - V_{in\max} - m\arg in \quad \Rightarrow$$

$$\frac{N_P}{N_{S1}} \le \frac{BV - V_{spike} - V_{in\max} - m\arg in}{V_{Out1} + V_{d1\,fw}} \qquad \text{Eq. 5}$$

For 150W power output, the proposed power switch is STC08DE150, with BV=1500V. Assuming V_{spike}=200V, margin=200V and V_{d1fw}=1V. From Eq. 5 results:

$$\frac{N_P}{N_{S1}} \le 10 \qquad \text{Eq. 6}$$

From Eq. 2, imposing $V_{in}=V_{inmin}$=220V, N_p/N_s = 10, and considering the normal mode switching frequency, the maximum duty cycle and the maximum on time are:

$$D_{\max} = 52.8\% \quad \Rightarrow \quad Ton\max = 5.87\mu s \qquad \text{Eq. 7}$$

It is worth noticing that the value of the duty cycle calculated by Eq. 7 is a good trade-off to optimize both primary and secondary side performances. By the way, it must be pointed out that being D_{max}>50%, slope compensation may be necessary. This subject will be deeply analyzed in paragraph 7.

Once fixed the turn ratio between input and the higher power output, the flyback reflected voltage is fixed by Eq. 3 as well.

$$V_{fly} = \frac{N_P}{N_{S1}} \cdot \left(Vout1 + Vd1_{fw}\right) = 250V \qquad \text{Eq. 8}$$

It is now possible to calculate the two turn ratios referred to the slave Vout2 and to the auxiliary outputs.

$$\frac{N_P}{N_{S2}} = \left(\frac{Vfly}{Vout2 + Vd_{fw}}\right) = 33 \qquad \text{Eq. 9}$$

$$\frac{N_P}{N_{aux}} = \left(\frac{Vfly}{Vaux + Vd_{fw}}\right) = 15.8 \qquad \text{Eq. 10}$$

The next transformer design step is to fix the primary and/or secondary magnetization inductances. There are several criteria: the first one is to select the primary inductance in order to ensure continuous mode operation from full load to minimum load. This method, since a bigger primary magnetization inductance is requested, assures a very low output current ripple, increasing transformer primary turns. Furthermore, it makes the RHP zero lower, so that the loop stabilization will be more complicated. The second alternative criterion is to calculate primary and secondary inductances by defining maximum secondary ripple current. This last method fixes a limit for the rms current and does not require such a high primary magnetization inductance, but it may lead to a transition mode operation.

Figure 4. Waveforms and Nomenclature of the Continuous Mode Flyback Design

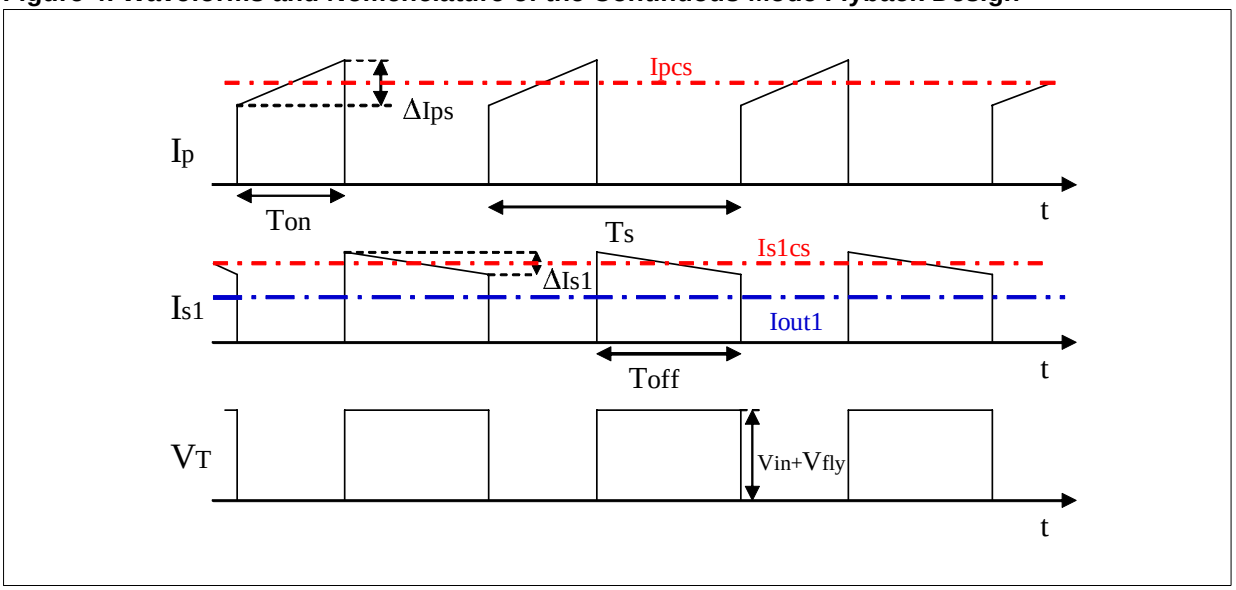


Figure 4 reports the most significant waveforms and relevant nomenclature to further proceed in the flyback design. From figure 4, we define IPCS the primary average current value and Δ_{IPS} the primary current variation during the on time, I_{S1CS} the secondary average current value and Δ_{IS1} the secondary current variation during the off time and I_{Out1} the secondary average current.

By adopting the second design method, we now fix the maximum secondary ripple current ΔI_S% in the following equations:

$$\Delta I_{S1\max} = 2 \cdot \Delta I_S \cdot I_{S1CS} = 2 \cdot \Delta I_S \cdot \frac{I_{Out1\max}}{1 - D_{\max}} \quad \text{Eq. 11}$$

where $\Delta I_{S1\max}$ is the maximum secondary current variation and ΔI_S is the ripple current. Therefore we have:

$$L_{S1} = \frac{\left(V_{Out1} - Vd_{fw}\right) \cdot \left(T_S - T_{ON\max}\right)}{\Delta I_{S!\max}} \quad \text{Eq. 12}$$

where L_{S1} is the secondary magnetization inductance. Imposing ΔI_S%= ±30% from Eq. 11 and Eq. 12 results:

$$L_{S1} = 16.17\mu H \quad \text{Eq. 13}$$

while the primary magnetization inductance is:

$$L_P = \left(\frac{N_P}{N_{S1}}\right)^2 \cdot L_{S1} = 1617\mu H \quad \text{Eq. 14}$$

Once fixed turn ratios and the primary inductance value, some extra calculation is needed to choose either the transformer or the external components for flyback stage. Since design specifications request one high power output only, while the slave and the auxiliary outputs need a very small power, for designing the transformer we can only consider a single output. Based on this supposition the relevant design parameters are here below reported.

Fixed N_p/N_s = 10 and L_p = 1.6 mH.

Primary Winding:

$$\Delta Ip = \frac{(Vin\min - Vcs_{on}) * Ton\max}{Lp} = \quad 0.8A \quad \text{Eq. 15}$$

$$Ipcs = \frac{Po\max}{(Vin_{\min} - Vcs_{on}) \cdot \eta \cdot D\max} = \quad 1.48A \quad \text{Eq. 16}$$

$$Ip_{pk} = Ip_{cs} + \frac{\Delta Ip}{2} = \quad 1.88A \quad \text{Eq. 17}$$

$$Ip_{rms} = \sqrt{D_{\max}\left[Ip_{pk}\left(Ip_{cs} - \frac{\Delta I_P}{2}\right) + \frac{1}{3}\left[Ip_{pk} - \left(Ip_{cs} - \frac{\Delta I_P}{2}\right)\right]^2\right]} =$$

$$= \quad 1.08A \quad \text{Eq. 18}$$

Master Secondary Winding:

$$Is1_{CS} = \frac{I_{Out1\max}}{1 - D\max} = \quad 13.24A \qquad \text{Eq. 19}$$

$$\Delta Is1 = \frac{(Vout1 + Vd_{FW}) \cdot (T - T_{ON\max})}{Ls1} = \quad 9.7A \qquad \text{Eq. 20}$$

$$Is1_{pk} = Is1_{CS} + \frac{\Delta Is1}{2} = \quad 18.9A \qquad \text{Eq. 21}$$

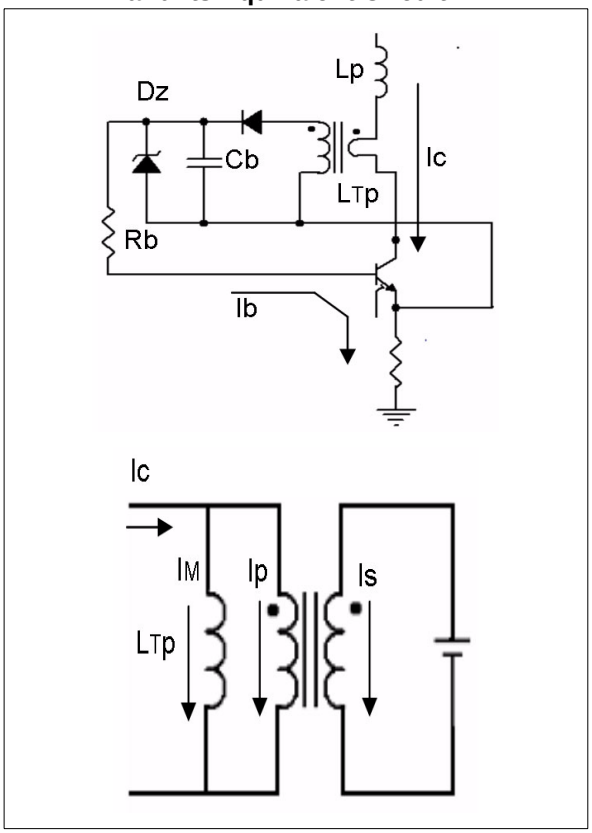
$$Is1_{rms} = \\ = \sqrt{(1 - D_{\max})\left[Is1_{pk}\left(Is1_{cs} - \frac{\Delta I_{s1}}{2} \right) + \frac{1}{3}\left[Is1_{pk} - \left(Is1_{cs} - \frac{\Delta I_{s1}}{2} \right) \right]^2 \right]} = \\ = \quad 9.29A \qquad \text{Eq. 22}$$

Above calculation have been made considering a continuous mode operation. This condition is assured by imposing $|\Delta I_S\%| < 100\%$. According to the reported design parameters, the transformer has been designed by Cramer and all remaining power parts have been chosen as reported in ST's application note AN1889.

5. BASE DRIVING CIRCUIT DESIGN

In practical applications, such as SMPS, where the load is variable, the collector current is variable as well.
As a consequence, it is very important to provide a base current to the device which is related to the collector one. In this way, it is possible to avoid the device over saturation at low load and to optimize the performance in terms of power dissipation.
The best and simplest way to do this is the proportional driving method provided by the current transformer, in figure 5.
At the same time, as already stated, it is very useful to provide a short pulse to the base to make the turn-on as fast as possible and to reduce the dynamic saturation phenomenon.
The pulse is achieved by using the capacitor and the zener in figure 5.

Figure 5. The Proportional Driving Schematic and its Equivalent Circuit



The driving network guarantees a zone with fixed I_C/I_B ratio that results imposed once the current transformer turn ratio has been chosen. From the ESBT STC08DE150 datasheet, and in particular looking at the storage time characterization, it is clear that a turn ratio equal to 5 is a good value to ensure the right saturation of ESBT at I_c = 2A, so that in the current transformer we can fix at first:

$$\frac{N_P}{N_S} = \frac{1}{5} \qquad \text{Eq. 23}$$

The core magnetic permeability of the current transformer has to be as high as possible in order to minimize the magnetization current I_m (that is not transferred to the secondary side but only drives the core into saturation). On the contrary, too high a permeability core may lead the core into saturation even with a very small magnetization current. To avoid that it is necessary to increase the number of primary turns and the size of the core as well. On the other hand, if a core with a very small magnetic permeability is chosen, it is possible to reduce the number of primary turns and the core size, but if the permeability is too small we may not have current on the secondary side because almost all the collector current

becomes magnetization current. As a compromise a ferrite material with a relative permeability in the range of 4500 ÷ 7000 is the best choice.

When a ferrite ring with some diameter has been selected, the minimum primary turns is determined to avoid the core saturation from the preliminarily fixed turn ratio N with 0.2. By applying the Faraday's law and imposing the maximum flux B_{max} equals to $B_{sat}/2$:

$$V_1 = N_{TP}\frac{d\varphi}{dt} \cong N_{TP}\cdot A_e \cdot \frac{\Delta B}{\Delta t} \quad \Rightarrow \quad N_{TP} = 2\frac{V_1 \cdot T_{on\max}}{A_e . B_{sat}}$$

Eq. 24

Where, B_{sat} is the saturation flux of the core and it depends on the magnetic permeability.

During the conduction time, the junction base-emitter of ESBT can be seen as a forward biased diode. To complete the secondary side load loop the voltage drop on both diode D and resistor R_B must be added in series with the base of the ESBT. The equivalent secondary side voltage source is given by:

$$V_S = V_{BEon} + V_D + V_{RB} \cong 2.5V$$

Eq. 25

Since the magnetization inductance cannot be neglected, only I_P, a fraction of the total collector current, will be transferred to the secondary. As a result, the magnetization current has to be first as low as possible. Meanwhile, the value of the magnetization inductance must be taken into account for a proper calculation of transformer primary turns and turns ratio. The magnetization voltage drop, that is, the voltage at the primary of the current transformer, can be now easily calculated:

$$V_1 = V_S\frac{N_{1T}}{N_{2T}} = 2.5\cdot\frac{1}{5} = 0.5 \quad [V]$$

Eq. 26

The magnetization current will be:

$$I_{M\max} = \frac{V_1 T_{ON\max}}{L_{TP}}$$

Eq. 27

The number of primary turns should be increased if I_{Mmax} is relatively high. But the core must have window area enough to hold all primary and secondary windings. Otherwise it is necessary to choose a bigger core size. Once both core material and size are fixed, the turn ratio must be adjusted to get the desired I_C/I_B ratio according to the equation below:

$$N_{eff} = \frac{I_P}{I_B} = \frac{I_{C\max} - I_{M\max}}{I_C \diagup 5}$$

Eq. 28

where I_{Mmax} is the maximum magnetization current.

The insulation between primary and secondary should be considered since the voltage on the primary side during the off time can overstep 1500V.

Next step is to select the zener diode, the capacitor C_b and the resistor R_b. The turn-on performance of ESBT is related to the initial base peak current and its duration t_{peak} that is approximately given by:

$$t_{peak} = 3R_bC_b$$

Eq. 29

A suitable value for R_b is 0.56. It can eliminate the ringing on the base current after the peak, and at the same time, it generates negligible power dissipation.

The value t_{peak} can be determined once the minimum on time is set based on the operation frequency. Bear in mind that in practical applications it should never be lower than 200ns. The value of Cb can be counted since the values of t_{peak} and Rb are known.

I_{peak} must be limited in order to avoid an extra saturation of the device. This action is made by the zener diode Dz that clamps the voltage across the small capacitor Cb. The zener must be chosen according to the following empirical formulas and inside the range of V_{Zmin} and V_{Zmax}:

$$V_{Z\max} = 2\left(I_{peak}R_b + 1\right)$$

$$V_{Z\min} = 2\left(I_{peak}R_b\right)$$

Eq. 30

The base peak current will be higher with higher clamp voltage (Dz) or smaller capacitance (Cb), which in turn will lead to a shorter duration of the peak time.

The higher and longer the base peak current, the lower the power dissipation during turn-on. But you need to limit the Ib peak both in terms of amplitude and time duration otherwise at low load a very high saturation level may result. If the device is over-saturated the storage time is too long with higher power dissipation during turn-off. Moreover a long storage time can also cause output oscillation especially at high input voltage.

To overcome the above mentioned problems it is recommended to fix the peak duration to 1/3 the minimum duty cycle.

6. CONTINUOS CURRENT MODE LOOP STABILIZATION

It is well known from literature that the transfer function of the continuous current mode (CCM) flyback converter is given by:

$$G_1(s)=\frac{v_{out1}(s)}{v_{comp}(s)}=\frac{N\cdot R\cdot(1-D)}{3\cdot R_S\cdot(1+D)}\cdot \frac{(1+sCR_C)\left(1-\frac{sL_pD}{N^2R(1-D)^2}\right)}{1+\frac{sCR}{1+D}} \quad \text{Eq. 31}$$

where N = N_p/N_s, R is the load, R_C is the electrolytic capacitor series resistance.

It is worth noticing that the transfer function has one pole and two zeros, whose one on the right half plane. The RHP zero is very difficult if not impossible to compensate and therefore must be kept well beyond the closed-loop bandwidth. As a result, the transient response of such system will be not extremely fast.

Considering now, the transfer function in the following form:

$$G_1(s)=\frac{v_{out1}(s)}{v_{comp}(s)}=k_1\cdot\frac{\left(1-\frac{s}{z_{11}}\right)\left(1-\frac{s}{z_{12}}\right)}{1-\frac{s}{p_{11}}} \quad \text{Eq. 32}$$

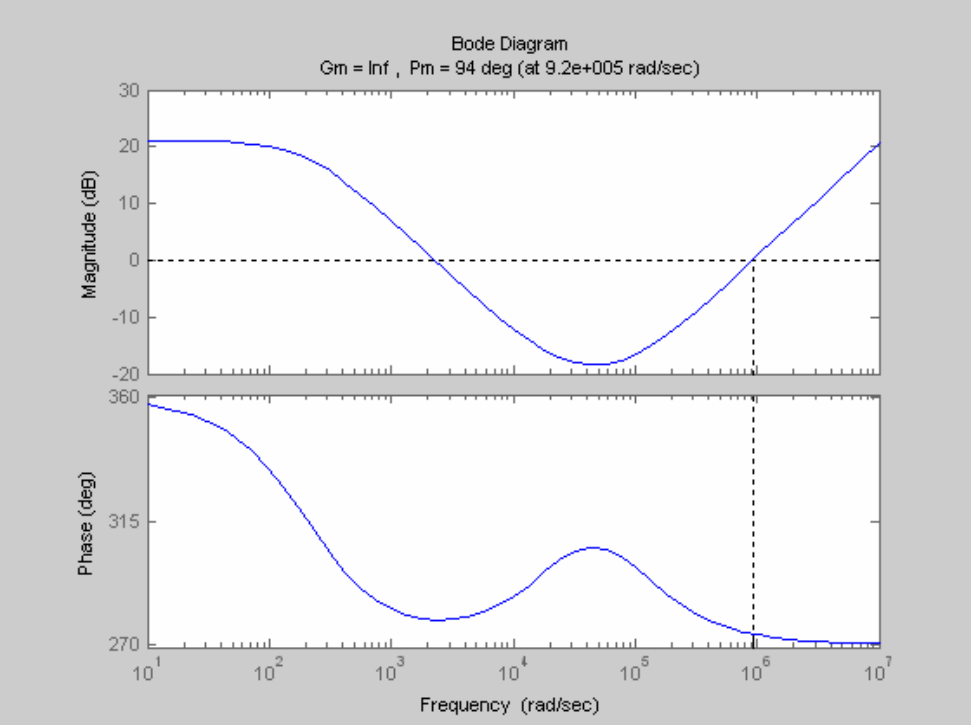
Substituting the values of this design in case of low input voltage (worst case), we obtain the frequency response reported in the following figure 6. Poles and zeros are reported in the below equations:

P_{11}= -202/rad=-32.1Hz

Z_{11}= -23Krad/s=-3.79KHz Eq. 33

Z_{12}= 88Krad/s=14.1KHz

Figure 6. Flyback Frequency Response at Minimum Input Voltage



A good line and load regulation implies a high DC gain, thus the open loop gain should have a pole at the origin. Normally, in this case we need a feedback network like the one in figure 7. Its transfer function is given by:

$$G_2(s) = \frac{v_{comp}(s)}{v_{out}(s)} = \frac{CTR_{\max} R_{COMP}}{R_B R_H C_F} \frac{1}{s} \frac{1 + s(R_H + R_F)C_F}{1 + sR_{COMP}C_{comp}}$$

Eq. 34

or:

$$G_2(s) = \frac{v_{comp}(s)}{v_{out}(s)} = k_2 \frac{1}{s} \frac{\left(1 - \frac{s}{z_{21}}\right)}{1 - \frac{s}{p_{21}}}$$

Eq. 35

To properly design the feedback loop, let us consider first the following transfer function and its bode plots (figure 8):

$$G_1(s) \cdot \frac{1}{s}$$

Eq. 36

It is preferable that the RHP zero is well beyond the closed loop cut off frequency. To make it, first of all, a gain is needed. Then, from figure 8, a 90 degrees phase margin could be achieved fixing both zero and pole of G_2 to cancel respectively pole p_{11} and zero z_{21} of G_1. In this case, we ideally get a phase margin of 90 degrees with a well defined gain. Observe that a high phase margin, making the system response quite slow, could help avoid undesired frequency changes. By the way, to assure a not too slow transient response, it is advisable to choose about 60 degrees phase margin. Referring to this real case, we can fix both zero and pole in order not to exactly cancel p_{11} and z_{21}.

According to the previous argument we fix the pole and zero as Eq. 37.

P_{21} = -11.1krad/s = -1.77kHz

Z_{21} = -245rad/s = -39Hz

Eq. 37

Figure 10 reports the overall open loop transfer function G1*G2.

Phase margin is very close to the desired value and it assures a good stability and quite fast transient response. Finally, it is interesting to check the loop stability for the highest input voltage and maximum output load. Under this condition, the frequency response of the system is shown in figure 11.

From figure 12, as expected, the phase margin is higher and hence the system stability margin is improved.

Figure 7. Converter Feedback Network

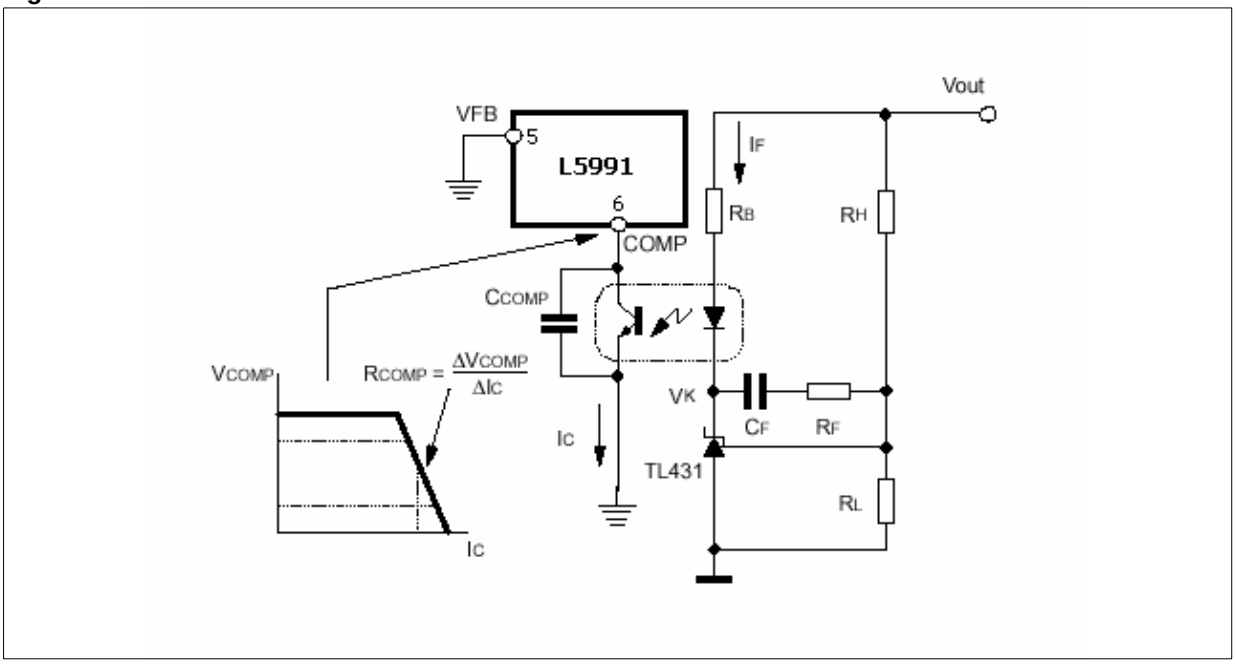


Figure 8. Flyback Frequency Response at Vinmin Adding a Pole at the Origin

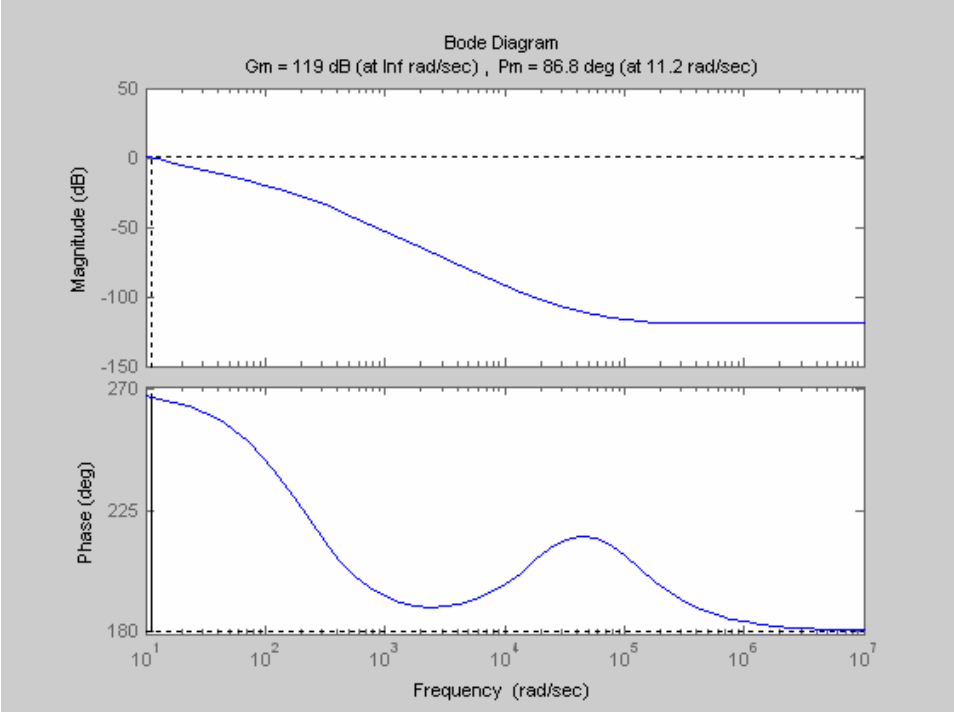


Figure 9. Frequency Response of the Feedback-transfer Function

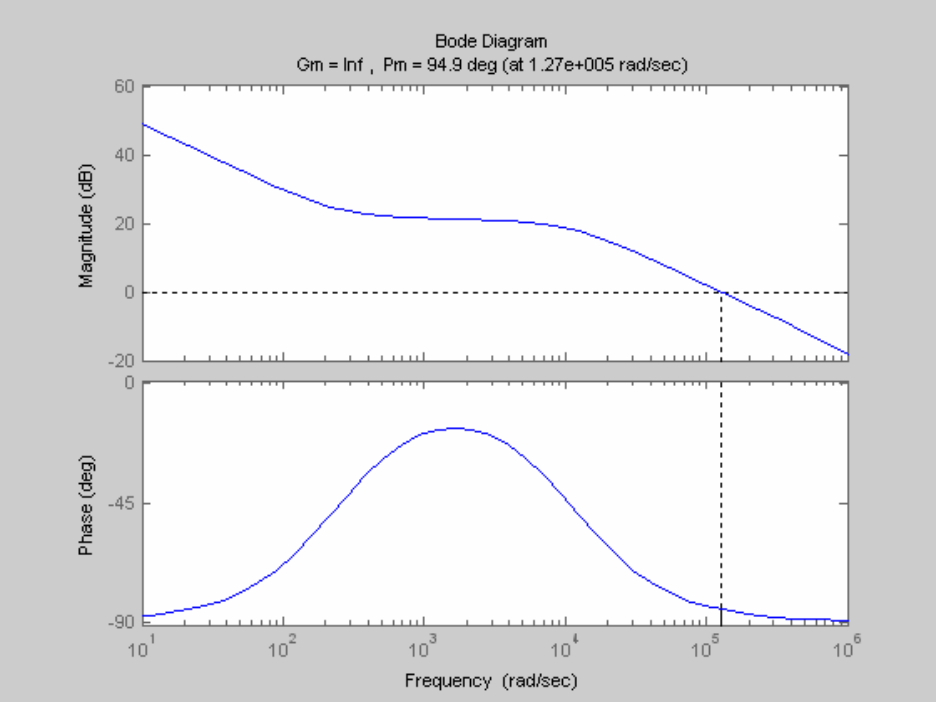


Figure 10. Stabilized Open Loop-transfer Function at Minimum Input Voltage

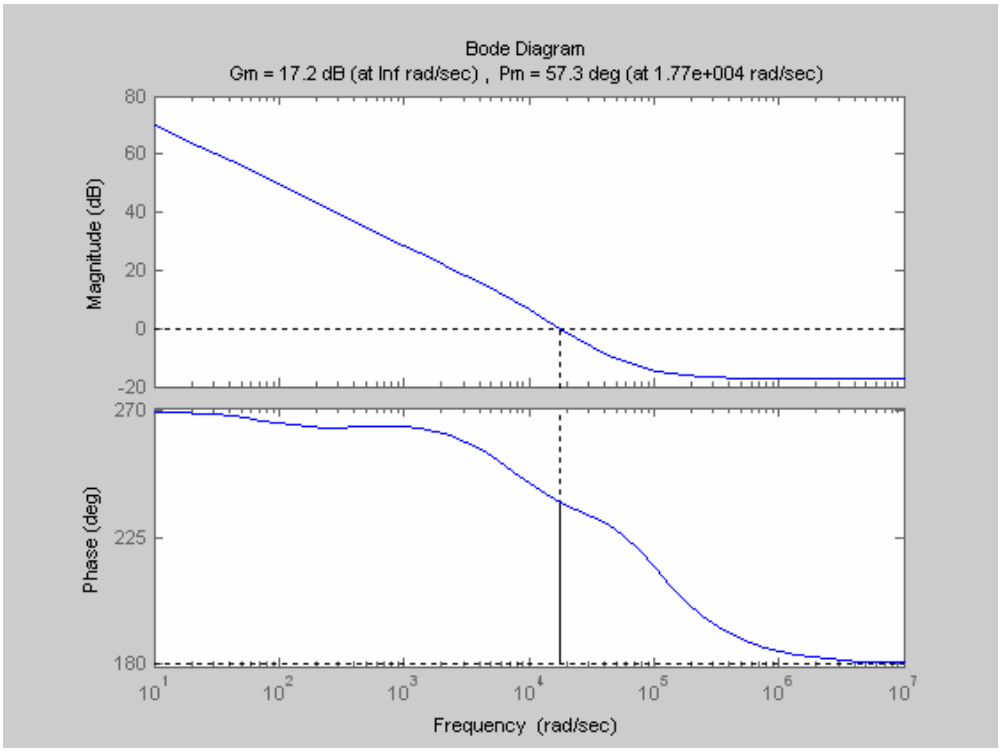


Figure 11. Flyback Frequency Response at Maximum Input Voltage

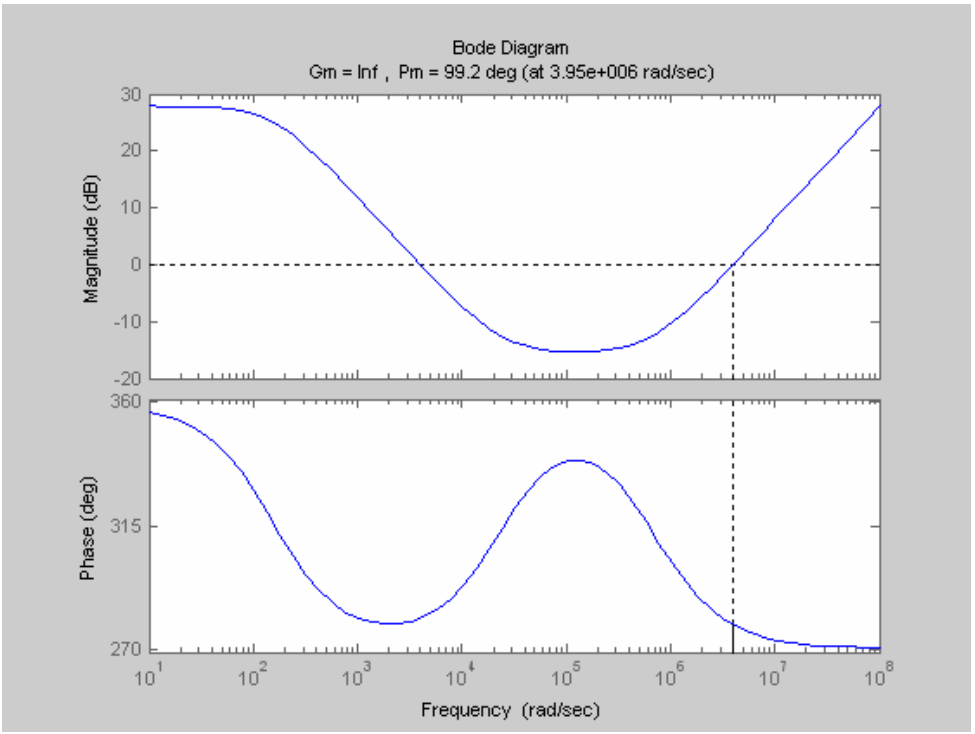
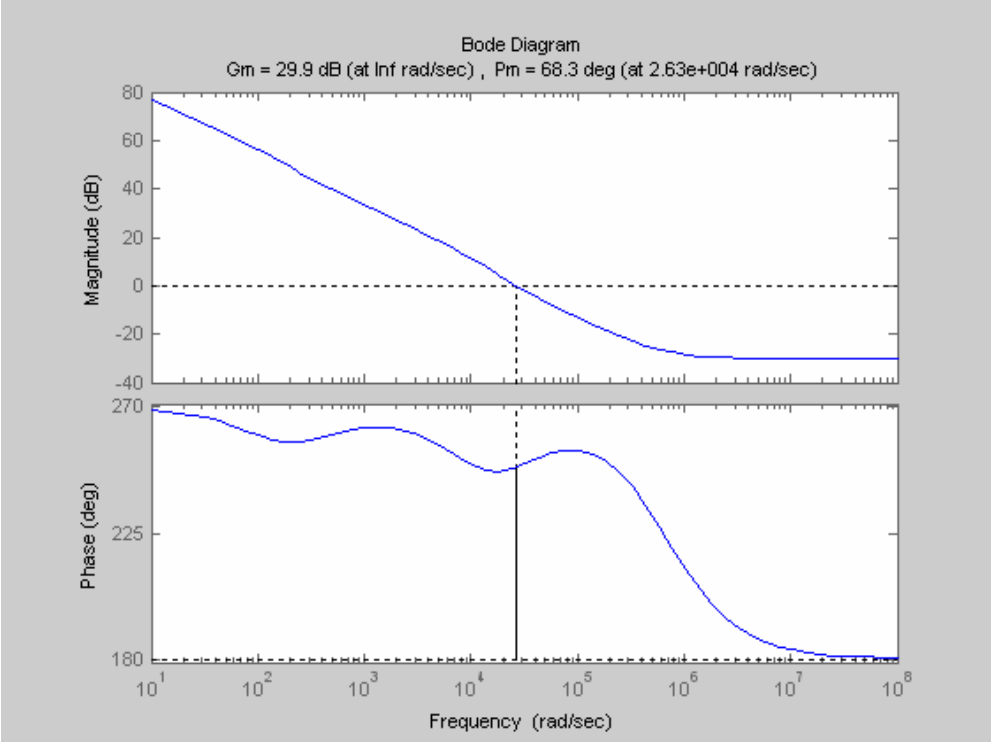


Figure 12. Stabilized Open Loop-transfer Function at Maximum Input Voltage



7. SLOPE COMPESATION FOR SUBHARMONICS SUPPRESSION

The L5991, as many PWM drivers for SMPS, applies a current mode control. This control method keeps the power transistor current peak constant at the needed level to supply the DC load with DC output voltage dictated by the voltage error amplifier. This is equal to keep constant the current peak at secondary side winding. The average current at secondary side is the DC load current and, however, to keep the current peak constant does not mean to keep the average current constant.

Because of this, in the unmodified current mode scheme, changes in the DC input voltage will cause momentary changes in the DC output voltage. The output voltage change will be corrected by the voltage error amplifier outer feedback loop, as this is the loop which ultimately sets the output voltage.

Again, however, the inner loop, while keeping peak inductor current constant, does not supply the correct average current and output voltage changes again. The effect is then an oscillation which commences at every change in input voltage and which may continue for some time. The mechanism can be better understood from an examination of the upslope and downslope of the output inductor currents.

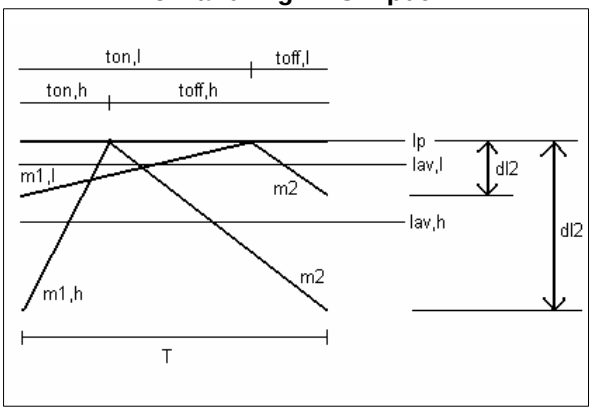
In figure 13, it can be seen that the average primary side current at low DC input is higher than the high DC input case. This can be seen quantitatively as:

$$I_{av} = I_p - \frac{dI_2}{2} = I_p - (\frac{m_2 t_{off}}{2}) =$$

$$= I_p - \left[\frac{m_2 (T - t_{on})}{2}\right] = I_p - \left(\frac{m_2 T}{2}\right) + \left(\frac{m_2 t_{on}}{2}\right)$$

Eq. 38

Figure 13. Average Primary Side Current at Low and High DC Input



Since the voltage feedback loop keeps the product of V_{dcton} constant, at lower DC input voltage, where the on time is higher, the average output inductor current I_{av} is higher, as can be seen from equation 38 and figure 13.

Furthermore, since the DC output voltage is proportional to the average, not to the peak, inductor current, as DC input goes down, DC output voltage will go up.

DC output voltage will then be corrected by the outer feedback loop and a seesaw action or oscillation will occur.

A second problem which generates oscillation in current mode is shown in figures 14 and 15.

From these figures, it can be seen that, at a fixed DC input voltage, if for some reason there is an initial current disturbance ΔI_1, after a first downslope the current will be displaced by an amount of ΔI_2.

Figure 14. Current Disturbance Effects at Duty Cycle <50%

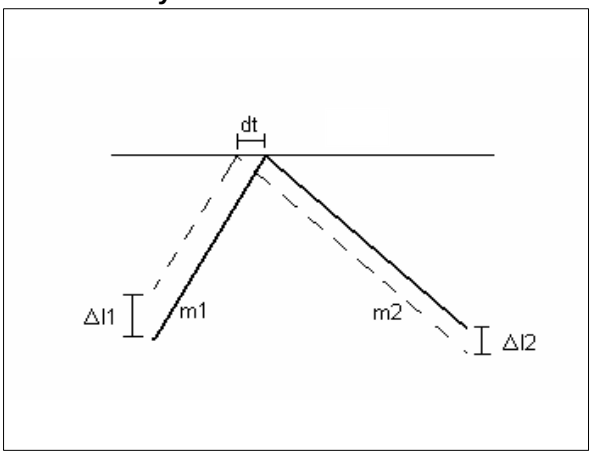
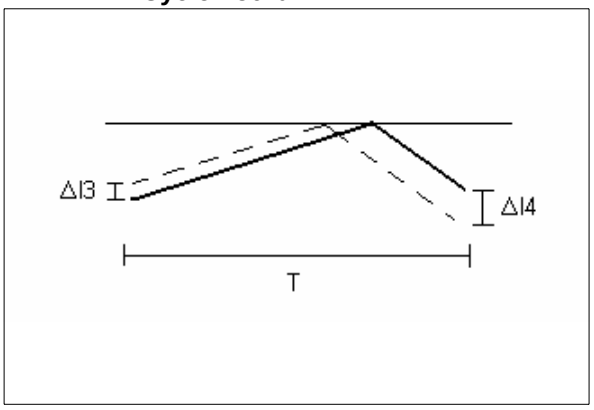


Figure 15. Current Disturbance Effects at Duty Cycle >50%



Furthermore, if the duty cycle is less than 50% ($m_2<m_1$) as in figure 14, the output disturbance ΔI_2 will be less than the input disturbance ΔI_1, and after some cycles, the disturbance will die out. But if the duty cycle is greater than 50% ($m_2>m_1$) as in figure 15, the output disturbance after one cycle is greater than the input disturbance.

This can be seen quantitatively from figure 14. For a small current displacement ΔI_1, the current reaches the original peak value earlier in time by an amount dt where $dt = \Delta I_1/m_1$. On the inductor downslope, at the end of the on time, the current is lower than its original value by an amount ΔI_2 where

$$\Delta I_2 = m_2 dt = \Delta I_1 \frac{m_2}{m_1} \qquad \text{Eq. 39}$$

Now with m_2 greater than m_1, the disturbances will continue to grow but eventually will decay, causing an oscillation.

Both current-mode problems mentioned above can be corrected as shown in figure 16, where the original, unmodified output of the error amplifier is shown as the horizontal voltage level OP. The scheme for correcting the previous problems (slope compensation) consists of adding a negative voltage slope of magnitude m to the output of the error amplifier. By a proper selection of m in the way discussed below, the inductor average DC current can be made independent of the power transistor on time. This corrects the problems indicated in both equations 38 and 39.

Figure 17 shows the upslope m1 and the downslope of the output inductor current. Remember that in current mode, the power transistor on time starts at every clock pulse and ends at the instant the output of the PWM comparator reaches equality with the output of the voltage error amplifier as shown in figure 16.

Figure 16. PWM with Current Mode Control

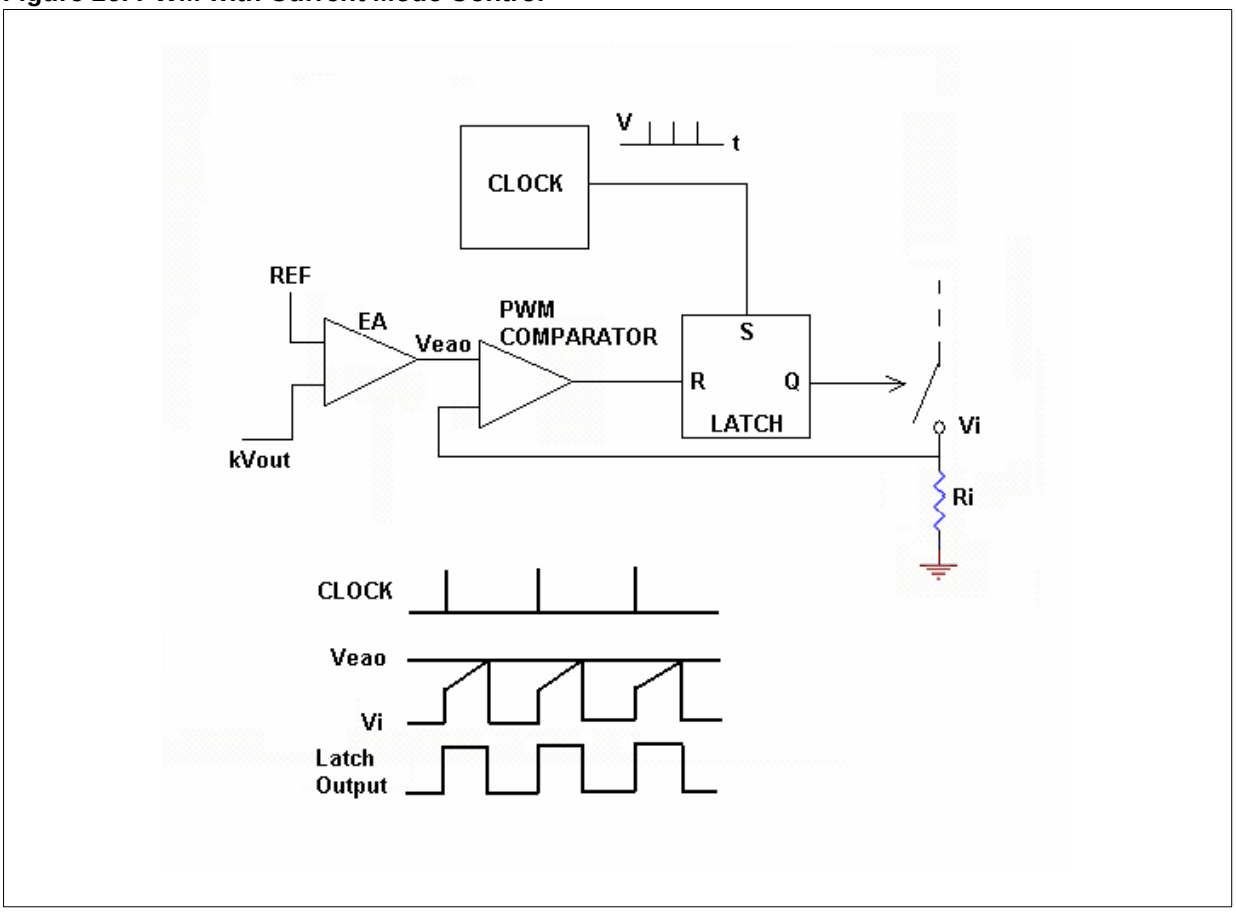
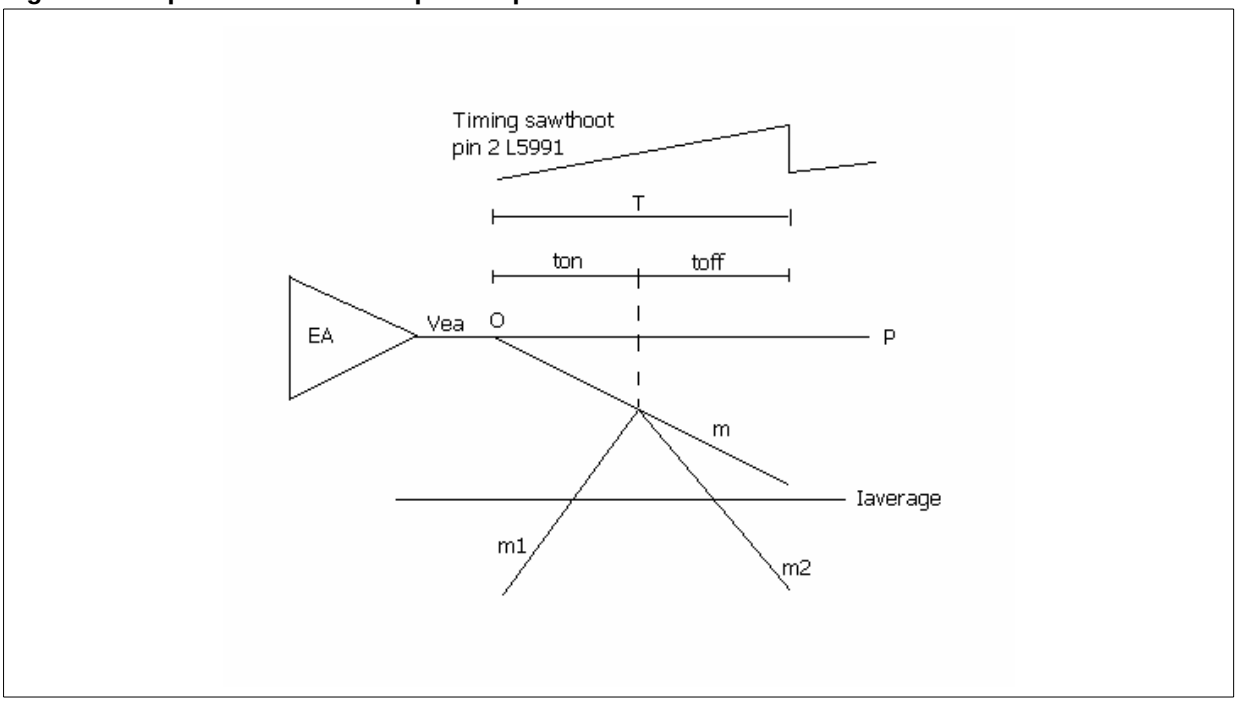


Figure 17. Implementation of Slope Compensation



In slope compensation, a negative voltage slope of magnitude $m=dV_{ea}/dt$ starting at clock time is added to the error amplifier output. The magnitude of m is, therefore, calculated.

In figure 17, the error-amplifier output at any time t_{on} after a clock pulse is

$$V_{ea} = V_{ea0} - mt_{on} \quad \text{Eq. 40}$$

where V_{ea0} is the error amplifier output at t_{on} equal to zero.

The peak voltage V_i across the primary current-sensing resistor R_i in figure 16 is

$$V_i = I_{pp}R_i = I_{sp}\frac{N_s}{N_p}R_i \quad \text{Eq. 41}$$

where I_{pp} and I_{sp} are the primary and secondary currents respectively. But $I_{sp}=I_{sa} + dI_2/2$, where I_{sa} is the average secondary or average output inductor current and dI_2, in figure 13, is the inductor current change during the off time (m_2t_{off}). Then

$$I_{sp} = I_{sa} + \frac{m_2 t_{off}}{2} = I_{sa} + \frac{m_2}{2}(T - t_{on}) \quad \text{Eq. 42}$$

Then

$$V_i = \frac{N_s}{N_p}R_i\left[I_{sa} + \frac{m_2}{2}(T - t_{on})\right] \quad \text{Eq. 43}$$

Equating eq. 40 and 41, which is what the PWM comparator does, we obtain

$$\frac{N_s}{N_p}R_i I_{sa} = V_{ea0} + t_{on}\left(\frac{N_s}{N_p}R_i\frac{m_2}{2} - m\right) - \left(\frac{N_s}{N_p}R_i\frac{m_2}{2}T\right) \quad \text{Eq. 44}$$

It can be seen in this relation that if

$$\frac{N_s}{N_p}R_i\frac{m_2}{2} = m = \frac{dV_{ea}}{dt} \quad \text{Eq. 45}$$

then the coefficient of the t_{on} term is zero and the average output inductor current is independent of the on time.

This, then, corrects the two above mentioned problems arising from the fact that without compensation, current mode maintains the peak constant, and not the average, output inductor current.

The same effect is obtained by adding a positive-going ramp to the output of the current-sensing resistor V_i and leaving the error-amplifier output voltage unmodified.

Adding the positive-going ramp to V_i is simple and is the most usual approach. Let us suppose that the slope of the ramp is dV/dt.

When the PWM driver finds the equality of its two inputs, the output terminates the on time. Then $V_i+(dV/dt)t_{on}=V_{ea0}$ substitute V_i from eq. 41:

$$\frac{N_s}{N_p}R_i\left[I_{sa} + \frac{m_2}{2}(T - t_{on})\right] + \frac{dV}{dt}t_{on} = V_{ea0} \quad \text{Eq. 46}$$

Then

$$\frac{N_s}{N_p}R_i I_{sa} + \frac{N_s}{N_p}R_i\frac{m_2}{2}T + t_{on}\left(\frac{dV}{dt} - \frac{N_s}{N_p}R_i\frac{m_2}{2}\right) = V_{ea0} \quad \text{Eq. 47}$$

From the above, it can be seen that if the slope dV/dt of the voltage added to V_i is equal to $(Ns/N_p)R_im_2/2$, the terms involving t_{on} in the preceding relation vanish and the secondary average voltage I_{sa} is independent of the on time.

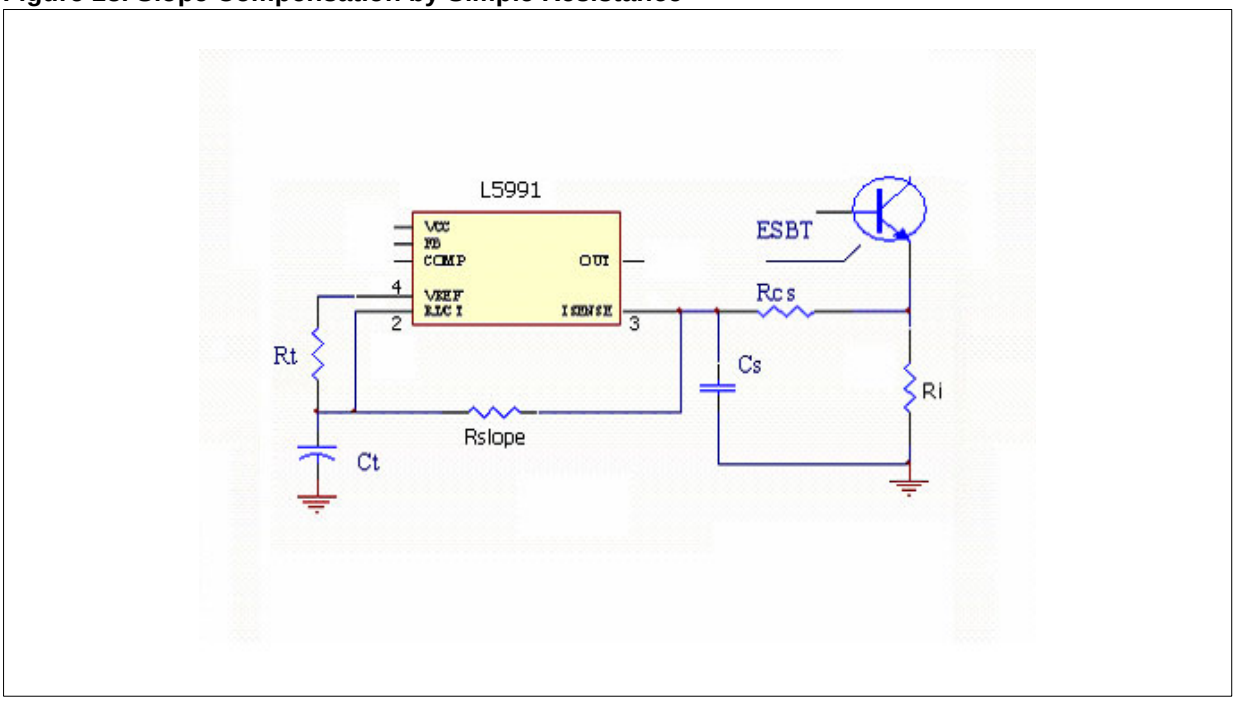
In the L5991 chip, a positive going ramp starting at every clock pulse is available at the top of the time capacitor (pin 2 in figure 18).

The voltage at that pin is:

$$V_{osc} = \frac{\Delta V}{\Delta t}t_{on} \quad \text{Eq. 48}$$

where $\Delta V = 2V$ and $\Delta t = 0.693*R_tC_t$.

Figure 18. Slope Compensation by Simple Resistance



As seen in figure 18, a fraction of that voltage whose slope is $\Delta V/\Delta t$ is added to V_i (the voltage across the current-sensing resistor). That slope is set at $(N_s/N_p)R_i(m_2/2)$ by the R_{cs}, R_{slope} resistors. Thus in figure 18, since R_i is much less than R_{cs}, the voltage delivered to the current sensing terminal (pin 13) is:

$$V_i + \frac{R_{CS}}{R_{CS}+R_{slope}}V_{osc} = V_i + \frac{R_{CS}}{R_{CS}+R_{slope}}\frac{\Delta V}{\Delta t}t_{on}$$

Eq. 49

and setting the slope of that added voltage equal to $(N_s/N_p)R_i(m_2/2)$, we obtain

$$\frac{R_{CS}}{R_{CS}+R_{slope}} = \frac{(N_S/N_P)R_i(m_2/2)}{\Delta V/\Delta t}$$

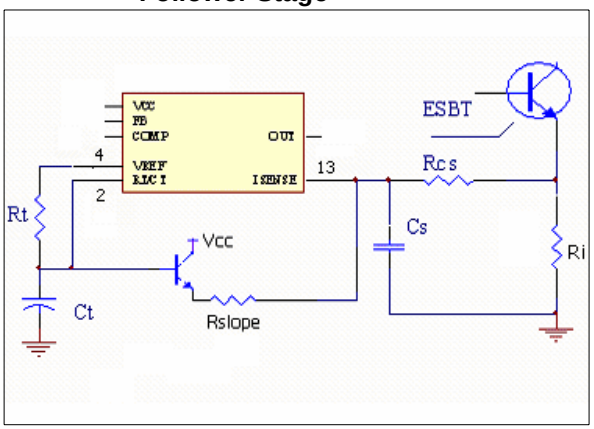
Eq. 50

where $\Delta V/\Delta t = 2/(0.693R_tC_t)$.

Since $R_{CS} + R_{slope}$ drain current off the top of the timing capacitor, the operating frequency changes.

Then either $R_{CS} + R_{slope}$ is made large enough so that the frequency change is small or an emitter follower is interposed between pin 2 and the resistors as shown in figure 19.

Figure 19. Slope Compensation by Emitter Follower Stage



We choose the second option for two reasons: the first one is due to the fact that it is difficult to avoid frequency changes with typical R_{CS} values. The second reason, related to the L5991 characteristics, is a little bit more complicated and it will be now explained.

In our design, after choosing R_{CS} = 1kΩ we have:

$$\frac{R_{CS}}{R_{CS}+R_{slope}} = \frac{(N_S/N_P)R_i(m_2/2)}{\Delta V/\Delta t} \cong 6.9k\Omega$$

Eq. 51

The closest value available is R_{slope} = 6.8kΩ. Therefore, first of all, to keep the frequencies established originally, the oscillator resistors can be chosen accordingly, and more important, since the valley value of the oscillator is about 1V, we have a voltage shift of:

$$\Delta V_i = \frac{R_{CS}}{R_{CS} + R_{slope}} 1V = \frac{1}{1+6.8} 1V = 128mV \quad \text{Eq. 52}$$

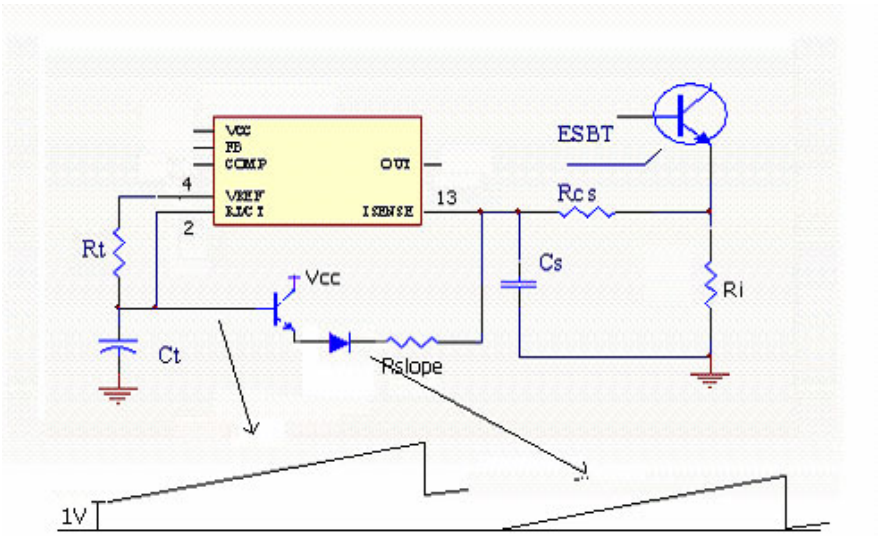
As already stated in the previous paragraphs, the PWM driver used in our design has a special feature. We can externally fix two different operating frequencies in order to improve the system power efficiency.

As mentioned in both AN1049 and L5991datasheet, the level at which the operating frequency changes is established by Vcomp, the error amplifier output voltage. Two thresholds are used to guarantee a hysteresis, avoiding uncertainty when switching from low to high frequency and vice-versa. As explained in the AN1049 the two values can be referred to the current sensing (pin 13) voltage. The upper level is 0.867V while the lower level is 0.367V.

If a simple resistance is used to make the slope compensation, a voltage shift is also introduced and its value computed in eq.52 is too high. In fact, to make the system work at low frequency it is necessary to undergo 0.367V and it may happen that the lower frequency is never reached.

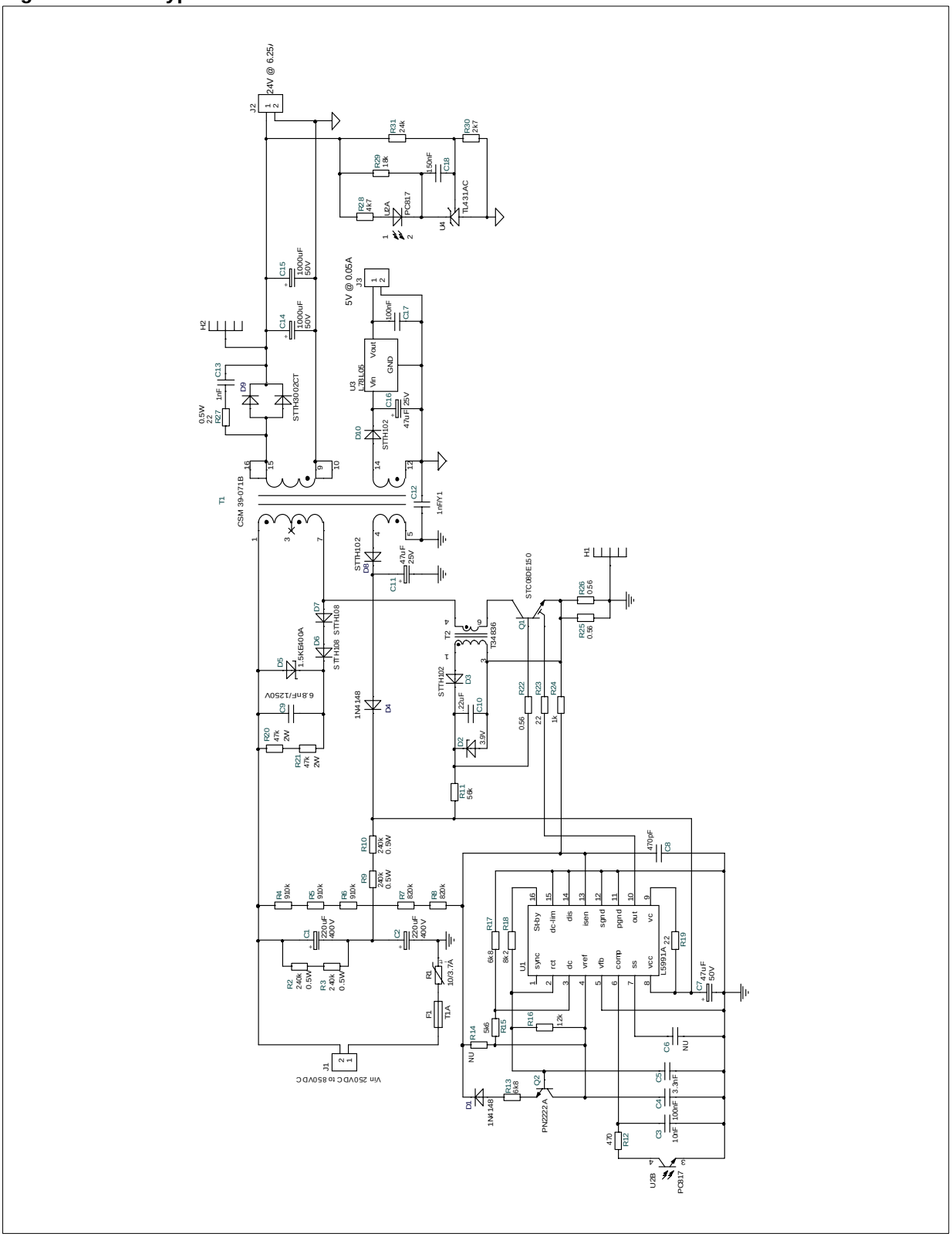
With the emitter follower of figure 19, besides avoiding any alteration in the oscillator functionality, we get about 0.5V voltage shift respect to pin2, and hence a consequent reduction of the ΔV_i previously calculated. To obtain $\Delta V_i = 0$ and assure the correct behavior of the PWM driver in the SMPS a diode in series with the emitter has been introduced as shown in figure 20.

Figure 20. Final Slope Compensation Schematic



8. PROTOTYPE IMPLEMENTATION AND EXPERIMENTAL RESULTS

Figure 21. Prototype Schematic



The theoretical design has been further improved by bench verification getting the final schematic reported in figure 21. The board has been successfully tested according to design specifications previously reported and additional features have been also verified.

D6 Snubber Circuit

This topology works both in discontinuous and continuous mode.

The output diode turns off at zero current when operating in discontinuous mode after the core is discharged. In continuous mode the diode turns off when Q1 is turned on.

At that time there is still current flowing through it and therefore forces a hard turn-off which causes ringing on the reverse recovery.

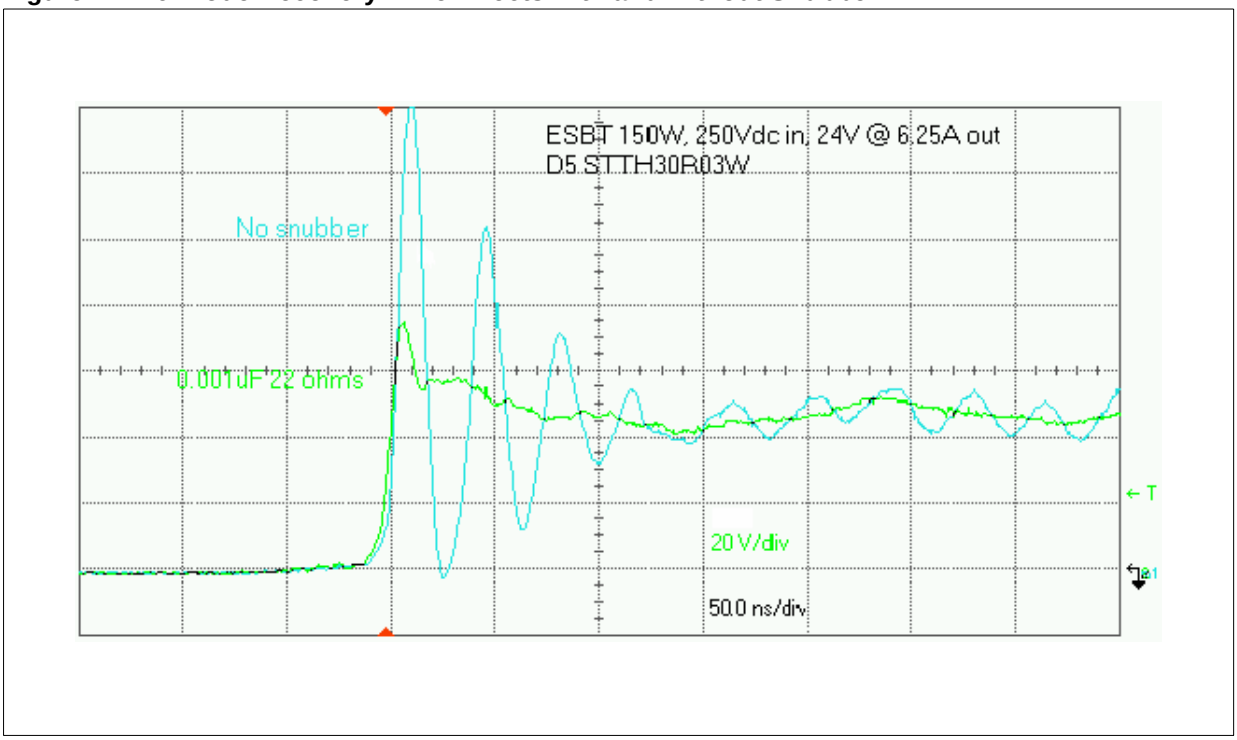
By adding a snubber based on a capacitance higher than the diode junction capacitance and a resistor tuned to the ringing of the leakage inductance and the diode capacitance, the peak reverse voltage spike and the ringing can be minimized.

The ringing often causes EMI issues and adds noise to sensitive PWM circuits. Figure 22 shows the diode at 6 amps.

The blue waveform is the diode recovery without snubbing, while the green one is the diode recovery after adding the snubber.

The resistor dissipates 0.23 watts in this example.

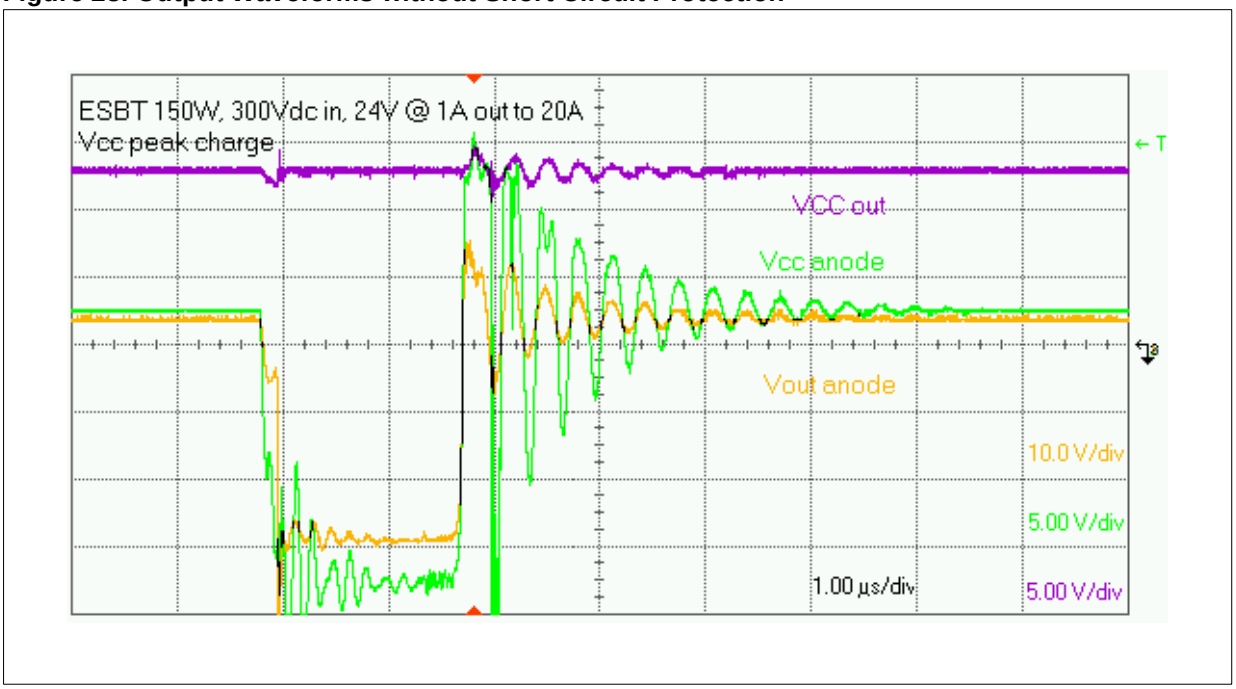
Figure 22. D6 Diode Recovery Time Effects with and without Snubber



Short Circuit

During an output overload or short circuit, the primary current ramps up higher and higher. This current is sensed by R8 which is turned into a voltage, filtered by R17 and C10 and fed to pin 13 of U1 (I sense). When this voltage reaches 1 volt the pulse is terminated. This is known as pulse by pulse current limit. The unit is protected against overstressing the main switch and output diode. In other words by choosing R8 we can limit the power of the unit. During short circuit the output power is limited to this value. Depending on the transformer coupling an output short should reflect a lower voltage to the auxiliary voltage supplying the L5991. When this voltage falls below the under voltage lockout of 8.4 volts, the L5991 shuts down and initiates a restart. In most cases because of the insulation in a transformer, it is difficult to achieve such results. As shown in figure 23, when the output is overloaded the transformer voltage falls to about 3 to 4 volts due to the drop of the diode traces and the output inductor. The 24 volts winding has 10 turns and the Vcc one has 6, so the voltage at the transformer pin of Vcc should be around 2.2 volts. The problem is the leakage inductance causing spikes and ringing whose peak charge the Vcc cap. as seen in figure 23 (violet waveform).

Figure 23. Output Waveforms without Short Circuit Protection



By adding a 22uH inductor in series with the Vcc winding and D3 we are able to filter out the spike and ringing to achieve Vcc to collapse below the under-voltage shutdown and re-initiate a start up. In this mode the high-cup mode is reached dissipating less power and keeping the thermal stresses low.

By adding a 22uH inductor in series with the Vcc winding and D3 we are able to filter out the spike and ringing to achieve Vcc to collapse below the under-voltage shutdown and re-initiate a start up. In this mode the high-cup mode is reached dissipating less power and keeping the thermal stresses low.

The shutdown is shown in the Figure 25 at 300V input. The hiccup mode duty cycle is 45ms on and 370ms off. As the input voltage is increased, the start up through resistors R25 becomes faster decreasing the off time. At 850 volt in the duty cycle is decreased to 50% protecting the power devices.

The most meaningful waveforms at different load and input conditions are reported in figures 26, 27, 28, 29.

Figure 24. Output Waveforms with Short Circuit Protection

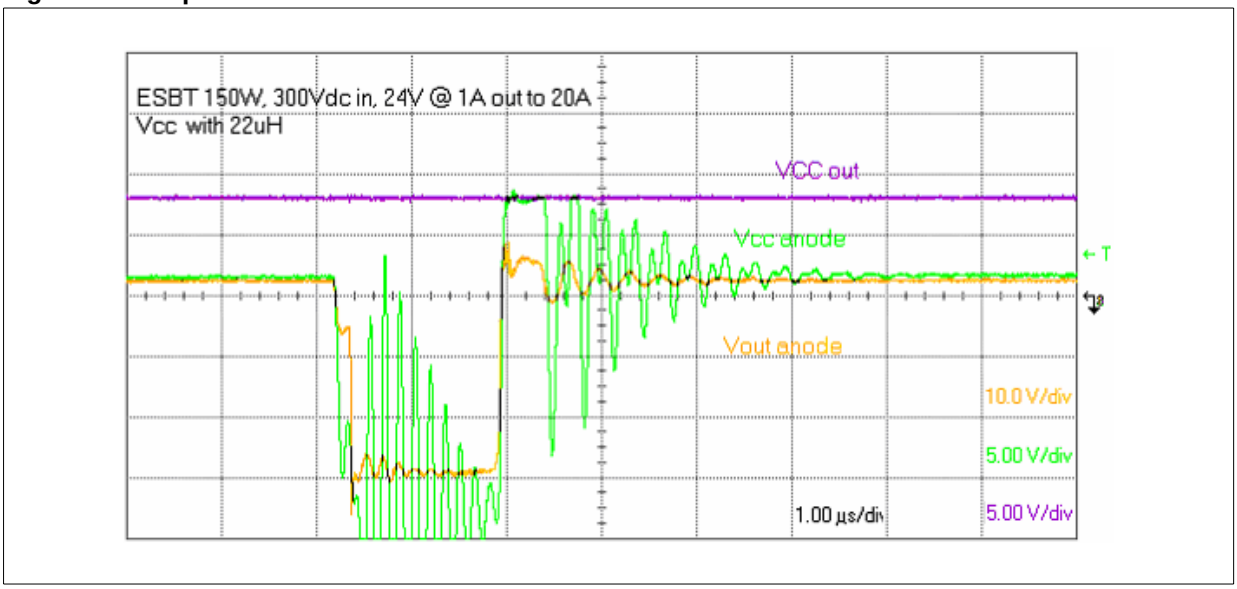


Figure 25. Hiccup Mode with Short Circuit Protection

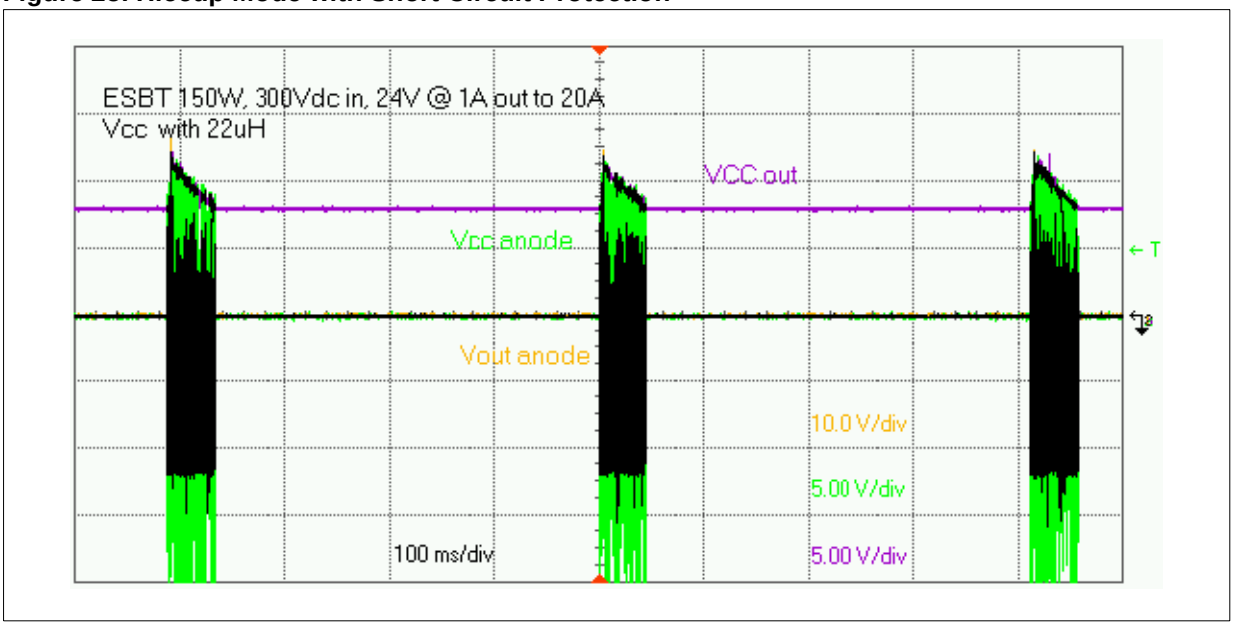


Figure 26. Steady State Vin=850V Pout=150W

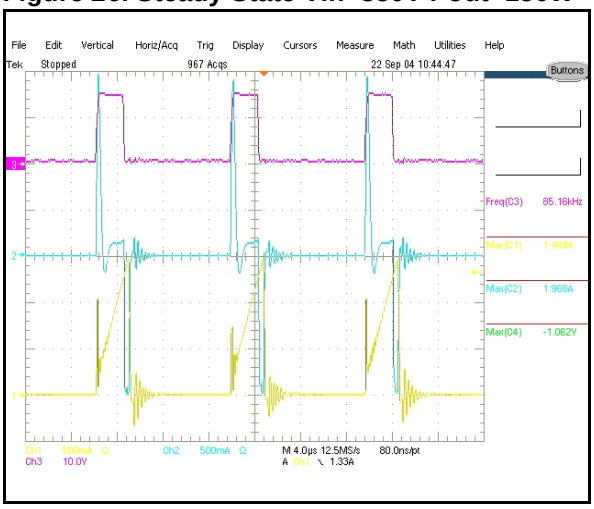


Figure 27. Steady State Vin=850V Pout=150W

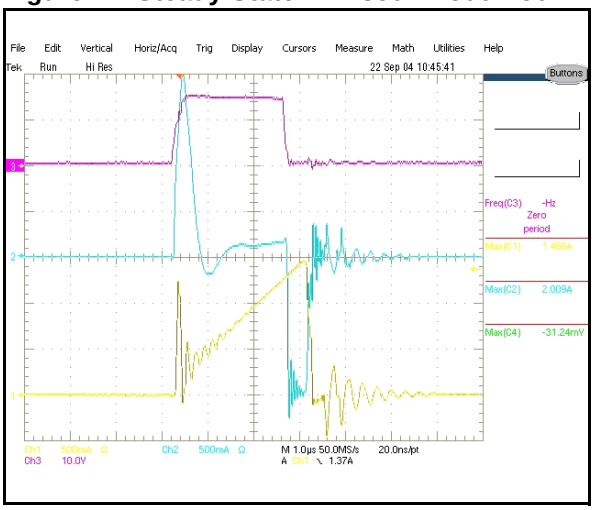


Figure 28. Steady State Vin=250V Pout=150W

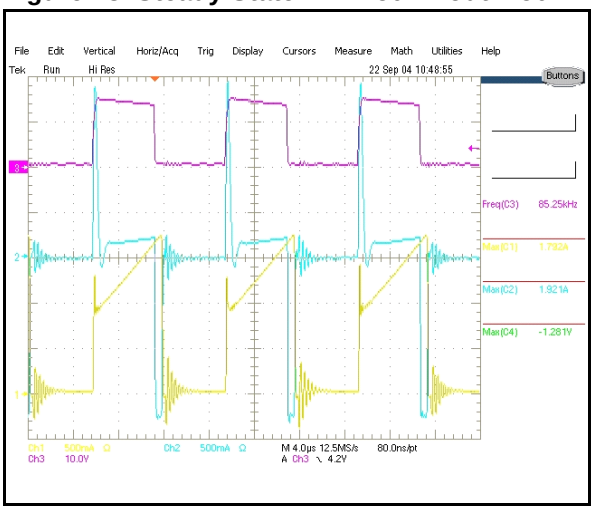


Figure 29. Steady State Vin=250V Pout=150W

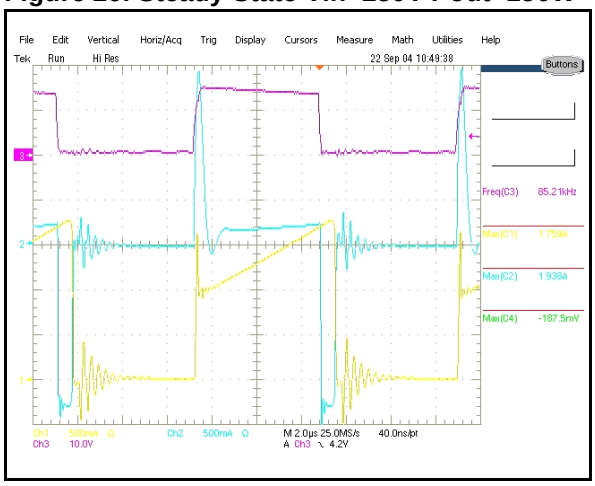


Figure 26, 27, 28, and 29 show the prototype steady state behavior, by reporting the gate voltage (violet waveform), the base current (blue waveform), and the collector current (yellow waveform) signals. The collector voltage signal has been not caught under maximum load condition because the probe parasitic capacitance generates an inner loop noise causing some undesirable oscillations.

Of course, safe operation for the ESBT™ in terms of maximum voltage spike on the collector has been also verified.

The switching frequency under maximum load condition is about 85Khz. The base current waveform highlights as the ESBT™ storage time is about 600ns, indicating the correct device saturation level and hence its optimal working condition.

Next waveforms will show the low load condition where the switching frequency is appreciably reduced to optimize, even in this condition, the power supply efficiency.

Figure 30. Steady State Vin=850V Pout=25W

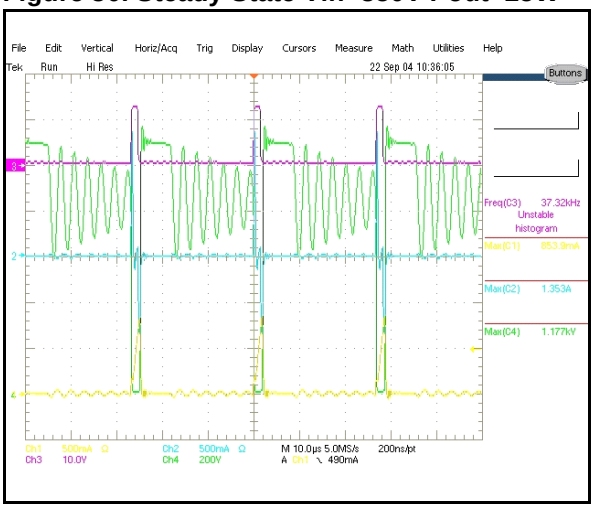


Figure 31. Steady State Vin=850V Pout=25W

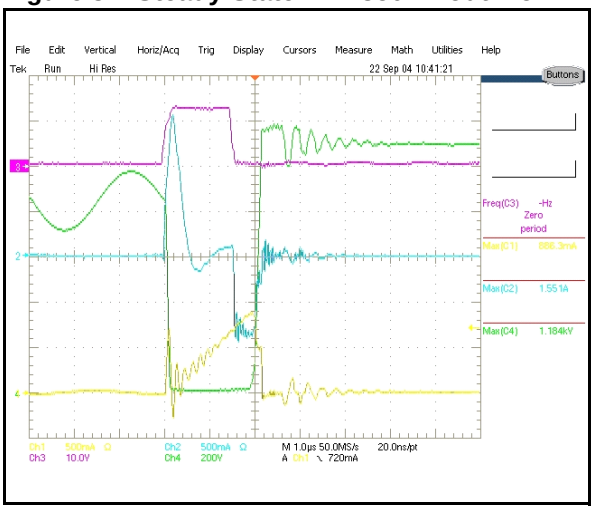


Figure 32. Steady State Vin=250V Pout=25W

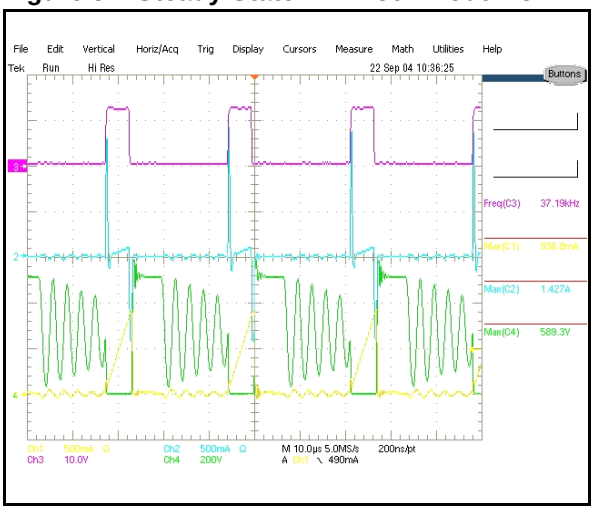


Figure 33. Steady State Vin=250V Pout=25W

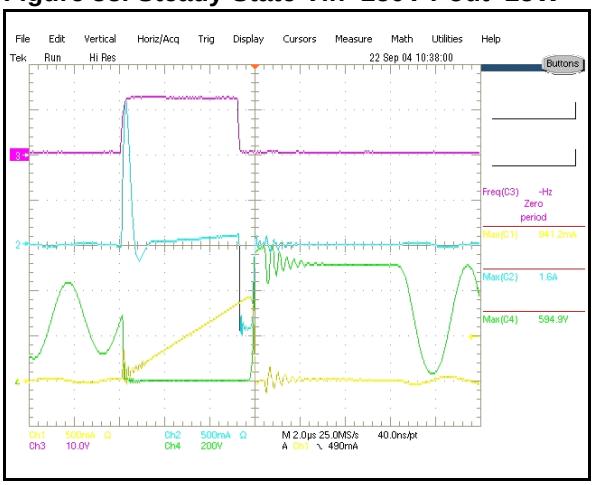
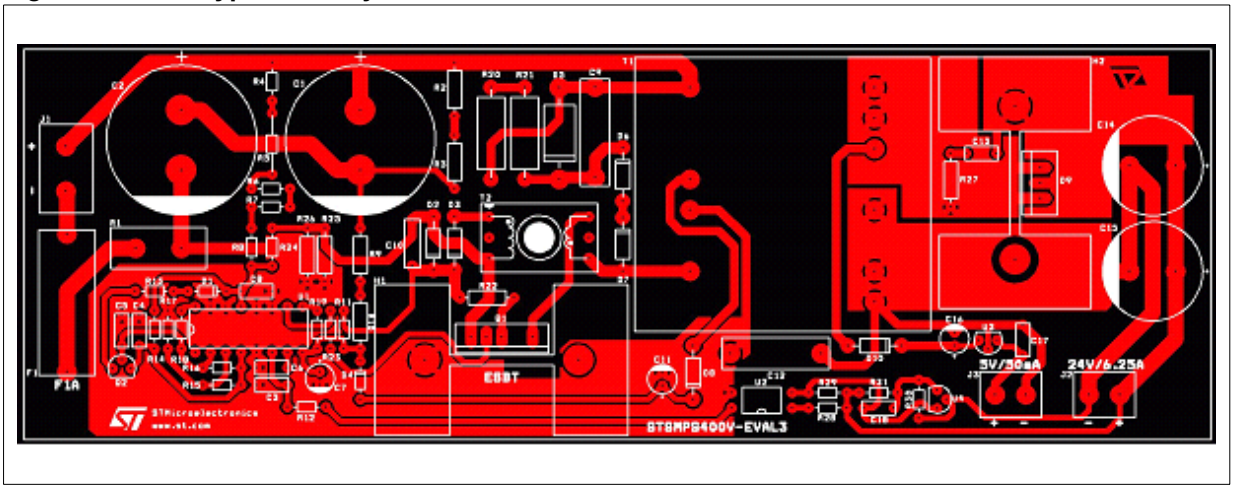


Figure 30, 31, 32 and 33 show the steady state behavior for the low load condition. In this case the switching frequency is about 37KHz, and the collector voltage signal (green waveform) has been added since in this less stressful condition the probe doesn't affect the system stability. From figure 31 is possible to see the very high voltage applied on the collector (1184V) during a normal working condition.

9. PCB LAYOUT

Figure 34. Prototype PCB Layout



The printed circuit board is reported in figure 34, while the relevant bill of material is listed in the schematic of figure 21.

REFERENCES:

- STMicroelectronics application note AN1889 "ESBT STC03DE170 IN 3-PHASES AUXILIARY POWER SUPPLY"

- STMicroelectronics application note AN1049 "MINIMIZE POWER LOSSES OF LIGHTLY LOADED FLYBACK CONVERTERS WITH THE L5991 PWM CONTROLLER"

- STMicroelectronics L5991 datasheet

- STMicroelectronics STC08DE150 datasheet

- Abraham I. Pressman, "Switching Power Supply Design", McGraw-Hill, Inc.